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GRAPHIC SYMBOLS FOR LOGIC DIAGRAMS

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FOREWORD*

This Standard represents the progress made to date in evolving graphical symbols for use in preparation of logic diagrams for systems of binary-state devices. The Standard contains two alternate but overlapping sets of symbols. Since agreement on a common set of symbols could not be obtained, no preference is implied between the two sets presented herein. This represents a solution that seems best under circumstances that presently prevail. It is anticipated that the Standard will be reviewed at the Task Group level at regular intervals, and eventually agreement will be sought for a set of graphical symbols based on a common symbology. It is hoped that groups that have not been represented heretofore will participate at Task Group level in the preparation of future revisions.

During the preparatory work on the Standard, the task of formulating, reviewing, and revising the various drafts was carried out by ad hoc committees established within the main Task Group. Every attempt has been made to insure that the personnel of the ad hoc working groups comprises an accurate cross-section of the individuals, committees, and other groups within the governmental, industrial, and technical organizations primarily concerned with the problem. As a result, the Standard is a coordination of the points of view of many groups, and represents as true an affirmative consensus as is now possible.

The burgeoning growth of computer technology throughout the world has brought renewed demands for international standardization. Coordination in international standardization has improved steadily through participation of members of the Task Group in meetings of the International Standardization Organization and other similar organizations.

Comments on the standard are invited for consideration in its future revision and should be forwarded to ASA Headquarters.

* This Foreword is not a part of the American Standard Graphical Symbols for Logic Diagrams, Y32.14.

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AMERICAN STANDARD GRAPHICAL SYMBOLS FOR LOGIC DIAGRAMS

1. INTRODUCTION AND GENERAL REQUIREMENTS

- 1.1 **Purpose**—This Standard establishes graphical symbols specifically designed for use in the preparation of logic diagrams for systems of two-state devices.
- 1.2 **Scope**—This Standard sets forth principles governing the formation of graphical symbols for logic diagrams in which connections between symbols are generally shown with lines. Definitions of logic functions, the graphical representations of these functions, and examples of their application are given.
 - 1.2.1 Two different but overlapping sets of graphical symbols are presented in this Standard: Uniform Shapes and Distinctive Shapes. For some functions there are different symbols in the two sets; for others the symbol is the same in both sets. Symbols from the non-overlapping parts of the two sets are not permitted on the same logic diagram.
 - 1.2.2 This Standard defines the requirement for logic diagrams. The presentation, in some cases, extends beyond the area of logic functions in order to preserve the context of symbology relating to logic diagrams.

2. APPLICABLE DOCUMENTS

- 2.1 **General**—The following document forms a part of this Standard to the extent specified herein.
American Standard for Graphical Symbols for Electrical and Electronic Diagrams Y32.2-1962.

3. DEFINITIONS FOR THIS STANDARD

- 3.1 **Logic Function**—a combinational, storage, delay, or sequential function expressing a relationship between signal input(s) to a system or device and the resultant output(s).
- 3.2 **Logic Symbol**—the graphical representation in diagrammatic form of a logic function.
- 3.3 **Logic Diagram**—a diagram that depicts by logic symbols and supplementary notations the details of signal flow and control, but not necessarily the point-to-point wiring, existing in a system of two-state devices.
 - 3.3.1 **Basic Logic Diagram**—a logic diagram that depicts logic functions with no reference to physical implementations. It consists primarily of logic symbols and is used to depict all logic relationships as simply as possible.
 - 3.3.2 **Detailed Logic Diagram**—a logic diagram that depicts all logic functions and also shows non-logic functions, socket locations, pin numbers, test points, and other physical elements necessary to describe the physical and electrical aspects of the logic.
 - 3.3.3 **Distinctive Shape Logic Diagram**—a basic or detailed logic diagram in which commonly used logic and non-logic functions are represented by enclosures with distinctive shapes. Functions less commonly used are represented by rectangles, within which an internal label denotes the function. It is the intention to develop new distinctive shapes and internal labels, as required.
 - 3.3.4 **Uniform Shape Logic Diagram**—a basic or detailed logic diagram in which both logic and non-logic functions are represented by rectangles, within which an internal label denotes the function. It is the intention to develop new internal labels, as required.
- 3.4 **States in Binary Logic**—The two physical states on each terminal of each signal line shall be referred to as the 0-state and the 1-state. The 0-state may be called the reference (inactive, anti-fiducial) state, and the 1-state the significant (active, fiducial) state.

The above must not be construed as implying that the 1-state requires more power, contains more energy, or is at a higher potential than the 0-state. The state designations are purely arbitrary as far as the physical interpretation is concerned.

- 3.5 Kinds of Logic.** If all signal line terminals in a logic diagram of a system, or device, have the same pair of physical states, and if both are electric potentials (currents), and if the more positive potential (current) is consistently selected as the 1-state, the resultant system, or device, is said to have positive logic. If the less positive potential (current) is consistently selected as the 1-state, the resultant system, or device, is said to have negative logic.

4. ASSIGNMENT OF LOGIC LEVELS TO BINARY LOGIC ELEMENTS

- 4.1** Consider a circuit whose output (F) is a function of two variables (A, B), and whose output and input levels are capable of assuming only +2 volts and -3 volts. Assume that the circuit behaves according to the following table of combinations:

INPUTS		OUTPUT
A	B	F
-3v	-3v	-3v
-3v	+2v	-3v
+2v	-3v	-3v
+2v	+2v	+2v

- 4.1.1** In positive logic the -3v level is the 0-state and +2v is the 1-state (see paragraph 3.5). Substitution of the logic values for the voltage levels results in the following table:

INPUTS		OUTPUT
A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

This is the truth table for the AND function. Therefore, the circuit is said to perform the AND operation.

- 4.1.2** In negative logic the -3v level is the 1-state and +2v is the 0-state (see paragraph 3.5). Substitution of the logic values for the voltage levels results in the following table:

INPUTS		OUTPUT
A	B	F
1	1	1
1	0	1
0	1	1
0	0	0

This is the truth table for the OR function. Therefore, the circuit is said to perform the OR operation.

- 4.2** Paragraphs 4.1.1 and 4.1.2 illustrate that a single circuit can perform either the AND operation or the OR operation. This duality has been employed in numerous single-device as well as multi-device systems.
- 4.3** Given a physical device characterized by a table of combinations, the logic function performed by the device is determined by the specified choices of the 1-states at its inputs and outputs.

Each choice of the 1-states at each input and each output of a logic circuit shall be specified on the detailed logic diagram in a manner that correctly represents the logic function designated by the logical designer.

- 4.4 In a diagram where positive logic, negative logic, or both is used, the state choices on the signal lines shall be identified as follows.
- 4.4.1 A small, open, right triangle at the point where a signal line joins a logic symbol indicates that the line's 1-state (activating) with respect to that logic symbol is the less positive potential (current).
 - 4.4.2 A small, filled, right triangle at the point where a signal line joins a logic symbol indicates that the line's 1-state (activating) with respect to that logic symbol is the more positive potential (current).
 - 4.4.3 The right triangle shall be so oriented as to point in the direction of signal flow.
 - 4.4.4 Either of the two kinds of right triangles, open or filled, may be omitted providing the convention is suitably noted on the diagram. In diagrams in which both kinds of right triangles would appear, only one kind may be omitted.
- 4.5 If lines are labeled with logic or English titles, they may apply to the 1-state indicated by either the nearest level indicator, the previous level indicator, or the following level indicator. Any such convention used must be noted on the diagram.

5. PRESENTATION TECHNIQUES

- 5.1 **Symbol Orientation**—does not affect the meaning of the symbol.
- 5.2 **Symbol Line Thickness**—does not affect the meaning of the symbol.
- 5.3 **Symbol Size**—does not affect the meaning of the symbol. An effort shall be made to keep like symbols of like size.
- 5.4 **Internal Functional Identification**—the internal functional identification of a rectangular block is part of the symbol.
- 5.5 **Internal Information**—(if included) shall follow the functional identification and will be referred to as tagging lines. (The internal functional identification is not considered to be a tagging line.)
 - 5.5.1 If a means of uniquely identifying a logic symbol is required, this information shall be contained in the first tagging line(s).
 - 5.5.2 The last tagging line(s) within the symbol, when used, shall provide a means of locating the logic hardware within the equipment system.
 - 5.5.3 **Additional Information**—may be included on intermediate tagging lines when required for clarity. This additional information may include such items as stylized waveforms, time delays, hardware information, etc.
- 5.6 **Peripheral Information**—Some of the additional information can best be presented outside of and adjacent to the symbol. For example, pin numbers, wave forms, test points.
- 5.7 **Signal Flow Direction**—While logic diagrams may completely indicate direction of signal flow by the symbols themselves, arrowheads superimposed on lines, an extended border on the input side of a rectangle, or a convention of unidirectional flow suitably noted on the diagram, may be used where required for clarity. No input shall enter a symbol in the vicinity of an output, or on the output side of a symbol e.g., the arc of a distinctive shaped symbol. Inputs may be drawn on any side of the symbol (except the output side), although the side opposite the output is preferred.

6. GENERAL LIST OF GRAPHICAL SYMBOLS

- 6.1 **Use of Symbols**—In the following listing of graphical symbols the Uniform Shape symbols are shown on the left and the Distinctive Shape symbols on the right. Logic diagrams must use symbols from one list or the other, not a mixture of the two. Symbols to be used on either list are shown in the center. The lines indicating input and output connections are not part of the symbol.

- 6.2 Symbol for AND



6.2.1 The output of an AND assumes the 1-state if and only if all of the inputs assume the 1-state. An example of the truth table for an AND with three inputs is:



INPUT			OUTPUT
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

6.2.2 In a device operated with positive logic, the truth table of 6.2.1 corresponds to the following table of combinations, where H stands for more positive (high) and L for less positive (low):

INPUT			OUTPUT
A	B	C	F
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

6.3 Symbol for OR



6.3.1 The output of an OR assumes the 1-state if one or more of the inputs assume the 1-state. An example of the truth table for an OR with three inputs is:



INPUT			OUTPUT
A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1