

American National Standard

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**DEPARTMENT
OF
DEFENSE**

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inside front cover

graphic symbols for logic diagrams (two-state devices)



american national standards institute, inc.

ANSI Y32.14-1973—IEEE Std 91-1973



Documents

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**IEEE Std 91-1973
ANSI Y32.14-1973
Superseding
MIL-STD-806B
26 Feb 1962 and
MIL-STD-00806C (SHIPS)
11 Aug 1965**

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**ANSI
Y32.14-1973**

**IEEE
Std 91-1973**

Revision of
ANSI Y32.14-1962
IEEE Std 91-1962
MIL-STD-806B
MIL-STD-00806C (Ships)

An American National Standard

**IEEE Standard Graphic Symbols for
Logic Diagrams (Two-State Devices)**

Sponsor

IEEE Standards Coordinating Committee 11 Graphic Symbols

Secretariat

**The Institute of Electrical and Electronics Engineers
The American Society of Mechanical Engineers**

Approved April 6, 1973

American National Standards Institute

Published by

**Institute of Electrical and Electronics Engineers
345 East 47th Street, New York, N. Y. 10017**

American National Standard

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Foreword

(This Foreword is not part of American National Standard Graphic Symbols for Logic Diagrams (Two-State Devices), Y32.14-1973, IEEE Std 91-1973.)

This revised standard is the latest development in a continuing activity to arrive at a useful series of logic symbols that will permit free interchange of information on logic design and the design of binary-operated automatic controls and systems. The present standard is the result of an active four-year effort to develop a standard that is consistent with current and ongoing developments in international practice in logic symbology taking place within the IEC (International Electrotechnical Commission). It is the latest step in a program that began within the IEEE's predecessor organizations in 1956 and continued within the ASA (now the American National Standards Institute).

In 1960, an ad hoc group on logic diagram graphic symbols was organized within ASA with the object of (1) reviewing early logic symbology developed by the Institute of Radio Engineers, the U. S. Air Force, the National Electrical Manufacturers Association, the American Institute of Electrical Engineers, and the International Federation of Automatic Control and (2) developing a draft for an American Standard. In the following year, the ad hoc committee was established as a permanent subcommittee, Y32.14, of the Graphic Symbols Committee, Y32, charged with the development of a logic symbols standard that had the concurrence of the Military and industry. By July 1961, a working group within the subcommittee had prepared five draft documents, and a substantial gap had been closed between various conflicting viewpoints; however, by August 1962, full agreement had not yet been reached. It was decided that such agreement would have to be postponed until a subsequent revision, and ANSI Y32.14-1962 (IEEE Std 91-1962) was approved and published. Work began immediately on an attempt to coordinate the new standard with MIL-STD-806. In 1965 Y32.14-1962 was adopted by the U. S. Navy, but full Department of Defense adoption did not follow, and as subsequent revisions of the Military Standard were proposed, it became clear that only with the development of a wholly new document would it be possible to achieve a substantial consensus of concerned activities.

In 1969 subcommittee Y32.14 was reorganized, and it began preparation of a draft standard that would have the acceptance of the U. S. Department of Defense and U. S. industry and be in accord with IEC developments. Fourteen drafts later, the subcommittee had achieved a standard that won approval of the American National Standards Institute and the Department of Defense and was substantially compatible with IEC Publication 117-15, Recommended Graphical Symbols: Binary Logic Elements.

This standard represents a major achievement in the continuing effort to reflect state-of-the-art accomplishments in standardized methods of communication. Symbology, like both language and technology, will continue to evolve, and the active participants in the present document will continue their role by transmitting USA viewpoints to IEC Technical Committee 3. It is intended that the contents of this standard will be modified as future needs dictate. Suggestions for improvement of this document are welcomed. They should be addressed to:

Secretary, American National Standards Committee Y32
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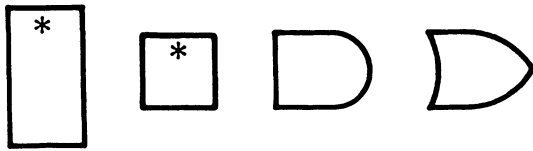
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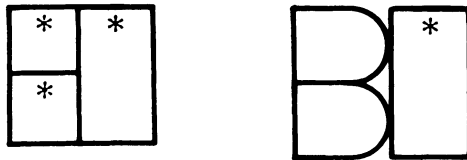
Quick Reference to Symbols

1. General Element Symbols

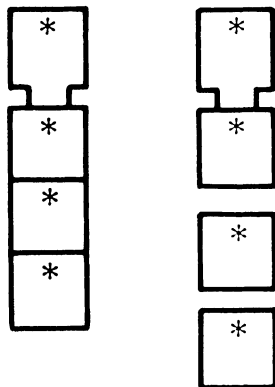
1.1, 1.2 Basic Symbols



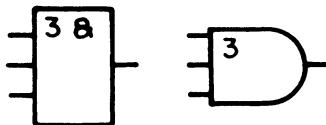
1.3 Contiguous Block



1.4 Common Control Block



1.5 Bundling, Grouping



2. Indicator Symbols

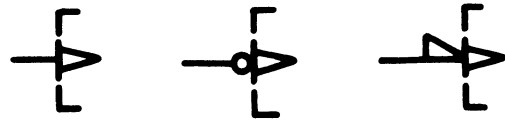
2.1 Negation Indicator



2.2 Polarity Indicator



2.3 Dynamic Indicator



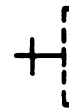
2.4 Nonlogic Indicator



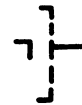
2.5 Extender-Connection Indicator



2.6 Inhibiting-Input Indicator

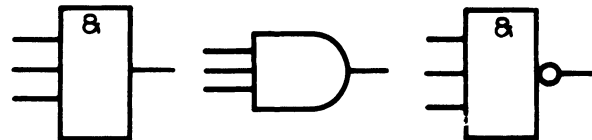


2.7 Output-Delay Indicator

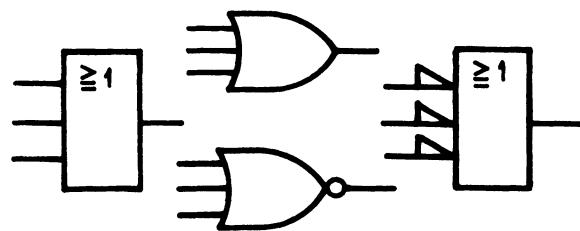


3. Combinational Logic Symbols

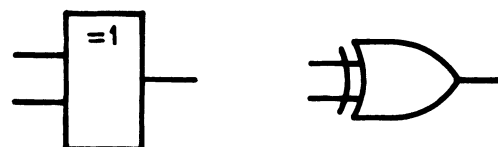
3.1 AND Function



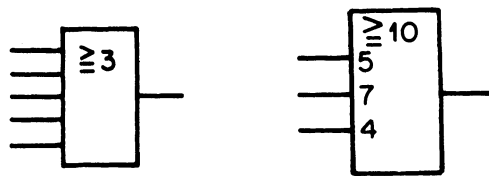
3.2 OR Function



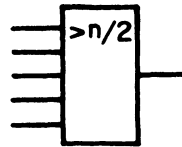
3.3 Exclusive OR Function



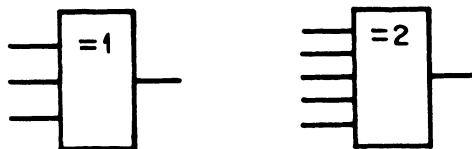
3.4 Logic Threshold Function



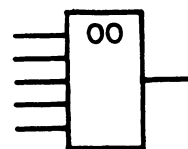
3.5 Majority Function



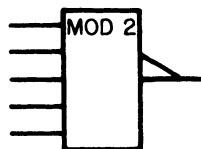
3.6 m and only m Function



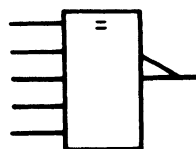
3.7 Even Function



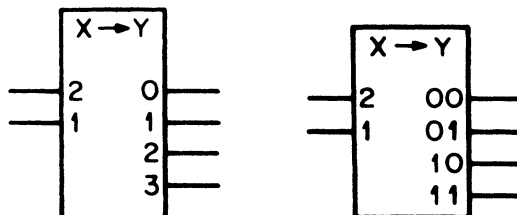
3.8 Addition Modulo 2 (ODD) Function



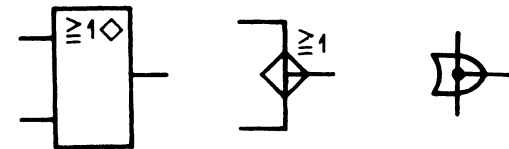
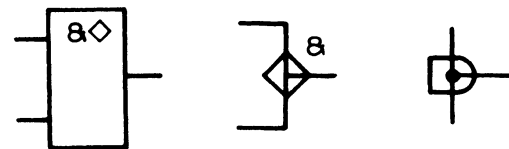
3.9 Logic Identity Function



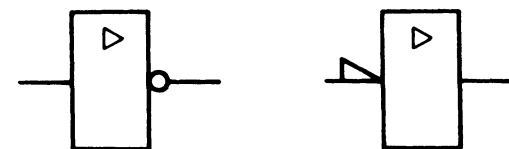
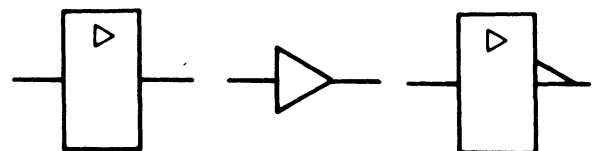
3.10 Coder



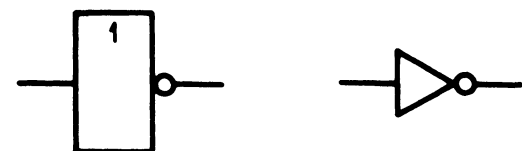
3.11 Distributed Connection (DOT-AND, DOT-OR)



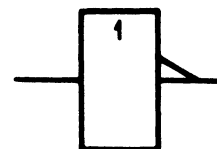
3.12 Amplifier Function



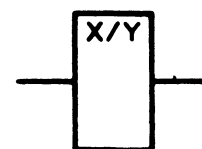
3.13 Inverter Function (Logic Negation Indicator)



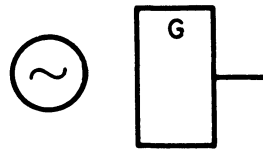
3.14 Inverter Function (Polarity Indicator)



3.15 Signal Level Converter



3.16 Oscillator

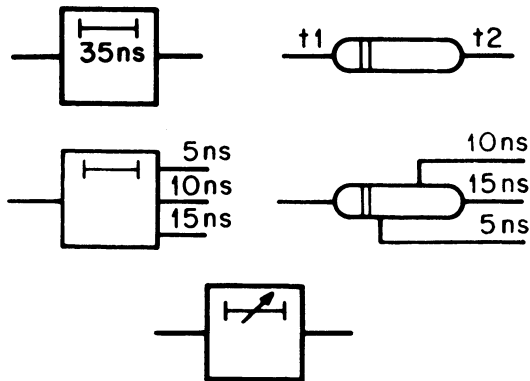


4. Sequential Logic Functions

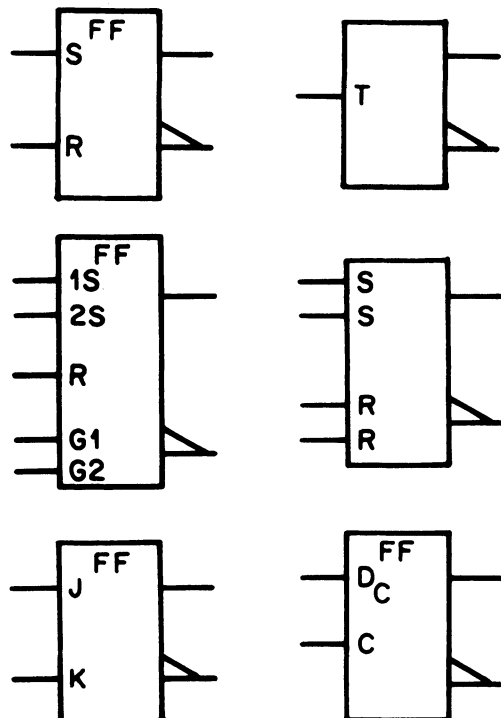
4.1 Monostable Element (Single Shot)



4.2 Delay Element

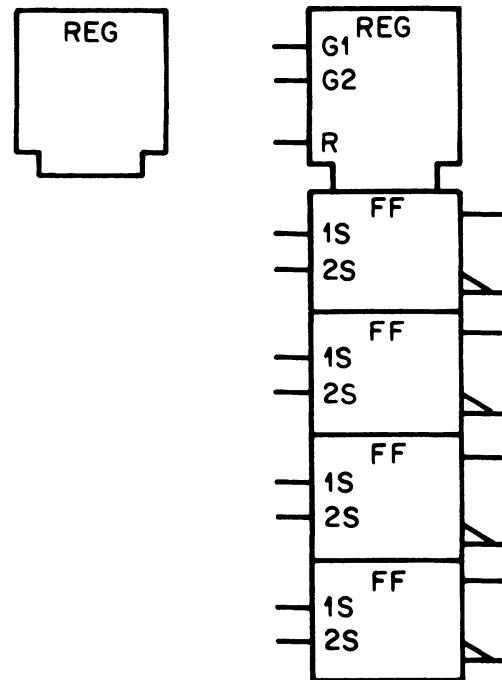


4.3 Flip-Flop

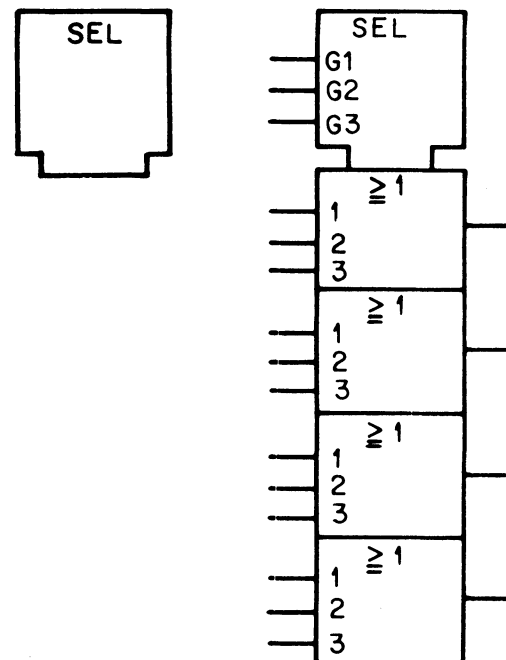


5. Control Block Functions

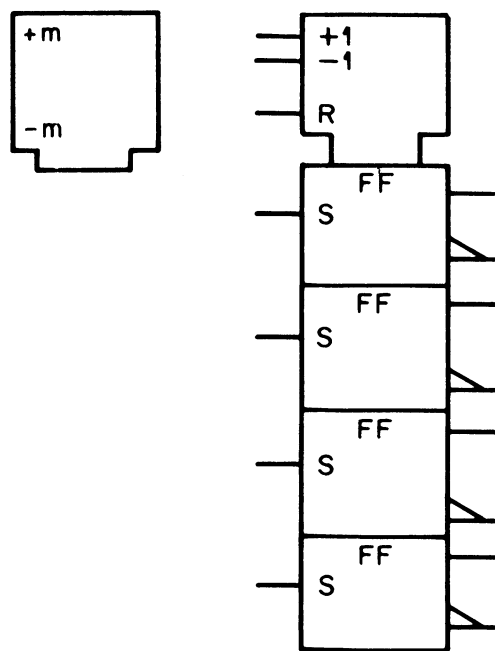
5.1 Register Control Block



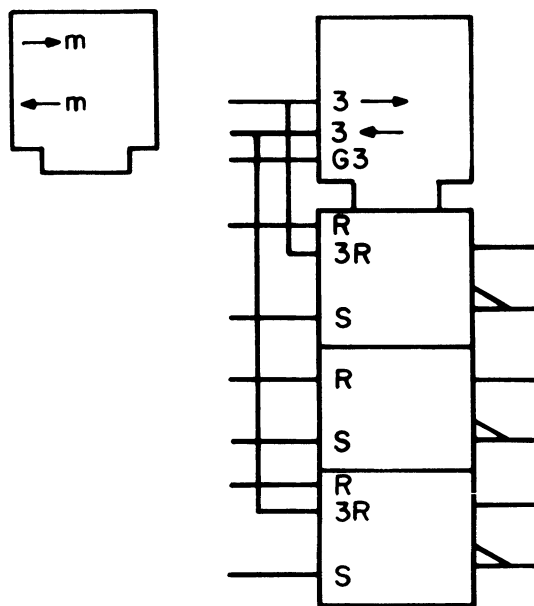
5.2 Selector Control Block



5.3 Counter Control Block



5.4 Shift Register Control Block

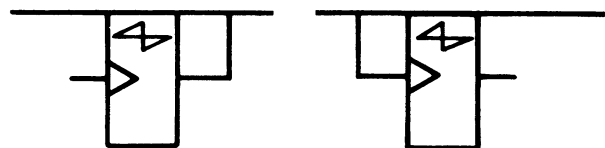


6. Miscellaneous Functions

6.1 Schmitt Trigger



6.2 Nonreciprocal Directional Coupler



An American National Standard

IEEE Standard Graphic Symbols for Logic Diagrams (Two-State Devices)

Introduction

11. Purpose and Scope

11.1 Purpose. This standard establishes the graphic symbols for use in the preparation of logic diagrams representing logic functions implemented with two-state devices. The primary purpose of this standard is to enable a user to readily read and understand the function of the logic without requiring a specific knowledge of the constructional details of the device represented.

11.2 Scope. This standard sets forth principles governing the formation of graphic symbols for logic diagrams in which the connections between symbols are generally shown with lines. Descriptions of logic functions, the graphic representation of these functions, and examples of their applications are given.

12. Applicable Documents

12.1 Industry Documents. The current editions of the following industry documents form a part of this standard to the extent specified herein:

American National Standard Abbreviations for Use on Drawings and in Text, Y1.1-1972¹

American National Standard Graphic Symbols for Electrical and Electronics Diagrams (Including Reference Designation Class Designation Letters), Y32.2-1970 (IEEE Std 315-1970)²

American National Standard Reference Designations for Electrical and Electronics

¹Obtainable from the American Society of Mechanical Engineers, 345 East 47 St., New York, N.Y. 10017, or the American National Standards Institute, 1430 Broadway, New York, N.Y. 10018.

²Obtainable from the Institute of Electrical and Electronics Engineers, 345 East 47 St., New York, N.Y. 10017, or the American National Standards Institute.

Parts and Equipments, Y32.16-1968 and Y32.16a-1970²

12.2 Military Standards. The current editions of the following military documents form a part of this standard to the extent specified herein:

Military Standard Abbreviations for Use on Drawings, Specifications, Standards, and in Technical Documents, MIL-STD-12³

Military Standard Mathematical Signs and Symbols for Use in Physical Sciences and Technology, MIL-STD-106³

12.3 International Documents. The following international agreement is cited as the recommendation for international use of the logic symbols in this standard:

International Electrotechnical Commission (IEC) Recommended Graphical Symbols — Binary Logic Elements, Publication 117-15

13. Definitions

13.1 Logic Variable. A variable which may assume one of two discrete states, the 1-state or the 0-state.

13.2 Logic Element. An element whose input and output signals represent logic variables, and whose output or outputs are defined functions of the inputs and of the variables (including time dependencies) internal to the element.

13.3 Logic Function. A combinational, delay, or sequential logic element defined in terms of the relationships which hold between input and output logic variables.

³Obtainable from DoD Single Stock Point, U.S. Naval Publications and Forms Center, Naval Supply Depot, Philadelphia, Pa. 19111.

13.3.1 Combinational Logic Function. A logic function wherein for each combination of states of the input or inputs, there corresponds one and only one state of the output or outputs.

NOTE: The terms combinative and combinatorial have also been used to mean combinational

13.3.2 Sequential Logic Function. A logic function wherein for at least one combination of states of the input or inputs, there exists more than one state of the output or outputs. The outputs are functions of variables in addition to the inputs, such as time, previous internal states of the element, etc.

13.3.3 Delay Logic Function. A sequential logic function wherein each state transition of the input signal causes a single delayed state transition at the output.

13.4 Logic Symbol. The graphic representation in diagrammatic form of a logic function.

13.4.1 Symbol Shape. Two general types of logic symbols are shown in this standard: (1) a rectangular-shape symbol in which the logic function is indicated by a qualifying symbol in its interior, and (2) a distinctive-shape symbol whose form uniquely identifies its logic function. See also Section I5.3.

13.5 Qualifying Symbol. That portion of a rectangular-shape logic symbol that denotes its logic function. See also Section I5.3.

13.6 Indicator Symbol. A symbol that identifies the state or level of an input or output of a logic symbol with respect to the logic symbol definition.

13.7 Control Designation Symbol. A symbol that identifies the particular manner, permissible or required, in which an input variable (possibly in combination with other variables) causes the logic element to perform according to its defined function.

13.8 States and Values of Logic Variables. In this standard the two physical values of a logic variable are referred to as the more positive level and the less positive level; while the two abstract states of a logic variable are referred to as the 1-state and the 0-state, corresponding to the qualities TRUE and FALSE, respectively, of symbolic or mathematical logic. The relationship, if any, be-

tween values and states is given in Section I3.9.

13.8.1 Physical Implementation of Logic Variables. The relation between the measurable values of a logic variable applicable to a particular technology and the general terms more positive level and less positive level as used in this standard should be consistently defined for that technology. For example, in the electrical/electronic technology, the logic variables would generally be represented by the more positive voltage level and the less positive voltage level.

13.9 Logic Conventions. See also Appendix D.

13.9.1 Positive Logic. When the 1-state of the variables is defined as the more positive of the two possible values, positive logic is used in the diagram.

13.9.2 Negative Logic. When the 1-state of the variables is defined as the less positive of the two possible values, negative logic is used in the diagram.

13.9.3 Mixed Logic or Direct Polarity Indication. When the 1-state of the variables is defined as the more positive or less positive of the two possible levels, depending upon the absence or presence of the polarity indicator symbol, mixed logic is used in the diagram. Direct polarity indication is an alternate term for mixed logic.

13.10 Logic Diagram. A diagram that depicts the two-state device implementation of logic functions with logic symbols and supplementary notations, showing details of signal flow and control, but not necessarily the point-to-point wiring.

14. Arrangement of the Standard

14.1 Conventions for This Standard. Unless otherwise noted, symbols are represented in this standard using the following conventions for consistency:

Signal flow is from left to right

Qualifying symbols (when used) are placed at the top center of the symbol

Symbols are oriented with input side on the left and output side on the right

When alternative symbols are shown, the relative position of the symbols does not imply a preference

I4.2 IEC Reference. Symbols or parts of symbols, together with their descriptions, notes, examples, and applications, which are consistent with IEC Publication 117-15, are identified by IEC (which is not part of the symbol).

I4.3 Revised or Deleted Symbols. Symbols from the earlier editions of the superseded standards which have been revised or deleted in this edition are shown in Appendix B.

I4.4 Placement and Use of Indicator Symbols. The section on indicator symbols is concerned only with the placement of such symbols with respect to the basic logic symbol. Applications concerned with the functional interpretation and use of indicator symbols appear in other sections. When indicator symbols are shown with only one of the two types of symbol shapes, their placement for the other symbol is exactly analogous.

I5. Diagram Preparation

I5.1 Drawing Note Requirement. All diagrams using the symbols defined in this standard shall refer to or have a note indicating that the diagram conforms to ANSI Y32.14-1973, Graphic Symbols for Logic Diagrams (Two-State Devices).

I5.2 Graphic Symbols Used in Existing Technical Documents. Unless otherwise specified, any changes or revisions to an existing drawing, specification, standard, or technical document, prepared under a previous edition of this standard, or a standard superseded by this standard, may show the latest graphic symbols, although the superseded graphic symbols may appear elsewhere in the document.

I5.3 Diagrams for International Use. The qualifying symbol in the rectangular-shape logic symbols of this standard (functional symbols cited in IEC Publication 117-15) may be included as additional information in distinctive-shape symbols. Such inclusion is recommended if the distinctive-shape symbol is used in logic diagrams intended for international use.

I5.4 Similar or Identical Graphic Symbols, Letter Combinations, and Notations. It is required that when graphic symbols with a

similar or identical shape or configuration but having different meanings are used from this standard or another standard, and when letter combinations or notations that are the same with different meanings are shown on the same drawing or set of drawings, steps shall be taken (such as reference or caution notes, comparison charts illustrating the conflicting symbols together with proper identification, use of asterisks or other flagging techniques, etc) to avoid misinterpretation of the symbols used. This requirement is especially critical if the graphic symbols used are from different disciplines and therefore represent devices, conductors, or lines of flow, that if misinterpreted might cause damage to the equipment or be dangerous to the life of servicing or operating personnel.

I5.5 Symbol Size and Shape. Although symbol size does not affect the meaning of the symbol, an effort shall be made to maintain a like symbol size for similar classes of symbols throughout a logic diagram. See Appendix A. Subscript letters and numbers should be the same size as the basic designating letter.

I5.6 Symbol Orientation. The orientation of a symbol outline does not affect the meaning of the symbol. Qualifying symbols, indicator symbols, control designation symbols, and tagging lines should be shown in normal reading order and orientation, regardless of symbol outline orientation.

I5.7 Qualifying Symbol Placement. The qualifying symbol which defines the logic function shall be placed consistently at either the top center or center of rectangular-shape symbols. For exception, see symbols 3.11.1 and 3.11.2. A qualifying symbol may also be included in distinctive-shape symbols if desired. See also Section I5.3.

I5.8 Line Width. The width of a line does not affect the meaning of a symbol. See Note 4.3B (flip-flop) for the suggested use of a thick line for a symbol.

I5.9 Signal Flow. The preferred direction of signal flow should be from left to right or top to bottom, or both.

NOTE: It is generally accepted practice that fault-tree diagrams show the signal from right to left.

Flow direction may also be indicated by the

orientation of the distinctive-shape symbol outlines, polarity indicators or control designation symbols, or flow arrowheads; by the placement of input (only) or output (only) indicators; or by a convention of unidirectional flow suitably noted. The flow arrowhead is a small arrowhead superimposed upon data or control lines connected to symbol inputs or outputs. The flow arrowhead shall not touch any part of the symbol.

NOTE: The use of a solid (or filled-in) arrowhead is consistent with ANSI Y32.2.

I5.10 Multiple Inputs and Outputs. A logic symbol may have any number of inputs and outputs provided that the symbol description requirements are met.

I5.11 Logic Convention Statement. Each logic diagram which represents a physical equipment and makes use of the logic negation indicator, symbol 2.1.1 (small circle), shall be suitably noted as to whether the positive or the negative logic convention prevails throughout that diagram.

I5.12 Indicator Symbols. Absence of indicator symbols on input or output lines denotes that the 1-state and 0-state referred to in the states of a logic variable are identical to the conventional 1-state and 0-state, respectively, of the input and output lines. See Appendix D for further information on indications of state or level conversion of these indicator symbols.

I5.13 Internal Information. Optional identification or detail references within the symbol outline, other than qualifying symbols, indicator symbols, and control designation symbols, are commonly referred to as tagging lines and may include

- Reference to logic element physical identification (circuit, module, or card type, etc)

- Location of logic element in the represented equipment (reference designation, ANSI Y32.16)

- Location of symbol in the logic diagram

- Details such as stylized waveforms or pulse characteristics

- Care shall be exercised to appropriately separate internal information from qualifying

symbols, indicating symbols, and control designation symbols, and sequence of arrangement should be detailed on the drawing or related documentation.

I5.14 External Information. Additional information, references, or details may be placed about the periphery of the symbol outline to identify terminal numbers, test points, waveforms, notes, etc. Care shall be exercised to appropriately separate external information from indicator symbols.

I5.15 Application and Generation of Symbols Not Shown (Buildups). No attempt has been made to list all possible applications (buildups) for both the rectangular-shape symbols and the distinctive-shape symbols. Some typical applications are shown. The same conventions apply to both types of symbols. Additional applications may be devised using basic symbols in the list to complete the buildup, provided they are a reasonable and intelligible use of the symbols. If a specific symbol appears in this standard for an item, however, it shall be used in lieu of buildup symbols of the individual elements unless a clarification of the internal operation of the item is necessary.

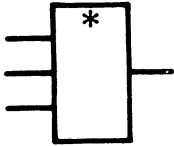
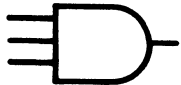
I5.15.1 NAND and NOR Symbols. In this standard, NAND and NOR functions were not assigned qualifying symbols since the NAND and NOR function can be easily obtained by using the negation indicator symbol with the symbol for an AND or OR function.

I5.16 Additional Symbols. For logic functions not covered in this standard or not capable of reasonable presentation in terms of groups of interconnected standard symbols, abbreviations from ANSI Y1.1⁴ (or suitable letter combinations in the absence of such abbreviations), graphic symbols from ANSI Y32.2, or mathematical signs and symbols from MIL-STD-106 may be used as qualifying (function) symbols inside the rectangular shape of a general element symbol, providing adequate reference information is provided on the logic diagram or associated documentation.

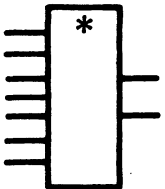
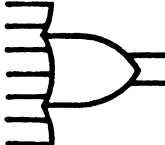
⁴For military applications use the latest edition of MIL-STD-12.

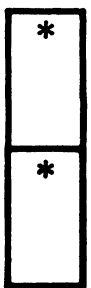
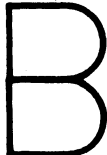
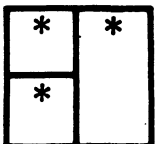
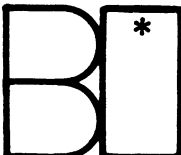
Graphic Symbols

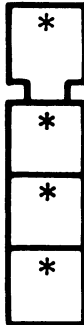
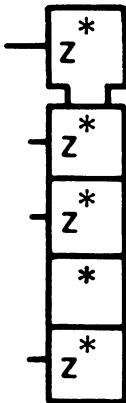
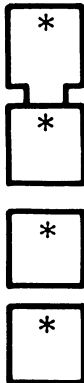
1. General Element Symbols

NUMBER	SYMBOL	DESCRIPTION
1.1	(STATEMENT)	Logic Element, basic symbol
	IEC  OR IEC 	Rectangular-Shape Symbol NOTE 1.1A: The aspect ratio of the symbol may vary according to the internal information required or the number of input or output lines that must be accommodated. See symbol 1.2.2. NOTE 1.1B: The asterisk (*) is always replaced by a qualifying symbol.⁵ See also Section I5.7 for placement of the qualifying symbol.
		Distinctive-Shape Symbol, examples NOTE 1.1C: The proportions of the symbol should remain constant, with variations restricted to symbol size. See Appendix A.
		NOTE 1.1D: A qualifying symbol may be included in a distinctive-shape symbol. See Section I5.7.
1.2 IEC	(STATEMENT)	Inputs and Outputs NOTE 1.2A: The lines representing the inputs and the lines representing the outputs are preferably placed on opposite sides of the symbol. See Sections I4.1 and I5.9. NOTE 1.2B: A logic symbol may have any number of inputs and outputs, providing the symbol description requirements are met. See also Note 1.1B
1.2.1	IEC  	<i>Typical Applications</i>

⁵(This footnote is not a part of ANSI Y32.14-1973.) The letter-form qualifying symbols shown in Appendix B are likely to appear on diagrams prepared in some segments of industry until full standardization coordination is attained.

NUMBER	SYMBOL	DESCRIPTION
1.2.2		<i>Symbol Extension to Accommodate Seven Inputs, typical application</i> NOTE 1.2.2A: Only the distinctive-shape symbol may use a line extended from the input side to accommodate a large number of inputs; for rectangular-shape symbols, the aspect ratio shall be altered as appropriate.
		

1.3 <u>IEC</u>	(STATEMENT)	Contiguous Block NOTE 1.3A: Two symbols may share a common boundary parallel to the direction of signal flow when there is no logic connection or dependency between the two symbols. For exception see symbol 1.4. NOTE 1.3B: Two symbols may share a common boundary perpendicular to the direction of signal flow when there is a single logic connection without logic inversion or dissimilar polarities between the two symbols. See also Note 1.1B
1.3.1		<i>With Two Elements Shown, typical application</i>
		
1.3.2		<i>With Three Elements Shown, typical application</i> NOTE 1.3.2A: In this application, there is a logic connection between the upper left-hand symbol and the right-hand symbol, and a logic connection between the lower left-hand symbol and the right-hand symbol. There is no logic connection between the two left-hand symbols.
		

NUMBER	SYMBOL	DESCRIPTION
1.4		Common Control Block NOTE 1.4A: To be used in conjunction with an array of related symbols for purposes of having all common logic lines grouped and connected to the common control block symbol See also Note 1.1B
1.4.1		<i>With Contiguous Block Symbol Array</i>, typical application NOTE 1.4.1A: Convention: To establish the relationship between the inputs connected to the common control block and the individual elements, one or more of the following methods shall be used. (1) Labeling a common input with S, R, etc, in the case of an array of flip-flops. (2) Dependency notations (see Section 3.1.7 and Note 4.3.1B).
1.4.1.1		<i>With Contiguous Block Array, Having One Input Common to Only Three of the Four Blocks</i> NOTE 1.4.1.1A: If in an array of logic elements some inputs are common to a number of, but not all, elements, and the dependency notation of Section 3.1.7 is not used, these common inputs are connected to either a common control block or to one of the symbols of the array. These common inputs shall be labeled with the letter Z. In the case of two or more series of common inputs the Z shall be followed by an identifying numeral. If one or more common inputs are connected to a particular element of the array, the labels of these inputs shall be placed inside the symbol representing that element. NOTE 1.4.1.1B: The short line outside the individual contiguous blocks is a part of the symbol and not a connecting line.
1.4.2		<i>With Separated Block Symbols Array</i>, typical application NOTE 1.4.2A: This arrangement should be used if there is a need to show individual signal lines between adjacent symbols.