

IEEE Standard Specifications for an I/O Expansion Bus: SBX Bus

Sponsor

**Technical Committee on Microprocessors and Microcomputers
of the
IEEE Computer Society**

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Foreword

(This Foreword is not a part of IEEE Std 959-1988, IEEE Standard Specifications for an I/O Expansion Bus: SBX Bus.)

During the 1980s, the rapid technological advances in computer technology have positively impacted societies world-wide. The driving force behind computer technology advancement has been the dramatic improvements in VLSI (very large scale integration) component technology. The magnitude of VLSI technology changes is so compelling, that systems based on the latest technologies have substantial advantages over their predecessors. VLSI technologies are projected to continue their exponential rates of change throughout the 1990s.

Two concerns are raised by the tremendous rate of change of computer technology. First, no one supplier can keep up on all fronts of computer technology advancements. And second, today's state-of-the-art designs will be technically obsolete in 2–4 years. The move toward standards is in direct response to both of these concerns. Standards play a pivotal role in the absorption of computer technology by providing the key technology decouplers and access points that facilitate the mixing of products from multiple vendors and modular upgrades with new technology over time.

This standard was created as a means of quickly integrating the latest I/O-oriented VLSI into system designs. The standard defines an interface between a baseboard and a small piggyback module. This physical partitioning allows generic baseboards to be quickly and easily customized by the addition of small easily designed modules. Since these modules typically contain only one VLSI device and a few support ICs, they can be designed much more quickly than a full baseboard. Further, with the standardization of the interconnect interface, numerous vendors have created hundreds of compatible modules. Thus, this standard provides designers rapid access to the wide diversity of the latest VLSI in the form of small modules that piggyback onto baseboards.

This standard was originally developed in 1980 by Intel Corporation to provide I/O flexibility for its line of 8- and 16-bit MULTIBUS single-board computers. This original bus was called the Intel System Bus Extension and named the SBX bus. To promote multivendor acceptance, Intel submitted its SBX specifications to the IEEE Microcomputer Standards Committee as a basis for independent standardization in 1981. A working group was formed, and the first draft of IEEE P959 was written in 1982.

The working group had the following members:

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Warren Buster
John Craig
Glen Dokken
Lawrie Eaton

Gordon Force
Peter Hoa
Steve Leibson
Pete MacWilliams
Richard Main

Juan Monico
Douglass Sherrod
Tom Thorsteinson

By 1983, this group had refined the P959 specification into its near-final draft, draft 3. In June of 1984, draft 3 was published in *IEEE Micro* magazine for public comment. A year later, the Microcomputer Standards Committee approved P959 draft 3 to proceed to a ballot of the sponsoring Technical Committee on Microprocessors and Microcomputers (TCMM).

The TCMM sponsor ballot was began in late 1987, with approval reported in March 1988. Minor comments from this ballot resulted in the creation of draft 4 of the specification. The final steps in the IEEE standardization process were complete in June 1988 when the IEEE Standards Board Review Committee (REVCOM) recommended approval, and the full IEEE Standards Board unanimously approved the draft 4 specification.

The following persons were on the balloting committee that approved this document for submission to the IEEE Standards Board:

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1. General

1.1 Scope

One of the most important parts of any computer system is the I/O. Many systems require different types of I/O depending on the specific application. In addition, the system designer is faced with a significant challenge to keep up with new technology in I/O devices types, interfaces, and the LSI components designed to support them. The IEEE 959 I/O expansion bus is designed to address these needs. Using this standard interface allows small increments of I/O to be added or modified in an easy, cost-effective way.

The IEEE 959 I/O expansion bus is specified independent of processor or board type. Each expansion interface supports up to sixteen 8-bit I/O ports directly. Enhanced addressing capability is available using slave processors or FIFO devices. In addition, each expansion interface may optionally support a DMA channel capable of data rates up to 2 16-bit Mwords/sec. These features are supported for both 8- and 16-bit data paths.

This specification has been prepared for those users who intend to design or evaluate products that will be compatible with the IEEE 959 I/O expansion bus. For this purpose, functional, electrical, and mechanical specification are covered in detail. The intent of the specification is to guarantee compatibility between baseboards and expansion modules while not restricting the actual designs any more than necessary. Additional design considerations that are not part of the actual specification are presented in the appendixes.

1.2 Definitions

The following paragraphs contain definitions that are used throughout this specification. More detailed definitions can be found in the appropriate section of this specification.

1.2.1 General System Term Definitions

compatibility: The degree to which devices may be interconnected and used without modification, when designed as defined in Sections 2., 3., and 4. of this specification. Section 6. discusses the various levels of compliance that the specification allows.

operation: The process whereby digital signals effect the transfer of data across the interface by means of a sequence of control signals. Operations may be either interlocked or full speed.

interface: A shared boundary, between two systems or parts of systems, through which information is transferred.

system: A set of interconnected elements that achieve a given objective through performing a specific function.

arbitration: The process of determining which requesting device will gain access to a resource.

1.2.2 Signals and Paths

bus: A signal line or set of signal lines used by an interface system to connect a number of devices and to transfer data.

byte: A group of eight adjacent bits of data that are operated on as a unit.

word: Two bytes operated on as a unit.

data path: Signal lines on a bus associated with data.

high state: The more positive voltage level; used to represent one of two logical binary states (see 3.1.1 for more details).

low state: The more negative voltage level; used to represent one of two logical binary states (see 3.1.1 for more details).

signal: The physical representation of a logical value.

signal level: The relative magnitude of a signal when compared to a reference. Signal levels in this specification are specified in volts.

signal line: One of a set of signal conductors in an interface system used to transfer messages among interconnected devices.

active-high signal: A signal for which the logical-true (activated) state is represented by the high electrical state, and the logical-false (deactivated) state is represented by the low electrical state. In this specification, the active-high signal can be identified by the absence of an asterisk (*) at the end of the signal name (refer to 3.1.1 for more details).

active-low signal: A signal for which the logical-false (deactivated) state is represented by the high electrical state, and the logical-true (activated) state is represented by the low electrical state. In this specification, the active-low signal can be identified by the presence of an asterisk (*) at the end of the signal name (refer to 3.1.1 for more details).

two-directional signal line: A signal line that may be defined in either direction across an interface, and that cannot be defined in both directions simultaneously. The direction of operation for a two-directional signal line in a system is a configuration option.

bidirectional signal line: A signal line that may be defined in either direction across an interface. The direction is determined by control signals for each operation.

2. Functional Description

The IEEE 959 I/O Expansion Bus concept allows low-cost, highly flexible I/O expansion for computer boards. This section provides an overall understanding of the concept by describing the elements of the bus system, the bus interface signals, and the bus operations.

2.1 Bus Elements

There are two basic elements in the IEEE 959 I/O Expansion Bus: the baseboard and the expansion module.

2.1.1 Baseboard

A baseboard is any board that provides one or more I/O expansion interfaces (connectors) that meet the electrical and mechanical requirements of this specification. Logically, the baseboard is always the master device, making it responsible for generating all addresses, chip selects, and commands. As a master device for DMA transfers, the baseboard is required to provide the DMA controller function. Mechanically, the baseboard shall supply latching connector(s) and mounting hole(s) for attaching the expansion module with nylon screws and spacers. See Figs 1 and 2 for mounting details.

2.1.2 Expansion Module

An expansion module is a small specialized I/O board that attaches to a baseboard. Each expansion module can be one of two standard sizes, single wide and double wide; each is shown in Figs 1 and 2, respectively. The purpose of an expansion module is to convert the general bus interface into a specific I/O interface. An example of this would be an RS232 serial interface module. The IEEE 959 I/O expansion bus is specifically designed to simplify the expansion module interface. In many cases, LSI peripheral components can connect to this interface directly.

2.2 Bus Signals

The IEEE 959 I/O expansion bus signals can be grouped into seven classes based on the functions they perform. The classes are as follows:

- 1) Address and chip select lines
- 2) Data lines
- 3) Control lines
- 4) Interrupt lines
- 5) Option lines
- 6) Power lines
- 7) Reserved lines

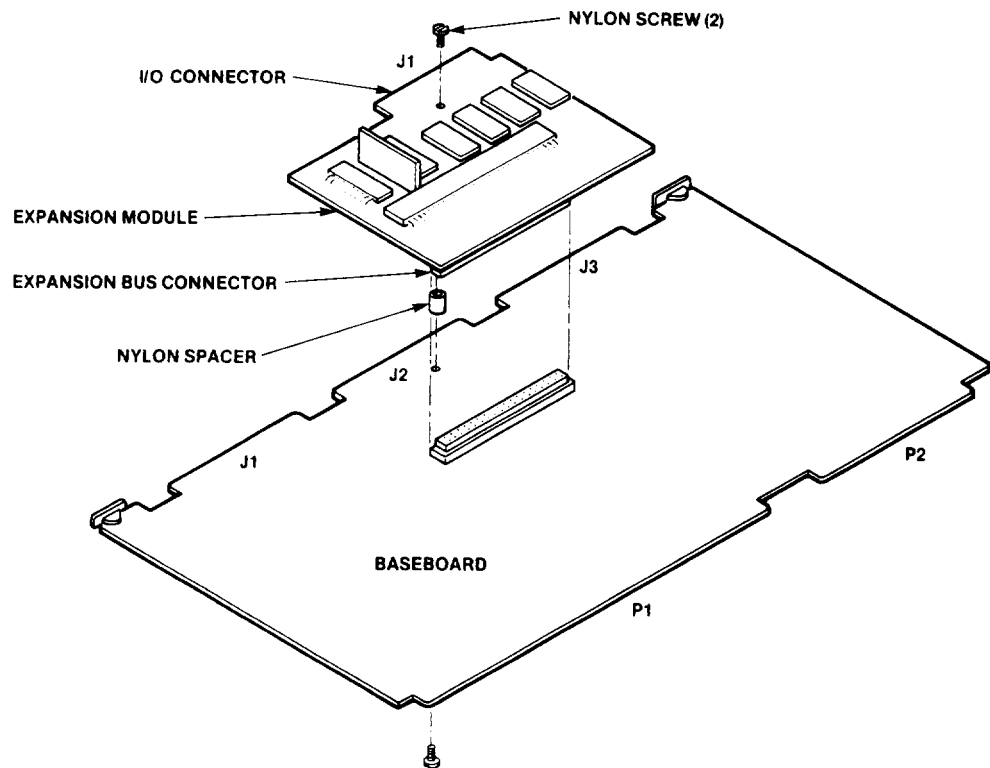


Figure 1— IEEE 959 I/O Expansion Bus System with Single-Wide Expansion Module

2.2.1 Address and Chip Select Lines.

These lines can be broken into two groups.

Function	Signals
Address	MA0, MA1, MA2
Chip Select	MCS0*, MCSI*

The function of these signals is somewhat unique. A typical bus would simply have address lines and require the slave device to create its own chip selects. The IEEE 959 I/O expansion bus requires the baseboard to generate chip selects. This feature simplifies the expansion modules with only minimal impact to the baseboard.

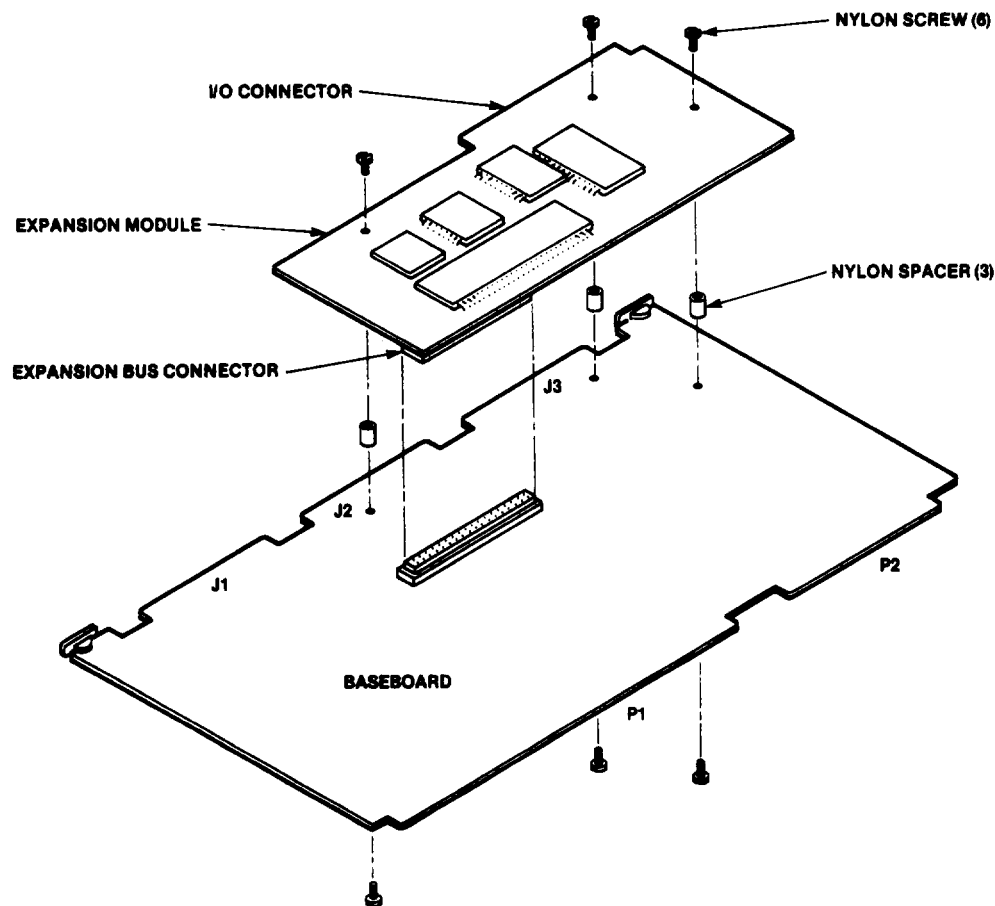


Figure 2— IEEE 959 I/O Expansion Bus System with Double-Wide Expansion Module

2.2.1.1 Address Lines (MA0, MA1, MA2).

The address lines are active high signals generated by the baseboard from the low order address lines. MA0 is the least significant address bit. For an 8-bit baseboard, these lines connect directly to the least significant address bits: A0, A1, and A2. For a 16-bit baseboard, the address line connections are MA0 to A1, MA1 to A2, and MA2 to A3 (A0 is used along with byte high enable to control byte/word transfers). During DMA operations, the state of the address lines is undefined.

2.2.1.2 Chip Selects (MCS0*, MCSI*).

The chip selects are active low signals generated by the baseboard to enable communication with the expansion module. These lines may transition when they are not required to be valid. It is the responsibility of the expansion module to qualify the chip select signals with commands (note that this is done internally in many LSI components). Chip selects shall remain high during a DMA operation.

The chip selects on a 16-bit baseboard with a 16-bit expansion module have two functions. In addition to enabling communication, they control high-byte, low-byte, specified by the three address lines. For 16-bit boards, there are two cases: 8-bit expansion module and 16-bit expansion module.

For a 16-bit baseboard driving an 8-bit expansion module, the chip select operation is similar to the 8-bit baseboard. The 8-bit expansion module connects to the low byte on the data bus, which makes it only accessible through even ports (odd ports transfer over the high byte). Each chip select therefore enables eight consecutive even ports as determined by the three address lines. (Note that this mode also allows each chip select signal to enable eight consecutive 16-bit ports for 16-bit expansion modules.)

The chip selects on a 16-bit baseboard with a 16-bit expansion module have two functions. In addition to enabling communication, they control high-byte, low-byte, and word transfer modes. MCS0* is used to enable a low-byte transfer (even ports), MCS1* is used to enable a high-byte transfer (odd ports) and both are used for a word transfer. The three address lines determine which of eight 16-bit ports are being addressed.

2.2.2 Data Lines (MD0–MD15).

The data lines are used to transmit or receive data to or from the expansion module ports. The 16 active-high, bidirectional lines are organized in two groups (bytes) of eight lines each. The low byte (MD0–MD7) is used for all transfers on 8-bit baseboards and for all even-byte transfers on 16-bit baseboards. MD0 is the least significant bit of this byte. The high byte (MD8–MD15) is used for all odd-byte transfers on 16-bit baseboards. MDS is the least significant bit of this byte. Table 1 presents a summary of the data bus functions for different configurations.

Table 1— Data Base Function for Different Configurations		
Configuration	Lines Used	
	MD0–MD7	MDS–MD15
8-bit baseboard	X	—
16-bit baseboard with:		
8-bit expansion module	X	—
16-bit expansion module — even byte	X	—
16-bit expansion module — odd byte	—	X
16-bit expansion module — word	X	X

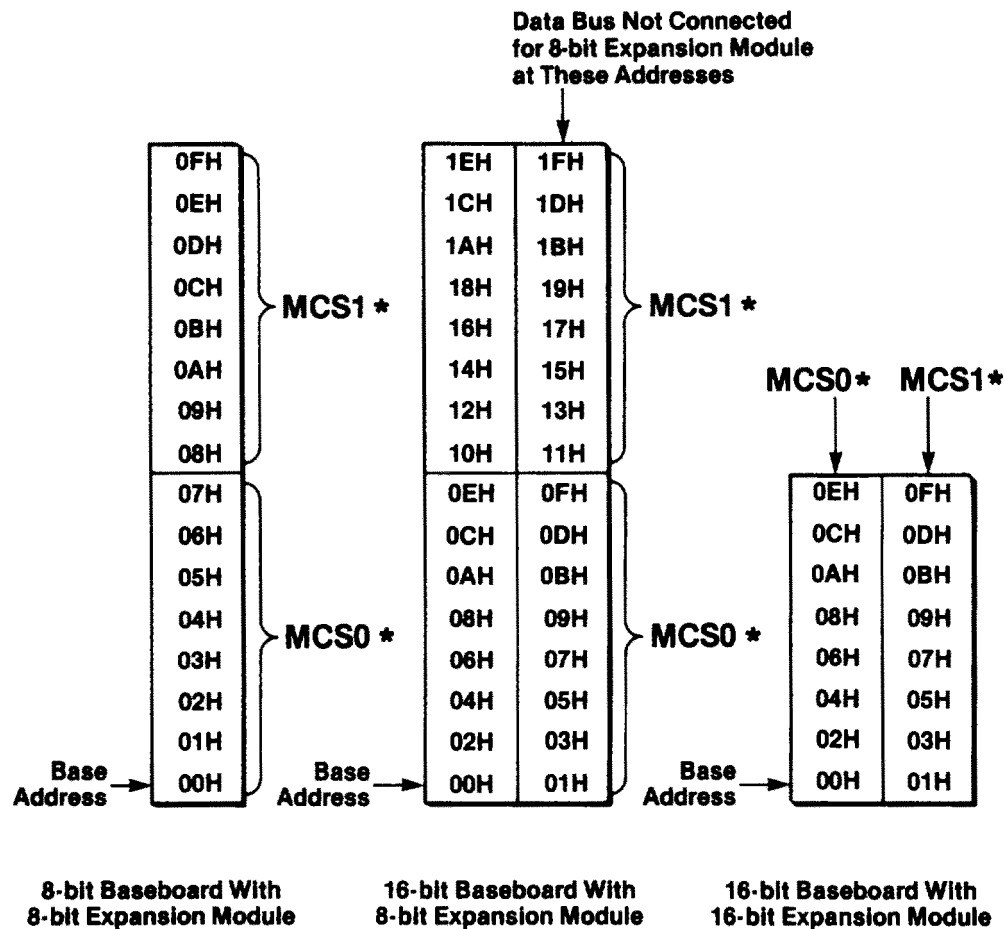


Figure 3— Chip Select Address Ranges

2.2.3 Control Lines

The following signals are classified as control lines:

CLASS	FUNCTION	SIGNAL
Commands	I/O Read I/O Write	IROD* IOWRT*
Direct Memory Access (DMA)	DMA Request DMA Acknowledge Terminate DMA	MDRQT MDACK* TDMA
Initialize	Reset	RESET
Clock	Expansion Module Clock	MCLK
System Control	Expansion Module Wait Expansion Module Present	MWAIT* MPST*

2.2.3.1 Command Lines (IORD*, IOWRT*).

The command lines are active-low signals generated by the baseboard. An active command line indicates to the expansion board that the address and chip select lines are valid and that the selected expansion module (that is, one with active chip select) should perform the specified operation. The I/O read command (IORD*) is used by the baseboard to request data to be transferred from the expansion module. The I/O write command (IOWRT*) is used by the baseboard to transfer data to the expansion module.

2.2.3.2 Direct Memory Access (DMA) Lines.

The DMA lines control the communication link between a DMA controller on the baseboard and the expansion module. The use of these lines is optional on both the baseboard and the expansion module.

2.2.3.2.1 DMA Request (MDRQT).

This active-high signal from the expansion module to the baseboard DMA controller requests that a DMA cycle be initiated. Upon request of this signal the DMA controller begins arbitration for the baseboard's local bus.

2.2.3.2.2 DMA Acknowledge (MDACK*).

This active-low signal from the baseboard to the expansion module indicates that a DMA operation has been granted (DMA controller has the bus). Like a chip select, this signal may transition when not valid and therefore shall be qualified by commands on the expansion module.

2.2.3.2.3 Terminate DMA (TDMA).

This active-high signal is used to terminate a DMA transfer to or from the expansion two-directional DMA control signal. The specific direction shall be determined by configuration (that is, jumper or software controlled tri-state driver). Once configured, TDMA may only operate in one direction. When generated by the expansion module, TDMA is used to terminate the DMA transfer. When generated by the baseboard, TDMA is used to signal the end of a DMA transfer to the expansion module. Baseboards that support DMA shall be configurable to support TDMA in either direction. An expansion module may support or not support TDMA, as required.

2.2.3.3 Initialize (RESET).

This active-high signal is generated by the baseboard to put the expansion module into a known state. The baseboard shall generate a power up reset when power is applied. During normal operation after a power up reset sequence, the expansion module may be reinitialized with a standard reset signal (refer to 3.2 for more details).

2.2.3.4 Expansion Module Clock (MCLK).

This input to the expansion module is a general-purpose timing signal. The 9–10 MHz clock is asynchronous to all other bus signals.

2.2.3.5 System Control.

There are two system control signals (MWAIT* and MPST*) that are defined in the following paragraphs.

2.2.3.5.1 Expansion Module Wait (MWAIT*).

This active-low signal is generated by the expansion module to extend the current data transfer operation. While MWAIT* is activated, the baseboard is forced to insert wait states into the current bus cycle, allowing the expansion module more time to complete the requested operation. The MWAIT* signal is generated or enabled by a combination