

IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control System

An American National Standard
**IEEE Standard FASTBUS Modular
High-Speed Data Acquisition
and Control System**



Published by
The Institute of Electrical and Electronics Engineers, Inc



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**ANSI/IEEE
Std 960-1986**

An American National Standard
**IEEE Standard FASTBUS Modular
High-Speed Data Acquisition
and Control System**

Sponsor

**Nuclear Instruments and Detectors Committee
of the
IEEE Nuclear and Plasma Sciences Society**

Approved June 14, 1984

IEEE Standards Board

Approved November 28, 1984

American National Standards Institute

ISBN 0-471-84472-1

Library of Congress Catalog Number 85-081331

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December 12, 1985

SH10223

Foreword

(This Foreword is not a part of ANSI/IEEE Std 960-1986, IEEE Standard FASTBUS Modular High-Speed Data Acquisition and Control System.)

This standard defines a modular data-bus system for data acquisition and control. Mechanical, signal, electrical, and protocol specifications are given that are sufficient to assure compatibility between units from different sources of design and production. This standard applies to systems consisting of modular electronic instrument units that process or transfer data or signals, normally in association with computers or other automatic data processors.

The system on which this standard is based (US Department of Energy Report DOE/ER-0189, as amended) was developed by the NIM Committee* of the US Department of Energy, consisting of representatives of the US National Laboratories and other major laboratories. Representatives of the ESONE Committee of European Laboratories, as well as of individual European and Canadian laboratories, have also contributed to the development of this standard. Comments and inquiries should be addressed to:

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This standard was reviewed and balloted by the Nuclear Instruments and Detectors Committee of the IEEE Nuclear and Plasma Sciences Society and by the American National Standards Committee on Nuclear Instruments, N42. It has also been endorsed by the ESONE Committee of European Laboratories.

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An American National Standard
**IEEE Standard FASTBUS Modular
High-Speed Data Acquisition
and Control System**

1. Introduction and General Information

FASTBUS is a standardized modular data-bus system for data acquisition, data processing and control. A FASTBUS system consists of multiple bus segments that can operate independently, but link together for passing data and other information. FASTBUS can operate asynchronously using a handshake protocol to reliably accommodate different speed devices without prior knowledge of their speed. It can also operate synchronously without handshake for transfer of data blocks at maximum speed.

1.1 Document Outline. Complex systems such as FASTBUS are more easily understood if the specifications are accompanied by general descriptive material that places the details of the various parts of the system in perspective. Hence, this section presents an overview of the principal characteristics and operations of FASTBUS. Most of the ensuing sections contain, in addition to the mandatory parts of the specification, descriptions of the usage of the features being specified. Section 2 contains the definitions of words that have a special meaning for FASTBUS systems. The symbols used in diagrams to designate various parts of a FASTBUS system are defined, and a list of commonly used abbreviations is given. The remaining sections lay down the specifications for the FASTBUS system. This is followed by a series of appendixes that give more descriptive information concerning some FASTBUS features. Capitalized words are used in this section to indicate words that have a special meaning for FASTBUS.

1.2 System Overview. Most FASTBUS design features stem from a consideration of the requirements of contemporary data acquisition systems. The need for high speed is met by providing for parallel operation of many processors that can com-

municate with each other as well as with data acquisition and control devices. The communication protocol used by processors and devices has a large data and address field and is defined in an implementation-independent manner so as to be able to take advantage of advances in technology. The need for flexibility is met by a modular design that readily permits many options in system configuration.

Modular instrumentation systems are distinguished by the method used to interconnect the devices that form the system. Mechanical, electrical, and logical aspects of the connection need to be specified. The electrical connections are made by a set of signal lines called a SEGMENT. While FASTBUS DEVICES can be simply connected by CABLE SEGMENTS, such an arrangement may incur speed penalties. The more usual situation is that the required functionality at a given location is attained by a number of MODULES grouped together in a CRATE in order to share a common backplane bus (Fig 1.2(a)). This bus, called a CRATE SEGMENT or SEGMENT, like the CABLE SEGMENT, forms a logical element of a FASTBUS system.

Using the FASTBUS protocol, a SEGMENT functions as an autonomous bus interconnecting one or more MASTER DEVICES with a number of SLAVE DEVICES. All bus operations involve a MASTER-SLAVE relationship between the initiator, which must be a MASTER, and the responder, which must be a SLAVE. A

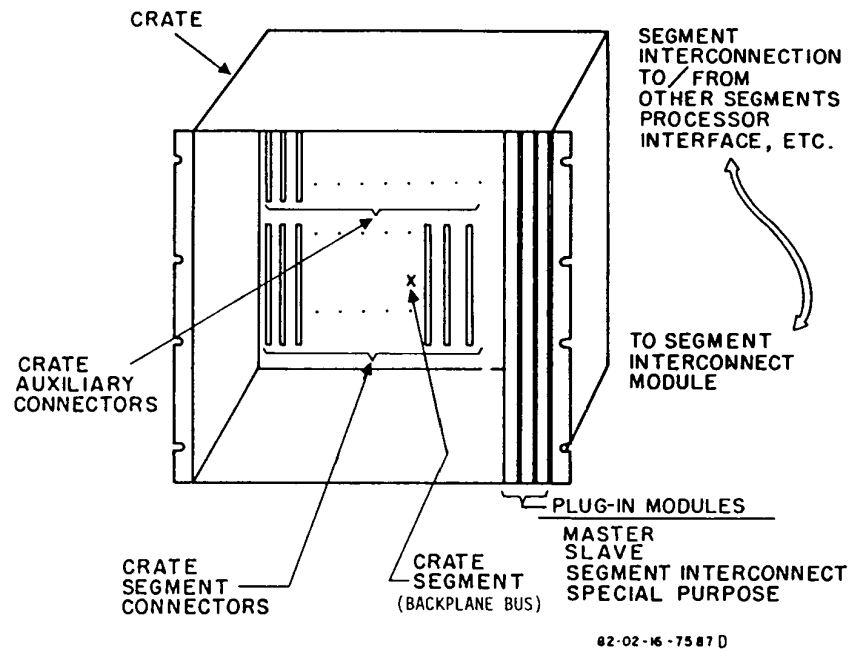


Fig 1.2(a)
Basic FASTBUS Elements

MASTER is capable of requesting and obtaining control of the SEGMENT to which it is connected in order to communicate with a SLAVE. If the communication is with another MASTER, then, for the duration of the operation, the responding MASTER acts as a SLAVE. A SLAVE cannot gain bus mastership but can make a Service Request that a MASTER on the same SEGMENT can use to initiate a procedure to service the request. MASTERS have a more versatile interrupt mechanism in that they can gain bus mastership and write an interrupt message to an interrupt service device. With multiple MASTERS on a SEGMENT, techniques must be provided to resolve concurrent requests for use of the bus. Each MASTER is assigned an Arbitration Level to use during Arbitration Cycles. In response to timing signals from the SEGMENT Arbitration Timing Controller, circuitry in each MASTER determines which of the contending MASTERS will next be granted bus mastership. No time penalty is usually associated with this arbitration procedure since the next MASTER can be selected before the current MASTER completes its operation.

Multiple MASTERS on a single SEGMENT share a common bus. Contention for use of this bus may reduce throughput as seen by a given MASTER because of the time it spends waiting to gain Mastership of a busy bus. Since SEGMENTS operate independently, distributing the MASTERS among several SEGMENTS can reduce the contention problem and increase throughput to the extent that the information needed by each MASTER can be localized on its SEGMENT.

A MASTER on one SEGMENT must also be able to quickly communicate with a SLAVE on another SEGMENT. This ability is provided by SEGMENT INTERCONNECTS (SIs) that temporarily link independent SEGMENTS (Fig 1.2(b)). All SEGMENTS through which the operation passes must be available at the same time in order to complete an intersegment operation. The arbitration mechanism, along with circuitry in each SI, extends the resolution of bus contention problems to off-segment as well as on-SEGMENT MASTERS. Since one SEGMENT can be linked to any of a number of different SEGMENTS, system configurations can be implemented that optimize time-critical data paths.

The means by which a pair of SIs on different SEGMENTS communicate with each other is not specified, thus allowing the technique most suitable for a given application to be chosen. A powerful technique, which is specified in Appendix E, makes use of a CABLE SEGMENT for this connection. DEVICES other than SIs may be connected to a CABLE SEGMENT. Such DEVICES also follow the FAST-BUS protocol and require switches for position-dependent GEOGRAPHICAL ADDRESSING and must be provided with power.

Other techniques for linking SEGMENTS involve the use of BUFFERED INTERCONNECTS and SEGMENT EXTENDERS. The BUFFERED INTERCONNECT is a device that stores and forwards FASTBUS operations thus breaking the synchronism between MASTER and SLAVE. The EXTENDED SEGMENT concept allows a number of SEGMENTS to share the same GROUP ADDRESS. This sharing is accomplished by the use of SEGMENT EXTENDERS whose simplicity, as compared to SEGMENT INTERCONNECTS, is obtained at the price of somewhat reduced flexibility in system topology and operations for members of the EXTENDED SEGMENT.

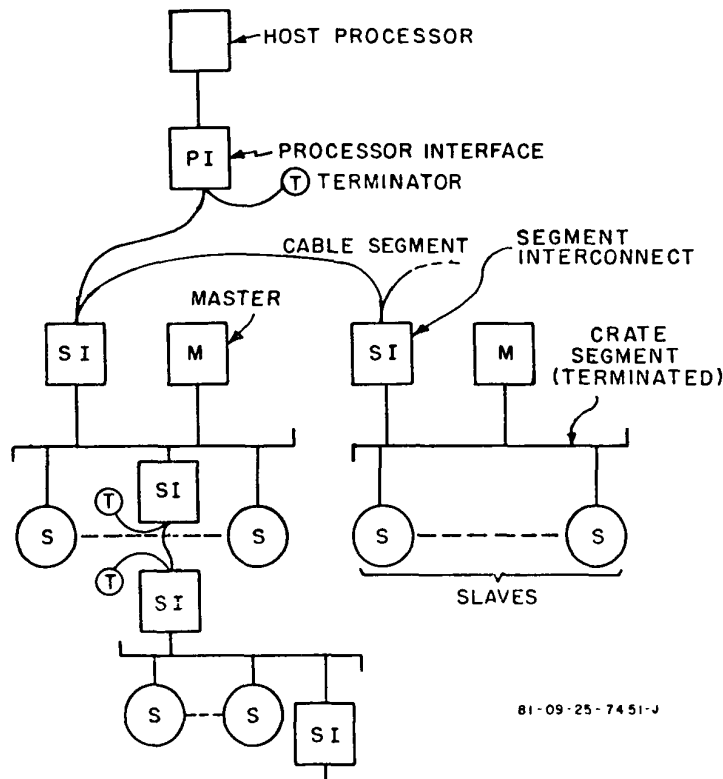


Fig 1.2(b)
Example of FASTBUS System Topology

While most, if not all, **MASTERS** will have some processing ability, the **FAST-BUS** system design also envisages the connection of large and small computers to the system. Such a connection is made by a **PROCESSOR INTERFACE** that gains entry to the **FASTBUS** system through either a **CABLE SEGMENT** or a **CRATE SEGMENT** (Fig 1.2(b)). System requirements dictate that each system contains one processor that has complete knowledge of the structure of the system. In particular, it must be able to access every **SEGMENT** of the system and know how the **SEGMENTS** are to be interconnected. This processor, called the **HOST**, initializes the system by telling each side of each **SI** what operations it is to pass on to its other **SEGMENT**. By using **GEOGRAPHICAL ADDRESSING**, the **HOST** can ascertain the physical location and type of each **DEVICE** in the system and, as needed, assign **LOGICAL ADDRESSES** to the **DEVICES**. **LOGICAL ADDRESSES** allow a **DEVICE** to use an **INTERNAL ADDRESS** field matched to its needs that is independent of position within a **SEGMENT**.

The principal characteristics and capabilities of FASTBUS can be summarized as follows:

- Speed limited only by propagation and logic delays (typically better than 10 MHz for ECL)
- Large Address and Data Fields (32 bits)
- Segmented Bus to allow parallel processing
- System-wide communication capability
- Block transfers with or without handshake
- Uniform system-wide protocol
- Interrupt and arbitration features

1.2.1 FASTBUS Operations. The FASTBUS operations defined in Section 5 make use of a multiline bus whose signal assignments are as indicated in Table 1.2.1. A CABLE SEGMENT consists of the group of 60 lines at the top of the list while a CRATE SEGMENT includes, in addition, the other listed lines as well as power lines. Signals are classified according to use as indicated in Table 1.2.1.

Most FASTBUS operations begin with a MASTER requesting and being granted bus mastership. The MASTER then selects a SLAVE by a primary address cycle and follows this by any number of data transfer cycles, after which the bus is released.

A primary address cycle is started by the MASTER asserting the SLAVE'S address on the 32 Address/Data (AD) lines followed by Address Sync (AS). This assertion of the address word sets up a path, through SEGMENT INTERCONNECTS if necessary, between MASTER and SLAVE. When the SLAVE recognizes its address, it responds with the Address Acknowledge signal (AK). The protocol requires that AS and AK remain asserted until the operation is completed. This AS/AK lock serves to cause all other devices to ignore bus activity thus allowing the communicating pair to employ any protocol they both understand as long as the AS/AK lock is not broken. In order to facilitate the construction of compatible DEVICES, however, standard protocols for most useful operations have been specified.

On receipt of the AK response from the SLAVE, the MASTER removes the address information from the AD lines and uses these lines for data during the ensuing data transfer cycles. After the AS/AK lock between MASTER and SLAVE has thus been established, a Read operation can be initiated by the MASTER asserting the Read (RD) and Data Sync (DS) lines as in Fig 1.2.1. The SLAVE responds by placing data on the AD lines and issuing DK, which is used by the MASTER to latch the data. For a Write operation, the MASTER asserts data on the AD lines and follows this assertion by the Data Sync (DS). The SLAVE responds by issuing a Data Acknowledge (DK). The operation is terminated by the MASTER removing all its signals, including AS, from the bus. The SLAVE, sensing the removal of AS, removes all its signals including AK.

Since Address and Data Cycles are easily distinguishable, the three Mode Select lines, MS, are used by the MASTER to modify the meaning of the address information and to independently specify the type of data transfer. In a primary address cycle, control or data space can be specified as well as single or multiple listener (Broadcast) mode. In a data cycle, random data, secondary address, or handshake or pipelined (non-handshake) block transfer can be specified.

Table 1.2.1.
FASTBUS Signals

Mnemonic	Signal Name	Use	Number	Comments
AS	Address Sync	T	1	For address and reporting status of connection
AK	Address Acknowledge	T	1	
EG	Enable Geographical	C	1	
MS	Mode Select	C	3	for data and control of data transfers
RD	Read	C	1	
AD	Address/Data	I	32	
PA	Parity	I	1	
PE	Parity Enable	I	1	
SS	Slave Status	I	3	
DS	Data Sync	T	1	for bus arbitration
DK	Data Acknowledge	T	1	
WT	Wait	A	1	for bus arbitration
SR	Service Request	A	1	
RB	Reset Bus	A	1	
BH	Bus Halted	C	1	
AG	Arbitration Grant	TA	1	
AL	Arbitration Level	IA	6	
AR	Arbitration Request	A	1	for bus arbitration
AI	Arbitration Request Inhibit	CA	1	
GK	Grant Acknowledge	TA	1	
			60	
TX	Serial Line Transmit	S	1	for FASTBUS Serial Protocol
RX	Serial Line Receive	S	1	
GA	Geographical Address Pins (position encoded, not bussed)*	F	5	CRATE SEGMENT only
TP	T Pin (not bussed)*	X	1	
DL	Daisy Chain Left	X	3	
DR	Daisy Chain Right	X	3	
TR	Terminated Restricted Use	X	8	
UR	Unterminated Restricted Use	X	2	
FP	F Pins (free use, not bussed)		4	
R	Reserved		5	
Description of Use Symbols				
T	= Timing for address and data cycles			
C	= Control for address and data cycles			
I	= Information for address and data cycles			
A	= Asynchronous—timing not directly related to data transfers			
TA	= Timing for arbitration bus			
IA	= Information for arbitration bus			
CA	= Control for arbitration bus			
S	= Serial data, timing independent of parallel bus			
F	= Fixed information—constant			
X	= Special purpose			

*On CABLE SEGMENTS switches are used instead of GA and T pins.

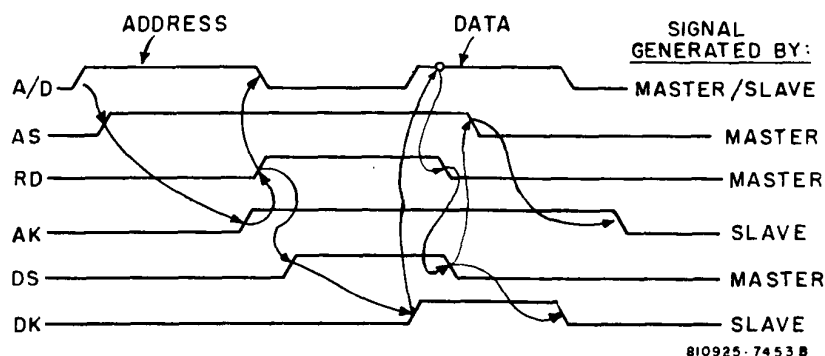


Fig 1.2.1
Basic Handshake Read Operation
(as seen by Master)

Similarly, the three Slave Status information lines, SS, are used to indicate the success or reason for failure of an Address or a Data Cycle. Addressing difficulties can occur at SEGMENT INTERCONNECTS because the SI does not respond (Network Failure) or cannot gain access to its Far-side SEGMENT (Network Busy) or gets preempted by a higher priority operation (Network Abort). Bus lockup caused by unused addresses on the destination SEGMENT are avoided by timers in the MASTER and in the SI which places the address on the destination SEGMENT.

During a Data Cycle, in addition to being able to indicate that it can either accept no more data or has no more data to send, a SLAVE can also signal that it is currently busy or that it has detected one of several classes of error.

1.2.2 Segment Interconnects. A SEGMENT INTERCONNECT monitors the activity on the two SEGMENTS it connects, waiting for an address to appear that is in the set of addresses it has been programmed to recognize. It responds to a recognized address asserted on one of the SEGMENTS (Near-side) by requesting use of the other SEGMENT (Far-side) and asserting the given address on that SEGMENT when it gains control. The two SEGMENTS remain locked together until the operation is complete. The address asserted on the Far-side may, in turn, be recognized by another SEGMENT INTERCONNECT and may be passed to yet another SEGMENT. An arbitrary number of SEGMENTS can be linked as needed for a given operation. The address contains all the information needed to direct the appropriate SIs to form the correct connections.

In order to use the address to provide the routing information in a practical way, the total address space available to the system is divided among the SEGMENTS in such a way that the most significant bits of the address specify which SEGMENT is addressed. This high-order part of the address is called the GROUP ADDRESS (GP) field. More than one GROUP ADDRESS may be assigned to a SEGMENT to accommodate SEGMENTS containing DEVICES using large amounts of address space. DEVICES on a SEGMENT are distinguished by the MODULE ADDRESS which is adjacent to the GP field and may include some of the low-order GP field bits. The combined GROUP and MODULE ADDRESS fields form the

DEVICE ADDRESS which serves to locate a DEVICE anywhere in the system. The remaining (low-order) bits in the address, the INTERNAL ADDRESS FIELD, serve to specify a part or function within the DEVICE. Because of a special type of Data Cycle called the Secondary Address Cycle, the number of different parts or functions within a DEVICE that can be accessed is not limited to the number allowed by the INTERNAL ADDRESS FIELD.

One simple implementation of the SI uses the high-order address bits to address an internal memory that contains a pattern indicating which addresses are to be passed. When the system is initialized, each SI memory is loaded with the patterns needed to route all permitted operations correctly.

With this scheme, there are no restrictions on the kinds of interconnections that may be made between SEGMENTS. For example, they may be connected in a tree structure with a large computer at the trunk and data acquisition DEVICES as the leaves. If a high traffic demand between two widely separated SEGMENTS causes excessive tie-up of the intermediate SEGMENTS, the two SEGMENTS can be directly linked by a SEGMENT INTERCONNECT thus bypassing the intermediate SEGMENTS. No DEVICE address changes are required because of this addition, and once the route tables in the SIs are reinitialized to make use of the new route, the interfering traffic will disappear from the formerly intermediate SEGMENTS. Tree, star, and ring structures can all be accommodated by this scheme.

When a MASTER initiates a FASTBUS operation it always starts an internal Response Timer set to time out at a time appropriate for the SEGMENT on which it resides. If the operation has to pass through one or more SIs, the MASTER must be made aware that additional delays will be encountered before a response is received. Any SI passing an operation asserts WAIT (WT) on the SEGMENT from which the operation arrived and starts a timer suitable for the SEGMENT to which the operation is passed. The WT signal causes a MASTER (and the SI acts as a MASTER on the SEGMENT to which it passes an operation) to stop its timer. The timer is reinitialized when the WT signal is removed. In this way an operation can work its way through a system without causing timeouts to occur unless, of course, a SEGMENT is reached that neither gives a normal response nor asserts the WT signal. A Long Timer in each MASTER is used to detect deadlock situations that arise, for example, when conflicting requests are placed upon resources. After a Long Timer timeout, a MASTER waits for a random Retry Period before again trying to complete the Operation.

1.2.3 Control and Status Registers. Certain registers and functions in DEVICES need to be separated in address space from the normal data registers in a way that provides some protection from accidental access and does not interfere with the allocation of addresses to the normal data portions of the DEVICES. For example, two memory DEVICES should be able to have their addresses set so that the memories are adjacent in address space, allowing them to be used as one larger memory. However, they may contain control registers and status registers associated with memory protection or error detection and correction, and these registers must also be accessible. Furthermore, it is desirable that DEVICES have basic status and information registers in standard locations so that they can be readily accessed by standard shared programs.

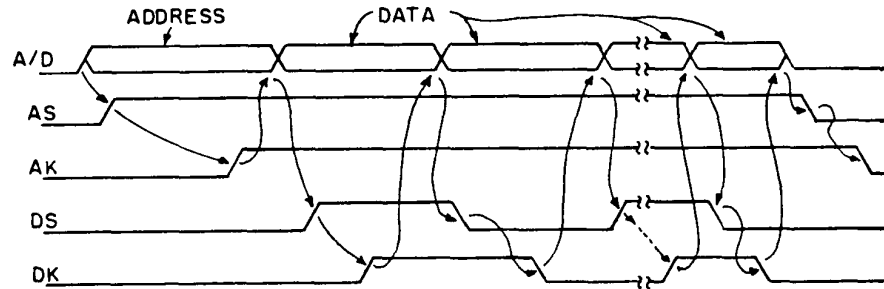
The method chosen to accomplish this is to select control/status register (CSR) space in a primary address cycle by suitable coding of the MS lines. This is followed by a secondary address cycle to select a register in CSR space, and a data cycle to transfer to or from the registers. Secondary addressing provides a full 32-bit address for use within a DEVICE, which is enough address space so that it can easily be allocated in standard ways without fear of a shortage. Standard locations in dedicated CSR registers are specified for all the usual control and status bits. DEVICES are required to contain an identifier unique to the DEVICE type that is used during system initialization. This identifier is located in status register 0 so that even simple DEVICES with no address decoders can respond correctly with little added cost.

1.2.4 Geographical Addressing. The most general form of device addressing is LOGICAL ADDRESSING in which the address of the DEVICE is independent of its physical location in the system. However, FASTBUS only requires that GEOGRAPHICAL ADDRESSING, in which a DEVICE is accessed by addressing its physical location on a SEGMENT, be implemented. Hence it is always possible to determine the location of DEVICES for use as a record or check. GEOGRAPHICAL ADDRESSING must be used to initialize a system having address registers set by software. When such a system is powered up, the registers that will contain the DEVICE ADDRESS information are randomly set. GEOGRAPHICAL ADDRESSING is used to address the DEVICES in order to load their address registers with the proper contents. The first 256 addresses on any SEGMENT are reserved for special purposes and the first 32 of these are used to implement GEOGRAPHICAL ADDRESSING. There are five coded pins (GA4–GA0) at each DEVICE position of a CRATE SEGMENT. These pins are coded so that 0 identifies the rightmost DEVICE position when the crate is viewed from the front and the number coded increases by one for each MODULE position moved to the left. When a GEOGRAPHICAL ADDRESS (0 to 31) is on the bus, the Enable Geographical Address (EG) control line is asserted either by ancillary logic on the segment or by the current MASTER. When EG is asserted during a Primary Address Cycle, DEVICES compare their coded pins with the five low order address bits on the AD lines and respond if a match is found. All DEVICES must have this capability but need not implement LOGICAL ADDRESSING.

The GEOGRAPHICAL ADDRESSING mechanism can be used to access the control and information registers in uninitialized DEVICES so that an automatic procedure can be used to initialize them. The normal logical address recognition logic in a DEVICE is disabled until the DEVICE has been initialized.

Devices on CABLE SEGMENTS use switches to implement the GEOGRAPHICAL ADDRESS.

1.2.5 Block and Pipelined Transfers. A block transfer consists of an address cycle followed by any number of data cycles of the same type, that is, all read or all write. The connection between MASTER and SLAVE is handled as described above with full handshaking at the beginning and end of an operation. Speed is enhanced by making use of both transitions of the Data Sync and Data Acknowledge signal pair while still providing full handshake protection for the data transfers if desired. Fig 1.2.5 shows a Write Block Transfer.



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Fig 1.2.5
Write Block Transfer
(as seen by Master)

It is possible to perform a block transfer without data cycle Handshakes, a Pipelined Transfer, between DEVICES that can handle the same data rates. In the case of a write, for example, after the initial handshake address cycle to establish the AS/AK lock, the MASTER simply asserts data words and DS transitions at whatever rate is appropriate. DK responses are ignored for timing purposes, but should be used for counting the number of words transferred and for monitoring responses. In effect, DS becomes a strobe which the SLAVE uses to find the data words in a synchronous transmission. In the case of a read, the MASTER still provides DS as the clock that the SLAVE uses to determine the transfer rate, but the data is accompanied by DK which the MASTER uses as the data strobe.

Handshake protected operations require each data word to be on the bus for at least two propagation delays, while the data flows to its destination and the acknowledge flows back to the source. When handshake response is not used, however, several data words could be flowing through the bus transmission lines at the same time and data can be transmitted at the full bandwidth of the bus.

In most cases, operations will use full Handshake protection. The data cycle Handshake permits either party to pause, if necessary, and allows either party to terminate an operation early (in case a buffer overflows, for example) with both parties having full knowledge of how many words were successfully transmitted. Operations without data cycle Handshake require the MASTER to know the capabilities of the SLAVE and the bandwidth of the entire path in order to choose a workable DS clock rate. If the operation does not push this rate near its limit, it is better to use the more reliable Handshake mode.

If during the course of a Block Transfer the MASTER detects (via the Arbitration Request line) other users requesting the bus, it may relinquish the bus and later resume the Block Transfer.

1.2.6 Address Locked and Arbitration Locked Operations. The operations described above can be generalized to allow data flow to reverse direction. An Address Locked Operation consists of a primary address cycle followed by any number of secondary address and/or data cycles. For example, during a Read-Modify-Write cycle, the MASTER asserts address information, reads data, reverses

the signal direction on the AD lines by removing the RD signal, and writes the modified data back to the SLAVE. (See Fig 1.2.6.) Such an operation is uninterruptable by any other processor, since it is locked the whole time by the AS/AK lock and no other device can use the bus. It thus forms the kind of indivisible operation needed in multiple processor systems for coordinating use of shared resources.

An uninterruptable operation can be extended even further as long as MASTER and SLAVE agree on the meaning of each bus cycle. For example, the address that connects MASTER and SLAVE could be followed by a secondary address cycle followed by another data cycle.

Address Locked Operations may include Block Transfers. In Address Locked Operations the direction of data flow may be changed between block transfers or between individual non-block transfer words.

A still more general locked operation on the bus is called an Arbitration Locked Operation; a sequence of operations by one MASTER directed to a number of different PRIMARY ADDRESSES that is not interruptable by any other MASTER because the originating MASTER does not allow bus arbitration to take place. This can be very useful for synchronizing a set of SLAVES that are shared by several processors, so that a sequence of operations can be performed without interference by other processors. This mechanism works even if the SLAVES are on different SEGMENTS, as the SEGMENT INTERCONNECT is designed to maintain any connection until the MASTER releases the bus for arbitration.

1.2.7 Sparse Data Scan. In many large data acquisition systems not all DEVICES acquire data in each time interval of interest. FASTBUS provides a mechanism—the Sparse Data Scan—that allows the rapid location of DEVICES containing valid data. The Sparse Data Scan feature makes use of the unbussed T pin located at each DEVICE position on the CRATE SEGMENT backplane. The T pin at position n is connected to Address/Data line n. A MASTER wishing to start a Sparse Data Scan issues a broadcast command to all appropriate DEVICES on a SEGMENT asking those with data to respond on their T pins. A read of the AD lines then indicates which DEVICES should be interrogated for data. This

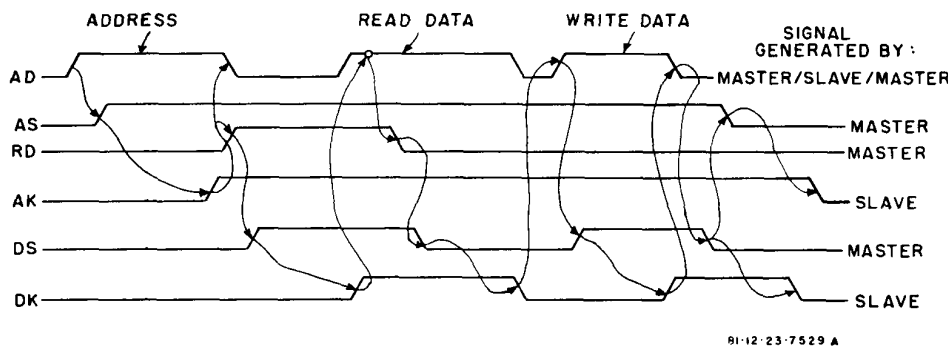


Fig 1.2.6
Address-Locked Operation:
Read-Modify-Write (as seen by Master)

capability can be provided on a CABLE SEGMENT by using patch pins or switches.

1.2.8 Broadcast Operations. In a Broadcast operation, a MASTER can connect to more than one SLAVE during a single PRIMARY ADDRESS cycle. Broadcasts can be used for various purposes, such as synchronizing DEVICES or clearing a bank of counters. Since several SLAVES may be involved, no meaningful handshake between SLAVE and MASTER is possible. However, a SYSTEM HANDSHAKE from ancillary logic on each segment of any route informs the MASTER that its command has propagated to every SEGMENT to which it was addressed. The MASTER asserts an address along with an MS code to indicate that a Broadcast address is being asserted. The Address Field is used to specify whether the Broadcast is to be a LOCAL one to a specific SEGMENT or a GLOBAL one either to all SEGMENTS in a pattern controlled by information in the SEGMENT INTERCONNECTS or to all SEGMENTS beyond a specified one. In addition to being able to specify the SEGMENTS to be affected by a Broadcast, the Address Field can be used to select either a class of DEVICE on the affected segments or a function to be carried out. Defined functions include the Sparse Data Scan, DEVICE T pin assertion (either unconditionally or only if the DEVICE is asserting a Service Request) and addressing by MASTER T pin assertion on the next cycle.

In SEGMENT INTERCONNECTS the route table entries corresponding to a GROUP ADDRESS of zero are used for routing Global Broadcasts. More than one SEGMENT INTERCONNECT may recognize and pass a Broadcast message since no individual Handshakes are returned. The pattern formed by a propagating Broadcast message must be a simple tree with no cross connections. This rule has to be enforced by the initialization program.

When the Broadcast address has propagated successfully throughout the system, the SYSTEM HANDSHAKE is generated by the ancillary logic in cooperation with the SEGMENT INTERCONNECTS. The following Data Cycles make use of the SYSTEM HANDSHAKE. Thus, any kind of standard Write or Read Operation may be performed simultaneously on a set of DEVICES by a Broadcast.

Broadcasts may take some time to start, since they must wait for all conflicting use of the SEGMENTS involved to complete. Once the system connection is complete, however, speed of execution of the Data Cycles is limited only by System Handshake and propagation delays.

1.2.9 Arbitration for Bus Mastership. One of the most important requirements of a multi-processor system is a method for allocating control of the SEGMENTS to the various MASTERS that may be contending for bus Mastership simultaneously. Part of the circuitry to accomplish this, which resides on each independent SEGMENT, is called the Arbitration Timing Controller (ATC).

Ten bus lines are dedicated to SEGMENT priority arbitration. Each master is assigned a six-bit Arbitration Level. Masters wishing to gain bus mastership assert the Arbitration Request line (AR). If the Grant Acknowledge, GK, line is not asserted, the Arbitration Timing Controller starts an Arbitration Cycle by asserting the Arbitration Grant, AG, signal. Requesting Masters respond by asserting their arbitration levels on to the six Arbitration Level lines, AL. On each Arbitration

Level line an asserted bit will override any non-asserted bits. Each requester continually compares its Arbitration Level with the code on the AL lines bit-by-bit from most to least significant positions. If a requester detects a bit on the bus, which it is not asserting, it removes from the bus all of its own bits of lesser significance. After a time determined by the ATC, only the highest Arbitration Level remains asserted on the AL lines and each competitor knows if it has won or lost. When the Arbitration Timing Controller has determined that the bus is completely free ($AS = AK = WT = GK = 0$), it stops asserting AG and the winning MASTER responds by asserting GK and assuming bus Mastership. The MASTER continues to assert GK until it is willing to allow another Arbitration Cycle. This is usually after the last Address Cycle of its sequence of operations thus allowing the next MASTER to be selected before the current MASTER has finished its Data Cycles.

Two compatible protocols are possible with the specified arbitration scheme. In one of these protocols Arbitration Requests are made without regard to the presence of any other requests leading to the possibility of low priority MASTERS being denied bus mastership for intolerably long periods of time. In the other, the *assured access* protocol, Arbitration Requests are made only if the Arbitration Request Inhibit line is false. This line is set by the ATC at the start of an Arbitration Cycle and reset only when no Arbitration Requests are outstanding. Hence, all Arbitration Requests existing at a given instant of time are satisfied before any new ones can be made. MASTERS using either protocol can share the same SEGMENT since the protocols differ only in the conditions for asserting AR.

Of the 64 possible priority codes, zero is not used because it is easily confused with an idle bus. Codes 1 through 31 are available for use within the SEGMENT, and 32 through 63 are available for use as *system* priorities for unique assignment within communicating parts of a system. The Local priorities 1-31 must be assigned uniquely to DEVICES within a given SEGMENT, but can be reused on every SEGMENT. When a SEGMENT INTERCONNECT connects a MASTER to another SEGMENT, the Level used for arbitration on the second SEGMENT will normally be that of the SI rather than that of the originating MASTER. However, if one of the system priorities was used by the originating MASTER, the SI will propagate that priority onto the second SEGMENT, which it is free to do since the system priorities are unique along a route. The system priorities can be useful in preventing undue delay for important Broadcasts, and can help expedite important messages which might otherwise suffer from fluctuating priorities as they form paths through the system.

No interruption or preemption of the current operation is possible. A MASTER is free to keep the bus as long as it wishes. If it sees $AR = 1$ while $AS = AK = 1$, it knows that other MASTERS in the system are being blocked by the current operation. The controlling MASTER should normally release the bus within a reasonable time in order to allow other MASTERS to acquire bus Mastership. It should allow either one Arbitration Cycle or a random Retry Delay to occur before again requesting bus Mastership. The general solution to the problem of contention and deadlock in FASTBUS is to give up and retry after a random delay.

1.2.10 Interrupts. An Interrupt is a request from a DEVICE to a processor for service or attention. Since Interrupts may have to cross SEGMENT boundaries, and since they must carry information, they are handled by normal FASTBUS operations.

The interrupting DEVICE addresses an interrupt-sensing control register region in a processor interface and writes its own address and possibly other information into the registers. The processor then has all the information needed to access the interrupting device and service it at some later time.

In some systems, large numbers of simple DEVICES may need to make requests for service without having the capability of gaining bus mastership and performing an interrupt write operation. Such DEVICES may assert the Service Request (SR) line, which can be monitored by a special Service Request handling device. This device can gain Mastership and find the requester by means of the T pins, polling, or other means. The Service Request handling DEVICE may then perform the necessary service itself or it may send a normal Interrupt message on behalf of the simple requester to some other processor. SEGMENT INTERCONNECTS can be instructed to pass SR from one SEGMENT to the other.

1.2.11 Timing. The relationships between the timing signal transitions in FASTBUS are defined in an implementation independent manner and supplementary timing information is required for guaranteed operation in a specific environment. This information falls into two classes:

- (1) Signal delays to ensure that correct mutual timing relationships are met and that bus signals are of sufficient duration to be recognized.
- (2) Timeouts in MASTERS that recognize that an expected response has failed to occur and to initiate a recovery procedure.

An associated signal, WT, when asserted, has the action of blocking subsequent bus timing signals and also resetting Master timeouts. Thus, it can be used to freeze the state of the bus for diagnostic purposes; in addition, however, it is used as part of the intersegment timing protocol so that timeouts need to be specified only for local rather than global conditions.

1.2.12 Initialization. Upon power-up all DEVICES are placed in a passive state and respond only to Geographical Addressing. They must therefore be initialized before use. Initialization consists in carrying out a number of operations some of which, such as the proper setting of Logical Addresses and loading of Route Tables in SIs, require a general knowledge of the entire system and its structure; while others, such as the setting of amplifier gains or zeroing counters, are peculiar to a given DEVICE or group of DEVICES.

For each FASTBUS system one processor, the HOST, contains a complete description of the system to which it is attached. The FASTBUS system must be so structured that every DEVICE in it can be accessed by the HOST. The HOST, with its knowledge of the system structure, can by standard algorithms initialize Route Tables in SIs ensuring that rules concerning routes and Broadcast trees, as well as any compatible constraints imposed by the user, are followed. The HOST's initialization program also assigns Arbitration Levels to MASTERS and Logical Addresses to DEVICES and carries out DEVICE specific operations.

The initialization process proceeds in a methodical way. First, all the SIs, start-

ing with those on the same SEGMENT as the HOST and then working outward, are initialized. For each SI the HOST first accesses the Near-side and loads the Route Table and Arbitration Level for Operations to its Far-side. Operations to the Far-side are then enabled and the HOST loads the Far-side Route Table and Arbitration Level and finally enables the SI for Operations in the opposite direction, that is, back towards the HOST. This continues until all SIs have been initialized. SLAVES and MASTERS are initialized next. Enabling of MASTERS is carried out last to avoid the possibility of a MASTER trying to access as yet uninitialized parts of the system.

All FASTBUS system topology information, as well as data specific to the initialization of each DEVICE, is best maintained in a data base managed by the HOST. After system initialization it may be necessary to refer to this data base if problems arise with the system or a DEVICE. For example, DEVICES seeing RB normally require, at the least, being reenabled; and replacement DEVICES require initialization. The centralization of the required information and actions makes for a more easily managed system.

1.2.13 Diagnostic Tools. Because all FASTBUS signals appear at each position of a CRATE SEGMENT, a DEVICE can be placed in the crate to monitor all FASTBUS activity. It is possible to design such DEVICES so that they respond to only certain types of operations. The Bus Cycle history can be stored in the DEVICE for later recall and analysis.

A powerful yet simple diagnostic tool is provided by such a DEVICE which has the ability to assert the WT signal. Besides resetting and inhibiting the Response Timer in MASTERS, this signal inhibits any changes in the state of the five timing signals, AG, AS, AK, DS, and DK, effectively stopping all activity on the FASTBUS. Hence, the state of the bus can be examined after each timing transition using simple test equipment, by removing and reapplying WT.

2. Conventions, Definitions, Abbreviations, and Symbols

This section includes notations, logic signal conventions, definitions, abbreviations and symbols used in conjunction with this document.

2.1 Interpretation of this Standard

Clauses using the word *shall* are mandatory. Clauses enclosed in blocks, as here, are mandatory.

Definitions of recommended or preferred practice (to be followed unless there are sound reasons to the contrary) include the word *should*.

Examples of permitted practice generally include the word *may* and leave freedom of choice to the designer or user.

Decimal notation is normally used in the text. Except where clear in the context, binary numbers are followed by the letter b (that is, 01100b) and hexadecimal numbers by the letter h (that is, 1A3F5h).

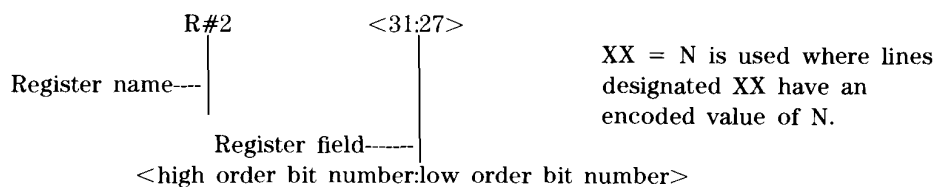
In order to conform with the specification of the FASTBUS system, an equipment or system shall satisfy the mandatory requirements in this standard.

Non-FASTBUS equipment that does not interfere with the operation of the FASTBUS features as defined in this standard is considered compatible with the FASTBUS system.

No part of this standard is intended to exclude the use of equipment that is compatible in the preceding sense, even if it does not conform fully to the specification.

No license or other permission is needed in order to use this standard.

2.2 Notations and Logic Signal Conventions. The following notation is used in this document for defining registers and bits in registers:

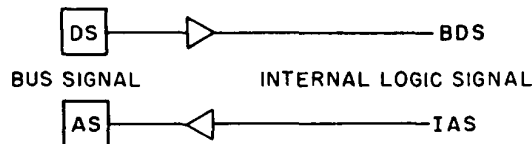


Positive logic is assumed, that is, the higher state of the signal is true; the lower state is false. Signal names reflect this, that is:

AK implies that if high it is true.

AK* implies that if high it is false, that is, AK is active low.

If FASTBUS were implemented in ECL, one would label the bus signal Address Acknowledge AK, but in a TTL system the label would be AK*. Bus signals are usually boxed in logic circuits. For example see adjacent figure.



Logic graphic symbols used generally conform with ANSI/IEEE Std 91-1984, IEEE Standard Graphic Symbols for Logic Functions, using positive logic or IEC Pub 113-7-1981, Part 7: Preparation of Logic Diagrams.

Use of positive logic symbols as in ANSI/IEEE 91-1984 is recommended. Using these symbols to interconnect lines usually results in non-negated outputs being connected to non-negated inputs.

The following examples show the notation used for Lines and Signals:

SS	All SS Lines and Signals
SS0	SS Line or Signal with weight 1
SS1	SS Line or Signal with weight 2
SS2	SS Line or Signal with weight 4
SS = 2	Encoded value of the set of SS Lines or Signals
SS<2:0>	SS2, SS1 and SS0
SS1 = 1	Logic state of SS1

2.3 Definitions

Address. Synonymous with Primary Address.

Address Cycle. Synonymous with Primary Address Cycle.

Address Locked Operation. An Operation directed to a single Primary Address containing a mixture of Read and Write Cycles, possibly including Block Transfers as well.

Ancillary Logic (ANC). Logic required for each Segment but not part of any Device. Operations associated with Arbitration, Geographical Addressing, System Handshake and Run/Halt Control are carried out in the Ancillary Logic which may also contain Segment terminators.

Arbitration Cycle. The process by which the next Master to be granted bus mastership is determined. It is initiated by the Arbitration Timing Controller and is complete when the winning Master assumes bus mastership.

Arbitration Locked Sequence. A sequence of operations by one Master, directed to a number of different Primary Addresses, which is not interruptable by any

other Master because the originating Master does not allow bus arbitration to take place.

Arbitration Timing Control (ATC). Logic associated with each Segment for the purpose of supervising and generating the arbitration control signals, Run/Halt control and Broadcast System Handshake. (This is part of the Ancillary Logic.)

Assured Access Protocol. A potential Master is operating in the Assured Access Protocol if, on detecting an AI assertion, it will not assert AR and thus will not participate in subsequent Arbitration Cycles until all Devices currently asserting AR have obtained bus Mastership and completed their operations.

Backplane. Circuit board (typically printed) at the rear of a Crate which, by means of its attached connectors, mates with the Modules and constitutes the Crate Segment.

Base Group Address. The Group Address (GP) value which is used for Geographical Addressing on a Segment. Normally the lowest GP assigned to the Segment.

Block Transfer. The portion of a FASTBUS Operation in which a Master either sends data to or receives data from an Attached Slave on every transition of Data Sync. The Slave acknowledges receipt of or sends data with every transition of Data Acknowledge.

Broadcast (Broadcast Operation). An operation directed to one or more Slaves on one or more Segments.

Broadcast Address. A Primary Address asserted by a Master during a Broadcast.

Broadcast, Global. A Broadcast to Slaves on all Segments of a Multi-Segment system that can be reached from the originating Segment.

Broadcast, Linear. A Broadcast to a subset of the Segments affected by a Global Broadcast. The subset can be either a specified Segment or up to a specified Segment or beyond a specified Segment.

Broadcast, Local. A Broadcast which is effective only on the originating Segment.

Buffered Interconnect (BI). A Device which implements an inter-Segment connection such that the FASTBUS Protocol (FBP) on one Segment is not synchronized with that on the other.

CAMAC. An internationally standardized modular instrumentation and digital interface system as defined in ANSI/IEEE Std 583-1982, IEEE Standard Modular Instrumentation and Digital Interface System (CAMAC), and the corresponding documents EUR 4100-1972, CAMAC: A Modular Instrumentation System for Data Handling, and IEC Pub 516-1975, A Modular Instrumentation System for Data Han-

dling; CAMAC System. (CAMAC is often treated as an acronym for "Computer Automated Measurement and Control.")

Connected System. All Segments of a Connected System are capable of communicating directly with one another through SIs. Note that because of the route map table implementation of message paths Segments of a system that are connected electrically by SIs are not necessarily also logically connected in the sense used here.

Control and Status Register (CSR). A register used to control the operation of a Device and/or record the status of an Operation. It is accessible through a separate Address Space in a FASTBUS Device. CSR#0, mandatory for all Devices, contains the manufacturer's ID for the Device and a number of Device status bits as well as some user defined bits.

CSR Space. A FASTBUS Primary Address Cycle may specify with a code on the MS control lines one of two separate address spaces in a Device: CSR Space and Data Space. CSR Space contains registers for control of and status reporting registers for the Device. Its allocation and usage is a part of the FASTBUS specification. See also Data Space.

Crate (FASTBUS Crate). The mechanical housing for FASTBUS modules in a Crate Segment.

Daisy-Chain. A backplane connection between adjacent Module stations that allows information to flow between Modules independent of the FASTBUS protocol.

Data Cycle. The portion of a FASTBUS Operation in which a Master either sends data to or receives data from an attached Slave. It begins with the Master causing a Data Sync transition and terminates with the Master receiving a Data Acknowledge transition from the Slave.

Data Space. That address space which Devices may have which is recommended for use in data operations. There are few constraints applied to Data Space uses. See also CSR Space.

Device (FASTBUS Device). Any equipment capable of connecting to a Segment and responding to the mandatory features of the FASTBUS Protocol.

Device Address (DA). The (32-m)-bit identifying number assigned to a FASTBUS Device that is compared with the signals on the AD lines during a Logical Primary Address Cycle of a FASTBUS Operation. The Device Address is formed by the Group and Module Address Fields. The (remaining) low-order m-bits are assigned to the Internal Address Field.

Device Class—Broadcast. Selective Broadcast-Class specified by CSR#7. Controls Device response to subsequent cycles within the Broadcast.

ESONE. A multi-national committee representing European nuclear laboratories. It produced the initial CAMAC specification and collaborates with NIM in the maintenance and extension of CAMAC and in the development of FASTBUS.

Far-Side (of an SI or BI). That port of an SI or BI electrically farther from the originating Master.

FASTBUS. The standard modular high-speed data acquisition and control system defined by this document.

FASTBUS Protocol (FBP). The format and sequence of control and data messages in FASTBUS. Formats are specified by the FASTBUS signal line assignments. Sequences are specified by Operations.

Geographical Address (GA). The Primary Address of a Device based on the physical (Geographical) location of the Module, and determined by coded backplane pins, or (on a Cable Segment) by switches. For a Crate Segment Geographical Address zero is for the rightmost position when the Crate is viewed from the front and the address increases by one for each Module position moved to the left.

Geographical Address Control (GAC). Logic associated with each Segment for supervising and generating signals for Geographical Addressing.

Group Address (GP). The high order (left justified) bits assigned in the Device Address Field of a FASTBUS Address which are used to identify the Segment on which a Device is located; more than one Group Address may be assigned to a given Segment. See Base Group Address.

Handshake. An interlocked exchange of signals between a Master and a Slave, controlling the transfer of data.

Host Processor. The data processing and control processor assigned to exercise overall supervision over a FASTBUS system. Contains detailed knowledge of the system topology.

Interconnect. See Segment Interconnect and Buffered Interconnect.

Internal Address Field (IA). The group of low-order bits (right justified and contiguous to the Device Address Field on the left) assigned in the Address of a FASTBUS Device which is used to identify internal locations within a FASTBUS Device. Secondary Address Cycles allow the number of different locations accessed to exceed that available in the Internal Address Field.

Interrupt Operation. A FASTBUS Write Operation to an Interrupt Service Device, notifying it that the sender requires attention.

Interrupt Service Device (ISD). A Processor or other Device which can respond to Interrupt Operations.

Logical Address. A Primary Address of 32 bits consisting of the Device Address and Internal Address. It is independent of the location of the Device on a Segment.

Master. A Device which is capable of asserting or controlling an Operation on a Segment according to the FASTBUS Protocol. A Master may, in addition, contain Slave logic.

Mastership. A Master is asserting Mastership when it has control of the Segment to which it is attached and is asserting GK or AS.

Minimum Pulse Down Time. In order for all Devices to detect the zero state of a signal between the occurrence of two successive one states of the signal, the zero state must last for at least a bus dependent Minimum Pulse Down Time.

Module (FASTBUS Module). Any FASTBUS Device that can be housed in a FASTBUS Crate, that can connect to a Crate Segment and that conforms with the mandatory specifications in this Standard for a FASTBUS Module.

Module Address (MA). The group of bits assigned in the Device Address Field of a FASTBUS Address which identifies the Module on its Segment. The Module Address may partially overlap the Group Address.

Module Auxiliary Connector. The standard connector that mounts above the Module Segment Connector on a Module Circuit Board.

Module Circuit Board. The printed board that is the circuit part of a FASTBUS Module.

Module Segment Connector. The standard connector that mounts on a FASTBUS Module and mates with the Crate Segment Connector for connection of the Module to the Segment.

Module Supplementary Board. Any board in a FASTBUS Module that does not make connection with the Crate Segment.

Near-Side (of an SI or BI). That port of an SI or BI that is electrically closer to the originating Master.

Next Transfer Address. A pointer in a Slave to the Module register which will be accessed during the next data transfer. The NTA Register may be written during a Primary Address Cycle and may be Read or Written during a Secondary Address cycle. During Block and Pipelined Transfers the NTA may be automatically modified between Data Cycles.

NIM. (1) A committee sponsored by the US Department of Energy and associated with the US National Bureau of Standards. It produced the NIM instrumentation

system specifications, endorsed the use of CAMAC, and collaborates with ESONE in the maintenance and extension of CAMAC.

(2) A standardized modular instrumentation system consisting of NIM MODULES and NIM BINS as defined in US Department of Energy Report TID-20893, Standard Nuclear Instrument Modules.

Null Operation. A Primary Address Cycle followed by no Data Cycles. It determines if the system contains a Device capable of responding to the Primary Address used. It can be used to reserve Segment Interconnects for an Arbitration Locked Sequence.

Operation. A Primary Address Cycle followed by zero or more Data Cycles and a Termination Sequence.

Parity (for FASTBUS). A bit, optionally appended to a FASTBUS word, whose value is chosen to make the total number of one bits (including the parity bit) odd. It is used for error checking since receipt of an even number of one bits implies a transmission error.

Pattern Select. A Broadcast Address specifying that all Devices seeing the Broadcast remain attached to the Master only if their T pins are asserted during the immediately ensuing Write Data Cycle.

Pending Master. The Master which participated in and won the most recent Arbitration Cycle. As a result it will assume bus Mastership when the current Master releases the bus.

Pipelined Transfer. The portion of a FASTBUS Operation in which a Master either sends data to or causes data to be sent by an Attached Slave on every transition of Data Sync. The Slave acknowledges receipt of or sends data with every transition of Data Acknowledge. The Master does not wait for an acknowledge signal from the Slave before causing another Data Sync transition.

Position. The location of a Module in a Crate. The Position number corresponds to the Geographical Address.

Primary Address. An address assigned to a Device by means of which a Master is able to establish contact with the Device or a subdivision of the Device. Primary Address types are Logical, Geographical and Broadcast Addresses.

Primary Address Cycle. The portion of a FASTBUS Operation in which a Master addresses a Slave on the Address/Data (AD) lines. The address type is specified by the EG and MS control lines. It begins with the Master asserting the Address Sync (AS) line and terminates with the Master receiving an Address Acknowledgement on the AK line. Logical, Geographical or Broadcast Addresses are asserted during Primary Address Cycles.

Processor Interface (PI). The interface device between a Processor and a FASTBUS Segment.

Read Cycle (Read). A cycle in which the direction of data flow is from Slave(s) toward a Master.

Reserved. Bus lines, connector pins, codes, bits, etc held for future assignment by the NIM Committee. They are not to be used until and except as so assigned.

Response Timer. A timing device within a FASTBUS Master or Segment Interconnect used to terminate an Operation which has failed to complete within a given (excessive) period of time.

Retry Period. The time a Master waits after failing to receive a response before trying the Operation again. This time should be randomized to avoid system deadlocks.

Route Table. The list of Group Addresses recognized by an SI for passing Operations to its Far-Side Segment.

Route Tracing Mode. A mode of SI operation which generates an error diagnostic response instead of the normal passing of an Operation.

Run/Halt Switch (RH). A switch normally operated by the Run/Halt switch activator bar on Crate Segments and on the ATC on Cable Segments which stops bus traffic so that Modules can be safely inserted or removed without affecting other Modules on the Segment.

Secondary Address. An Address for use within a Device. It is provided by a Secondary Address Cycle which loads the NTA register of the Device following a Primary Address Cycle or a Data Cycle.

Secondary Address Cycle. A Data Cycle in which a Master uses the Address/Data (AD) lines to load a Secondary Address into the NTA register of a Device.

Segment. A specific transmission medium which supports the FASTBUS Protocol and to which FASTBUS Devices may attach. A Segment is capable of supporting autonomous operation and communicating with other Segments via Segment Interconnects.

Segment, Cable. A FASTBUS Segment consisting of a cable together with appropriate connectors for mating with Devices.

Segment, Crate. A FASTBUS Segment that consists of a backplane mounted on a FASTBUS Crate and having connectors to mate with a multiplicity of FASTBUS Modules.

Segment, Extended. A multiplicity of Crate Segments accessed by the same Group Address. Unlike Operations on Segments linked by Segment Interconnects, independent Operations on each of the Segments that are part of an Extended Segment never proceed concurrently. Depending on the method of implementation, some restrictions may exist as to the placement of Masters. Depending on the disposition of Modules on the Extended Segment, some Broadcast Operations may not be useable or may require special interpretation.

Segment Extender (SE). A Device for connecting two Segments to form an Extended Segment or part of an Extended Segment.

Segment Interconnect (SI). A Device which implements an inter-Segment connection such that the FBP on the two Segments is synchronized. When an Operation is passing through an SI, the SI acts as a Slave on the Near-side and as a Master on the Far-side.

Segment Interconnect, Active. A Segment Interconnect is said to be Active if it is asserting AS=1 on the Far-Side Segment.

Segment Interconnect, Reserved. A Segment Interconnect is said to be Reserved if it has gained mastership of the Far-Side Segment and is asserting GK=1 onto that Segment.

Service Request Handler (SRH). A Master responsible for monitoring the Service Request line, SR, on a Segment or a group of Segments. When SR = 1 the SRH requests Bus Mastership and after obtaining Mastership determines which Module(s) is asserting SR, either by polling or by a Broadcast Operation. The SRH may subsequently service the pending request(s) itself, or may issue Interrupt Messages to other Devices on behalf of the Module(s) asserting SR. SR is usually asserted only by Modules which lack Mastership capability.

Skew Time. The minimum time that the assertion of a FASTBUS timing signal must be delayed after the assertion of information and/or control signals to allow for differences in propagation time of signals on a FASTBUS Segment.

Slave. A Device which responds to Masters according to the FBP.

Slave, Attached. An Attached Slave is one that in the previous Primary Address Cycle recognized its address and address type and as a result will participate in the ensuing Data Cycles.

Slot. A Module connector position on a Crate Segment backplane (see Position).

Sparse Data Scan (SDS). A technique by which arrays of modules with low data occupancy may be scanned efficiently, i.e., without accessing every potential data site.

System Handshake. A Handshake in a Broadcast Operation where the Handshake signal is from the last Segment of the addressed system rather than from individual Devices.

Termination Sequence. The process by which the AS/AK lock is broken.

Timeout. A Timeout occurs when a protective timer completes its assigned time without the expected event occurring. Timeouts prevent the system from waiting indefinitely in case of error or failure.

Tree Structure. A set of Connected Segments with no loops (cross connections).

Wait Timeout Period. The time a Master will wait after recognizing WT before terminating the Connection.

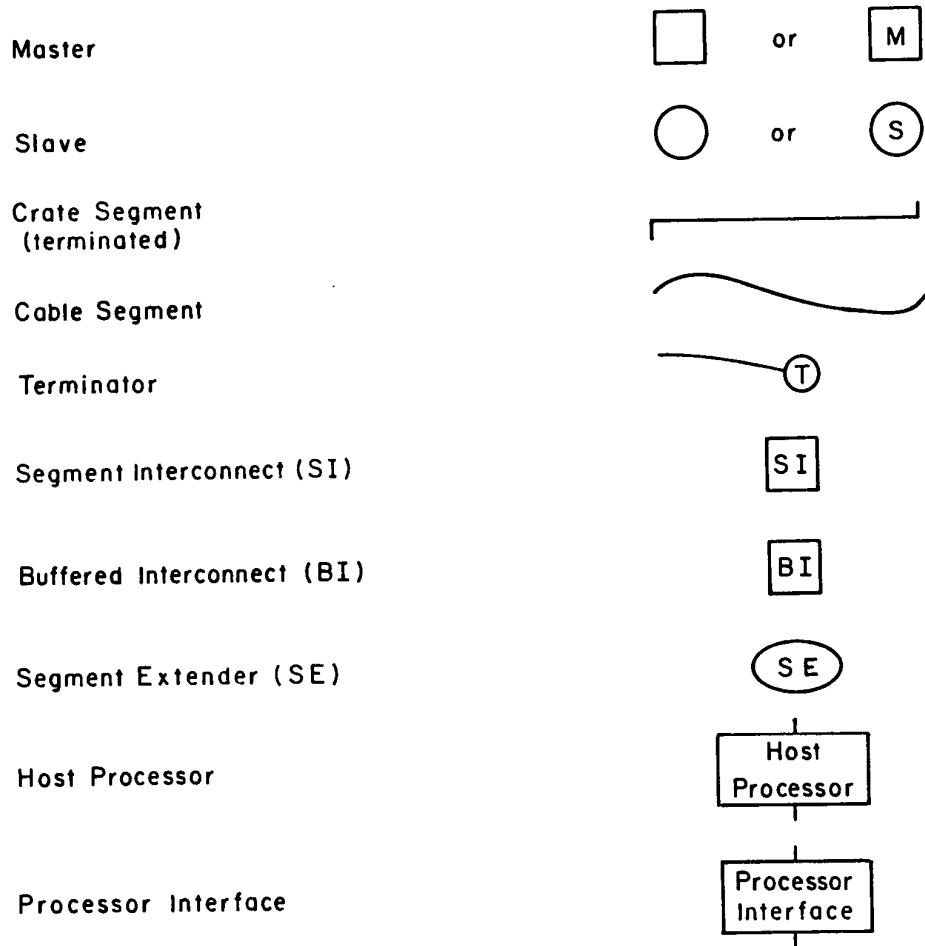
Write Cycle (Write). A cycle in which the direction of data flow is from a Master to Slave(s).

2.4 Acronyms

A	Asynchronous (Type of line)
AD	Address/Data
AG	Arbitration Grant
AI	Arbitration Request Inhibit
AK	Address Acknowledge
AL	Arbitration Level
ANC	Ancillary Logic
AR	Arbitration Request
AS	Address Sync
ATC	Arbitration Timing Control
BH	Bus Halted
BI	Buffered Interconnect
C	Clear Bit
C	Control (Type of line)
CA	Control for Arbitration Bus (Type of line)
CSR	Control and Status Register
DA	Device Address
DAR	Daisy Chain A Return
DBR	Daisy Chain B Return
DK	Data Acknowledge
DL	Data Chain Left
DLA	Daisy Chain Out Left
DLB	Daisy Chain In Left
DRA	Daisy Chain In Right
DRB	Daisy Chain Out Right
DS	Data Sync
ECL	Emitter-Coupled Logic
EG	Enable Geographical
F	Fixed Information (Type of pin)
F (pins)	Free Pins
FBP	FASTBUS Protocol
FIFO	First In, First Out
G	Global Bit
GA	Geographical Address
GAC	Geographical Address Control
GK	Grant Acknowledge

GP	Group Address
GP	Group Address Field
I	Information (Type of line)
IA	Internal Address
IA	Information for Arbitration Bus (Type of line)
ID	Device Identification
IDC	Insulation Displacement Connector
ISD	Interrupt Service Device
L	Local Bit
LED	Light Emitting Diode
LSB	Least Significant Bit
M	Master
MA	Module Address
MAC	Module Auxiliary Connector
MCB	Module Circuit Board
MS	Mode Select
MSB	Most Significant Bit
MSC	Module Segment Connector
NTA	Next Transfer Address
PA	Parity
PE	Parity Enable
PI	Processor Interface
PROM	Programmable Read-Only Memory
R	Read
R	Reserved Line
RB	Reset Bus
RD	Read Line
RH	Run/Halt Switch
RX	Receive Serial Line
S	Slave
S	Set Bit
S	Serial Data, Timing Independent of Parallel Bus (Type of line)
SDS	Sparse Data Scan
SE	Segment Extender
SHL	System Handshake Logic
SI	Segment Interconnect
SR	Service Request
SRH	Service Request Handler
SS	Slave Status
T	Timing (Type of line)
TA	Timing for Arbitration Bus (Type of line)
TP	T Pin
TR	Terminated Restricted Use Line
TTL	Transistor-Transistor Logic
TX	Transmit Serial Line
UR	Unterminated Restricted Use Line
W	Write
WT	Wait

2.5 Symbols



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3. Signals, Signal Lines, and Pins

This section contains a description of the terminology used when referring to signals, signal lines and pins as well as a brief outline of their usage.

3.1 Types of Signal Lines. The signals used by FASTBUS may be classified in the following way:

Timing. Transitions of these signals are used to delimit FASTBUS cycles involving either address, data or arbitration information.

Control. The level of these signals is examined at the transition of a timing signal to further specify the type of operation. Interpretation of the Control Lines is dependent upon the associated timing transition.

Information. The level of these signals at a transition of a timing signal is associated with the action specified by the control lines and the initiating timing transition.

Asynchronous. A number of FASTBUS signals may be initiated by events which are not synchronized with the FASTBUS protocol. Examples are Service Request and Arbitration Request.

Serial Data. An independent serial bus which implements the FASTBUS Serial Network Protocol.

Fixed. Information indicating a Module's physical position on a Crate or Cable Segment is Fixed in that this information is associated with physical position and cannot be changed by FASTBUS Operations.

3.2 Signal Nomenclature. Signals are designated in the following way: If XX is the bus signal, then on logic diagrams BXX is used to designate the buffered (In) bus signal and IXX the internally generated (Out) bus signal. The state, or change of state, of the XX signal is indicated as follows:

XX(u)	The 0 to 1 transition (up).
XX(d)	The 1 to 0 transition (down).
XX(t)	The transition from one level to the other (toggle).
XX=1	Signal asserted.
XX=0	Signal not asserted.

3.3 Brief Description of Signals, Lines, and Pins. In addition to containing the name of the signal to be described each subheading in this section includes, in brackets, the signal usage as defined in Table 1.2.1 followed by the possible sources of the signal. Unless otherwise stated in the description, each signal is implemented as a bussed line in both Crate and Cable Segments.

The FASTBUS signal lines and pins described in Section 3.3 shall be provided on FASTBUS Segments and shall be used in accordance with the mandatory requirements detailed in this document.

3.3.1 AS Address Sync (T, Master). The AS timing signal is asserted a skew time after the Address/Data (AD) and Mode Select (MS) lines have been asserted by a Master that has acquired bus mastership. On receipt of this signal, Slaves compare the address and its type with those that it has been designed or programmed to recognize. Slaves that do not recognize the address take no further action until the next AS(u) when they again make the address comparison.

3.3.2 AK Address Acknowledge (T, Slave, or ANC). The AK timing signal is asserted by a Slave upon recognition of either its Geographical or Logical Address in a Primary Address Cycle. The receipt of AK by the originating Master indicates that, according to the state of MS<2:0>, either a single Slave or a Broadcast connection has been made. For a single Slave connection AK is generated by the Slave while for a Broadcast connection AK is generated by the Ancillary Logic.

3.3.3 EG Enable Geographical (C, Master, or ANC). The EG control signal is asserted by a Master or by the Ancillary Logic. On receipt of this signal Slaves compare their Geographical Address as determined by the coded GA pins on a Crate Segment, or by switches on a Cable Segment Device, with the Address coded on the low order AD lines.

3.3.4 MS Mode Select (C, Master). The three Mode Select control signals are asserted by a Master during an Address Cycle to specify the type of connection. During Data Cycles the Master asserts these lines and RD to specify the data transmission mode. For an Address Cycle MS indicates access to either Data Space or CSR Space of a specific Device or several Devices (Broadcast mode). For a Data Cycle the MS control signals specify Random Data, Secondary Address, Block Transfer or Pipelined Transfer.

3.3.5 AD Address/Data (I, Master, or Slave). The thirty-two AD information lines are used to transfer information during FASTBUS Operations. The AD signals are asserted by the Master for Write Cycles and by the Slave for Read Cycles. The lines are designated AD<31:00> where AD31 is the most significant bit.

3.3.6 SS Slave Status (I, Slave). In a Primary Address cycle the three SS information signals are asserted by a Segment Interconnect or a Slave to indicate the status of the Network or Device connection respectively. In a Data Cycle these signals are asserted by an Attached Slave to indicate the Slave's status. In both cases an SS=0 response indicates that the cycle was successful.

3.3.7 DS Data Sync (T, Master). The DS timing signal is asserted by a Master to initiate a Data Cycle. On receipt of this signal, Attached Slaves examine the RD signal to determine whether to assert data on the AD lines (RD=1, Read) or to

accept data ($RD=0$, Write). $MS<2:0>$ are likewise interpreted to determine the mode of the operation. The Master must wait a skew time after settling of the control and information lines before asserting DS.

3.3.8 DK Data Acknowledge (T, Slave, or ANC). A single Attached Slave always asserts the timing signal DK in response to DS. For the Broadcast mode DK is issued by the System Handshake (see Section 7). The status of MS at Primary Address time determines the source of DK.

3.3.9 RD Read (C, Master). The Master asserts RD to specify to the Attached Slave the direction of data flow on the AD, PE, and PA lines. For Address and Write data cycles $RD=0$ and the Master asserts AD, PE and PA; for Read data cycles $RD=1$ and the Slave asserts these lines.

3.3.10 PE Parity Enable (I, Master, or Slave). The PE information signal is asserted by a Device to indicate that odd parity is being generated for the AD lines. The line may be asserted by a Master for Address and Write Cycles and by Slaves for Read Cycles. The assertion of PE does not guarantee that a parity check will occur.

3.3.11 PA Parity (I, Master, or Slave). The Master or Slave generating parity asserts PA. PA is set to logic 1 if $AD<31:00>$ has an even number of bits set to logic 1.

3.3.12 WT Wait (A, Any Device). The assertion of WT resets and inhibits response timeouts in a Master and inhibits a Master's or Slave's assertion of timing transitions. This signal is generated by Segment Interconnects, Slaves and Diagnostic Modules to indicate to the originating Master that an extended delay will occur before the expected response. Diagnostic use of WT allows the system to be single stepped.

3.3.13 AR Arbitration Request (A, Master). The AR control signal is asserted by a Master to request control of its Segment. The Arbitration Timing Controller, on receipt of AR, starts an Arbitration Cycle as soon as permitted by the current Master.

3.3.14 AG Arbitration Grant (TA, ANC). The Arbitration Grant line, AG, is asserted by the ATC to synchronize Arbitration Cycles during which contending Masters decide which will be the next bus Master.

3.3.15 AL Arbitration Level (IA, Master). The Arbitration Level lines, $AL<05:00>$, are asserted by Masters participating in an Arbitration Cycle. The lines asserted represent the Master's priority on its local Segment or in the system. The rules for assertion of AL are given in detail in Section 6.

3.3.16 GK Grant Acknowledge (TA, Master). Grant Acknowledge, GK, is asserted by the Master which participated in and won the most recent Arbitration Cycle. Until GK is asserted the Master is called the Pending Master. The Current Master is the one asserting GK or AS. The rules for assertion of GK are given in Section 6.

3.3.17 AI Arbitration Request Inhibit (CA, ANC). The ATC asserts AI to indicate the presence of unsatisfied requests after an Arbitration Cycle. Masters which operate in the Assured Access Protocol, will not assert AR and thus abstain from participating in subsequent Arbitration Cycles until all Masters currently asserting AR have obtained Mastership and completed their operations.

3.3.18 SR Service Request (A, Master, or Slave). A Device which requires service may assert the signal SR at any time. A Master monitoring SR may after gaining bus Mastership take appropriate action.

3.3.19 RB Reset Bus (A, Master, or Master via SIs). The RB signal is asserted by a Master with sufficient knowledge to force a Segment into its reset or quiescent state. This asynchronous signal may be used to precondition a Segment before initialization or diagnostics. In the latter case, it is important to minimally disturb a Segment prior to beginning diagnostic procedures.

3.3.20 BH Bus Halted (C, ANC). The BH signal is asserted only by the Run/Halt logic in the ATC when it senses a Halt request from the Run/Halt Switch. This signal, generated in conjunction with AK, indicates the inactive, halted status of the Segment allowing all Devices residing on the Segment to protect themselves from spurious (transient) signals that can be generated for any reason at this time on the bus. It is especially intended to protect against a false RB signal.

3.3.21 GA Geographical Address (F, Hardwired). The GA pins are five binary encoded pins at each Module position in a Crate Segment which uniquely encode the position on the Segment. GA=00 represents the rightmost position in the Crate as viewed from the front. When EG is asserted the Device in each Module location compares its coded pins with the five lowest AD lines in order to determine if it is being addressed Geographically. Each Device on a Cable Segment has five switches which are used in lieu of the GA pins for Geographical Addressing.

3.3.22 TP T Pins (I, Slave). Each Module location has a T pin connected to a unique AD line. The T pin for Module location 00 (Crate position 00) connects to AD00, etc. These pins are used to indicate data present in response to the beginning of a Sparse Data Scan, or to show a pattern response such as indicating the source of SRs on a Segment. These pins can also be used for Device selection.

3.3.23 DL, DR Daisy Chain (I, Master, or Slave). Two independent daisy chains, A and B, are provided in Crate Segments to allow token passing between adjacent Modules. At each Module position both chains have connections to the adjacent Module position on the left (DLA and DLB) and on the right (DRA and DRB). Each chain has a return line (DAR and DBR). Chain A is used to pass information from right to left; chain B is used from left to right. See Table 13.2.1 and Fig 14.2.1(a).

Use of the FASTBUS daisy chain shall not interfere with the use of the FASTBUS protocol.

The use of the daisy chains is not specified in this standard.

The daisy chains are not continuous across empty Module positions. This must be taken into account when configuring a Crate Segment for daisy chain applications.

3.3.24 TX, RX Serial Network Lines (A, Master, or Slave). The Serial Network lines on the Crate Segment provide any Module with convenient access to the FASTBUS Serial Network. Use of these lines follows the FASTBUS Serial Network Protocol. The connection between the Serial Network lines on a Crate Segment and the rest of the FASTBUS Serial Network can be made by an interface in a Module or on a circuit board on the rear of the Crate Segment.