

IEEE Standard for an 8-Bit Microcomputer Bus System: STD Bus

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of the
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Foreword

(This Foreword is not a part of IEEE Std 961-1987, IEEE Standard for an 8-Bit Microcomputer Bus System: STD Bus.)

The 8-bit microcomputer bus system described herein is derived from the industry bus known as the STD bus. The STD bus is a modular packaging and interconnect scheme for 8-bit microprocessor card systems. The bus size and bus organization were selected to serve the interface between any 8-bit microprocessor and a variety of memory and I/O functions. The card size was selected for modular function-per-card packaging using LSI and VLSI semiconductor technology.

The STD bus was introduced in 1978 as a planned industry standard. To encourage its acceptance as a standard the bus was made freely available to industry without patents, trademarks, or copyrights. An industry-supported manufacturer's group was formed to manage and maintain the bus standards and to encourage and enhance a modular methodology in applying microprocessors.

In 1980, following two years of trial use, the manufacturer's group elected to pursue IEEE standardization to achieve more rigid control of the standard.

In response to a Project Authorization Request submitted by the Technical Committee on Microprocessors and Microcomputers, Working Group P961 was authorized by the IEEE to study the development of an 8-bit microcomputer bus standard. The plan of the working group is to build on the physical, logical, and electrical standards defined by the manufacturer's group and to provide timing standards that would allow users to determine compatibility of products from many sources.

The 8-bit bus focuses on the integration of specialized I/O functions with microprocessor technology through a modular busing scheme. It assumes the creation of many specialized interfaces by a wide and varied range of technical and scientific disciplines.

The purpose of this standard is to define the physical, logical, electrical, and timing requirements to ensure the highest degree of compatibility for bus card products. The physical, logical, and electrical requirements are exact and explicit; however, the wide range of processor types accommodated makes it impossible to define absolute timing requirements.

The purpose of this standard is to define absolute physical, logical, and electrical requirements and to define those timing parameters that must be specified to allow the user to determine timing compatibility.

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Correction Sheet

Users of IEEE Std 961-1987 should refer to Section 5, Mechanical Specifications, on page 29 of the standard. ANSI/IEEE Std1101-1987, IEEE Standard for Mechanical Core Specifications for Microcomputers, was mistakenly included in this printing of IEEE 961, and will be removed at the time of the next reprinting.

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IEEE Standard for an 8-Bit Microcomputer Bus System: STD Bus

1. Scope

This standard provides specifications for applying 8-bit microprocessors to a low-cost modular busing scheme. The signals for this bus are generally derived directly from the processor device and are buffered but not retimed. This scheme results in some modules being processor-device dependent. The body of this standard provides a core specification for the device-independent parameters. Appendixes provide device-dependent parameters for various processors.

1.1 Application

This specification defines an 8-bit microprocessor bus standard where the small card size, in conjunction with LSI semiconductor technology, creates a modular by-function approach to control-oriented system design. The standard card size, connector, and pinout lend themselves to a bused motherboard that permits any card to work in any slot.

The bus interface connector as shown in Fig 1 is dedicated to microprocessor control of the card functions. Peripheral and I/O device connections are made at the edge of the card defined as the user interface. This layout gives an orderly signal flow across the card from the bus interface to the user interface. Peripheral and I/O devices can be connected to the system using their own unique connectors and cabling. Complete functions can be modularly added to the system by installing a card with its cable.

1.2 Inclusions

This standard specifies the following:

- 1) Card dimensions
- 2) Bus connector
- 3) Bus pin assignment
- 4) Signal definitions
- 5) Electrical requirements
- 6) Read/write timing sequences
- 7) Read/write time duration parameters

1.3 Exclusions

This standard does not specify

- 1) Card functions
- 2) User interface
- 3) Interchangeability
- 4) Backplane design

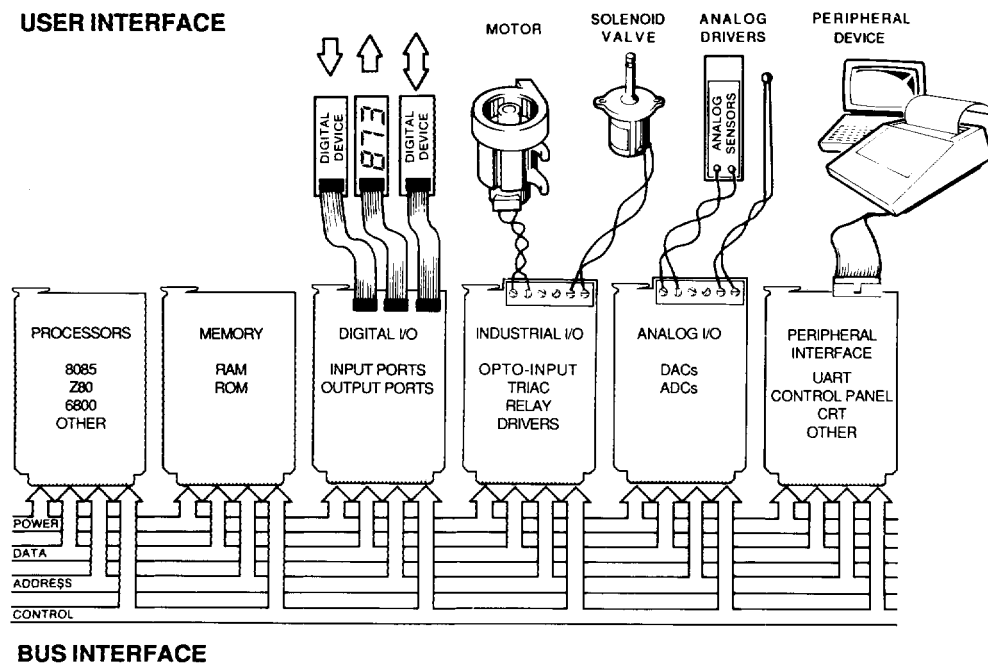


Figure 1— Bus Implementation

1.4 Definitions

assert: To place a signal in its logic 1 state.

backplane: The printed circuit board that contains the connectors and interconnect traces.

card: A printed circuit board and components that make up the modules that plug in to the bus backplane.

master: A card controlling a bus transaction is considered to be a master. The master that is currently controlling the bus is the current master. The card that is host to all other masters is the permanent master. All masters that are not the permanent master are temporary masters.

slave: A card that responds to a bus transaction is considered to be a slave.

2. Logical Specifications

2.1 Bus Pin Assignments

The bus pinout is organized into the five following functional groups. The organization and pinouts are shown in Fig 2. Signal flow direction is referenced to the current master.

Logic Power Bus: Pins 1–6
 Data Bus: Pins 7–14
 Address Bus: Pins 15–30
 Control Bus: Pins 31–52
 Auxiliary Power Bus: Pins 53–56

	COMPONENT SIDE				CIRCUIT SIDE			
	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION	PIN	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
LOGIC POWER BUS	1	VCC	In	Logic Power (+ 5 V dc)	2	VCC	In	Logic Power (+ 5 V dc)
	3	GND	In	Logic Ground	4	GND	In	Logic Ground
	5	VBAT	In	Battery Power	6	VBB	In	Logic Bias (- 5 V dc)
DATA BUS	7	D3/A19	In/Out	Data Bus/Address Ext	8	D7/A23	In/Out	Data Bus/Address Ext
	9	D2/A18	In/Out		10	D6/A22	In/Out	
	11	D1/A17	In/Out		12	D5/A21	In/Out	
	13	D0/A16	In/Out		14	D4/A20	In/Out	
ADDRESS BUS	15	A7	Out	Address Bus	16	A15	Out	Address Bus
	17	A6	Out		18	A14	Out	
	19	A5	Out		20	A13	Out	
	21	A4	Out		22	A12	Out	
	23	A3	Out		24	A11	Out	
	25	A2	Out		26	A10	Out	
	27	A1	Out		28	A9	Out	
	29	A0	Out		30	A8	Out	
CONTROL BUS	31	WR*	Out	Write to Memory or I/O	32	RD*	Out	Read Memory or I/O
	33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Out	Memory Address Select
	35	IOEXP	In/Out	I/O Expansion	36	MEMEX	In/Out	Memory Expansion
	37	REFRESH*	Out	Refresh Timing	38	MCSYNC*	Out	CPU Machine Cycle Sync.
	39	STATUS 1*	Out	CPU Status	40	STATUS 0*	Out	CPU Status
	41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In	Bus Request
	43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In	Interrupt Request
	45	WAITRQ*	In	Wait Request	46	NMIRQ*	In	Nonmaskable Interrupt
	47	SYSRESET*	Out	System Reset	48	PBRESET*	In	Pushbutton Reset
	49	CLOCK*	Out	Clock from Processor	50	CNTRL*	In	AUX Timing
AUXILIARY POWER BUS	51	PCO	Out	Priority Chain Out	52	PCI	In	Priority Chain In
	53	AUX GND	In	AUX Ground	54	AUX GND	In	AUX Ground
	55	AUX +V	In	AUX Positive (+ 12 V dc)	56	AUX -V	In	AUX Negative (- 12 V dc)

* Low-level active indicator

Figure 2— Bus Connector Pin Assignment

2.2 Signal Descriptions

2.2.1 Power Buses (Pins 1–6 and 53–56)

The dual power buses accommodate logic and analog power distribution. As many as five separate power supplies can be used with two separate ground returns as shown in Table 1. Separate grounds allow analog circuits to be isolated from the digital ground. The practice is to connect all grounds at a single point, usually at the power source.

Logic power on pins 1 and 2, and digital ground on pins 3 and 4 are required for all cards. The other power pins are optional.

2.2.2 Data Bus (Pins 7–14) (8-bit, bidirectional, 3-state, active-high)

Data bus direction is controlled by the current master and is affected by such signals as read (RD*), write (WR*), and interrupt acknowledge (INTAK*).

All cards should release the data bus to a high-impedance state when not in use. The permanent master shall release the data bus in response to bus request (BUSRQ*) input from a temporary master, as in DMA transfers.

The data bus lines may be multiplexed for address space expansion. The pin assignment for address expansion shall be as defined in Fig 2.

2.2.3 Address Bus (Pins 15-30) (16-bit, 3-state, active-high)

The address originates at the current master. The permanent master shall release the address bus in response to a bus request (BUSRQ*) input from a temporary master.

The address bus may be extended to 24 bits by multiplexing 8 additional address bits on the data bus. The pin assignment for address expansion shall be as shown in Fig 2.

The address bus provides 16 address lines for decoding by either memory or I/O. Memory request (MEMRQ*) and I/O request (IORQ*) control lines distinguish between the two operations. The number of address lines and how they are used is determined by the microprocessor type, as shown in Table 2.

Table 1— Power Bus Pin Assignments

PIN	DESCRIPTION	COMMENTS
1 & 2	Logic Power	Logic power source (+ 5 V dc)
3 & 4	Digital Ground	Logic power return bus
5	Backup Voltage	Battery voltage (+3.5 to +5.0 V dc)
6	Logic Bias Voltage	Low-current logic supply (-5 V dc)
53 & 54	Auxiliary Ground	Auxiliary power return bus
55	Auxiliary Positive	Positive DC supply (+12 V dc)
56	Auxiliary Negative	Negative DC supply (-12 V dc)

Table 2— Examples of Address Bus Utilization

PROCESSOR TYPE	NUMBER OF MEMORY ADR LINES	ADDRESS LINES DURING REFRESH	NUMBER OF I/O ADDRESS LINES	
			I/O MAPPED	MEMORY MAPPED
8080/85	16	-	lower 8	16
Z80	16	lower 7	lower 8	16
NSC800	16	lower 8	lower 8	16
6800	16	-	-	16
6809	16	-	-	16
6502	16	-	-	16
8088	16	-	16	16

2.2.4 Control Bus (Pins 31–52)

The control bus signal lines are grouped into five areas: memory and I/O control, peripheral timing, clock and reset, interrupt and bus control, and serial priority chain.

2.2.4.1

Memory and I/O control lines provide the signals for fundamental memory and I/O operations. Simple applications may only require the following six control signals. All cards shall support these six memory and I/O control lines.

PIN 31 WR* Write to memory or output (3-state, active-low).

WR* originates from the current master and indicates that the bus data will be written to the addressed memory or output device. The selected device shall use this signal to write the data to the memory or output port.

PIN 32 RD* Read from memory or input (3-state, active-low).

RD* originates from the current master and indicates that data will be read from memory or from an input device. The selected input device or memory shall use this signal to gate data onto the data bus.

PIN 33 IORQ* I/O address select (3-state, active low).

IORQ* originates from the current master and shall indicate an I/O read or write operation. IORQ* may also be used to control processor-dependent peripheral devices.

PIN 34 MEMRQ* Memory address select (3-state, active-low).

MEMRQ* originates from the current master and shall indicate a memory read or write operation. MEMRQ* may also be used to control processor-dependent peripheral devices.

PIN 35 IOEXP I/O expansion (3-state, high expand, low enable).

IOEXP originates from the current master and shall be used to expand or enable I/O port addressing. An active-low shall enable the primary (8-bit) I/O address space. I/O cards shall decode IOEXP.

PIN 36 MEMEX Memory expansion (3-state, high expand, low enable).

MEMEX originates from the current master and shall be used to expand or enable memory addressing. An active-low shall enable the primary (64K) memory address space. Memory cards shall decode MEMEX. MEMEX may be used to allow memory overlay such as in bootstrap operations. A control card may switch out the primary memory to make use of an alternate memory.

2.2.4.2

Peripheral timing control lines provide signals that enable the use of the bus with microprocessors that service their own peripheral devices. The 8-bit bus is intended to service any 8-bit microprocessor; however, most peripheral devices operate only with the processor they are designed for. Four control lines of the bus are designated for peripheral timing. These lines are defined specifically for each type of microprocessor so it can serve its own peripheral devices (examples are shown in Table 3). Cards requiring signals on the peripheral timing control lines shall specify their processor dependency.

PIN 37 REFRESH* (3-state, active-low).

REFRESH* may originate from the current master or from a separate control card and should be used to refresh dynamic memory. The nature and timing of the signal may be a function of the memory device or the processor. In systems without refresh, this signal can be any specialized memory control signal. Systems with static memory may disregard REFRESH*.

PIN 38 MCSYNC* Machine cycle sync. (3-state, active-low).

MCSYNC* shall originate from the current master. This signal should occur once during each machine cycle of the processor. MCSYNC* defines the beginning of the machine cycle. The exact nature and timing of this signal are processor-dependent. MCSYNC* keeps peripheral devices synchronized with the processor operation. It can also be used for controlling a bus analyzer, which can analyze bus operations cycle-by-cycle.

MCSYNC* shall be used to de-multiplex extended addressing from the data bus.

PIN 39 STATUS 1* Status control line 1 (3-state, active-low).

STATUS 1* shall originate from the current master to provide secondary timing for peripheral devices. When available, STATUS 1* should be used as a signal for identifying instruction fetch.

PIN 40 STATUS 0* Status control line 0 (3-state, active-low).

2.2.4.3

Interrupt and bus control lines allow the implementation of bus control schemes such as direct memory access, multiprocessing, single stepping, slow memory, power-fail restart, and a variety of interrupt methods. Priority for multiple interrupts or bus requests can be supported by either serial or parallel priority schemes.

Table 3— Examples of Peripheral Timing Control Lines

	REFRESH*	MCSYNC	STATUS 1	STATUS 0
PROCESSOR	PIN 37	PIN 38	PIN 39	PIN 40
8080	†	SYNC*	M1*	†
8085	†	ALE*	S1*	SO*
Z80	REFRESH*	(RD+WR+INTAK)*	M1*	†
NSC800	REFRESH*	ALE*	S1*	SO*
8088	†	ALE*	S1*	SO*
6800	†	02*	UMA*	R/W‡
6809	†	EOUT(02*)	†	R/W‡
6809E	†	EOUT(02*)	LIC*	R/W‡
6502	†	02*	SYNC*	R/W‡

*Low-level active

†Not used

‡Read high, write low

PIN 41 BUSAK* Bus acknowledge (active-low).

BUSAK* originates from the permanent master and is used to indicate that the bus is available for use by a temporary master. The permanent master shall respond to a bus request (BUSRQ*) by releasing the bus and asserting a bus acknowledge (BUSAK*). BUSAK* should occur at the completion of the current machine cycle. This signal should be combined with a priority signal if multiple controllers need bus access.

PIN 42 BUSRQ* Bus request (active-low, open collector/drain).

BUSRQ* originates from a temporary master and causes the permanent master to suspend operations on the bus by releasing all 3-state bus lines. The bus should be released when the current machine cycle is completed. BUSRQ* shall be used in applications requiring direct memory access (DMA). This signal can be an input or output, or it can be bidirectional, depending on the supporting hardware.

PIN 43 INTAK* Interrupt acknowledge (active-low).

INTAK* originates from the permanent master to indicate to the interrupting device that it is ready to respond to the interrupt. For vectored interrupts, the interrupting device shall place the vector address on the data bus during INTAK*. This signal can be combined with a priority signal, if multiple controllers need access to the permanent master.

PIN 44 INTRQ* Interrupt request (active-low, open collector/drain).

INTRQ* originates from any slave function to interrupt the processor on the permanent master. It should be masked and ignored by the processor unless it is deliberately enabled by software. If the processor accepts the interrupt it should acknowledge by asserting INTAK*. Other actions depend on the specific type of processor, the interrupt handling software, and the hardware support of the interrupt mechanism.

PIN 45 WAITRQ* Wait request (active-low, open collector/drain).

WAITRQ* may originate from any master or slave and shall cause the current master to suspend operations as long as it remains low. The current master should hold in a state that maintains a valid address on the bus. WAITRQ* can be used to insert wait states in the processor cycle. Examples of its use include slow memory and I/O operations and single stepping.

PIN 46 NMIRQ* Nonmaskable interrupt (active-low, open collector/drain).

NMIRQ* may originate from any master or slave and shall be used as an interrupt input of the highest priority to the permanent master. It should be used for critical processor signaling such as power-fail indication.

2.2.4.4

Clock and reset lines provide the bus with basic clock timing and reset capability.

PIN 47 SYSRESET* System reset (active-low, open collector/drain).

SYSRESET* originates from any system reset circuit, which may be triggered by power-on detection or by the pushbutton reset. All cards with circuits requiring initialization should use SYSRESET*.

PIN 48 PBRESET* Pushbutton reset (active-low, open collector/drain).

PBRESET* may originate from any card and is used as an input to the system reset circuit.

PIN 49 CLOCK* Clock from the permanent master.

CLOCK* originates from the permanent master and is a buffered processor clock signal for use in system synchronization or as a general clock source.

PIN 50 CNTRL* Control.

CNTRL* may originate from any card for special clock timing. It may be a multiple of the processor clock signal, a real-time clock signal, or an external input to the processor.

2.2.4.5

Priority chain lines are provided for serial priority of interrupt or bus requests. Two bus pins, PCI and PCO, are allocated to the priority chain. Logic is required on each card that needs to participate in the priority chain. Cards not needing the chain shall jumper PCI and PCO on the card. The direction of the chain through the card is from pin 52 on the right to pin 51 on the left, viewed from the user edge.

PIN 51 PCO Priority chain out (active-high).

PCO originates from every card as a signal sent to the PCI input of the next lower card in priority. A card that needs priority shall hold PCO low.

PIN 52 PCI Priority chain in (active-high).

PCI originates directly from the PCO of the next highest card in priority. A high level on PCI gives priority to the card sensing the PCI input. The PCI input shall have a resistive pull-up to +5 V on all cards participating in the chain to satisfy the highest priority position.

3. Timing Specifications

This section contains timing for processor-independent operations. The only operations defined to be processor-independent are memory and I/O read and write operations. Processor-dependent operations for various processors are included in the appendixes.

3.1 Signal Time Sequences

The bus signal sequences are given for memory and I/O read and write operations. The signal sequences are defined at the bus to guarantee card compatability.

3.1.1 Address Selection Signal Sequences

The expansion signals, the address bus signals, and the request signals are used to select the data location for memory and I/O read and write operations. These signals are referred to as the address selection signals and are shown in Fig 3.

The expansion signal (MEMEX, IOEXP) is intended for selection of alternate memory or I/O address space.

The address bus signals (A0-A23) are used to uniquely identify a data location within the memory or I/O space.

The request signals (MEMRQ*, IORQ*) provide the selection between memory and I/O operations.

The address selection signals may occur in any sequence. The last signal to occur determines the signal timing.

All address selection signals shall be stable prior to memory and I/O read and write operations.

3.1.2 Read Signal Sequences

The read sequence shown in Fig 4 is controlled from the current master, except for the data bus signals which are a response from the memory or I/O card.

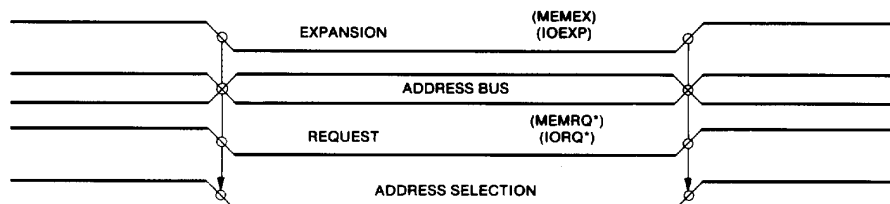


Figure 3— Address Selection Signal Sequence

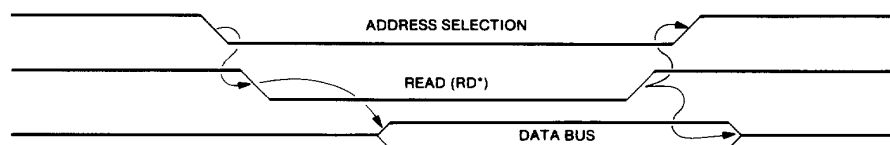


Figure 4— Read Signal Sequences

The read signal causes a read operation to occur at the selected memory or I/O location. The read signal should change state within the address selection signal but may change at the same time. The trailing edge of the read signal shall indicate that the data has been transferred. The read signal shall hold the data bus active until the master accepts the data.

The data bus signals contain the data byte to be transferred to the master. These signals shall remain stable until the read signal is removed.

3.1.3 Write Signal Sequences

The write sequence shown in Fig 5 is controlled from the current master. The address selection, data, and write signals all originate from the current master.

The data bus signals contain the data byte to be transferred to memory or I/O. The data may occur before or after the leading edge of the write signal. The data shall be stable for a specified duration prior to the trailing edge of the write signal. The data shall remain stable for a specified duration after the trailing edge of the write signal.

3.2 Signal Time Durations

Signal time durations are defined that will enable users to determine card compatibility for memory or I/O read and write operations.

3.2.1 Read Timing

Critical read timing is shared between the current master and the memory or I/O card. The current master controls the read access time (t_{ARD}) and has a requirement of a read data setup time (t_{SRD}). The memory or I/O device has a read access time (t_{AR}) requirement and controls how long the read data will be held on the bus (t_{HRD}). These timing relationships are shown in Fig 6.

Card compatibility for read operations shall be determined by comparing the specified required read access time of a memory or I/O card against the available read access time of a master card. Master card t_{AR} shall be greater than or equal to memory or I/O card t_{AR} .

Master cards shall specify:

t_{AR} ; maximum available Read Access time,

where t_{AR} equals t_{ARD} minimum less t_{SRD} minimum

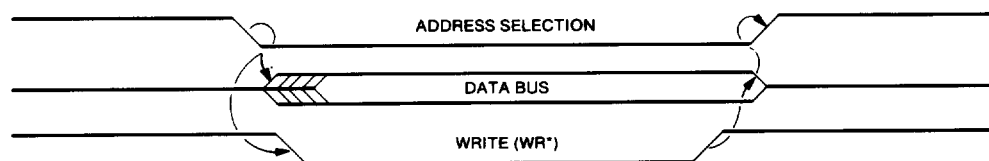


Figure 5— Write Signal Sequence

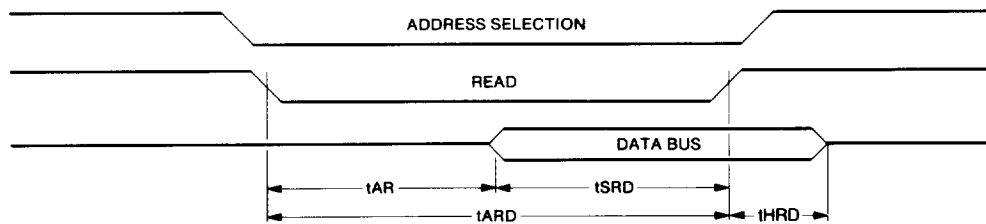


Figure 6— Critical Read Timing

Memory or I/O cards shall specify:

- t_{AR} ; maximum required read access time. Since address selection may occur at the same time as read, t_{AR} must specify the worst-case access time.
- t_{HRD} ; maximum read data hold time.

3.2.2 Write Timing

Critical write timing for compatibility is limited to the write data setup time (t_{SWD}) and write data hold time (t_{HWD}) required by the memory or I/O card as shown in Fig 7.

Card compatibility for write operations Shall be determined by comparing the specified required write data setup and hold times of a memory or I/O card against the available write data setup and hold times of a master card.

Master t_{SWD} shall be greater than or equal to memory or I/O t_{SWD} .

Master t_{HWD} shall be greater than or equal to memory or I/O t_{HWD} .

Master cards shall specify:

t_{SWD} , minimum available write data setup time.

t_{HWD} , minimum available write data hold time.

Memory or I/O cards shall specify:

t_{SWD} , minimum required write data setup time.

t_{HWD} , minimum required write data hold time.

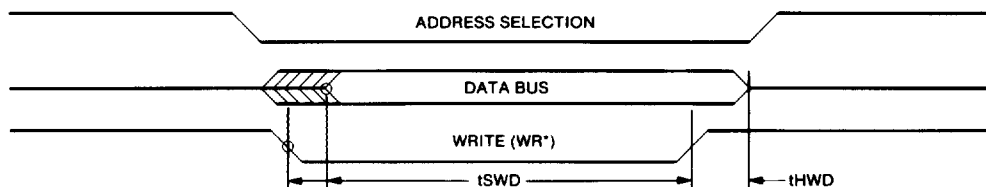


Figure 7— Critical Write Timing