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Sponsor

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on
Graphic Symbols and Designations

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Foreword

(This Foreword is not a part of ANSI/IEEE Std 991-1986, IEEE Standard for Logic Circuit Diagrams.)

The contributors to this standard represent a broad range of institutions, technologies, and documentation needs. They include industrial, governmental, and educational organizations, producers and consumers of devices and equipment, users and nonusers of computer-aided design and drafting, and a range of aesthetic preferences. That a consensus of such diverse interests could be achieved in producing this standard is indicative of a need for a common practice in this field.

Work on this standard started in 1972, in an ad-hoc working group on Logic Diagrams, under the preparing group for Y14.15, Electrical Diagrams. Work was suspended for several years while the International Electrotechnical Commission, Technical Committee 3 developed Publication 117, Part 7, to which the United States contributed. In 1982 a new subcommittee was formed, operating as part of the IEEE Standards Coordinating Committee for Graphic Symbols and Designations, SCC 11. It decided to prepare a new draft incorporating:

- 1) The 1975 draft of the original working group,
- 2) IEC Publication 113, Part 7, insofar as practical (in the present standard, some parts and illustrations are very similar to the IEC document; differences and additions result from new developments in symbols for logic functions and new perceptions of current needs), and
- 3) Such parts of ANSI Y14.15-1968 (R 1973) as applied to logic circuit diagrams, but with updating to remove duplication of requirements found in referenced standards and to apply the material explicitly to logic circuit diagrams.

After ten drafts the present document was completed and submitted to the IEEE Standards Board for approval.

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IEEE Standard for Logic Circuit Diagrams

1. Introduction

1.1 Purpose

The purpose of this standard is to provide standard practices and information for use in the preparation of diagrams depicting logic functions.

1.2 Scope

This standard provides guidelines for preparation of diagrams depicting logic functions. It includes definitions, requirements for assignment of logic levels, application of logic symbols, presentation techniques, and labeling requirements with typical examples. The techniques are presented in the context of electrical/electronic systems, but also may be applied to nonelectrical systems (for example, pneumatic, hydraulic, or mechanical).

2. Applicable Documents

2.1 Industry Standards

The latest editions of the following industry documents form a part of this standard to the extent specified herein:

American National Standards

ANSI X3.4-1977, American National Standard Code for Information Interchange.¹

ANSI X3/TR-1-1983, American National Standard Dictionary for Information Processing.

ANSI Y1.1-1972 (R 1984), American National Standard Abbreviations for Use on Drawings and In Text.

¹ ANSI publications are available from the Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018.

ANSI Y14.1-1980, American National Standard Drawing Sheet Size and Format.

ANSI Y14.2M-1979, American National Standard Line Conventions and Lettering.

ANSI Y14.15-1966 (R 1973), American National Standard Electrical and Electronics Diagrams (includes Supplements ANSI Y14.15a-1971 and ANSI Y14.15b-1973).

ANSI/IEEE Std 91-1984, IEEE Standard Graphic Symbols for Logic Functions.²

ANSI/IEEE Std 100-1984, IEEE Standard Dictionary of Electrical and Electronics Terms.

ANSI/IEEE Std 194-1977, IEEE Standard Pulse Terms and Definitions.

ANSI/IEEE Std 200-1975, IEEE Standard Reference Designations for Electrical and Electronics Parts and Equipment.

ANSI/IEEE Std 260-1978 (R 1985), IEEE Standard Letter Symbols for Units of Measurement (SI Units, Customary Inch-Pound Units, and Certain Other Units).

ANSI/IEEE Std 280-1985, IEEE Standard Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

ANSI/IEEE Std 315-1975, Graphic Symbols for Electrical and Electronics Diagrams (Including Reference Designation Class Designation Letters).

2.2 Military Standards

The latest edition of the following Department of Defense document forms a part of this standard to the extent specified herein and shall be used for DoD contracts in place of the equivalent Industry Standards listed above:

MIL-STD-12, Military Standard Abbreviations for Use on Drawings, Specifications, Standards, and in Technical Documents.³

2.3 International Standards

This standard is compatible (except as noted) with the following publications:

IEC Publication 113 (1971 - 1983), Diagrams, Charts, Tables.⁴

ISO 31/1-1978, Quantities and Units of Space and Time.⁵

ISO 646-1983, 7-bit Coded Character Set for Information Processing Interchange.

² IEEE publications are available from IEEE Service Center, 445 Hoes Lane, Piscataway, NJ 08854.

³ MIL publications are available from Superintendent of Documents, US Government Printing Office, Washington, DC 20402.

⁴ IEC publications are available in the United States from the Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018, USA. The IEC publications are also available from International Electrotechnical Commission, 3, rue de Varembe, Case postale 131, 1211 —Genève 20, Switzerland/Suisse.

⁵ ISO publications are available in the United States from the Sales Department, American National Standards Institute, 1430 Broadway, New York, NY 10018, USA. ISO publications are also available from the ISO Office, 1, rue de Varembe, Case postale 56, CH-1211, Genève 20, Switzerland/Suisse.

3. Definitions

The following definitions are for use with this standard. For other use and for definitions not contained herein, see ANSI/IEEE Std 100-1984.⁶

graphic symbol: A figure, mark, or character conventionally used on a diagram, document, or other display to represent an item or a concept.

logic symbol: A graphic symbol that represents a logic function.

qualifying symbol: A graphic symbol added to another to provide additional information. For a logic element, a graphic symbol added to the basic outline to designate the overall logic characteristics of the element or the physical or logic characteristics of an input or output of the element.

negation bar: A line over a signal label that indicates logic inversion of that signal.

element: As used within this standard, a representation of all or part of a function within a single outline, which may, in turn, be subdivided into smaller elements representing subfunctions of the overall function. Alternatively, the function so represented.

logic circuit diagram: A circuit diagram that predominantly uses symbols for logic functions to depict the overall function of a circuit.

basic logic diagram: A logic circuit diagram that depicts, in simple form, the intended function of a circuit. It does not necessarily contain constructional or engineering information, nor does it represent exactly the final physical form.

detailed logic diagram: A logic circuit diagram that depicts, in detail, a circuit as actually implemented. It contains information that can be used for manufacturing or maintenance purposes, but it does not necessarily include engineering information that is not concerned with logic functions.

logic state: One of two possible abstract states that may be taken on by a logic (binary) variable.

0-state: The logic state represented by the binary number 0 and usually standing for an inactive or false logic condition.

1-state: The logic state represented by the binary number 1 and usually standing for an active or true logic condition.

logic level: Any level within one of two nonoverlapping ranges of values of a physical quantity used to represent the logic states.

NOTE — A logic variable may be equated to any physical quantity for which two distinct ranges of values can be defined. In this standard, these distinct ranges of values are referred to as logic *levels* and are denoted H and L.

H is used to denote the logic level with the more positive algebraic value, and L is used to denote the logic level with the less positive algebraic value.

In the case of systems in which logic states are equated with other physical properties (for example, positive or negative pulses, presence or absence of a pulse), H and L may be used to represent these properties or may be replaced by more suitable designations.

high (H) level: A level within the more positive (less negative) of the two ranges of the logic levels chosen to represent the logic states.

low (L) level: A level within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states.

signal state: The logic state corresponding to the truth-value of the statement or expression represented by a signal name.

⁶When reference is made to any publication throughout this standard the user should refer to Section 2. for the full title and location of availability.

logic conventions and polarity indication

positive logic convention: The representation of the external 1-state and the external 0-state by the high (H) and low (L) levels, respectively.

negative logic convention: The representation of the external 1-state and the external 0-state by the low (L) and high (H) levels, respectively.

direct polarity indication: The indication of the relationship between the internal logic state and the external logic level at each input and output of the every logic element directly by means of the presence or absence of the polarity symbol (∇).

4. General Requirements

4.1 Content

4.1.1 Basic Logic Diagram

This diagram shall show the conceptual principles of a circuit. It shall include as a minimum the required logic symbols and other necessary functional symbols, together with their signal and major control path connections. Other information such as waveforms, formulas, and algorithms may be included. Physical location, pin connection, and assembly level information are usually omitted.

4.1.2 Detailed Logic Diagram

This diagram shall show the information necessary for manufacture, installation, maintenance, and training for a logic circuit or system. It shall include as a minimum:

- 1) Graphic symbols for logic functions and other devices (see Section 6.)
- 2) Connections among symbols (signal, control, and power) (see Section 7.)
- 3) Reference designations (see 6.4.1.1)
- 4) Terminal identification (see 6.4.1.5)
- 5) Signal-level conventions applicable to the diagram: positive or negative logic, logic states or levels (for example, H and L) (see Section 5.)
- 6) Information necessary to trace paths and circuits among sheets of the diagram (see 7.4)

4.1.3 Combined Forms of Circuit Diagrams

Provided that approved standards are followed, diagrams combining logic circuit information with conventional schematic (mechanical, or electrical) diagram information may be prepared.

4.2 Drawing Size and Format

Drawing sizes and formats used with diagrams shall conform to ANSI Y14.1-1980. In general, the smallest standard format compatible with the nature of the diagram should be selected. See also Appendix 11..

4.2.1 Drawing Zones

On logic diagrams with many logic elements, it is often helpful to have a coordinate system to permit referencing particular areas or zones on the sheet (see ANSI Y14.1-1980). This is especially helpful when many sheets are required and cross references between sheets are numerous. Signal tracing is expedited if reference can be made from one point in a diagram to both sheet and zone of another point.

4.2.2 Supplemental Drawing Number Location

If a diagram is reproduced for an instruction book or similar purposes and the title block is not retained, it may be desirable to include the original drawing number within the reproduced area. This drawing number (if included) should be shown close to the lower right edge of the reproduced area in a lettering size comparable to that used for notes and other detailed reference material.

4.3 Diagram Titles

The title of the diagram should include the name of the circuit or equipment followed by the diagram type. For example: MEMORY CONTROLLER, MODEL 1134 — CIRCUIT DIAGRAM.

4.4 Diagram Revisions

Provision shall be made on all logic circuit diagrams for recording revisions. The record of changes made in each revision shall be identified⁷ by either a number, letter or character, and the date of the revision. When it is possible to make a brief detailed explanation of the revision, this is desirable. When a detailed explanation is not practicable, a note covering the general nature of the revision should be included. A reference to a change order document may be shown in lieu of an explanation.

4.5 Lettering

Lettering style, size, spacing, and legibility shall conform to ANSI Y14.2M-1979 .

NOTE — Lettering height and spacing affect symbol size and overall layout of diagrams. See Appendix B for guidelines including those applying to diagrams that are used both as a part of the engineering drawing set and in technical manuals.

4.5.1 Orientation

All lettering within a diagram shall be readable from no more than two orientations of the diagram, 90° apart.⁸

4.6 Lines

Line width and quality shall be such that, after reproduction of the diagram at the required size, all lines shall be legible and without breaks. For detailed recommendations concerning line width, see Appendix B.

Thick lines may be used for general use (including symbols and connecting lines) and for lettering. Thin lines should be approximately half the width of the thick lines.

If emphasis of special features, such as main or transmission paths, is essential, an extra-thick line, approximately twice the width of thick lines, may be used to provide the desired contrast.

Line conventions for use on logic circuit diagrams are shown in Fig 1.

⁷For US Department of Defense applications, the identification shall be an uppercase letter, used in alphabetical sequence, omitting the letters I, O, Q, S, X, and Z.

⁸For special IEC requirements, see Appendix 11..

	LINE APPLICATION	LINE THICKNESS
	FOR GENERAL USE	<u>THICK</u>
	MECHANICAL CONNECTION, SHIELDING, AND FUTURE CIRCUITS LINE	<u>THICK</u>
	BRACKET-CONNECTING DASHED LINE	<u>THICK</u>
USE OF THESE LINE THICKNESSES OPTIONAL	BRACKETS, LEADER LINES, ETC	<u>THIN</u>
	FUNCTIONAL- OR MECHANICAL-GROUPING BOUNDARY LINE (PHANTOM LINE)	<u>THIN</u>
	FOR EMPHASIS	<u>EXTRA THICK</u>

Figure 1—Line Conventions for Diagrams

4.7 Abbreviations

For rules applying to connecting-line labels, see Section 8. Other abbreviations used on diagrams shall conform to ANSI Y1.1-1972 (R 1984).⁹ If the term is not included in ANSI Y1.1-1972 (R 1984), an abbreviation given in other standards recognized as National Standards may be used. If no suitable abbreviation exists, a special abbreviation may be used, but shall be explained by a note on the diagram.

4.8 Letter Symbols

Letter symbols for units of measurement shall conform to ANSI/IEEE Std 260-1978 (R 1985).

Letter symbols for quantities used in electrical science and electrical engineering shall conform to ANSI/IEEE Std 280-1985.

4.9 Layout and Presentation

4.9.1 Coverage

A logic diagram, which may consist of several sheets, should be prepared for each distinct unit, or assembly of units, intended to fulfill a defined purpose. It may thus relate to a single unit or to several units that together form a functional entity. In cases where the logic diagram cannot be shown on a single sheet, the division into separate sheets should be based on the purpose of the diagram.

4.9.2 Planning

Basic logic diagrams are prepared primarily for design engineers. It is possible, in many cases, for the basic diagram to be converted to a detailed diagram simply by adding the required labeling. If this can be foreseen, the basic diagram should initially be laid out with sufficient space left both inside and outside of the symbols to accommodate future labeling.

⁹See also 2.2.

4.9.3 Signal Flow

The principal direction of signal flow should be from left to right or, alternatively, from top to bottom. Flow direction may be indicated by the orientation of symbols, logic polarity symbols, or flow arrowheads, or by a convention of unidirectional flow suitably noted. Regardless of the convention used, the signal flow shall be clearly indicated. The flow arrowhead is a small arrowhead superimposed upon data lines or control lines. The flow arrowhead shall not touch any part of the symbol.

4.9.4 Layout

The layout shall be such that the main features are prominently shown. The parts should be spaced to provide an even balance between blank spaces and lines. Sufficient blank area should be provided in the vicinity of symbols to avoid crowding of information. Functionally related symbols should be grouped (see 4.9.5) and placed as close to one another as the requirements of annotation and the avoidance of overcrowding will allow. Large spaces should be avoided, except that space provision may be made for anticipated circuit additions.

The logic diagram shall use a layout that follows the circuit, signal, or transmission path either from input to output, source to load, or in the order of functional sequence. Long interconnecting lines between parts of the circuit should be avoided. Similar basic circuits should be drawn in a similar form (this does not prevent the use of simplified representation to depict repeated circuits).

Where practical, signal flow lines should begin and terminate at the outer edge of the sheet. If this is not practical, references to the terminations may be made by the use of drawing zones.

4.9.5 Grouping of Symbols

If a circuit contains symbols that need to be shown grouped, the grouping may be indicated by means of a boundary (phantom) line enclosure (see Fig 1). The phantom line enclosure may be omitted if sufficient space is provided between groups. Typical groupings are by function or by physical location (for example, unit assemblies, subassemblies, printed circuits, integrated circuits, sealed units). Labeled brackets may be used in place of a boundary line to identify functional groups of symbols if there is sufficient space between groups, so that confusion is unlikely as to which group any symbol belongs. The dashed line used to indicate shielding also implies that the symbols enclosed by the dashed line are grouped (see Figs 31 and 32).

5. Logic Conventions and Polarity Indication

5.1 Relationship Between Logic States and Logic Levels

When logic symbols are used to represent physical devices, it is necessary to establish the relationship between logic states and the nominal values (logic levels) of the physical quantities used to represent these states. There are two methods by which this may be done:

- 1) The use of the symbol for logic negation $\bigcirc$ and requires the adoption of a single logic convention, either positive or negative, for the whole diagram (see 5.2)
- 2) The use of direct polarity indication in which the presence or absence of the logic polarity symbol $\triangle$ indicates the required relationship between logic level and internal logic state at each input and output of every logic symbol on the diagram (for direct polarity indication, see 5.3).

5.2 Single Logic Convention

With this method the correspondence between a given external logic state and logic level is the same at all inputs and outputs on the diagram.

The symbol for logic negation $\neg$ shall be used as required to define the relationship between the *external* logic state and the *internal* logic state. Specifically the presence of the logic negation symbol at an input or output signifies that the internal and external states are the complements of one another for that terminal. The absence of the logic negation symbol signifies that the internal and external states are the same for that terminal. The symbol for logic polarity shall not be used with this method.

The convention in use, either positive logic or negative logic (see 5.2.1 and 5.2.2), shall be clearly stated on the diagram or in referenced documentation. This statement can include a useful, small waveform diagram with indications of the logic states and, if necessary, of the nominal value of corresponding physical quantities.

NOTE — Different logic conventions may be used for different parts of the same diagram; for example, on either side of an interface between contrasting technologies — the convention applying to each part should be clearly shown and the areas of the diagram to which each applies should be clearly delineated.

5.2.1 Positive Logic Convention

For every logic connection, the more positive value of the physical quantity H-level corresponds to the external 1-state. The less positive value L-level corresponds to the external 0-state. This may be stated on a diagram thus:



See Fig 31 for an example of a diagram using positive logic.

5.2.2 Negative Logic Convention

For every logic connection, the less positive value of the physical quantity L-level corresponds to the external 1-state. The more positive value H-level corresponds to the external 0-state. This may be stated on a diagram thus:



5.3 Direct Polarity Indication

With this method the relationship between the internal logic state and the external logic level of each input and output of every logic element is indicated directly by means of the presence or absence of the logic polarity symbol ∇ . Specifically, the presence of the polarity symbol at an input or output indicates that the external low level corresponds to the internal 1-state for that terminal. The absence of the polarity symbol signifies that the external high level corresponds to the internal 1-state for that terminal. No relationship between an external logic state and either an internal logic state or an external logic level is defined by the symbol. A relationship between the external logic level and a signal state is defined only by the signal name (see 8.2.2.1). *In this system the symbol for logic negation shall not be used, except within a symbol outline as permitted by ANSI/IEEE Std 91-1984.*

Direct polarity indication has been called *mixed logic* implying that both positive and negative logic are present on a diagram using that method. This is misleading since the fixed relationship between logic levels and external logic states inherent in a single logic convention does not exist with direct polarity indication. Therefore, the term *mixed logic* is deprecated.

For diagrams prepared with direct polarity indication but showing no logic polarity symbols, a statement indicating that direct polarity is employed shall be placed on the diagram or in referenced documentation.

6. Symbols for Devices and Functions

6.1 Standard Symbols

Graphic symbols shall conform to the following applicable standards: ANSI/IEEE Std 91-1984 and ANSI/IEEE Std 315-1975.

If no suitable standard symbol exists, any special symbol used shall be explained by a note on the diagram.

The use of a symbol in the illustrations of this standard does not preclude the use of alternatives permitted by the graphic symbol standards.

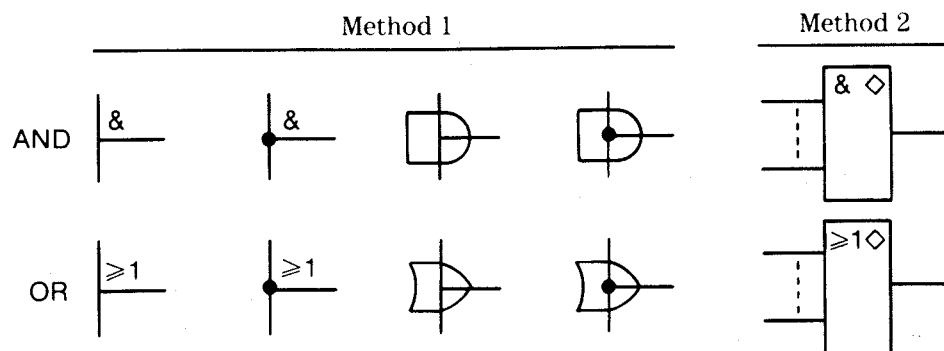
6.1.1 Symbols for Logic Elements

Each logic element should be shown by the symbol that best depicts actually the logic function performed by the element in the system. Thus, in Fig 31, the same type of hardware element is represented once by the symbol for an OR element with negated inputs (designated U4D) and elsewhere by the symbol for AND element with negated output (NAND) (designated U4B and U4C).

6.1.2 Distributed Connections (Dot-AND, Dot-OR)

The connection of certain logic elements to achieve the effect of an AND or an OR operation without the use of additional logic elements shall be depicted using the symbols shown in ANSI/IEEE Std 91-1984.

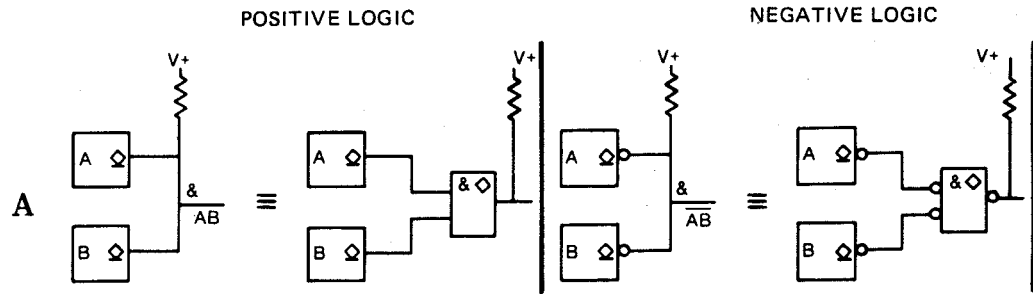
There are two basic methods for showing the distributed-AND function and two basic methods for showing the distributed-OR function. In each case, the first method uses one of the usual methods of showing a junction with the addition of either a qualifying symbol or a surrounding distinctive-shape symbol to denote the logic performed. Method 2 replaces the junction with a rectangle containing the “&” or “ ≥ 1 ” qualifying symbol appropriate to the AND or OR function, respectively. This qualifying symbol is followed by the qualifying symbol $\diamond$ indicating that the logic is performed by a distributed connection instead of by a separate element.



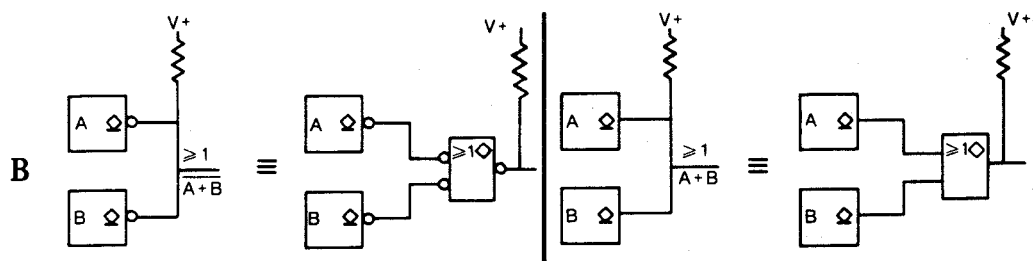
Method 2 permits the use of qualifying symbols for negated inputs and negated outputs with positive and negative logic, and for the polarity indicator with direct polarity indication. These are used with the rectangular symbol in the same manner that they are used if the logic were performed by discrete logic gates with one exception: all the inputs and the outputs shall show the same qualifying symbol since a distributed connection cannot be inverting.

Method 1 does not lend itself to the use of the input and output qualifying symbols. Therefore, to understand the logic performed by the distributed connection, it is necessary to consider the types of outputs that are connected together.

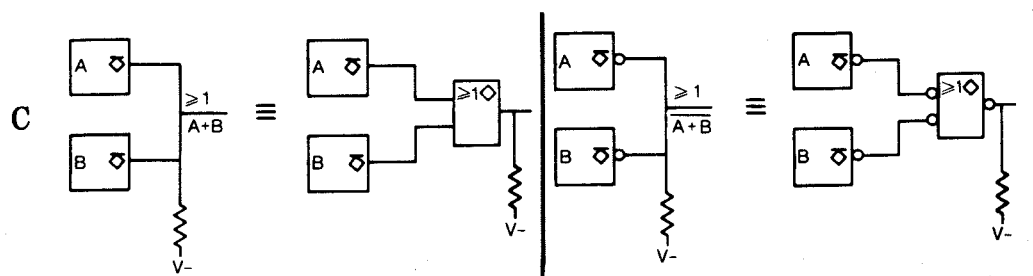
L-type open-circuit outputs (for example, n-p-n open collectors) connected together perform either active-high ANDing or active-low ORing. H-type open-circuit outputs (for example, n-p-n open emitters) connected together perform either active-high ORing or active-low ANDing. See Fig 2. For definitions of open-circuit outputs, see ANSI/IEEE Std 91-1984 .



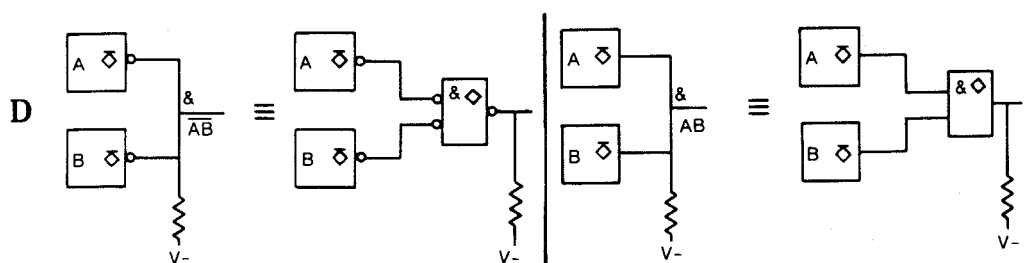
Distributed-AND Connection Formed by Interconnecting L-Type Open-Circuit Outputs



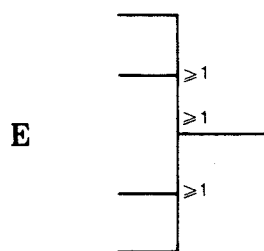
Distributed-OR Connection Formed by Interconnecting L-Type Open-Circuit Outputs



Distributed-OR Connection Formed by Interconnecting H-Type Open-Circuit Outputs



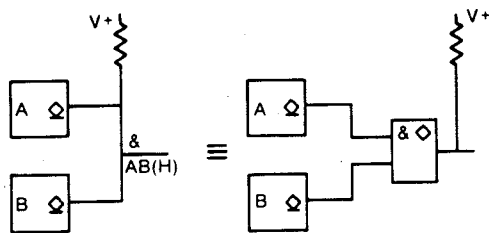
Distributed-AND Connection Formed by Interconnecting H-Type Open-Circuit Outputs



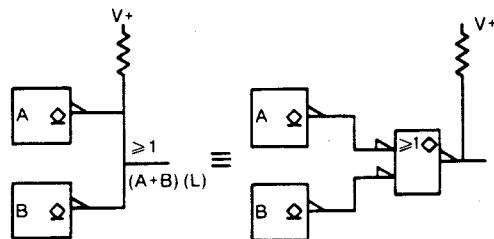
Distributed-OR Multiple Connection

Figure 2—Distributed Connections

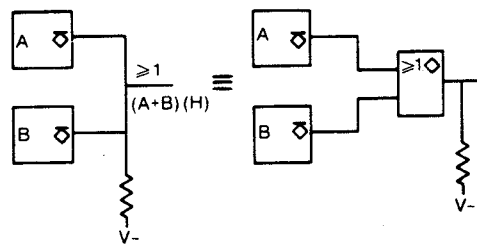
DIRECT POLARITY INDICATION



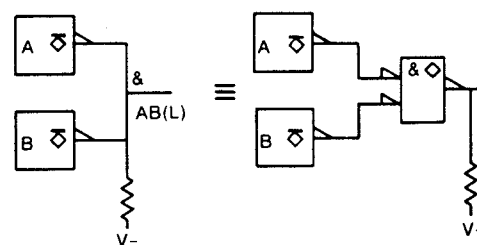
Distributed-AND Connection Formed by Interconnecting L-Type Open-Circuit Outputs



Distributed-AND Connection Formed by Interconnecting H-Type Open-Circuit Outputs



Distributed-OR Connection Formed by Interconnecting H-Type Open-Circuit Outputs



Distributed-OR Connection Formed by Interconnecting L-Type Open-Circuit Outputs

NOTES: (1) The AND or OR symbol may be repeated at the outputs of the elements or at other suitable places.

(2) All external components required to implement the function should be shown or referred to in a table.

Figure 2—Distributed Connections (continued)

Figure 2 assumes that the same negation symbols or polarity symbols can be appropriately used at the driving outputs and the driven inputs. This is the recommended practice; however, sometimes it is not possible to follow this practice at all points in a diagram. The presence or absence of negated output or active-low output qualifying symbols does not influence which type of logic, AND or OR, applies. In Fig 3 the AND and the OR representations are equivalent.

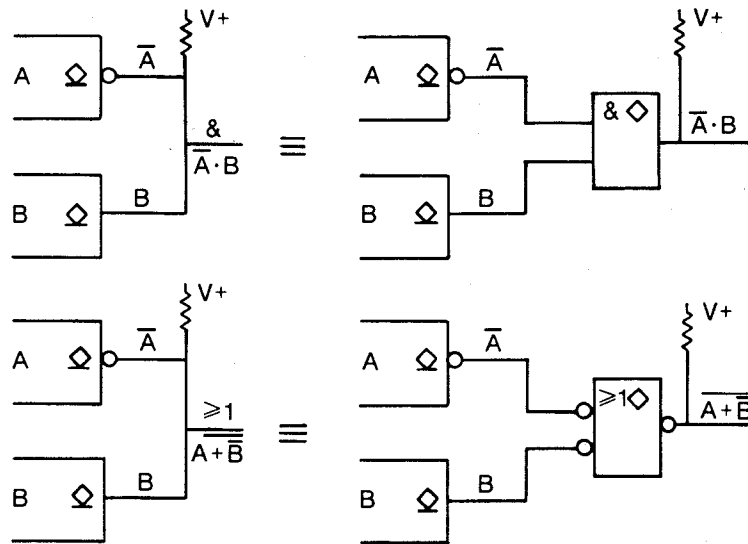


Figure 3—Distributed Connections with a Mix of Negated and Unnegated Outputs (Positive Logic Shown)

The same principle applies for direct polarity indication. In Fig 4 the AND and the OR representations are equivalent.

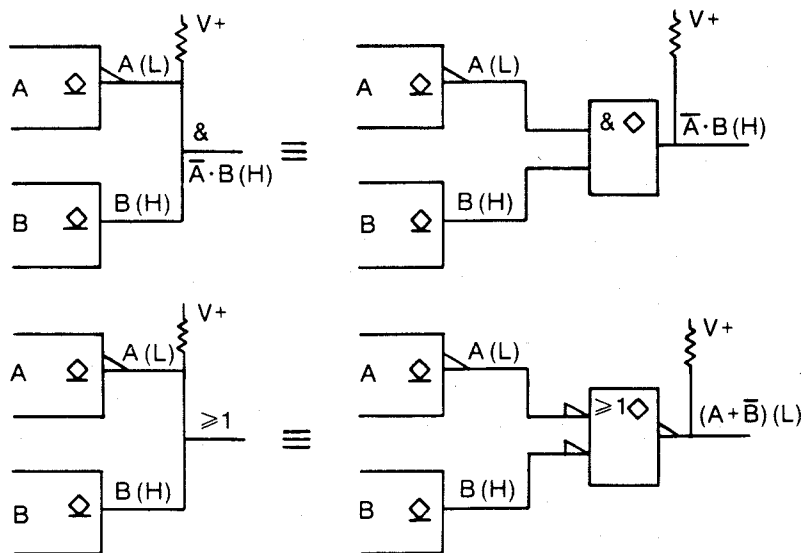


Figure 4—Distributed Connections with a Mix of Active-High and Active-Low Outputs

6.2 Size

In most cases, the meaning of a symbol is defined by its form and contents. The size and the line thickness do not, as a rule, affect the meaning of the symbol.

In some cases, it may be desirable to use different sizes of symbols to

- 1) Emphasize certain aspects, or
- 2) Facilitate the inclusion of additional information

Logic symbol size should be governed by the space necessary for internal annotations and the length of the side needed to accommodate input and output lines at an acceptable spacing. In Fig 5 a binary logic AND element symbol is shown at the left as specified in ANSI/IEEE Std 91-1984 . The symbol at the right has been increased in size to facilitate the addition of pin numbers, designations, and other application information.

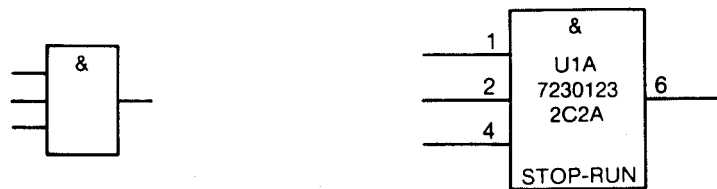


Figure 5—Enlargement of Symbol Outline to Accommodate Application Information

Graphic symbols may be drawn to any proportional size that suits a particular diagram, provided the selection of size takes into account the anticipated reduction or enlargement. On any printed document, nonlogic symbols should be no smaller than 0.6 times the size shown in ANSI/IEEE Std 315-1975 . If those symbols are drawn approximately 1.5 times the size shown, the resulting drawings may be reduced as much as 2.5 to 1. Detailed recommendations regarding the size and proportions of logic symbols may be found in ANSI/IEEE Std 91-1984 .

6.3 Orientation

Symbols or parts of symbols that lend themselves to being rotated or mirror imaged may also be manipulated for simplification of circuit layout, provided

- 1) Proper orientation of lettering is maintained (see 4.5.1),
- 2) Signal flow on the resultant diagram is generally from left to right or top to bottom, and
- 3) The requirements of ANSI/IEEE Std 91-1984 and ANSI/IEEE Std 315-1975 are met.

The logic symbols contained in ANSI/IEEE Std 91-1984 have been designed for the usual case of inputs on the left and outputs on the right, and this orientation is preferred.

6.3.1 Orientation of Logic Symbol Lettering

In diagrams where two orientations of the lettering are permitted, all lettering inside a logic symbol including alphanumeric qualifying symbols should be oriented parallel to the predominant direction of the input and output lines on the symbol. See Fig 6.¹⁰

¹⁰For special IEC requirements, see Appendix 11..

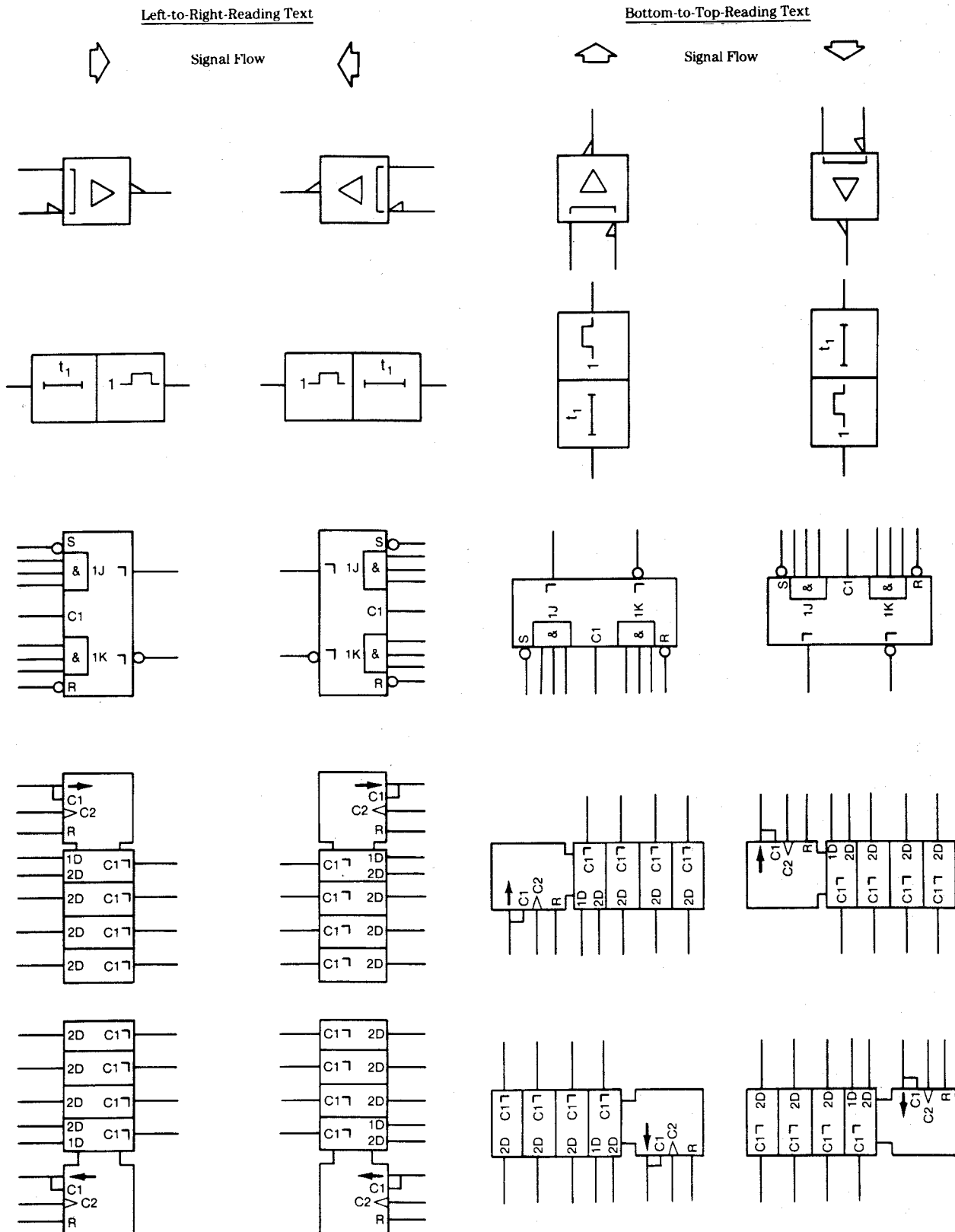
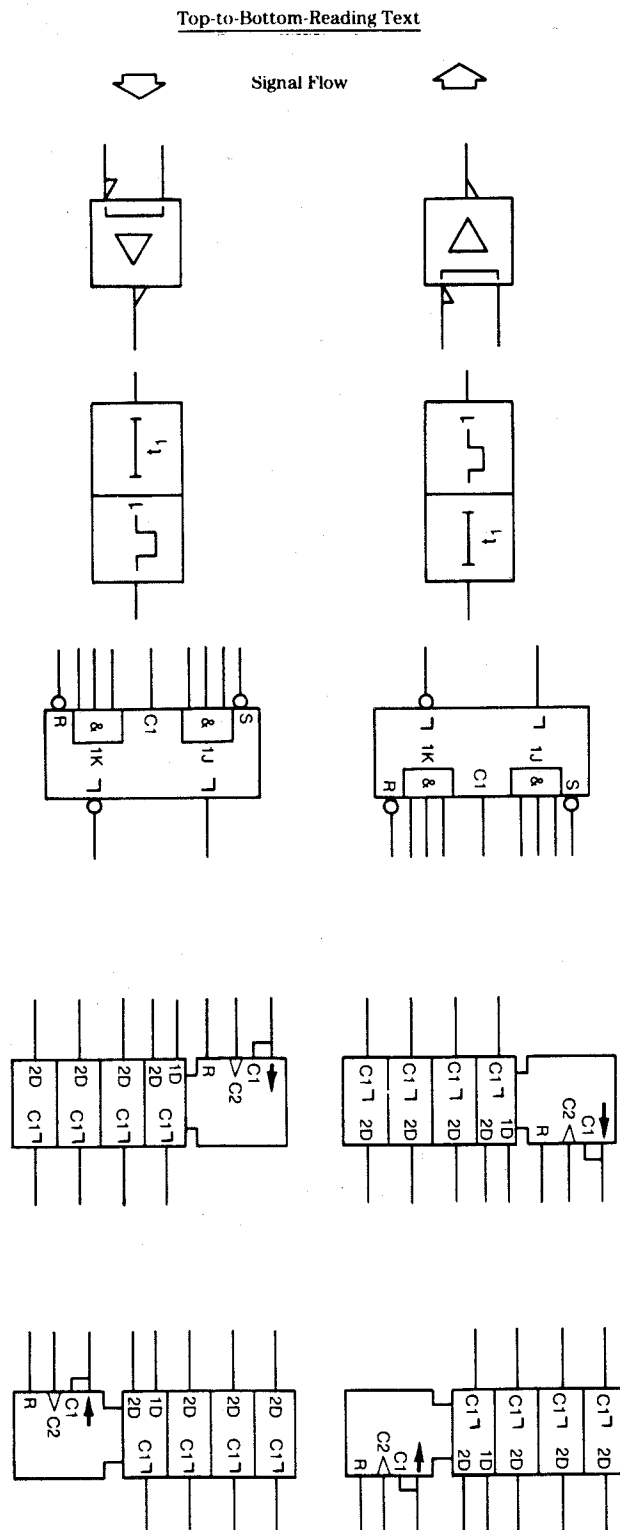


Figure 6—Logic Symbol Orientation Examples for Diagrams that Permit Two Orientations of Text



NOTE: Arrows showing the direction of signal flow have been omitted from the individual symbols. The need to add arrowheads must be considered in the context of the diagram in which the symbol appears.

Figure 6—Logic Symbol Orientation Examples for Diagrams that Permit Two Orientations of Text (continued)

6.3.2 Orientation of Qualifying Symbols Derived from Characteristic Curves

If part of a symbol is derived from the characteristic curve of a device, this part of the symbol shall not be rotated. However, in logic symbols, orientation shall be maintained with respect to the lettering within the symbol. See Fig 7.

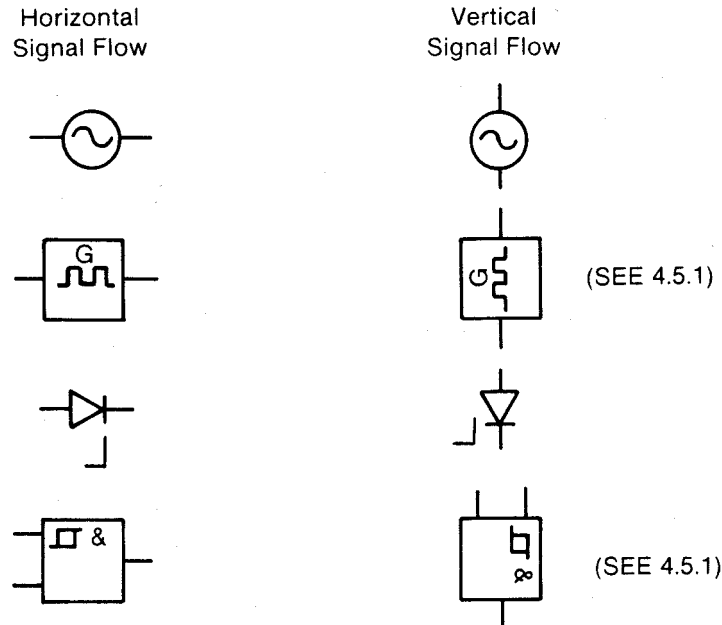


Figure 7—Orientation of Qualifying Symbols Derived from Characteristic Curves
(See NOTE to Fig 6)

6.4 Application and Identification Information

Identification or detailed references within or adjacent to symbols, other than qualifying symbols, indicator symbols, and control symbols, are referred to as application information (tagging lines). See Fig 8.

6.4.1 Types of Application Information

Depending upon the kind of logic diagram and its hardware implementation: all, none, or any combination of the types of application information that follow may be needed.

6.4.1.1 Reference Designation

Reference designations uniquely identify symbols on a diagram and shall be in accordance with ANSI/IEEE Std 200-1975 and the applicable portion of ANSI/IEEE Std 315-1975. All letters and digits that make up a reference designation shall be of the same size and on the same line, with no spaces or hyphens between them. Reference designations are required on detailed logic circuit diagrams.

All symbols representing elements contained within the same physical package (device) shall carry the same basic reference designation. If a device is represented by several detached symbols (see 6.8), then each symbol should carry a different alphabetic suffix to the reference designation.

The examples in this standard conform to the Unit Numbering Method of ANSI/IEEE Std 200-1975 .

6.4.1.2 Element Physical Identification (Type Designation, Reference Number, Part Number, Circuit Diagram Number, etc)

In the case of highly complex function elements, the logic element physical identification (type designation, type number) may be provided as part of the symbol function information.

6.4.1.3 Physical Location of Device (In the Assembly)

6.4.1.4 Functional Use (Function of Element in the Particular Circuit)

6.4.1.5 Terminal Identification (Required on Detailed Logic Diagrams)

Terminal identification or pin numbers shall be shown outside of and adjacent to the symbol. They may be placed adjacent to the connection line or in a break in the connection line. See Figs 9, 10, and 11 for typical examples. If a single terminal on the symbol represents a multiplicity of physical device terminals, reference shall be made to supporting information that provides individual terminal identification.

6.4.1.6 Other Information (Such as Values, Stylized Waveforms, and Pulse and Timing Characteristics)

6.4.2 Application Information Placement

Care shall be exercised to separate application information from qualifying symbols, indicating symbols, and control designation symbols. Arrangement and meaning of application information should be consistent on a set of drawings, and should be explained on the diagram or in supporting documentation.

The sequence of application information and identification information should remain the same even if all types of information are not provided; the lines of application information should be compressed, leaving no blank lines.

6.4.2.1 Logic Symbols

The preferred placement of application and identification information for logic symbols is internal to the symbol. A suggested arrangement of information is shown in Fig 8 (a), (b), and (c). If the information is shown external to the logic symbol it shall be placed adjacent to the symbol, and should be in the same sequence as if it were internal to the symbol.

6.4.2.2 Nonlogic Symbols

Application and identification information for nonlogic symbols shall be placed adjacent to the symbol with the reference designation on the first line and the remaining information provided on succeeding lines in the same order as for logic symbols on the diagram. See Fig 8 (d) for an example.

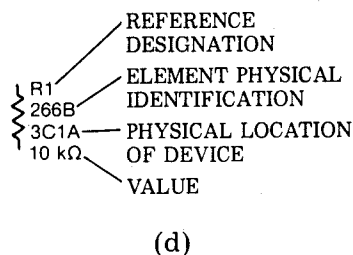
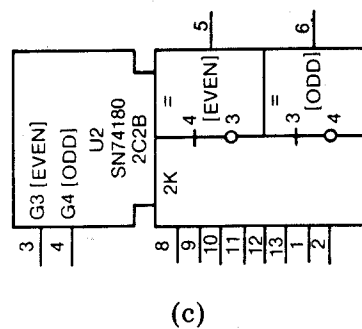
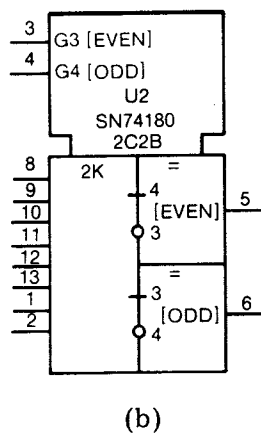
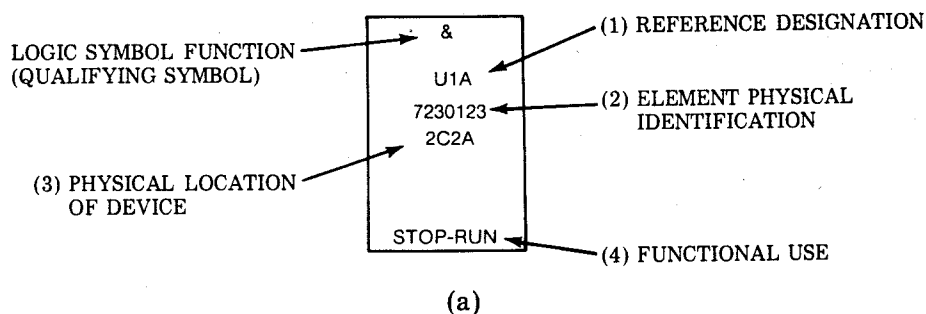


Figure 8—Application Information: Typical Examples

6.5 Inputs and Outputs with Multiple Functions

Some logic devices have inputs or outputs that serve more than one function. For example, a terminal may be an input and an output at different times, or an input may be a clock input and a level-operated control input. Multiple-function terminals may be depicted in the following ways:

- 1) The individual functions may be shown as separate inputs or outputs tied together outside the symbol outline.

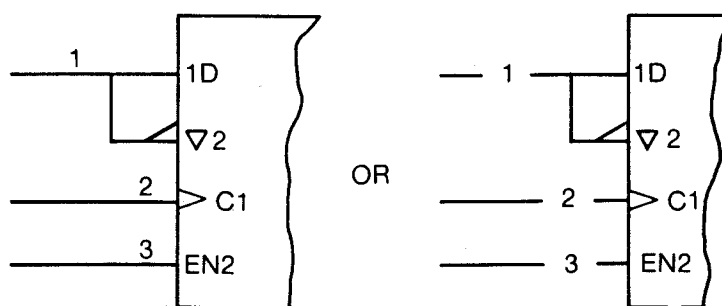


Figure 9—Multiple-Function Terminal (Terminal 1) Shown as Separate Lines

This method requires that the terminal identification (pin number) be positioned on or adjacent to the combined circuit path. This location of the terminal identification indicates that the connection is internal to the device.

- 2) If all functions require identical polarity and dynamic symbols and if no ambiguity is likely regarding which labels apply to the input and output functions, then a single terminal may be shown and a solidus (/) used to separate the labels associated with the separate functions.

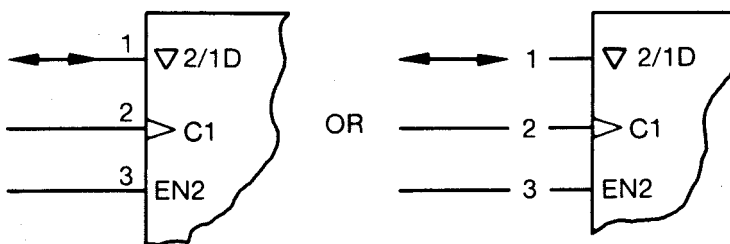


Figure 10—Multiple-Function Terminal (Terminal 1) Shown as a Single Line

- 3) To simplify a diagram, a multiple-function terminal may be depicted more than once at the symbol outline with the terminal identification repeated, provided the requirements of 7.4 are met.

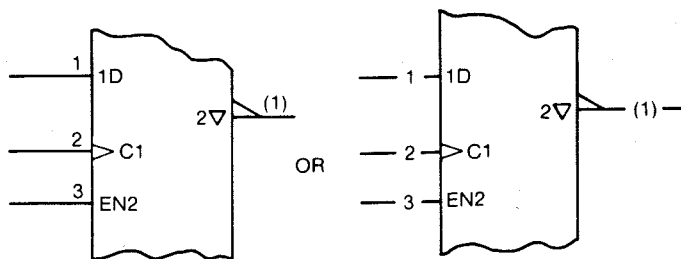


Figure 11—Multiple-Function Terminal (Terminal 1) Repeated on Symbol Outline

If necessary to identify repetitive information, this may be done by placing the repeated terminal identification in parentheses or by a special identifier explained on the diagram.

6.6 Abbreviated Representation of Symbols

6.6.1 Identical Inputs and Outputs

A set of identical inputs to or outputs from an element (inputs or outputs having identical functions and labels) may be shown in abbreviated form by using the symbol $\text{---}/\text{n}$ for multiple conductors and a single input or output line at the element. This technique cannot be used if terminal identifiers are required at the symbol.

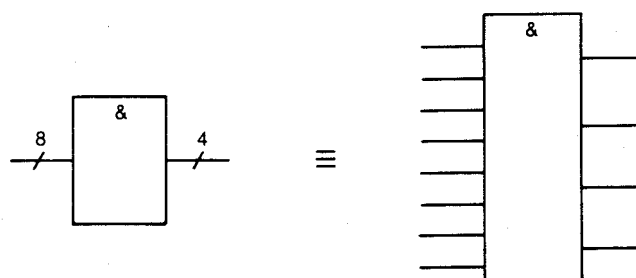


Figure 12—Abbreviated Representation of Identical Inputs and Outputs

6.6.2 Arrays of Identical Elements (See Fig 13.)

An array of identical elements may be indicated in abbreviated form by using the symbol $\text{---}/\text{n}$ for multiple conductors and the notation “mX” where m is to be replaced by a number indicating the number of elements in the array. In the case of logic symbols, this notation shall be placed in the position used for the normal general qualifying symbol. If this position is already occupied by a general qualifying symbol, then “mX” shall be placed in front of the general qualifying symbol.

NOTE — Because the elements are identical, the multiple conductors are distributed equally among the elements.