

IEEE Guide for the Application of Thyristor Surge Protective Devices

Sponsor

**Surge Protective Devices Committee
of the
IEEE Power Engineering Society**

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Abstract: Applications information on fixed voltage and gated thyristor surge protective devices (SPDs) are provided. Key device parameters and their sensitivities are explained. Several worked telecommunication circuit design examples are given.

Keywords: application guide, telecommunication circuits, thyristor surge protection devices

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Introduction

(This introduction is not part of IEEE Std C62.37.1-2000, IEEE Guide for The Application of Thyristor Surge Protective Devices.)

This application guide has been produced as the companion to the IEEE Std C62.37-1996, IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices (SPDs). The thyristor SPD parameters measured in IEEE Std C62.37-1996 are explained in terms of their application relevance and any operating condition sensitivities discussed. Several worked telecommunication circuit design examples are given, together with overviews of system problems, such as SPD coordination.

There are a very large number of thyristor SPD variants available. The two basic families of fixed-voltage and gated thyristor SPDs are further subdivided into bidirectional and unidirectional types. This guide provides information on these different types and the applications that they are most suited to. Substantive annexes provide information on design approaches, SPD technologies, device symbols, and equipment standards.

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IEEE Guide for the Application of Thyristor Surge Protective Devices

1. Scope

This application guide applies to thyristor surge protective device (thyristor SPD) components used in systems with voltages up to 1000 V rms or 1200 V dc. These components are designed to limit overvoltages and divert surge currents by voltage clamping and crowbarbing (switching to a low impedance) actions. Although telecommunication circuits are the main application of thyristor SPDs, this guide will also provide useful information for other protection applications.

This guide is intended to complement the IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices (IEEE C62.37-1996). The definitions used in these two standards are the same.

This publication contains information on

- a) Basic function and component description
- b) General terms and definitions
- c) Electrical environment
- d) Parameter interpretation and application
- e) Example designs
- f) SPD technology comparison

When used in conjunction with IEEE Std C62.37-1996, this guide will give the user guidance in interpreting its specifications and in selecting the correct product.

2. References

This guide shall be used in conjunction with the following publications:

IEC 60050-191 (1990-12): International Electrotechnical Vocabulary (IEV)—Chapter 191: Dependability and quality of service.¹

¹IEC publications are available from IEC Sales Department, Case Postale 131, 3, rue de Varembe, CH-1211, Genève 20, Switzerland/Suisse. IEC publications are also available in the United States from the Sales Department, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY 10036, USA.

IEC 61000-4-5 (1995-03): Electromagnetic compatibility (EMC)—Part 4: Testing and measurement techniques—Section 5: Surge immunity test.

IEEE C62.37-1996, IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices.²

IEEE C62.41-1991 (Reaff 1995), IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits.

IEEE C62.42-1992 (Reaff 1999), IEEE Guide for the Application of Gas Tube Arrester Low-Voltage (Equal to or Less than 1000Vrms or 1200 Vdc) Surge-Protective Devices.

3. Definitions

For the purpose of this guide, the following definition has been used in addition to those in IEEE Std C62.37-1996 and *The Authoritative Dictionary of IEEE Standards Terms* [B8]³.

3.1 anti-parallel (connection): A parallel combination of two semiconductor elements, where the main current entry electrode of one element connects to the main current exit electrode of the other element, allowing one element to pass current in one voltage polarity and the other element to pass current in the opposite voltage polarity. (*syn*: **inverse-parallel connection** in IEEE 100 [B8])

4. Basic function and component description

This clause covers the basic device structure, its equivalent circuit, characteristic values, operational parameters, and structures with increased functions.

4.1 Basic device structure

Thyristor overvoltage protectors are manufactured by creating a series of N-type and P-type layers in a silicon chip. The basic thyristor structure has three PN junctions that require four layers (NPNP). As one layer can be the starting silicon itself (N or P-type silicon) a further three layers have to be made.

Figure 1 shows the simplified structure of a unidirectional thyristor SPD. The switching quadrant (see Figure 3) occurs when the bottom contact is positive with respect to the top contact. Also shown are the lumped equivalent circuit elements created by the semiconductor layers. This example started manufacture with an N⁺ slice of silicon. Layers of P material are then created at the top and the bottom. A further N⁺ region is then made on the top surface. Finally the top and the bottom metallization are added to provide contacts. The upper right section of the contact metal is not shown in order to illustrate the detail of the topside silicon surface.

4.2 Device equivalent circuit

In Figure 1, transistor TR1 is formed by the N⁺PN⁺ layers. Similarly transistor TR2 is formed by the PN⁺P layers. The device breakdown voltage is determined by the breakdown of the central N⁺P layers, which form a shared collector-base junction for transistors TR1 and TR2. For clarity, the breakdown function is shown as breakdown diode D1. Resistance R1 is the lateral resistance of the P layer. Resistor R2 together with resistor R1 shunt the base-emitter junction of transistor TR1 to define the value of holding current, I_H .

²IEEE C62.41-1991 (Reaff 1995), IEEE Recommended Practice on Surge Voltages in Low-Voltage AC Power Circuits.

³The numbers in brackets refer to the bibliography listed in Annex E.

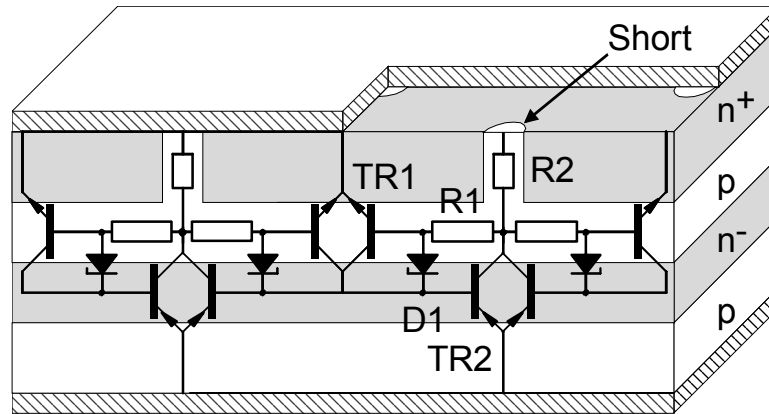


Figure 1—Simplified thyristor SPD

Resistor R2 has a relatively low value of resistance and is considered as a localized short circuit between base and emitter. During the manufacturing process, the emitter N^+ diffusion is perforated with a series of dots to create these short circuits. In Figure 1, some of the top metallization has been omitted to show the P-type shorting dots.

Figure 2 shows how the lumped circuit elements are equivalent to a thyristor. Transistors TR1 and TR2 are connected as a regenerative pair. In an unbiased condition, these transistors will be in an off state and present a high circuit impedance. If sufficient positive voltage is applied, diode D1 will break down and supply current to the transistor base regions. Initially, only transistor TR2 will conduct as the base-emitter shunt resistance of transistor TR1 will bypass the current. In this condition, the device voltage-current characteristic will be determined by the collector-emitter breakdown characteristic of transistor TR2. When sufficient current flows through the shunt resistance to initiate conduction of transistor TR1, the transistor pair will regenerate and switch (crowbar) to a low-voltage, on-state condition. The transistor pair will remain in this condition until the conducted current is too small to maintain sufficient voltage across the shunt resistance to activate transistor TR1. The current at which the transistor pair begins to switch off is called the holding current.

A simplified model of the lumped equivalent circuit replaces transistors TR1 and TR2 with a thyristor. This thyristor has a breakdown diode connected between its N-type and P-type gates and a resistive shunt between the P-type gate and cathode (see Figure 2). (An alternative version is possible with the resistive shunt between the N-type gate and the anode.)

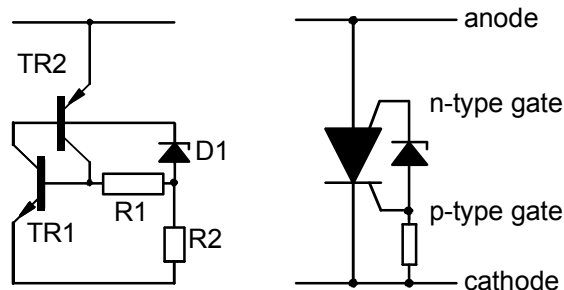


Figure 2—Lumped circuit and thyristor equivalent

4.3 Switching characteristics

The switching characteristic of a thyristor SPD consists of the following four regions:

- Off-state
- Breakdown
- Negative resistance
- On-state (see Figure 3)

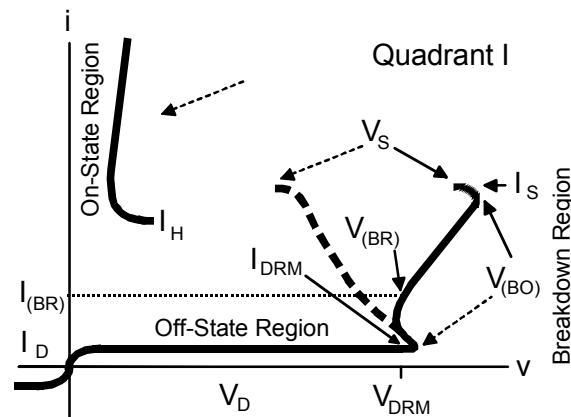


Figure 3—Thyristor SPD switching characteristic

4.3.1 Off-state region

The off-state region is the high-resistance, low-current portion of the voltage-current characteristic. This region extends from the origin to commencement of breakdown. The off-state current is the sum of junction reverse current and any surface leakage current. Two measurements are typically made in this region: off-state current (I_D), measured with the dc off-state voltage (V_D) applied; and repetitive peak off-state current (I_{DRM}), measured with the rated repetitive peak off-state voltage (V_{DRM}) applied.

4.3.2 Breakdown region

The breakdown region is the low-resistance, high-voltage portion of the voltage-current characteristic. This region begins where the low-current portion of the voltage-current characteristic changes from a high dynamic resistance to a region of substantially lower dynamic resistance for an increasing magnitude of current. Finally, this region terminates when sufficient thyristor regeneration occurs to initiate switching. Depending on the thyristor design and temperature, the end of the breakdown region may be at a higher or lower voltage than at the start. The low-resistance characteristic of this region is the result of junction breakdown combined with transistor action. The maximum voltage that occurs in the breakdown region is defined as the breakover voltage [$V_{(BO)}$]. Additional measurements may be made of the breakdown voltage [$V_{(BR)}$] at a given breakdown current [$I_{(BR)}$] and the voltage and current at the switching point [V_S , I_S].

4.3.3 Negative-resistance region

The negative-resistance region represents the trajectory from the breakdown region switching point to the on-state condition. This region is a dynamic condition, where the thyristor regeneration (internal positive current feedback) increases with time, causing an increased current demand that pulls down the voltage across the thyristor until the on-state condition is reached.

4.3.4 On-state region

The on-state region is the low-resistance, high-current portion of the voltage-current characteristic. In the on-state condition, the thyristor is fully regenerated and develops the minimum voltage drop for the current flowing. The minimum current that will just maintain the on-state condition is defined as the holding current, I_H . Currents below this value will cause the thyristor to switch off.

4.4 Performance criteria of thyristor SPDs

The performance of a thyristor SPD can be categorized as system loading, in terms of current drawn, holding current and capacitance; equipment protection, defined as peak let-through voltage and fault mode; and durability (reliability), assessed as surge and environmental life.

NOTE—The term “reliability” is context sensitive, see Annex A.

4.4.1 System loading

Under normal system operation, the thyristor SPD should be effectively transparent. The thyristor SPD should not cause system loading by drawing excessive current under stand-by or maximum signal conditions, failing to restore normal operation after a surge or causing capacitance unbalance.

Stand-by loading is covered by the off-state current, I_D , parameter. For most telephone applications a test bias voltage, V_D , of -50 V is appropriate. Off-state current increases with temperature therefore a maximum value at the highest expected system ambient temperature needs to be specified.

The maximum system voltage without major voltage clipping can be defined by one of two parameters. To guarantee that the thyristor SPD is still in the off-state at the highest signal amplitude, the rated repetitive peak off-state voltage, V_{DRM} , must be higher than this level. In many systems, a few milliamperes of current due to clipping of the ring signal will not interfere with the system operation. In these cases, the low current [$I_{BR} \leq 20$ mA] breakdown voltage, $V_{(BR)}$, may be specified as equal to the highest signal amplitude. The voltage value of both of these parameters will be reduced at low temperatures and so the required values should be specified at the lowest expected system ambient temperature.

When the signal wires are protected by the thyristor SPDs to ground, ac line unbalance can be caused by the difference in protector capacitance. The off-state capacitance of a thyristor SPD increases with increasing junction temperature, T_J , and decreases with increasing bias voltage, which is comprised of the dc voltage, V_D , and the ac signal voltage, V_d . When $V_D \gg V_d$, the capacitance value is independent of the value of V_d . Over the range of normal telecommunication frequencies, the capacitance is essentially constant. To estimate accurately the capacitance unbalance of the thyristor SPD pair, the test conditions must reflect those of normal operation.

After the thyristor SPD has switched to the on-state to divert a surge current, it must switch off to restore normal operation after the surge has ended. The thyristor SPD holding current, I_H , is the current value at which it switches off. The holding current value decreases as the junction temperature or the circuit impedance increases. The holding current should be greater than the maximum available dc current under the worst-case conditions.

4.4.2 Equipment protection

To protect, the thyristor SPD peak let-through voltage shall not exceed the equipment voltage capability under all surge conditions. In some applications, the maximum surge level is unknown and the desirable fault mode will be specified.

An overvoltage can be due to an impulse or a relatively long ac stress. The peak impulse let-through voltage will increase as the impulse rate of rise increases. Under ac surge conditions, heating and the resultant junction temperature rise increases the breakover voltage [$V_{(BO)}$]. At low currents, heating is due to breakdown region losses. At high currents, heating is due to on-state losses.

In telecommunication applications, there are two classes of protector—primary and secondary. Primary protection is applied at the system location where it may prevent most of the stressful energy from propagating beyond the designated interface. Secondary protection is applied subsequently to the primary protection and is subject to lower and better-defined stress levels. When a surge greatly exceeds the capability of a thyristor SPD it fails catastrophically, it may be desirable that the primary protector fails short circuit and so prevents the surge from propagating further. Primary protectors are normally tested to ensure their failure mode is appropriate to their application.

4.4.3 Durability

The thyristor SPD should have an adequate service life, and a design life in excess of 20 years is typical. Most of this period would be under normal operating conditions, and the product would have to pass a series of aggressive environmental tests to verify life expectancy. Surge conditions are a small, but significant, proportion of the service life. Surge durability is typically evaluated by repetitively surging the protector at various current levels.

4.5 Additional thyristor SPD structures

4.5.1 Gated thyristor SPD

These devices have a gate (G, g) terminal that controls the switching region characteristics, and two principal terminals provide the protective function. Three gate types are possible, as this additional terminal may be connected to either an intermediate P or N layer (Figure 4) of the thyristor SPD or a combined NP region (Figure 7). Some gated thyristor SPDs are designed to also allow operation without gate control. Without gate control the device operation and characteristics are the same as a fixed-voltage thyristor SPD (see 3.2).

In all gated thyristor SPDs, there will be the equivalent of a PNP transistor and an NPN transistor connected as a regenerative pair (Figure 4). In an unbiased condition, this transistor pair will be in an off state and present a high circuit impedance. The gate terminal layer and its adjacent principal terminal layer form a PN junction. When current is conducted by this PN junction, charge carriers are injected into the transistor pair. If sufficient gate current flows, the transistor pair will regenerate and switch (crowbar) to a low-voltage, on-state condition. The transistor pair will remain in this condition until the principal current is too low to maintain the conduction of the transistor pair.

There are two possible current loops for the gate current. One exists when the circuit producing the gate current is connected to the gate and its adjacent principal terminal. The other exists when the circuit providing the gate current is connected between the principal terminals. When the thyristor SPD is in the off state, there will not be any substantial current flow directly between the principal terminals. In this condition, the current flow loop is completed by the circuit connected between the gate and its nonadjacent principal terminal. The current flow path is adjacent principal terminal, gate terminal, and through the gate network to the nonadjacent principal terminal.

The most common circuit use for these devices is in the common gate configuration. By biasing the gate with an external reference voltage, such as the protected integrated circuit (IC) supply voltage, the protection voltage will track the value of the reference voltage. A P-gate device, with the gate biased negatively with respect to the anode, will provide negative transient voltage protection with respect to the anode. Similarly, an N-gate device, with the gate biased positively with respect to the cathode, will provide positive transient voltage protection with respect to the cathode.

These devices can also be current triggered in a conventional manner. In some cases, this is done by connecting the gate and adjacent electrode in series with the protected line wire.

4.5.2 Unidirectional blocking thyristor SPD

The switching quadrant performance of this device structure (Figure 4) is covered in 4.3. The inherent (fixed) voltage breakdown can be lowered by gate control, either by use of a single gate or both together. In the non-switching quadrant, current flow will be blocked by the reverse-biased N-P anode junction.

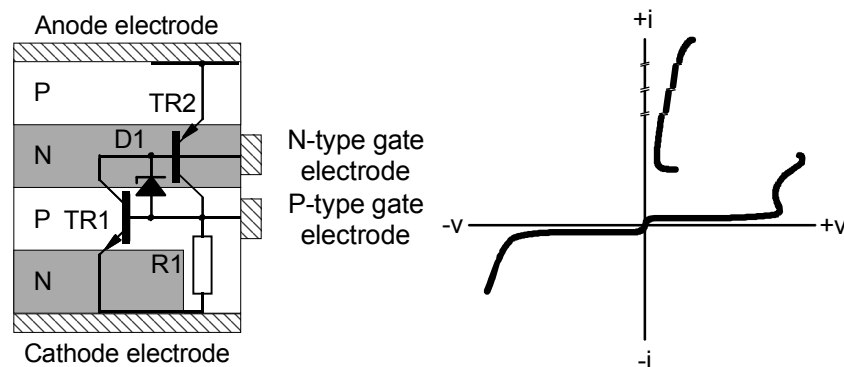


Figure 4—Unidirectional blocking thyristor SPD

4.5.3 Unidirectional conducting thyristor SPD

The switching quadrant performance of this device structure (Figure 5) is covered in 4.3. The inherent (fixed) voltage breakdown can be lowered by gate control, either by use of a single gate or both together. In the non-switching quadrant, current will be conducted by the forward-biased PN diode.

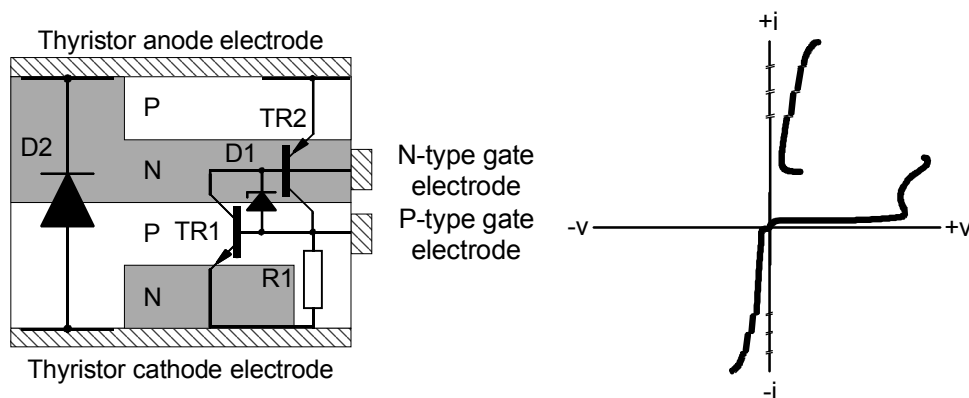


Figure 5—Unidirectional conducting thyristor SPD

4.5.4 Bidirectional thyristor SPD

This thyristor SPD has two unidirectional blocking thyristor SPD sections that are anti-parallel connected to give switching in quadrant 1 and quadrant 3 (see Figure 6). The inherent (fixed) voltage breakdown in each quadrant can be lowered by controlling the appropriate gate or gates.

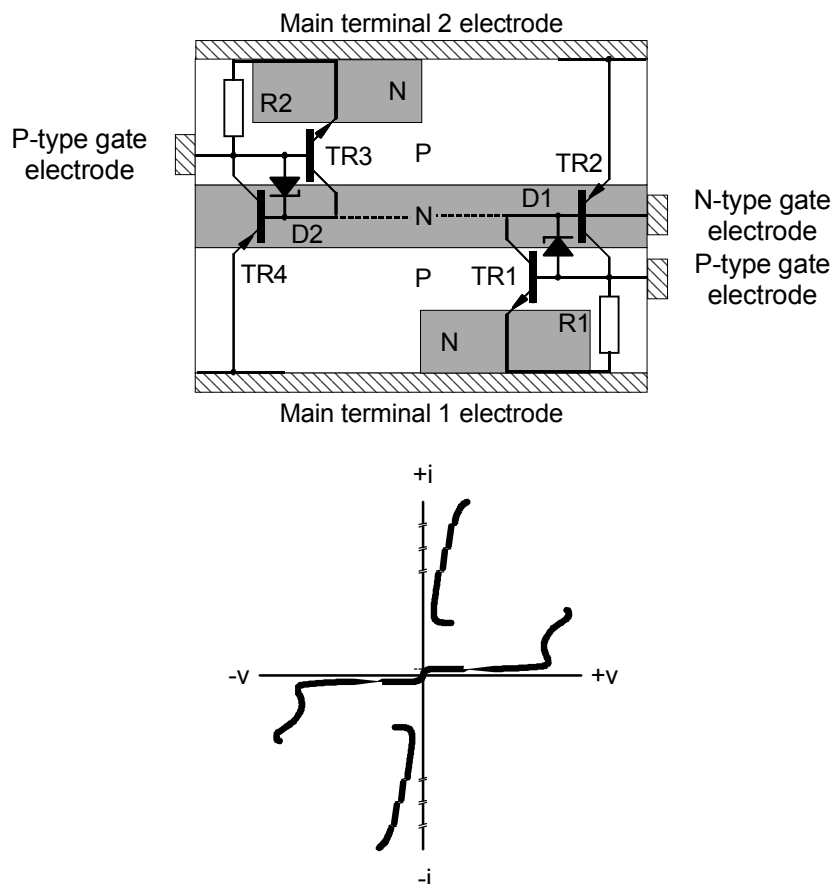


Figure 6—Bidirectional thyristor SPD

4.5.5 Bidirectional TRIAC thyristor SPD

This bidirectional thyristor SPD has a special gate structure (see Figure 7) that permits control in both quadrants with a single gate terminal. This is the standard TRIAC (TRIode for AC control) structure.

5. General terms and definitions

For the purposes of this guide, the definitions listed in 5.1 apply.

5.1 Types of thyristor SPD

The thyristor SPD is classified by the type of characteristic in quadrant 1 and in quadrant 3, and the number of terminals. At least one quadrant will have a switching characteristic (see Figure 8). The other quadrant may have a switching, blocking, or diode conduction characteristic (see Figure 8 and Figure 9). Devices with only one switching quadrant are called unidirectional and may have two (diode), three (triode), or four (tetraode) terminals. In addition, devices with two switching quadrants are called bidirectional and may have up to five (pentode) terminals (see Table 1).

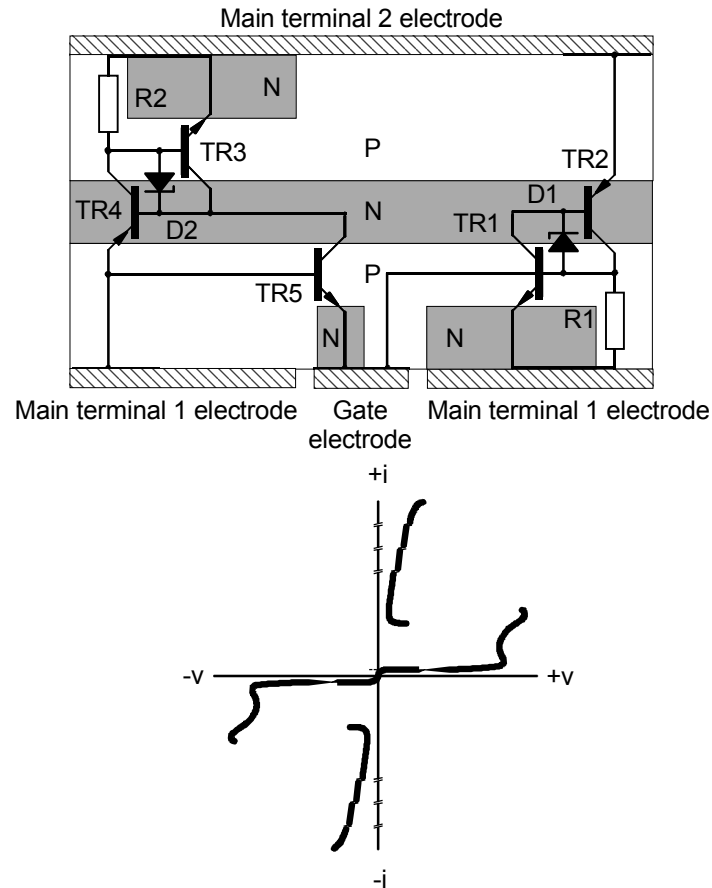


Figure 7—Bidirectional TRIAC thyristor SPD

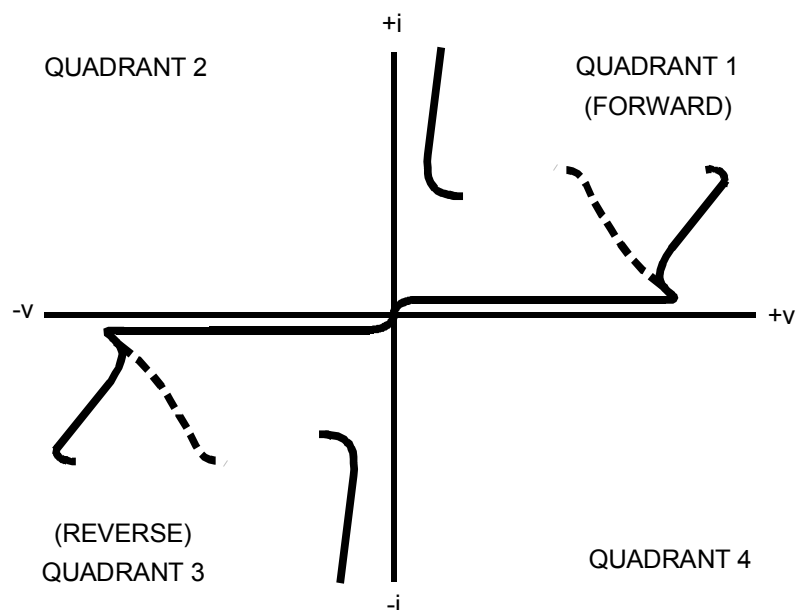


Figure 8—Switching characteristics in quadrant 1 and quadrant 3

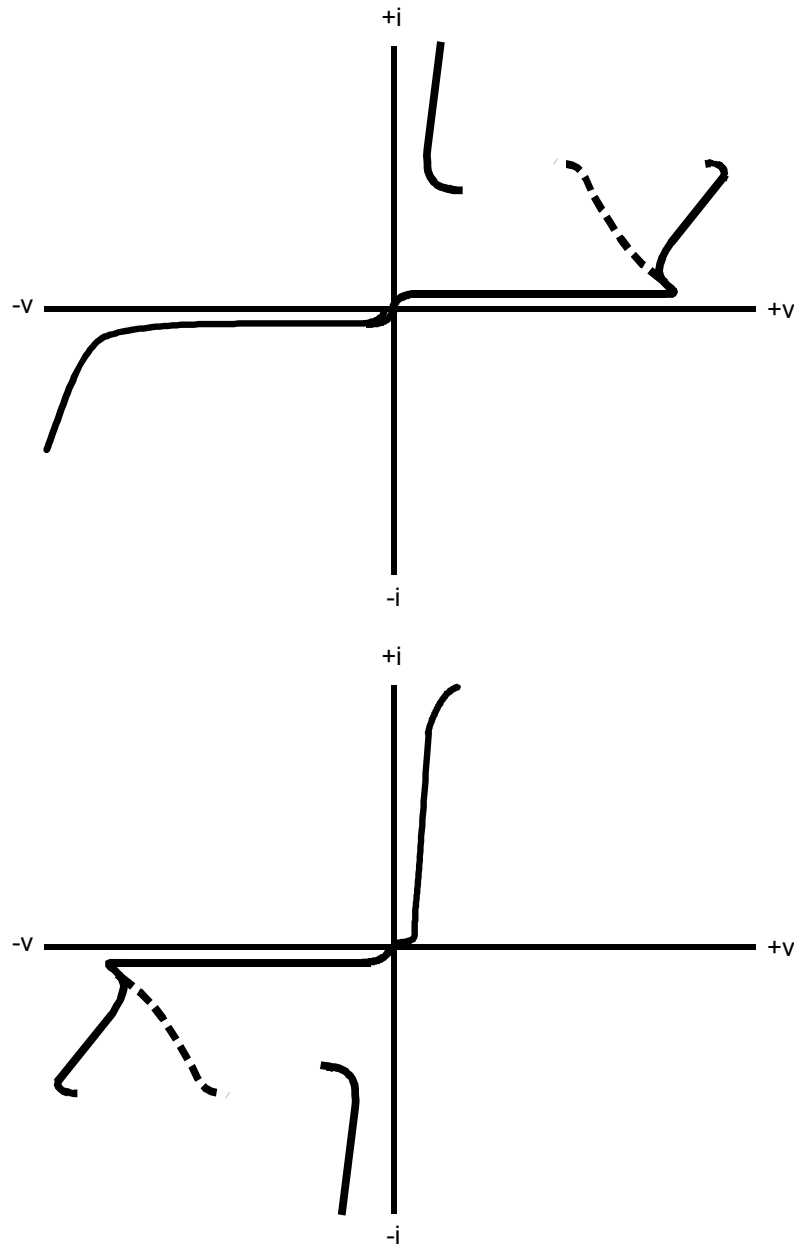


Figure 9—Examples of non-switching characteristics—reverse blocking in quadrant 3 and forward-conducting in quadrant 1

6. Electrical environment

Electrical and electronic systems and networks are subject to disturbances from external sources of electrical energy. These sources include electrical power circuits and natural phenomena, such as lightning. The effects of such disturbances may be confined to interference with normal use or operation, as in the case of noise or interference with signalling; or they may be capable of creating hazards to users and maintenance personnel or even damage to equipment. IEEE Std C62.42-1987 and IEEE Std C62.41-1991 contain further information on these environmental disturbances.

Table 1—Types of thyristor SPD

Number of terminals	Other quadrant characteristic		
	Blocking	Conducting	Switching
2 (diode)	Reverse-blocking or forward-blocking diode thyristor SPD	Reverse-conducting or forward-conducting diode thyristor SPD	Bidirectional diode thyristor SPD
3 (triode)	Reverse-blocking or forward-blocking triode thyristor SPD P-gate or N-gate	Reverse-conducting or forward-conducting triode thyristor SPD P-gate or N-gate	Bidirectional triode thyristor SPD P-gate or N-gate or combined P-gate and N-gate (TRIAC)
4 (tetrode)	Reverse-blocking or forward-blocking tetrode thyristor SPD P-gate and N-gate	Reverse-conducting or forward-conducting tetrode thyristor SPD P-gate and N-gate	Bidirectional tetrode thyristor SPD two gates
5 (pentode)			Bidirectional pentode thyristor SPD three gates

7. Parameter interpretation and application

This clause covers the relevance of thyristor SPD parameters to the system needs and details factors that affect those parameters. These parameters are grouped into the following three areas:

- Normal system operation
- Equipment protection
- Durability

7.1 Normal system operation parameters

These are parameters that affect the normal system operation. The thyristor SPD should not substantially interfere with the normal system operation; it should be transparent in normal system operation. Major performance areas are dc stand-by current, capacitive shunt impedance effects, distortion through signal clipping and restoration of service after an overvoltage.

7.1.1 Off-state current— I_D

Off-state current is the dc stand-by current that flows through the thyristor SPD when a dc voltage, V_D , is applied. The value of the applied test voltage, V_D , should be the same as the mean dc voltage level of the system. In many telecommunication systems, this would be the battery voltage level, which is typically -50 V.

Figure 10 shows the typical temperature variation of off-state current. The off-state current has two components—a leakage current across the chip surface and an internal reverse current that flows through the chip's blocking junction. Surface leakage increases slowly with increasing temperature. Reverse junction current increases rapidly with temperature, more than doubling with every 10°C rise.

Figure 10 shows that surface leakage current predominates at low temperatures and reverse junction current dominates at high temperatures. The crossover temperature of these two components depends on the chip size and surface quality.

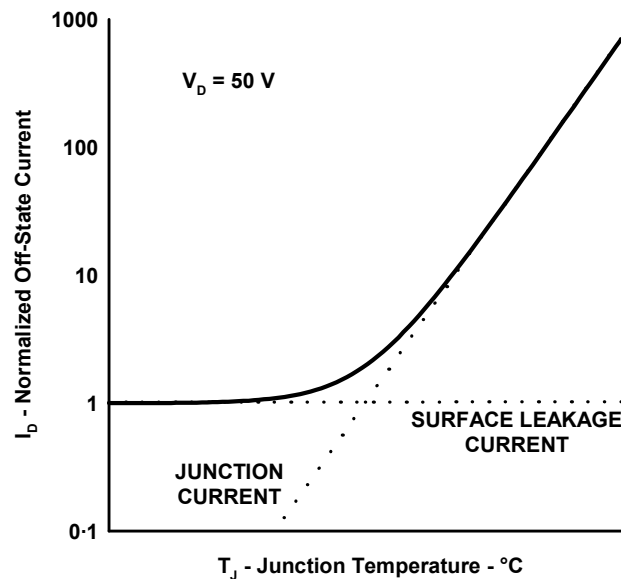


Figure 10—Normalized off-state current versus temperature

The test conditions for this parameter should specify the mean system dc voltage (V_D) and the highest system ambient temperature (T_A). In some systems, the mean system dc voltage may vary considerably from its nominal value, e.g., during battery charging, and this will affect the choice of the V_D value. Gated devices will need to have the gate terminal bias condition specified for this test.

Gated devices will also need the gate terminal dc stand-by current specified. Normally, a gate terminal junction will be reverse biased and have a characteristic similar to Figure 10. Measurement conditions should be specified similar to V_D . Current will be measured between the gate and one principal terminal. The measurement conditions should also include the condition of the other principal terminal (I_{GAS} , I_{GAO} , I_{GKS} , I_{GKO}). See IEEE Std C62.37-1996.

7.1.2 Repetitive peak off-state voltage— V_{DRM}

Repetitive peak off-state voltage is the maximum system voltage that can be applied to the thyristor SPD over a specified temperature range without the onset of clipping. Clipping causes system current to be diverted through the device.

Repetitive peak off-state voltage is a rating and is tested by applying V_{DRM} to the protector and measuring the resultant current that flows through the thyristor SPD. This voltage rating should be equal to or greater than the peak system operating voltage. In most analog telephone systems, the maximum voltage will occur during ringing, but occasionally maintenance test voltages may be higher.

Figure 11 shows how the single temperature value of V_{DRM} varies with temperature. The 25 °C value is normalized to unity. V_{DRM} is typically made up of an ac voltage with a dc voltage component. As the peak, repetitive off-state current is typically of the microampere order, the resultant power loss with V_{DRM} applied is very small. Practically, this makes the device junction temperature, T_J , rise above the local ambient temperature, T_A is very small. Under these circumstances, T_J and T_A can be regarded as equal in value. Figure 11 shows that V_{DRM} decreases with decreasing temperature and the lowest value will be at low temperatures. The critical value for V_{DRM} is at the lowest device (ambient) temperature, and it should be equal to or greater than the maximum system voltage.

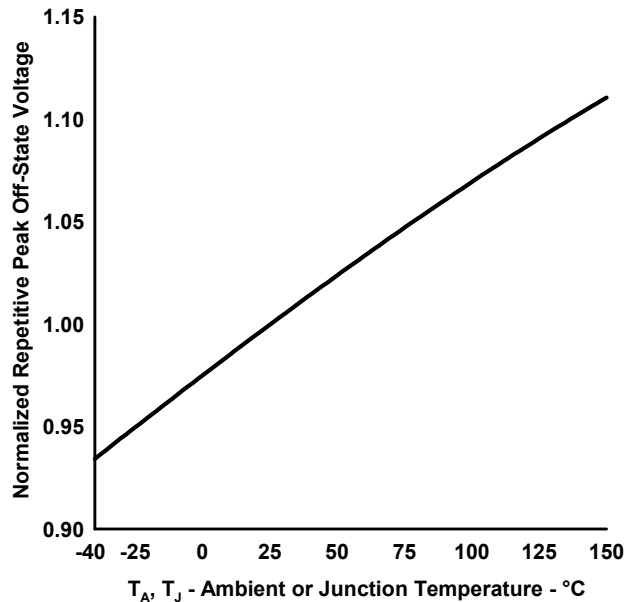


Figure 11—Normalized off-state voltage versus temperature

If the lowest temperature was 0, the V_{DRM} would have fallen to 0.975 of the 25 °C value. If the maximum system voltage was 200 V, V_{DRM} should be 200 V at 0 and the 25 °C verification check should be at $200/0.975 = 205$ V (measured at 25 °C). If the lowest device temperature was -40 °C, the values become 0.94 and 213 V.

The test conditions for repetitive peak off-state current should specify the maximum system peak voltage ($= V_{DRM}$ rating) and the system ambient temperature range (T_{AMIN} to T_{AMAX}).

For gated devices, this parameter may be covered by the V_D specification. Alternatively, these devices may be verified for V_{DRM} with the gate terminal open ($I_G = 0$) or connected to the appropriate principal terminal.

7.1.3 Critical rate of rise of off-state voltage— dv/dt

This is the maximum rate of rise of voltage that can be applied to the thyristor SPD over a specified temperature range without causing the device to switch on. The thyristor SPD should not switch on as a result of large dv/dt transitions that occur during normal system operation. In many telephone systems, these transitions do not exceed 50 V/ μ s. In such cases, a device dv/dt value of above 50 V/ μ s would give satisfactory performance. In addition, transition excursion would need to be in excess of at least 5 V to cause internal junction conduction. High dv/dt values of 1 kV/ μ s or more only reflect the inherent thyristor SPD technology, rather than a system need.

The device dv/dt rating should be based on the maximum system dv/dt applied as a ramp having an amplitude limited to the V_{DRM} value. In addition, gated devices will need to have the gate terminal bias condition specified.

7.1.4 Breakdown voltage— $V_{(BR)}$

This is a measure of the thyristor SPD voltage limiting at breakdown currents of a few milliamperes. It is comparable to the breakdown voltage of zener and avalanche diodes. If normal system operation causes device breakdown, system voltages will be clipped (limited), resulting in distortion and causing current

diversion through the thyristor SPD. In the telephone system, this action may cause equipment malfunction (e.g., false off-hook detection).

The preferred parameter for ensuring that the system voltages are not clipped is V_{DRM} . However, there has been a historical use of $V_{(BR)}$ (often called V_Z in older specifications) and the purpose of this clause is to provide background information. The breakdown voltage parameter is only used for fixed voltage, positive breakdown slope thyristor SPDs. It is inappropriate for fixed-voltage, negative breakdown slope and gated thyristor SPDs. These devices are specified by a V_{DRM} value and not by $V_{(BR)}$.

Breakdown voltage is a characteristic and is determined by applying a defined current to the device and measuring the resultant voltage. Test current levels in the range of 1 to 20 mA are typical. If $V_{(BR)}$ is specified, the minimum breakdown voltage value should be greater than the normal peak system operating voltage over the device temperature range.

Figure 12 shows how an avalanche breakdown voltage varies with temperature. The 25 °C value is normalized to unity. Figure 12 shows that $V_{(BR)}$ reduces with decreasing temperature and that the lowest value will be at low temperatures. The critical value for $V_{(BR)}$ is at the lowest device temperature, and it should be greater than the maximum system voltage by a few percent.

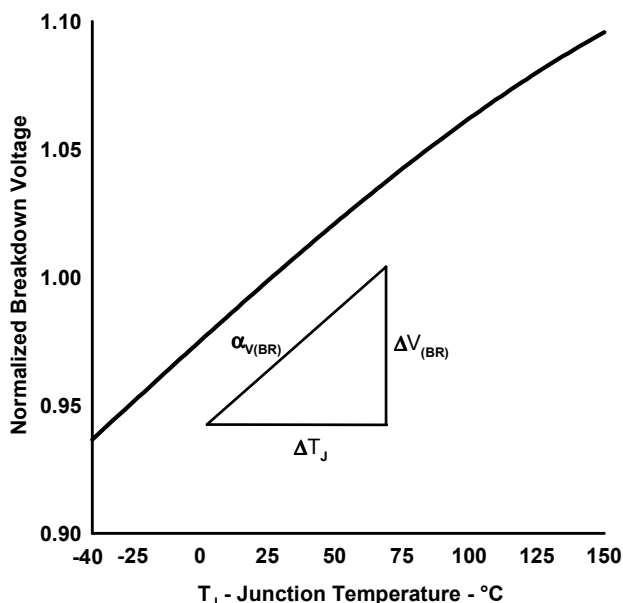


Figure 12—Normalized breakdown voltage versus temperature

The test conditions for breakdown voltage should specify the test current to be applied and the test temperature. If the test temperature is higher than the lowest system ambient temperature, the breakdown voltage temperature coefficient is required [$\alpha_{V(BR)}$ as shown in Figure 12]. The breakdown temperature coefficient will enable the calculation of the breakdown voltage at the lowest expected system ambient.

In most cases, the $V_{(BR)}$ parameter can be replaced by the same value V_{DRM} rating.

7.1.5 Holding current— I_H

This is a measure of the minimum current that will maintain the thyristor SPD in conduction after it has been switched to the on state. To ensure that the thyristor SPD switches off and restores normal system operation, the holding current must be greater than the maximum system dc short-circuit current.

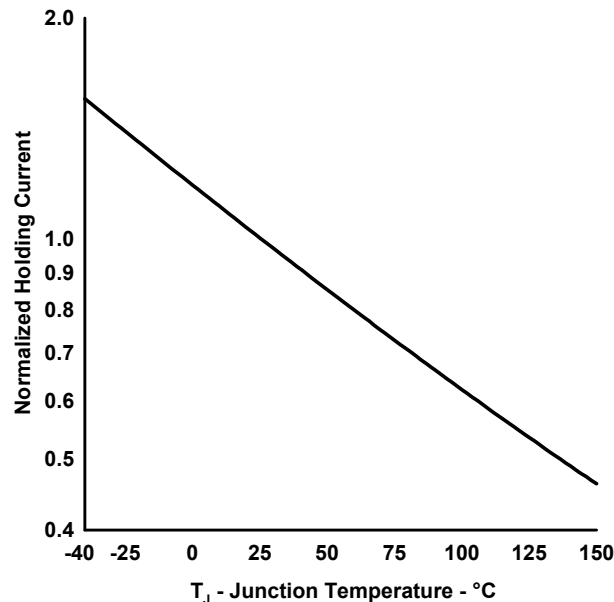


Figure 13—Normalized holding current versus temperature

Holding current is measured by switching the thyristor SPD to the on state and then reducing the on-state current until the device switches off. The current level that causes the device to switch off is taken as the holding current value.

Figure 13 shows that the holding current decreases with increasing temperature and that the lowest value will be at high temperatures. The critical value for I_H is at the highest device temperature, and it should be equal to or greater than the maximum system short-circuit current. At 70 °C, the holding current is about 0.7 of the 25 °C value.

In some cases, a temperature correction is required to allow for conduction losses. For example, consider the following parameters; system short-circuit current 100 mA, ambient temperature 70 °C, device on-state voltage 2 V, and device thermal resistance 60 °C/W. The device on-state dissipation would be $2 \text{ V} \times 0.1 \text{ A} = 0.2 \text{ W}$, leading to a temperature rise of $0.2 \text{ W} \times 60 \text{ °C/W} = 12 \text{ °C}$. So the holding current should be specified as 100 mA minimum at $70 \text{ °C} + 12 \text{ °C} = 82 \text{ °C}$ junction temperature.

The measured holding current value will reflect the residual temperature due to the previous heating history. It is important not to have large dissipation prior to measuring holding current, otherwise the holding current value will be reduced. Holding current has a minor sensitivity (<10%) to circuit resistance. It is the interaction of circuit source resistance and the shape of the thyristor SPD on-state characteristic that determines the switch-off (holding) current. The measured holding current decreases as the source resistance increases. The test conditions for holding current should specify the on-state current, the current ramp down rate, source resistance, and the maximum junction temperature. The measured holding current value should be greater than the maximum system short-circuit current.

For gated devices, gate terminal conditions will need to be specified.

7.1.6 Capacitance— C_O

The junctions, formed by the device NPNP structure, are the principle elements that define the device capacitance. The capacitance of a PN junction will depend on the applied dc bias, V_D ; ac test signal level, V_d ; and junction temperature, T_j .