

IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices

Sponsor

**Surge Protective Devices Committee
of the
IEEE Power Engineering Society**

Approved 23 October 1996

IEEE Standards Board

Approved 1 April 1997

American National Standards Institute

Abstract: This standard applies to two or three terminal, four or five layer, thyristor surge protection devices (SPDs) for application on systems with voltages equal to or less than 1000 V rms or 1200 V dc.

Keywords: test specification, thyristor surge protective devices

The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street, New York, NY 10017-2394, USA

Copyright © 1997 by the Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 1997. Printed in the United States of America

ISBN 1-55937-897-2

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Board. Members of the committees serve voluntarily and without compensation. They are not necessarily members of the Institute. The standards developed within IEEE represent a consensus of the broad expertise on the subject within the Institute as well as those activities outside of IEEE that have expressed an interest in participating in the development of the standard.

Use of an IEEE Standard is wholly voluntary. The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard. Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

Comments for revision of IEEE Standards are welcome from any interested party, regardless of membership affiliation with IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments.

Interpretations: Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of all concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE Standards Board
445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

Note: Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying all patents for which a license may be required by an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

Authorization to photocopy portions of any individual standard for internal or personal use is granted by the Institute of Electrical and Electronics Engineers, Inc., provided that the appropriate fee is paid to Copyright Clearance Center. To arrange for payment of licensing fee, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; (508) 750-8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Introduction

(This introduction is not part of IEEE Std C62.37-1996, IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices.)

This test specification has been developed to enable the unified definition, test, and evaluation of thyristor type surge protective device parameters. A thyristor surge protective device limits overvoltages by switching on and providing a low impedance path to divert the current resulting from the overvoltage. Fixed voltage thyristor surge protective devices have their limiting voltage determined by the manufacturing process. Gated thyristor surge protective devices may have their limiting voltage determined by the reference potential applied to the gate. By connecting the gate in series with the circuit conductors, overcurrent conditions can also initiate device switch on and current diversion.

Thyristor devices have been used since the early 70s to protect telecommunications equipment against induced and conducted overvoltages caused by lightning and ac systems. These devices were specially engineered to provide the required protection function. The device main features were an extended breakdown region and an abnormally high value of holding current. As a result, many of the conventional thyristor terms and test methods were inadequate for these thyristor surge protective devices. Being a new device variant, many existing surge protective device manufacturers and users applied terms and tests used for gas-discharge tubes or avalanche junction semiconductor surge protective devices. Compared to these established devices, the thyristor surge protective device has different circuit sensitivities and this resulted in poor parameter correlation between users and suppliers.

There was a need for a comprehensive thyristor surge protective device test standard that defined terms, detailed appropriate test circuits, and measurement conditions. The Low-Voltage Solid-State Surge Protective Devices Working Group 3.6.2 of the IEEE Surge Protection Devices Committee undertook the task of preparing such a standard. The Working Group was formed from experts and interested parties drawn from producers, users, service providers, standards authorities, equipment manufacturers, test equipment manufacturers, and laboratories.

The Accredited Standards Committee on Surge Arresters, C62, at the time of ballot, had the following members:

Joseph L. Koepfinger, Chair

John A. Gauthier, Secretary

Organization Represented

Name of Representative

Association of American Railroads Wayne Etter

Bonneville Power Administration G. E. Lee

Canadian Standards Association D. M. Smith

Electric Light and Power..... J. W. Wilson

R. A. Jones

W. A. Maguire

G. N. Miller (*Alt.*)

T. A. Wolfe

Institute of Electrical and Electronics Engineers J. L. Koepfinger

J. J. Burke

G. L. Gaibrois

W. H. Kapp

Richard Odenberg

Keith Stump

Edgar Taylor (*Alt.*)

Members-at-Large..... J. Osterhout

B. Pensar

Steven G. Whisenant

National Electrical Manufacturers Association Dennis W. Lenk

Larry Bock (*Alt.*)

Andi Haa

Paul Jeffries

Hans Steinhoff

Jonathan J. Woodworth

Dennis W. Lenk

National Institute for Science and Technology F. D. Martzloff

Rural Electrification Administration(vacant)

Underwriters Laboratories George Mauro

Individuals..... Joseph Osterhout

B. Pensar

Steven G. Whisenant

At the time this standard was completed, the Low-Voltage Solid-State Surge Protective Devices Working Group 3.6.2 had the following membership:

Richard Odenberg, Chair

Michael J. Maytum, Secretary

John Brittain

Nisar Chaurdhry

Curtis A. Domsch

Ernie Gallo

Jim Harrison

David W. Hutchins

Wilhelm Kapp

Benny H. Lee

William J. Shannon

John A. Siemon

Donald B. Turner

Dee Unterweger

Jonathan Woodworth

Don Worden

Other individuals who have contributed review and comments are:

Rickard Bentinger
Stan Bonnesen
Chrysanthos Chrysanthou
Barry Epstein

C.A. Francis, II
Robert Fried
Allan F. Holland
Joe L. Koepfinger

Ed H. Marrow, Jr.
Albert A. Martin
Kurt A. Meindorfer
George Templeton

The following persons were on the balloting committee:

Chrys Chrysanthou
David W. Hutchins
David W. Jackson
Wilhelm Kapp

Joseph L. Koepfinger
Francois D. Martzloff
Richard Odenberg
Joseph C. Osterhout

Edgar R. Taylor
Arnold Vitols
J. W. Wilson
Donald M. Worden

When the IEEE Standards Board approved this standard on 23 October 1996, it had the following membership:

Donald C. Loughry, *Chair*

Richard J. Holleman, *Vice Chair*

Andrew G. Salem, *Secretary*

Gilles A. Baril
Clyde R. Camp
Joseph A. Cannatelli
Stephen L. Diamond
Harold E. Epstein
Donald C. Fleckenstein
Jay Forster*
Donald N. Heirman
Ben C. Johnson

E. G. "Al" Kiener
Joseph L. Koepfinger*
Stephen R. Lambert
Lawrence V. McCall
L. Bruce McClung
Marco W. Migliaro
Mary Lou Padgett
John W. Pope

Jose R. Ramos
Arthur K. Reilly
Ronald H. Reimer
Gary S. Robinson
Ingo Rüschi
John S. Ryan
Chee Kiow Tan
Leonard L. Tripp
Howard L. Wolfman

*Member Emeritus

Also included are the following nonvoting IEEE Standards Board liaisons:

Satish K. Aggarwal
Alan H. Cookson
Chester C. Taylor

Rochelle L. Stern
IEEE Standards Project Editor

Contents

1. Overview.....	1
1.1 Scope.....	1
1.2 Tests	1
1.3 Applicability and device function.....	1
2. Definitions of rated and other parameters.....	2
2.1 Rated parameter values	2
2.2 Definitions.....	2
2.3 Additional definitions	3
2.4 Temperature dependence of parameters	4
2.5 Gated thyristor surge protection device (SPD)	5
3. Service condition	10
3.1 Normal service conditions	10
3.2 Unusual service conditions	11
4. Standard design test procedure	11
4.1 Standard design test criteria	11
4.2 Statistical analysis.....	12
4.3 Thyristor surge protection device (SPD) test conditions	12
4.4 Rating test procedures.....	13
4.5 Characteristic test procedures	18
5. Failure modes.....	43
5.1 Degradation failure mode	43
5.2 Catastrophic failure mode.....	43
5.3 “Fail-safe” operation.....	44
Annex A (informative) Thyristor terms.....	45
A.1 Definitions.....	45
A.2 General terms	48
Annex B (informative) Bibliography.....	50

IEEE Standard Test Specification for Thyristor Diode Surge Protective Devices

1. Overview

1.1 Scope

This standard applies to two or three terminal, four or five layer, thyristor surge protection devices (SPDs) for application on systems with voltages equal to or less than 1000 V rms or 1200 V dc. These protective devices are designed to limit voltage surges on communication circuits and on power circuits operating from direct current (dc) to 420 Hz. The thyristor SPD can be manufactured with unidirectional or bidirectional, symmetrical, or asymmetrical V-I characteristics. This standard contains definitions, service conditions, and a series of test criteria for determining the characteristics of a thyristor SPD. If the characteristics differ with the direction of conduction, each polarity shall be separately specified.

1.2 Tests

The tests in this standard are intended as design tests as defined in [B3]¹ and provide a means of comparison among various thyristor SPDs.

NOTE—Three terminal devices may consist of multiple thyristor elements, or thyristor and diode elements, in one package; or the third may connect to the gate of a thyristor.

1.3 Applicability and device function

Thyristor SPDs are designed to conduct the surge currents necessary to provide overvoltage protection in electrical circuits. The purpose of this document is to provide definitions and test methods for thyristor SPD that are used for the protection of telecommunications systems. Overvoltage threats originate from lightning and ac power lines. These threats appear in the system through induction or direct contact. The waveforms that are used in the tests are chosen to allow confirmation of manufacturer's data.

¹The numbers in brackets correspond to those publications listed in the bibliography, Annex B.

Other types of thyristors may exhibit similar characteristics. If they are used as thyristor SPDs, their surge suppression capabilities may be characterized according to this specification.

The thyristor SPDs exhibit a relatively high impedance in the off-state condition at normal system operating voltages before and after the surge. During the surge of sufficient voltage and current, the device will switch to a low-impedance (on-state) condition. After the surge has passed, the device is expected to recover to a high-impedance (off-state) condition. Consideration should be given to service conditions, temperatures, and device mounting when applying these parameters as variations may occur.

2. Definitions of rated and other parameters

2.1 Rated parameter values

For the purpose of this standard, the values of rated parameters are established by the manufacturer, according to statistical acceptance criteria as indicated in 4.2.

2.2 Definitions

The following apply specifically to thyristor SPDs and do not necessarily cover other devices. If the voltam-pere characteristics are asymmetrical, then the parameters shall be defined for each polarity.

The relation between some common terms on some typical device V-I graphs are illustrated in Figures 1–7. The characteristics of devices in the breakdown region can be complex and difficult to measure. All the points shown on the graphs may not be apparent on the actual device characteristic, and there may be additional inflection points not shown. Conceptually, all of the points will exist for every device, although points such as switching (V_s , I_s) and breakover $V_{(BO)}$, $I_{(BO)}$ may be nearly coincidental. Device specifications should only describe the relevant characteristics. For the method of defining impulse waveforms, see Figure 7 of [B2]. The minimum data that a manufacturer shall supply are those parameters listed in 2.2.1 through 2.2.13.

2.2.1 breakover current ($I_{(BO)}$): The instantaneous current flowing at the breakover voltage. (See 4.5.4 and Figures 1–7.)

2.2.2 breakover voltage ($V_{(BO)}$): The maximum voltage across the device in or at the breakdown region measured under specified voltage rate of rise and current rate of rise. (See 4.5.4 and Figures 1–7.)

2.2.3 holding current (I_H): The minimum current required to maintain the device in the on-state. (See 4.5.6 and Figures 1–7.)

2.2.4 non-repetitive peak on-state current (I_{TSM}): Rated maximum (peak) value of ac power frequency on-state surge current of specified wave shape and frequency which may be applied for a specified time or number of ac cycles. (See 4.4.3 and Figures 1–7.)

2.2.5 non-repetitive peak pulse current (I_{PPS}): Rated maximum value of peak impulse pulse current of specified amplitude and wave shape that may be applied. (See 4.4.4 and Figures 1–7.)

2.2.6 off-state capacitance (C_O): The capacitance in the off-state measured at specified frequency, f , amplitude, V_a , and dc bias, V_D . (See 4.5.7.)

2.2.7 off-state current (I_D): The dc value of current that results from the application of the off-state voltage. (See 4.5.1 and Figures 1–7.)

2.2.8 off-state voltage (V_D): The dc voltage when the device is in the off-state. (See 4.5.1 and Figures 1–7.)

2.2.9 on-state current (I_T): The current through the device in the on-state condition. (See 4.5.5 and Figures 1–7.)

2.2.10 on-state voltage (V_T): The voltage across the device in the on-state condition at a specified current. (See 4.5.5 and Figures 1–7.)

2.2.11 repetitive peak off-state current (I_{DRM}): The maximum (peak) value of off-state current that results from the application of the repetitive peak off-state voltage. (See 4.5.2 and Figures 1–6.)

2.2.12 repetitive peak off-state voltage (V_{DRM}): Rated maximum (peak) continuous voltage that may be applied in the off-state conditions including all dc and repetitive alternating voltage components. (See 4.4.1 and Figures 1–6.)

2.2.13 repetitive peak on-state current (I_{TRM}): Rated maximum (peak) value of ac power frequency on-state current of specified wave shape and frequency which may be applied continuously. (See 4.4.2 and Figures 1–7.)

2.3 Additional definitions

For certain applications some of the following terms may be necessary or useful. Listed also are those parameters specific to certain thyristor SPD technologies.

2.3.1 breakdown current (I_{BR}): The current through the device in the breakdown region. (See 4.5.8 and Figures 1–3.)

2.3.2 breakdown voltage (V_{BR}): The voltage across the device in the breakdown region (prior to the switching point) at a specified breakdown current, I_{BR} . (See 4.5.8 and Figures 1–3.)

2.3.3 critical rate of rise of off-state voltage (dv/dt): The maximum rate of rise of voltage (below V_{DRM}) that will not cause switching from the off-state to the on-state. (See 4.5.12.)

2.3.4 critical rate of rise of on-state current (di/dt): Rated value of the rate of rise of current which the device can withstand without damage. (See 4.4.8.)

2.3.5 forward current (I_F): The current through the device in the forward conducting state. (See 4.5.10 and Figures 3 and 6.)

2.3.6 forward voltage (V_F): The voltage across the device in the forward conducting state at a specified current I_F . (See 4.5.10 and Figures 3 and 6.)

2.3.7 impulse reset time ($t_{(Reset)}$): The time taken for a device to switch back into the off-state, in the presence of a specified value of dc short-circuit current, after being switched into the on state by a specified impulse. (See 4.5.13.)

2.3.8 insulation resistance: The equivalent insulation resistance of the device, computed by

$$\frac{V_D}{I_D} \text{ (See 4.5.1.)}$$

2.3.9 lifetime rated pulse currents: Rated values of the peak impulse current, I_{PP} , as a function of the number of pulses and wave shape, which may be applied over the device rated lifetime. (See 4.4.3 and 4.4.4.)

2.3.10 non-repetitive peak forward current (I_{FSM}): Rated maximum (peak) value of ac power frequency forward surge current of specified wave shape and frequency which may be applied for a specified time or number of ac cycles. (See 4.4.6 and Figures 3 and 6.)

2.3.11 peak pulse impulse current (I_{PPM}): Rated maximum value of peak impulse pulse current (I_{PP}) applied for 10 pulses with $10 \times 1000 \mu s$ waveform and maximum duty factor of 0.01% without causing failure. Refer to [B6]. (See 4.4.4.)

2.3.12 peak forward recovery voltage (V_{FRM}): The maximum value of forward conduction voltage across the device upon the application of a specified voltage rate of rise and current rate of rise following a zero or specified reverse-voltage condition. (See 4.5.11.)

2.3.13 repetitive peak forward current (I_{FRM}): Rated maximum (peak) value of ac power frequency forward current of specified wave shape and frequency which may be applied continuously. (See 4.4.7 and Figures 3 and 6.)

2.3.14 repetitive peak reverse current (I_{RRM}): The maximum (peak) value of reverse current that results from the application of the repetitive peak reverse voltage, V_{RRM} . (See 4.5.3 and Figures 1 and 4.)

2.3.15 repetitive peak reverse voltage (V_{RRM}): Rated maximum (peak) continuous voltage that may be applied in the reverse blocking direction including all dc and repetitive alternating voltage components. (See 4.4.5 and Figures 1 and 4.)

2.3.16 switching current (I_S): The instantaneous current flowing through the device at the switching voltage, V_S . (See 4.5.9 and Figures 1–7.)

2.3.17 switching resistance (R_S): The equivalent slope resistance of the breakdown region, R_S , computed by

$$\frac{(V_{(BO)} - V_S)}{(I_S - I_{(BO)})}$$

(See 4.5.9, 4.5.4, and Figures 4–6.)

2.3.18 switching voltage (V_S): The instantaneous voltage across the device at the final point in the breakdown region prior to switching into the on-state. (See 4.5.9 and Figures 1–7.)

2.4 Temperature dependence of parameters

2.4.1 maximum junction temperature (T_{JM}): The maximum value of permissible junction temperature, due to self heating, which a thyristor SPD can withstand without degradation. (See 4.5.17–4.5.18.)

2.4.2 temperature coefficient of breakdown voltage ($\alpha_{V(BR)}$; $(dV_{(BR)}/dT_J)$): The ratio of the change in breakdown voltage, $V_{(BR)}$, to changes in temperature. Expressed as either millivolts per degree Celsius (mV/°C), or percent per degree Celsius (%/°C) with reference to the 25 °C value of breakdown voltage (mV/°C or %/°C). (See 4.5.14.)

2.4.3 temperature derating: Derating with temperature above a specified base temperature, expressed as a percentage, such as may be applied to peak pulse current (See 4.5.16.)

2.4.4 thermal resistance ($R_{\theta JL}$; $R_{\theta JC}$; $R_{\theta JA}$): The effective temperature rise per unit power dissipation of a designated junction, above the temperature of a stated external reference point (lead, case, or ambient) under conditions of thermal equilibrium. (See 4.5.17.)

2.4.5 transient thermal impedance ($Z_{\theta JL(t)}$; $Z_{\theta JC(t)}$; $Z_{\theta JA(t)}$): The change in the difference between the virtual junction temperature and the temperature of a specified reference point or region (lead, case, or ambient) at the end of a time interval divided by the step function change in power dissipation at the beginning of the same time interval that causes the change of temperature-difference. (See 4.5.18.)

NOTE— It is the thermal impedance of the junction under conditions of change and is generally given in the form of a curve as a function of the duration of an applied pulse.

2.4.6 variation of holding current with temperature: The change in holding current, I_H , with changes in temperature. It is shown as a graph. (See 4.5.15.)

2.4.7 virtual junction temperature (T_J): A theoretical temperature representing the temperature of the junction(s) calculated on the basis of a simplified model of the thermal and electrical behavior of the device. (See 4.5.17–4.5.18.)

2.5 Gated thyristor surge protection device (SPD)

These devices have a gate (G , g) terminal that controls the switching region characteristics and the main terminals provide the SPD function. Two gate types are possible, as this additional terminal may be connected to either an intermediate p or n layer of the thyristor. The first is a p-gate device, which has the gate biased negatively with respect to the anode. The p-gate device provides negative transient voltage protection with respect to the anode. The second is an n-gate device, which has the gate biased positively with respect to the cathode. The n-gate device provides positive transient voltage protection with respect to the cathode.

The gated thyristor SPD has many forms. Options are single or dual switching quadrant, n-gate and/or p-gate, forward or reverse conducting or blocking quadrants. The following definitions give the terms and parameters in general form with specific devices detailed, including the symbol and references in parentheses.

2.5.1 gate reverse current, adjacent terminal open (I_{GAO} ; I_{GKO}): The current through the gate terminal when a specified gate bias voltage, V_G , is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is open circuited. (See 4.5.20, common-gate configuration.)

2.5.2 gate reverse current, main terminals short-circuited (I_{GAS} ; I_{GKS}): The current through the gate terminal when a specified gate bias voltage, V_G , is applied and the cathode terminal for a p-gate device or anode terminal for an n-gate device is short circuited to the third terminal. (See 4.5.2.)

2.5.3 gate reverse current, on-state (I_{GAT} ; I_{GKT}): The current through the gate terminal when a specified gate bias voltage, V_G , is applied and a specified on-state current, I_T , is flowing. (See 4.5.22 and Figure 7b).

2.5.4 gate reverse current, forward conducting state (I_{GAF} ; I_{GKF}): The current through the gate terminal when a specified gate bias voltage, V_G , is applied and a specified forward conduction current, I_F , is flowing. (See 4.5.23.)

2.5.5 gate switching charge (Q_{GS}): The charge through the gate terminal, under impulse conditions, during the transition from the off-state to the switching point, when a specified gate bias voltage, V_G , is applied. (See 4.5.24.)

2.5.6 gate-to-adjacent terminal breakover voltage ($V_{GK(BO)}$; $V_{GA(BO)}$): The gate to cathode voltage for a p-type device or gate to anode voltage for an n-gate device at the breakover point. This is equivalent to the voltage difference between the breakover voltage, $V_{(BO)}$, and the specified gate voltage, V_G . (See 4.5.26.)

2.5.7 gate-to-adjacent terminal peak off-state voltage (V_{GDM}): The maximum gate to cathode voltage for a p-gate device or gate to anode voltage for an n-gate device that may be applied such that a specified off-state current, I_D , at a rated off-state voltage, V_D , is not exceeded. (See 4.5.19.)

2.5.8 peak off-state gate current (I_{GDM}): The maximum gate current that results from the application of the peak off-state gate voltage, V_{GDM} . (See 4.5.19.)

2.5.9 peak gate switching current (I_{GSM}): The maximum value of current through the gate terminal during the transition from the off-state to the switching point, when a specified gate bias voltage, V_G , is applied. (See 4.5.25 and Figure 7b).

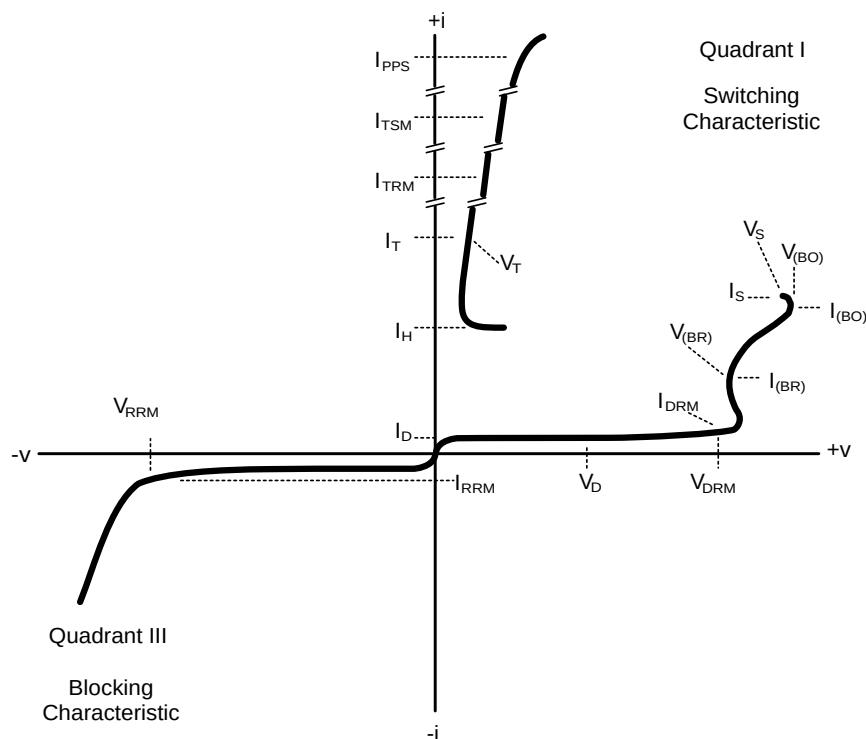


Figure 1—Graph illustrating symbols of terms for a reverse blocking positive breakdown slope thyristor SPD

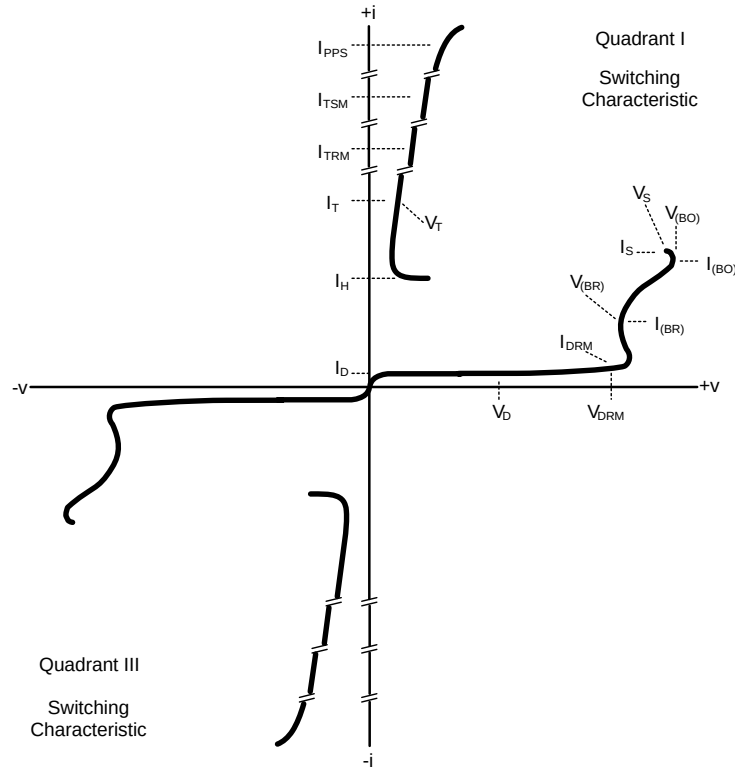


Figure 2—Graph illustrating symbols of terms for a bidirectional positive breakdown slope thyristor SPD

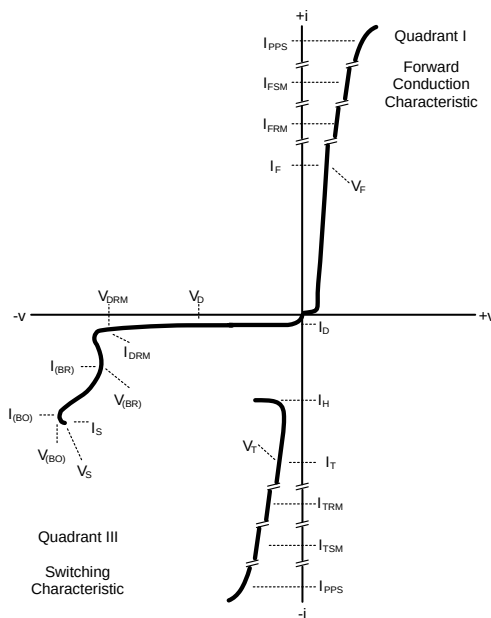


Figure 3—Graph illustrating symbols of terms for a forward conducting positive breakdown slope thyristor SPD

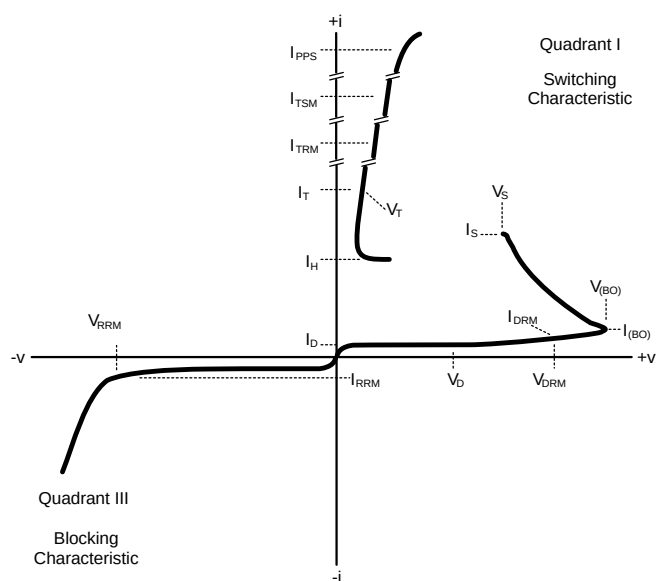


Figure 4—Graph illustrating symbols of terms for a reverse blocking negative breakdown slope thyristor SPD

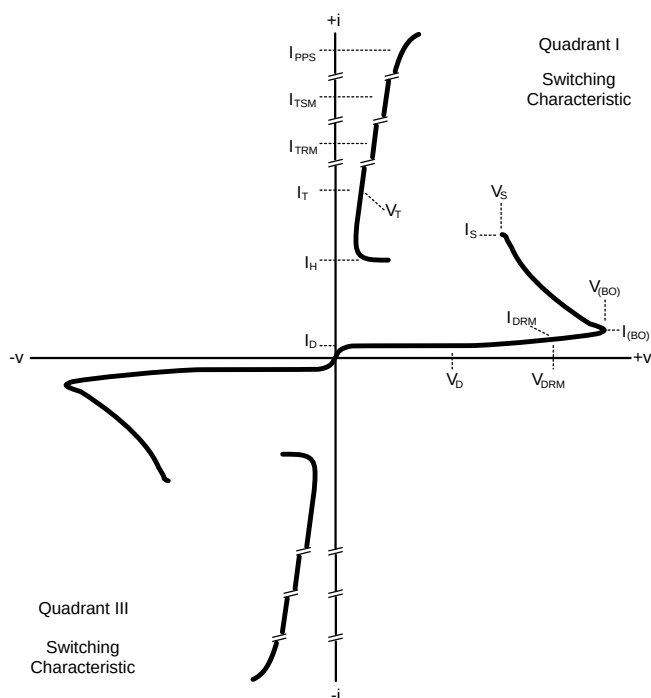


Figure 5—Graph illustrating symbols of terms for a bidirectional negative breakdown slope thyristor SPD

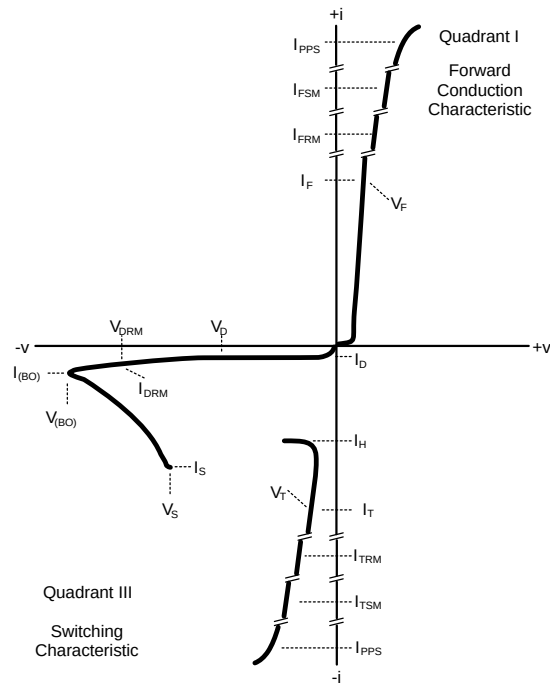


Figure 6—Graph illustrating symbols of terms for a forward conducting negative breakdown slope thyristor SPD

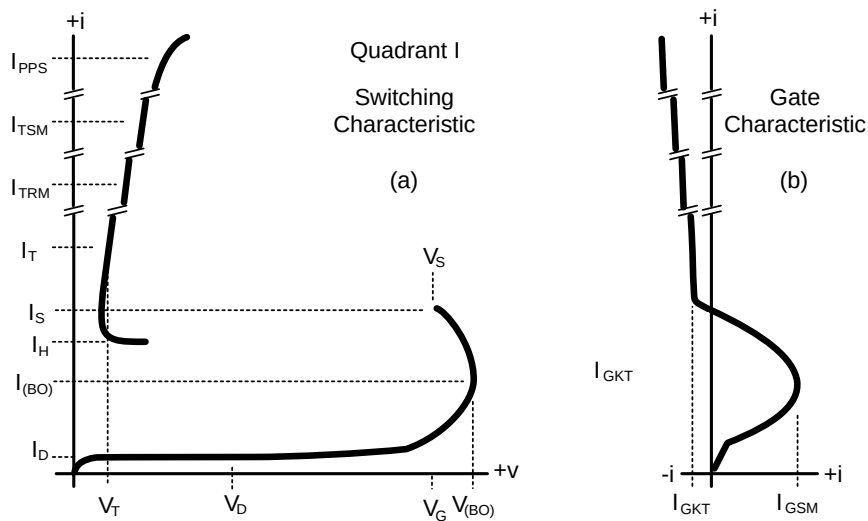


Figure 7—Graph illustrating symbols of terms for a gated thyristor SPD

3. Service condition

3.1 Normal service conditions

Thyristor SPDs conforming to this standard shall be rated for climatic ranges of temperature, humidity, and pressure. In the absence of special requirements, it is recommended that the listed values should be used. Some service conditions relate to the mandatory parameters of 2.2. This relationship is shown in parenthesis. Any other service condition should be specified by the manufacturer or requested by the user, as appropriate.

3.1.1 Climatic conditions

- a) Operating temperature range
 - 1) normal: 0 °C to 70 °C
 - 2) extended: –40 °C to 85 °C
- b) Storage temperature range
 - 1) normal: –40 °C to 150 °C
 - 2) extended: –65 °C to 150 °C
- c) Humidity range
 - 1) normal: 20% to 75%
 - 2) extended: 10% to 100%
- d) Air pressure range
 - 1) normal: 86 kPa to 106 kPa
 - 2) extended: 70 kPa to 106 kPa

3.1.2 Other environmental conditions

- a) Mechanical shock
- b) Mechanical vibration

3.1.3 Physical properties

- a) Solvent resistance
- b) Solderability
- c) Flammability
- d) Package rupture during overload
- e) Electrical connection to metal case

3.1.4 System conditions

- a) Nominal systems frequencies (off-state capacitance)
- b) Maximum continuous system voltage and current (repetitive peak off-state voltage, off-state current and holding current)
- c) Peak impulse currents (non-repetitive peak pulse current)
- d) Peak power frequency ac currents (non-repetitive peak on-state current)
- e) Surge repetition rate

3.1.5 Surge rating of the thyristor SPD under system conditions

- a) Rated non-repetitive peak current
- b) Rated non-repetitive peak pulse current temperature derating
- c) Lifetime rated pulse currents

3.2 Unusual service conditions

The following service conditions may require special consideration in the design or application of thyristor diodes and should be called to the attention of the manufacturer.

3.2.1 Environmental conditions

- a) Climatic conditions
 - 1) Temperature, humidity and pressure values exceeding normal service conditions
 - 2) Precipitation (rain, snow and hail)
 - 3) Other water sources (dipping, splashing, steam, submersion, condensation, ice, and frost formation)
- b) Biological conditions
 - 1) Flora
 - 2) Fauna
- c) Chemically active substances
 - 1) Damaging fumes or vapors
 - 2) Salt spray
 - 3) Flammable or explosive atmosphere
- d) Mechanically or electrically active substances
 - 1) Dust
 - 2) Soot
- e) Contaminating fluids
- f) Mechanical conditions
 - 1) Vibration (stationary or shock)
 - 2) Drop (stationary or shock)
- g) Impact
- h) Static load
- i) ESD

3.2.2 Physical conditions

Limitation on weight or dimension, including clearance to nearby conducting objects.

3.2.3 System conditions

- a) Electrical system conditions. Sustained overvoltages, temporary overvoltage (TOV), current conductive rates, or frequency operating conditions whereby the ratings of the devices are exceeded (see Clause 5, Failure modes).
- b) System impulse currents not within the rating of the device (see Clause 5, Failure modes).
- c) Exposure to direct lightning strike (see Clause 5, Failure modes).
- d) Electromagnetic field effects (see Clause 5, Failure modes).
- e) Unusual ground potential situations (see Clause 5, Failure modes).
- f) Any other unusual condition known to the user.

4. Standard design test procedure

4.1 Standard design test criteria

The design test described in 4.4.1 through 4.5.26 provide standardized methods for making single observations of a specified property of a thyristor SPD. These properties may vary from device to device making it necessary to provide statistical descriptions of the property in order to compare products.