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Design Guide for High-Speed Controlled Impedance Circuit Boards

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Developed by the IPC Controlled Impedance Task Group (D-21c) of the
High Speed/High Frequency Committee (D-20) of IPC

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Design Guide for High-Speed Controlled Impedance Circuit Boards

1 SCOPE

This guide is intended to be used by circuit designers, packaging engineers, printed board fabricators, and procurement personnel so that all may have a common understanding of each other's area.

The goal in packaging is to transfer a signal from one device to one or more other devices, through a conductor. High-speed designs are defined as designs in which the interconnecting properties affect circuit performance and require unique consideration.

The term "high-speed" as applied to logic or digital designs needs clarification in its usage. The three most common interpretations of high-speed are as follows. (1) High-speed as a reference to the rate of change of signal amplitude with time (frequently called the edge rate of a pulse) constitutes the most important usage. The edge rate puts the greatest performance demand on interconnecting structures. (2) High-speed as a reference to the data transmission rate (bits or bytes per second) is often used to describe the "speed" of a system. However, high data rates can be achieved with parallel bus architectures that do not necessarily require improved performance of an interconnecting structure. (3) High-speed as a reference to the speed (distance per unit time) of a signal propagating between devices has the smallest usage and, in many cases, is not important to the application.

Controlled impedance is the maintenance of some specified tolerance in the characteristic impedance of an interconnect line (transmission line) that is used to connect different devices on a circuit. Controlled impedance is often a design consideration for high-speed digital or high-frequency analog circuits. However, the reverse is not true, that is, high-speed digital or high-frequency analog circuit designs may not need to consider controlled impedance. The purpose of this document is to help the designer understand when controlled impedance should be considered in his/her circuit design and to describe concepts important to controlled impedance design.

2 APPLICABLE DOCUMENTS

The following standards contain provisions which, through reference in this text, constitute provisions of this document. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to

investigate the possibility of applying the most recent editions of the standards listed below.

2.1 IPC¹

IPC T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-TM-650 Test Methods Manual²

2.5.5.7 11/92 Characteristic Impedance of Lines on Printed Boards by TDR

IPC-2220 Design Standard Series

IPC-2251 Design Guidelines for the Packaging of High Speed Electronic Circuits

IPC-2252 Design and Manufacture Guide for RF/Microwave Circuit Boards

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4103 Specification for Base Materials for High Speed/High Frequency Applications

References, if presented at the end of a section, provide a more comprehensive treatment of the subject of that section.

3 ENGINEERING DESIGN OVERVIEW

Packaging of electronic equipment has traditionally been an area for mechanical considerations. However, today's packaging designs are becoming more complex because of the faster switching speeds and higher input/output densities available from today's electronic technologies. To take maximum advantage of device density and speed, designers must pay much more attention to problems of electromagnetic wave propagation phenomena associated with transmission of high-speed pulsed/switched signals within the system. New design disciplines and design strategies are needed. Controlled impedance circuit boards are a part of this strategy.

Interconnection and the packaging of electronic components primarily has been the domain of mechanical designers who were concerned with such factors as weight, volume, power, and form factor, and when interconnections

1. www.ipc.org

2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.htm)

were specified in to/from wire listing or net lists. Electrical signals were routed with only a few concerns, namely, that electrical continuity was maintained between points, that conductors had sufficient copper for the required current carrying capacity, and that sufficient clearance was maintained between conductors to prevent voltage breakdown in the insulator. Aside from providing a good electrical path, the electrical performance of the signal was not a major concern.

Advances in digital integrated circuits have introduced new devices that have extremely fast switching times and that are housed in high density microelectronic packages. To optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same time, provides superior electrical performance.

With recent advances in semiconductor processing technology, the output impedance of Complimentary Metal-Oxide Semiconductor (CMOS) devices are approaching that of Emitter-Coupled Logic (ECL) devices ($5\ \Omega$ to $6\ \Omega$) and can switch from one logic level to the other, a voltage swing of 5 V, in a $50\ \Omega$ environment, in as little as 1 ns. These fast level transitions demand all of the concern normally given the GaAs and ECL logic families.

3.1 Device Selection Device technology options include Transistor-Transistor Logic (TTL), Schottky TTL, CMOS, ECL and GaAs. Each technology has its own set of power requirements, operating temperature ranges, input-output (I/O) densities, input impedances, output impedances, signal threshold levels, noise sensitivities, response times and output pulse rise/fall times. Many circuit designs will have mixed technology where both Surface Mount Technology (SMT) and through-hole packaging are used to connect TTL, CMOS and ECL logic devices on a given circuit. These circuits may consist of interconnect lines with different widths (and, therefore, different characteristic impedance values), one width for each logic family on the circuit, or they may consist of a single width interconnect line that is designed to be within the performance margins of all the logic families on the circuit.

Chips can be individually mounted on a large board or assembled into small boards or multichip modules that are then mounted onto large boards. Large systems may require several large board assemblies with additional levels of interconnect between the boards. Noise, timing, and signal degradation will accompany transitions from one packaging level to the next because of mismatches in circuit impedance.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated-through holes in the board, as in dual in-line packages, to a series of lands for surface mount devices. Requirements for component packaging are dependent on

many factors including space, economics, electrical performance and reliability, as well as the predominant packaging style of the assembly. The components must be provided in a style that is compatible with the assembly processes used to manufacture the printed board assembly.

The component package must be considered when designing for high speed. In passive components, the primary factor that affects signal quality will be the lead length because leads provide additional inductance and capacitance that affect signal propagation and switching transients. To minimize these effects, the leads should be as short as possible. Surface mount devices can provide almost leadless packages which can be mounted directly to the interconnecting substrate.

Note: Manufacturer component data sheets often do not provide information on the parasitic values of package leads. These parameters are important to designers where high-speed signal propagation and noise are issues.

Active devices, components such as integrated circuits, are often offered in several package designs. In the past, Dual In-Line Packages (DIPs), using either plastic or ceramic substrates, have been the dominant package style. These packages typically are the largest packages and provide the poorest high speed operating environment due to their lead configuration. The next best package style for high-speed performance and high density circuitry is the surface mount package. Surface mount packages are the dominate package style in use today and are offered in a variety of package configurations/styles such as (Small Outline Integrated Circuits) SOICs, (Plastic Leaded Chip Carriers) PLCCs, Plastic Quad Flat Packages (PQFPs) or Thin Small Outline Packages (TSOPs). These packages will typically have lower lead capacitance and inductance than DIPs.

To obtain the optimum performance from the device, the die can be directly mounted to the substrate using either the Chip-on-Board (COB), Flip Chip, Chip Scale Package (CSP), Tape Automated Bonding (TAB), Ball Grid Array (BGA), Pin Grid Array (PGA) or similar approach. These mounting strategies offer an optimum approach since they minimize lead capacitance and inductance and improve package reliability and high-volume production capability. However, as with all mounting strategies, the quality and reliability of the interconnection for the application must be determined.

3.2 Interconnection

3.2.1 Connectors Interconnections may cause troubles in high speed application because of the impedance discontinuities that exist between the connector and the board and/or between the connector and the cable. At high frequencies, even changes in the geometries within a connector may cause discontinuities. If a continuous conductor

impedance environment is not provided, the propagating signal will reflect at the impedance discontinuities and this will result in degradation of signal integrity.

Many board-to-board connector systems are not designed for use in high-speed applications, and will degrade signal integrity if used in a high-speed board. Furthermore, the impedance of board-to-board connections are often not matched to the characteristic impedance of the signal conductors on the board themselves, and this causes further signal degradation. However, for high-speed circuits and systems, which typically use a 50 Ω impedance environment, high-bandwidth 50 Ω board-to-board connectors are readily available.

There are two primary approaches to reduce the impedance discontinuity caused by interconnect systems. The first approach is to provide a connector style such that the pin-outs can be arranged to provide a good signal path. For nondifferential signals, the electrical reference for the active signal line is the closest reference plane connection, which is either a voltage or ground plane. Nondifferential signal conductors rely on controlled geometries and nearby reference planes for impedance control. Therefore, signal pin quality, reference pin quality and their location control the electrical performance of the connection. To optimize the electrical performance of the connection, reference pins must be added to reduce the problems associated with an insufficient number of reference pins, such as poor shielding, inadequate ground reference, and increased reactance. As a "rule of thumb," a 3:1 signal pin to reference (ground or voltage) pin ratio is sufficient.

The second approach to reduce the impedance discontinuity is to modify the connector to minimize the magnitude of the discontinuity between boards. This can be achieved by shortening the pin length or by adding a reference ground plane within the connector.

Board mounted coaxial connectors are frequently used when only a few signal lines are connected to a circuit board or where signal isolation and/or signal integrity is critical.

3.2.2 Cables Discrete coaxial connectors and cables are sometimes used because they can couple high speed, high frequency signals to a circuit board with little signal degradation. A coaxial cable controls signal propagation speed, reduces crosstalk, lowers noise pick-up, and provides an excellent impedance match, particularly at higher frequencies. Discrete coaxial cables have been used with discrete wire boards for unique, high-speed applications. An optical cable can also be used with discrete wired boards for high frequency signals and for better signal isolation. Unique and specialized boards may require coaxial cables for the ultimate EMI control. Another consideration is discrete wiring boards have a lower I/O density and a higher fabrication cost than conventional boards.

3.3 Printed Board and Printed Board Assemblies Component placement is a critical factor in the design of high-speed systems. The effects of unsuitable placement can be significant and include concerns in the following areas:

- a. *Crosstalk Management* Crosstalk between conductive lines and/or devices is affected by the location of one device (and its corresponding interconnects) relative to another.
- b. *Impedance Control* Whether or not an interconnect needs to be considered a transmission line will depend on, for one, the length of the interconnect between devices.
- c. *Power Distribution* Not all power planes are available across the entire board.
- d. *Time Delays Between Circuits*
- e. *Thermal Management*

3.3.1 Board Design The number of signal layers in multilayer boards will be influenced by the density of interconnections within the board as well as the effect of crosstalk or coupling between signal lines. Crosstalk control may require placing additional dielectric layers or metal planes between signal layers and/or increased spacing between conductors on a given signal layer. However, the increased spacing decreases interconnect density.

The use of diagonal routing in addition to orthogonal routing on the same wiring layers may allow greater circuit density per layer and also increase possible placement geometries. The increase in possible placement geometries may help to increase circuit density and lower crosstalk.

A close relationship exists between interconnect design and circuit performance in high-speed digital circuits. This interdependence previously was noticeable only in the very highest performance computers and was ignored in low speed signal applications. However, due to increasing logic speeds, this interdependence now imposes new design rules, restrictions and process controls on products as ordinary as personal computers.

To meet the performance requirements of high speed digital circuits, the design of today's multilayer printed board must accommodate the requirements for:

- a. Propagation delay.
- b. Transmission line reflectance.
- c. Signal loss.
- d. High density interconnections.
- e. Crosstalk.
- f. Controlled impedance.

To achieve the design requirements, the designer must start by controlling the characteristic impedance of the transmission lines, which, in turn, minimizes reflections from lines that are properly terminated.

Controlled impedance conductors on boards can be used for signal interconnections between devices. For a given transmission line design (microstrip, stripline, etc.), the characteristic impedance can be controlled by the dielectric thickness, conductor thickness, conductor width, and relative permittivity (dielectric constant) of the substrate. These design and material parameters also affect signal propagation. Choosing a dielectric with a lower relative permittivity, ϵ_r , (see 3.4.2) results in faster signal propagation, but requires increasing the conductor width to maintain a given characteristic impedance value. Solder masks and conformal coatings also affect the characteristic impedance of external (on the surface of the board) transmission lines, as well as the effective relative permittivity (see 3.4.2.2). The type, thickness, and cure process of the solder mask, as well as the conductor thickness and width, affect the characteristic impedance of the transmission line.

Signal paths should be managed such that the system timing requirements are met. If it is desired to minimize signal losses, shorter paths are typically preferred. Even if it were possible to make a circuit capable of switching with infinite speed, the interconnection material would limit the performance of the systems because of the frequency dependent characteristics of the materials in the interconnect (see 3.4.2.1).

Space constraints, the number and complexity of interconnections, power distribution, and cost of manufacture are some factors that should be considered when determining the number of layers in a circuit board. The thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric, conductor width/thickness and the overall circuit length will impact electrical performance. The width and thickness of the conductor and the number of layers have an effect on manufacturing costs. The manufacturing costs include direct material cost, cost of fabrication, reduced yield, etc. Consequently, design options may need to be considered to provide flexibility in selecting the materials, fabrication processes, etc. that reduce manufacturing cost without sacrificing performance. For example, the manufacturing cost of a printed board may be prohibitively expensive if a dielectric with unique electrical properties, ideal for the given application, (such as low ϵ_r or low $\tan\delta$ (see 3.4.4) for high-speed low-loss signal propagation) is used but may be within budget if another dielectric and a slight design modification are used.

3.4 Performance Requirements Electromagnetic wave propagation theory must be considered in evaluating the performance of high-speed interconnects and circuit substrates. High-speed is characterized by the fast rise time of an electrical pulse, such as those pulses used in digital circuits. As the rise time of the pulse decreases, the frequency bandwidth (see 3.4.5) of the pulse increases and the digital circuit board looks increasingly like a high speed analog circuit.

3.4.1 Power Distribution System Both AC and DC power must be distributed in a circuit. Losses will occur in this power distribution circuit and, therefore, it must be designed to minimize power loss (which may result in heating or electromagnetic interference) and/or accommodate losses so that devices receive the required power. Losses in the power distribution may be grouped into two major categories, conductive losses (AC and DC) and dielectric (AC) losses.

3.4.1.1 DC Power Distribution The DC power distribution system extends from the conductors starting at the output of the power supply and ending at the input of each device. For systems with many circuit boards and supplies, a simulation of the interaction of each component is desirable to verify and assist the design effort. The voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance. When necessary, model analysis is used to determine the voltage drop between each integrated circuit location.

3.4.1.2 AC Power Distribution High-speed switching devices require equally high-speed changes in the electrical current delivered to their power inputs. If several high-speed devices are switched simultaneously, the power distribution system is required to meet the current delivery demands for all the high-speed devices simultaneously while still maintaining its voltage. This requirement demands low inductance connections to the devices from the power supply and high supply capacitance for each voltage in the system. At very high speeds, the impedance of the power supply is too high to supply the switching currents. As a result, the switching currents must be supplied by capacitors close to the devices. For higher speed circuits, capacitors are too slow and the currents must be supplied by the capacitance associated with the power and ground planes (the interplane capacitance) of the board.

The AC power distribution system must provide a low impedance, low inductance path to current flow, especially for high-speed signals. Furthermore, the power system must provide the switching current to the devices without lowering the supply voltage below the required minimum device level. These requirements are achieved by charge stored in discrete capacitors located on the board and near devices and charge stored in the interplane capacitance.

The AC system can be divided into three elements based on their frequency bandwidth. The element with the lowest frequency bandwidth is that consisting of the bulk IC decoupling capacitors. The next element is that consisting of localized high-frequency decoupling capacitors, and the highest frequency element is the capacitance associated with the power-to-ground spacing.

Bulk decoupling capacitors have the lowest bandwidth and are recharged by the power supply. The current associated with this element is higher than the current associated with the other elements.

The next element consists of discrete capacitors connected to the leads of the devices on the board. These capacitors may be useful with signal bandwidths up to 200 MHz or so. When these local capacitors discharge their current into the device, they are quickly recharged from energy stored in slower discharging bulk capacitors, thereby making them ready for their next discharge. These localized capacitors affect the highest frequency components of the current. The reactive impedance associated with these capacitors and their connections to the device, the switching transient impedance, is the cause of ground and/or V_{CC} bounce (see 3.4.14.5).

Decoupling capacitors must provide sufficient current for the devices to operate, including the high peak currents required during device switching. When the stored energy on the board is insufficient to power all the devices on the board, capacitors are placed near the devices for localized energy storage. In this case, the capacitors, and not the power planes, provide the immediate power required by the device for operation. These capacitors are connected between the power and ground planes. Capacitors having a range of capacitance values should be used to ensure that the input impedance of the power system is low over a large frequency range. Since discrete capacitors have an inductance and a resistance associated with them, they will have a resonance at which their impedance is lowest. Therefore, to obtain a power system impedance that is low over a large frequency range requires that many different capacitance values be used. Furthermore, to minimize inductance, it is good practice to use several capacitors to obtain the required capacitance value instead of one large capacitor. Decoupling capacitors also reduce overall system noise (see 3.4.15.1).

The highest bandwidth element is provided by the ground-to-power plane capacitance. These planes also provide a low inductance path to the device, which is important for signal integrity and electromagnetic emissions issues. The spacing between the power and ground planes gives the designer another parameter to vary in the design of their circuit. For example, by reducing the spacing between the ground and power planes, the local capacitance can be increased and the impedance and inductance decreased.

3.4.2 Relative Permittivity (Dielectric Constant) The relative permittivity, ϵ_r , of a material is defined as the ratio of the permittivity of the material to the permittivity of free space, ϵ_0 , which has a value of 8.854×10^{-12} F/m. The permittivity of a material is a complex value given by:

$$\epsilon = \epsilon' + j\epsilon'' \quad [3-1]$$

where $j = \sqrt{-1}$ and $\epsilon = \epsilon_r \epsilon_0$. In this document we will use the real part of the permittivity to represent the permittivity.

Dielectric constant is the term in common use in industry even though the “dielectric constant” varies with several parameters such as material composition, frequency, substrate orientation, temperature, etc.

The relative permittivity (ϵ_r) of the dielectric of an interconnecting structure will affect electrical performance. The value of ϵ_r is used in the design of the interconnect to ensure that the interconnect meets the characteristic impedance, capacitance, and propagation time requirements of the system. 3.4.6.2 and 3.4.7 describe the effects of ϵ_r on characteristic impedance and signal propagation. Considerations for measuring the effective relative permittivity (see 3.4.2.1) are described in 3.4.3.

3.4.2.1 Factors Affecting Relative Permittivity Factors that influence the relative permittivity of a given material include material composition, frequency, temperature, and water absorption. In addition, if the material is a composite, that is, a reinforced laminate, the value of ϵ_r may vary enormously as the relative amount of the constituents varies, which also may change after curing. The effects of the type of glass reinforcement and percent resin content for FR4 materials can be observed from the curves shown in Figure 3-1.

The data shown in Figure 3-1 are representative of different types of FR4 and is only used to show trends. More accurate values of $\epsilon_{r,FR4}$ should be obtained from the material supplier. Although Figure 3-1 shows values of $\epsilon_{r,FR4}$ for various frequencies, material suppliers commonly provide a value of $\epsilon_{r,FR4}$ that was measured at 1 MHz using capacitance methods.

3.4.2.1.1 Frequency Effects All materials exhibit frequency dependent dielectric properties. Substrates that are compositionally anisotropic, such as glass-fabric-reinforced epoxies (such as FR-4), will more than likely be dielectrically anisotropic (depending on the materials of the composition). This anisotropic behavior is dependent on the orientation of the electric field vector of the propagating electromagnetic signal with respect to the substrate axes.

3.4.2.2 Effective Relative Permittivity The effective relative permittivity, $\epsilon_{r,eff}$, is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. The $\epsilon_{r,eff}$ is dependent on the permittivities of all the materials that affect the propagation of the pulse on a transmission line and on the geometry of the transmission line. The $\epsilon_{r,eff}$ may not be dielectrically isotropic, such as in some fiber-reinforced materials (such as FR4) and many crystalline materials. $\epsilon_{r,eff}$ may deviate from by ϵ_r 10% or more.

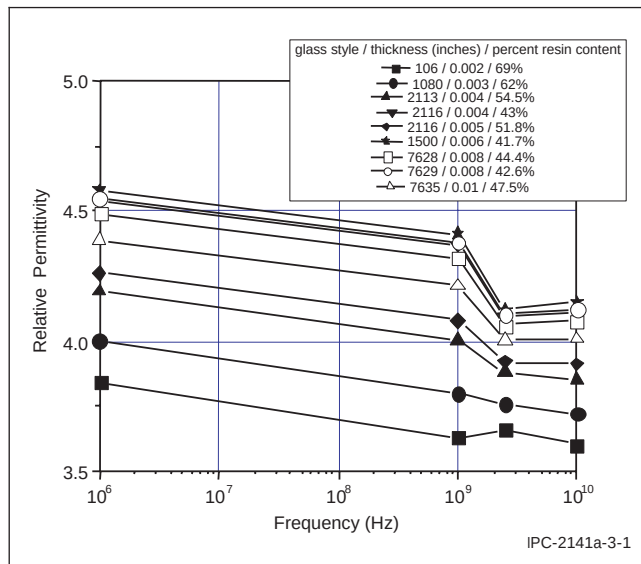


Figure 3-1 Relative permittivity of FR4 as a function of frequency for different glass reinforcement and percent resin content. The data used to generate these curves has been provided by Park/Nelco.

3.4.3 Measuring Effective Relative Permittivity As stated in 3.4.2.1, the value of ϵ_r is dependent on a variety of parameters, including material composition, temperature, humidity, and frequency. Consequently, the electrical measurements used to acquire ϵ_r and $\epsilon_{r,eff}$ should be performed under conditions that are similar to that of the final application.

An experimental value of $\epsilon_{r,eff}$ may be obtained using a Time Domain Reflectometry (TDR) technique (see Section 9) or by measuring the propagation delay (see 3.4.10.1) for a known length of transmission line and then calculating a value for $\epsilon_{r,eff}$.

Material suppliers typically quote values of ϵ_r at 1 MHz, determined using capacitance methods performed at 1 MHz. However, calculations of Z_0 of transmission lines fabricated on FR4 substrates will more closely agree with TDR measurements if the value of ϵ_r used in the calculations was obtained from measurements at frequencies greater than 1 GHz. This is because TDR bandwidths are typically greater than 1 GHz.

Frequency domain methods are also used to determine $\epsilon_{r,eff}$. In this case, the measurement frequencies should be selected such that the dielectric parameters obtained provide a precise prediction of the electrical characteristics of the finished printed board at its design frequencies. To extract ϵ_r from $\epsilon_{r,eff}$, models describing the electrical behavior of the transmission line as a function of geometry and materials must be used.

If $\epsilon_{r,eff}$ is not dielectrically isotropic, it may be necessary to measure the electrical characteristics of the material in two orthogonal directions that are parallel to the plane of the

board. These directions should be chosen to maximize the differences in the observed electrical characteristics of the material.

3.4.4 Loss tangent ($\tan\delta$, or dissipation factor) The loss tangent is the ratio of the imaginary part of ϵ , ϵ'' , to the real part of ϵ , ϵ' :

$$\tan\delta = \frac{\epsilon''}{\epsilon'} \quad [3-2]$$

The loss tangent describes the energy absorbed by the dielectric. Losses in the dielectric contribute to pulse attenuation (see 3.4.7.1) and degrade pulse rise times.

3.4.5 Bandwidth For a pulse, the bandwidth is the frequency at which the power spectrum has decreased to a given fraction of the magnitude of a reference frequency. Typically, the reference frequency is DC and the fraction is about 0.71 (or -3 dB). Since the performance characteristics of transmission lines in a printed board are often measured by time-domain reflectometry (TDR), it is necessary that the frequency bandwidth of the TDR system exceeds that of the signal propagating in the circuit. For example, the bandwidth of a TDR having a rise time of 100 ps is 3.5 GHz and should not be used to determine circuit properties for a 10 GHz application. (3.4.5.1 briefly describes frequency domain and time domain representations of a signal.) Some degradation of the rise time of the TDR pulse will occur in transmission through the test fixture and this reduces measurement bandwidth. To determine the bandwidth of the pulse, the following approximation is used:

$$BW = \frac{0.35}{t_r} \quad [3-3]$$

where t_r is the fastest of the pulse rise or fall times and is typically calculated as the interval between the instants the pulse crosses its 10% and 90% amplitude values. Signal rise times and bandwidths are dependent on device technology (see Table 3-1).

The data provided in Table 3-1 were obtained from data sheets and manuals published in 2001 and 2002. Because this information changes often, the manufacturers should be consulted for more accurate data. Table 3-1 provides a typical range of pulse rise times, bandwidths, and critical line lengths for the indicated logic family. However, rise time will be dependent on other parameters, such as technology (for example, Schottky, low-power Schottky, etc. for the TTL family), supply voltage, and load impedance.

3.4.5.1 Frequency and Time Domain Representations

Frequency domain representations of time signals are commonly used to show the frequencies contained in that signal. The frequency domain representations of a signal

Table 3-1 Typical Data for Some Logic Families (critical line length is described in 3.4.9)

Logic Family	Typical Rise/ Fall Time(ns)		Band- width (MHz)	Critical Electrical Length in FR-4 at Fastest Rise/Fall Time				Output Drive Current (mA)		Logic Input Threshold (V)		Typical Buffer Prop. Delay (ns)
				Microstrip		Stripline						
	Rise	Fall		inch	cm	inch	cm	I _{OL}	I _{OH}	V _{IL}	V _{IH}	
AGP	0.350	0.450	1000	0.63	1.60	0.50	1.27	20	-12	1.12	1.52	1.5
BiCMOS 74ABT	1.6	1.4	250	2.5	6.3	2.0	4.9	64	-32	1.1	1.9	3.6
BiCMOS 74BCT	0.700	0.700	500	1.24	3.15	0.98	2.49	64	-15	0.8	2.0	2.5
BICMOS 74LVT	2.7	2.8	130	4.80	12.2	3.8	9.8	64	-32	1.3	1.7	4.1
CMOS 74AC	1.7	1.5	233	2.7	6.8	2.1	5.3	24	-24	2.2	3.0	7.5
CMOS 74ACT	1.7	1.5	233	2.7	6.8	2.1	5.3	24	-24	0.4	2.1	10.0
CMOS 74ACQ	2.4	2.4	146	4.3	10.8	3.4	8.4	24	-24	2.3	2.9	9.5
CMOS 74ACTQ	2.5	2.4	146	4.3	10.8	3.4	8.4	24	-24	1.2	2.0	7.0
CMOS 74AHCT	2.4	2.4	146	4.3	10.8	3.4	8.4	24	-15	0.8	2.0	7.0
CMOS 74C	35.0	25.0	14	44.4	112.5	35	87.5	12	-14	0.7	3.5	70.0
CMOS 74FCT	1.5	1.2	292	2.1	5.4	1.7	4.2	64	-15	0.8	2.0	3.1
CMOS 74HC	3.6	4.1	97	6.4	16.2	5.0	12.6	6	-6	2.3	2.4	25.0
CMOS 74HCT	4.6	3.9	90	6.9	17.6	5.5	13.7	6	-6	1.3	1.4	25.0
CMOS 74LCX	2.9	2.4	146	4.3	10.8	3.4	8.4	24	-24	1.3	1.8	6.5
CMOS 74LV	3.0	3.0	116	5.3	13.5	4.2	10.5	8	-8	0.9	2.3	7.5
CMOS 74LVQ	3.5	3.2	109	5.7	14.4	4.5	11.2	12	-12	1.6	1.7	9.5
CMOS 74LVX	4.8	3.7	95	6.6	16.7	5.2	13.0	4	-4	1.4	1.7	12.0
CMOS 74VHC	4.1	3.2	109	5.7	14.4	4.5	11.2	8	-8	2.1	2.8	8.5
CMOS 74VCX	2.0	2.0	175	3.6	9.0	2.8	7.0	24	-24	0.8	2.2	2.5
CTT	0.600	0.750	583	1.07	2.70	0.84	2.10	8	-8	1.3	1.7	2.0
ECL 10K	2.2	2.2	159	3.9	9.9	3.1	7.7	50	-50	-1.7	-0.95	2.0
ECL 10KH	1.7	1.7	206	3.0	7.7	2.4	6.0	50	-50	-1.7	-0.95	1.0
ECL 100K	0.600	0.600	583	1.07	2.70	0.84	2.10	50	-50	-1.5	-0.90	0.800
ECL 300K	0.500	0.500	700	0.89	2.25	0.7	1.25	50	-50	-1.7	-0.95	1.55
ECL (E)	0.375	0.375	933	0.67	1.69	0.53	1.31	50	-50	3.3	4.0	0.300
LVPECL (EP)	0.110	0.110	3182	0.20	0.50	0.15	0.39	50	-50	1.6	2.4	0.160
LVPECL (LVEL)	0.220	0.220	1591	0.39	0.99	0.31	0.77	50	-50	1.6	2.4	0.300
PECL (EL)	0.225	0.225	1556	0.40	1.01	0.32	0.79	50	-50	3.3	4.0	0.250
RSECL (SiGe)	0.030	0.030	11700	0.06	0.14	0.04	0.11					
GaAs	0.300	0.100	3500	0.18	0.45	0.14	0.35	30	-30	0.8	2.0	0.250
GTL	1.2	1.2	292	2.1	5.4	1.7	4.2	40	-40	0.75	0.85	3.0
GTL+	0.300	0.300	1167	0.53	1.35	0.42	1.05	40	-40	0.80	1.20	3.0
HSTL	0.620	0.220	1591	0.39	0.99	0.31	0.77	8~48	-8~48	0.75	0.85	1.7
LVDS	0.300	0.300	1167	0.53	1.35	0.42	1.05	3.5	-3.5	1.07	1.41	2.0
SSTL	0.330	0.510	1060	0.59	1.50	0.46	1.17	8~20	-8~20	1.30	1.70	1.8
TTL 74	8.0	5.0	70	8.9	22.5	7	17.5	16	-15	0.8	2.0	20.0
TTL 74ALS	2.3	2.3	152	4.1	10.4	3.2	8.1	24	-15	0.8	1.6	10.0
TTL 74AS	2.1	1.5	233	2.7	6.8	2.1	5.3	64	-15	0.5	1.9	6.2
TTL 74F	2.3	1.7	206	3.0	7.7	2.4	6.0	64	-15	0.9	1.8	6.5
TTL 74FR	2.1	1.5	233	2.7	6.8	2.1	5.3	64	-15	0.6	2.2	3.9
TTL 74H	7.0	7.0	50	12.4	31.5	9.8	24.5	20	-0.25	0.8	2.0	15.0
TTL 74L	35.0	30.0	12	53.3	135.0	42.0	105.0	2	-0.4	0.8	2.0	35.0
TTL 74LS	15.0	10.0	35	17.8	45.0	14.0	35.0	24	-15	0.8	1.8	18.0
TTL 74S	2.5	2.0	175	3.6	9.0	2.8	7.0	64	-15	0.8	1.8	6.0



insight into the periodicity of a signal and are easier to use than time domain representations. For example, for a sinusoidally varying signal, it is more convenient to represent the signal as a kroneker delta in the frequency domain than as a series of continuous values, the sinewave.

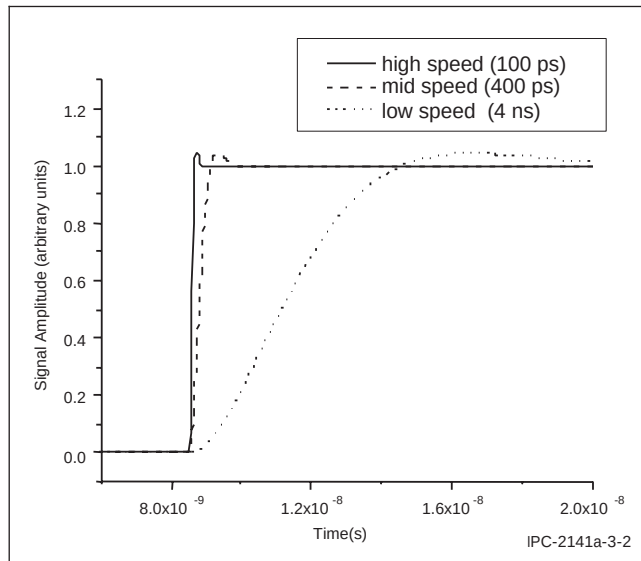


Figure 3-2 Step-like Waveforms. Transition duration values are shown in parenthesis.

A signal commonly encountered in circuits is a rectangular pulse, which may be used for clock signals and data. Figure 3-2 shows three different pulses, each with a different transition duration (or rise time). The higher the bandwidth of the pulse, the shorter is its transition duration (see 3.4.5).

To represent a time domain signal in the frequency domain (or vice versa), mathematical operators, called transforms, are used. The most commonly-used transform is the Fourier transform. The Fourier transform exploits the periodicity of a signal to generate the frequency domain representation, the spectrum, of that signal. The spectrum can be presented as either a complex number (real and imaginary parts) or as magnitude and phase. Each frequency component of the spectrum has a unique real and imaginary part (or magnitude and phase). The continuous Fourier transform of a continuous signal is given by:

$$\begin{aligned}
 H(f) &= \int_{t=0}^{\infty} h(t)e^{-j2\pi ft} dt \\
 &= \int_{t=0}^{\infty} f(t)[\cos(2\pi ft) - j\sin(2\pi ft)] dt \\
 &= a(f) - jb(f)
 \end{aligned}
 \quad [3-4]$$

where $h(t)$ is the signal, and $H(f)$ is the Fourier transform of the signal. The magnitude and phase are derived from the real and imaginary parts. The magnitude spectrum, $M(f)$, is found from:

$$M(f) = \sqrt{a^2(f) + b^2(f)} \quad [3-5]$$

and the phase spectrum, $\theta(f)$, from:

$$\theta(f) = \tan^{-1}\left(\frac{b(f)}{a(f)}\right) \quad [3-6]$$

As mentioned in 3.4.5, the bandwidth is typically defined as the frequency at which the power spectrum drops to -3 db relative to the DC power. Figure 3-3 shows the power spectrum of the pulses related to those shown in Figure 3-2. (To avoid showing unnecessary spectral artifacts, like oscillatory behavior, the spectrum shown in Figure 3-3 are actually the spectra of the derivatives of the pulses shown in Figure 3-2.).

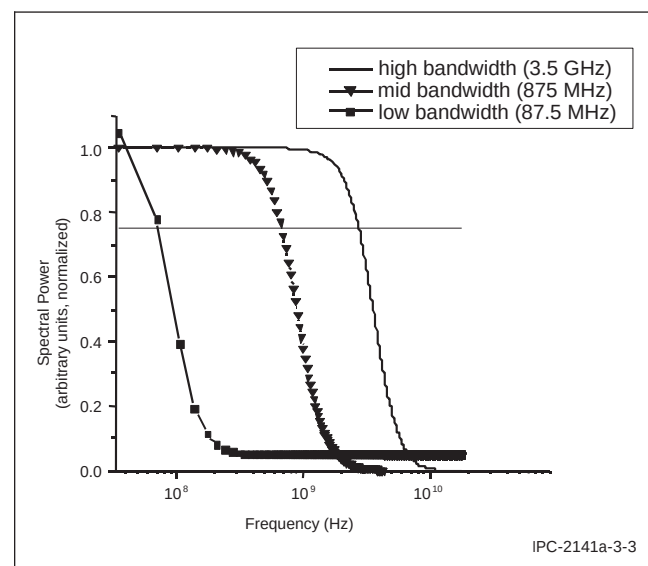


Figure 3-3 Spectra of the derivatives of the waveforms shown in Figure 3-2.

3.4.6 Capacitive Line Versus Transmission Line Environment

Conductors can behave either as lumped elements (resistance, inductance or capacitance) or as distributed elements (transmission lines) depending on the length of the conductors relative to the frequencies of the signal propagating along the conductor (see 3.4.9). At low frequencies, a signal path on a circuit board may be represented electrically as a capacitance in parallel with a resistance. However, as the frequency is increased, this approach of lumped circuit modeling is no longer accurate and signal paths must be regarded as transmission lines. The analysis required to determine if the conductor behaves like a transmission line can be performed in either the frequency or the time domain. However, the critical point to remember for digital signals is that it is the pulse rise time, and not the rate at which the device is clocked, that is the key determining factor. The clock rate is limited by the rise time, thus the faster the rise time is, the faster the clock frequency may be. The critical design parameters and requirements will depend on the purpose of the line.

3.4.6.1 Capacitive Line The purpose for a capacitive line is to store charge and it is short in length. The charging time of the capacitive line and, consequently, the voltage on this line, depends on the current. The propagation time of the short capacitive line is usually less than the rise time of the digital pulse traveling on the line. Consequently, reflections from the ends of the transmission line can add to the signal, thereby degrading the pulse integrity. Specifically, because the line is so short, the reflections cause the rise time of the pulse to broaden. This broadening effect can be described equivalently as the result of a lumped element RC filter, where R is given by the load impedance and C is given by the capacitance of the transmission line and other elements connected to the line. The impedance of the lumped element line can be calculated as a resistance in series with an inductance and a shunt capacitance:

$$Z_{0,L} = \sqrt{R_L^2 + \frac{\omega^2 L^2}{(1 - \omega^2 LC)^2}} \quad [3-7]$$

where R_L , L , and C represent the lumped resistance, inductance, and capacitance for a given length of line.

3.4.6.2 Transmission Line For transmission lines, the design intent is to provide a known and common impedance environment that facilitates impedance matching to the devices populating a printed wiring board. Impedance matching is necessary to ensure the integrity of high-speed logic pulses. Discontinuities in impedance are the source of reflections that will degrade the integrity of the digital pulse and these discontinuities occur at the terminations (ends) of the transmission lines or at physical discontinuities in the transmission line. The characteristic impedance, Z_0 , of a uniform continuous transmission line is given by:

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad [3-8]$$

where R , L , G , and C are the resistance, inductance, conductance, and capacitance of the transmission line per unit length, ω is the angular frequency, $\omega = 2\pi f$, and f is frequency. R and L are functions of the conductor properties (conductivity and permeability) and transmission line geometry. R and L are also frequency dependent because the penetration of the current into the conductors is frequency dependent: R increases with frequency and L decreases with frequency. L decreases to a limit because L is actually the sum of an internal self inductance, L_i , and an external self inductance, L_e , where L_e is fixed but L_i decreases as the penetration of the current into the conductor decreases. G and C are functions of the dielectric properties (permittivity) and the geometry of the transmission line. G and C may be a function of frequency but this dependence is a consequence of a frequency-dependent

permittivity. Usually the permittivity is constant over the frequency range that the circuit operates so that C is also constant. Typically $G \ll \omega C$ and is ignored. Although Z_0 is a complex value (contains a real and an imaginary part), it is sometimes approximated as a real value from the following ideal approximation:

$$Z_{0,I} = \sqrt{\frac{L}{C}} \quad [3-9]$$

A more accurate approximation to the magnitude of the characteristic impedance of the transmission line is obtained by using a second-order Taylor series expansion of Z_0 (equation [3-8]) with $G = 0$:

$$Z_0 \approx \sqrt{\frac{L}{C}} \left(1 + \frac{R^2}{8\omega^2 L^2} \right) \quad [3-10]$$

From these last two equations for the characteristic impedance, we can see that Z_0 increases if L increases or if C decreases.

Characteristic impedance is important in high speed printed wiring boards for several reasons. First, the amount of current that is required to drive a conductor depends on Z_0 via Ohm's law, which is: $V = IZ_0$. Second, in high speed systems with impedance mismatches along the signal path, reflections will occur. Reflections not only reduce the amount of power reaching the receiver, but may also cause ringing (noise) along the circuit. These forms of signal degradation can cause systems to malfunction due to missing data pulses (from attenuation drop out) or spurious data pulses (from reflection noise).

The resistivity of the conductor, typically copper, does not contribute significantly to the high speed circuit impedance because the conductivity of most practical conductors is high and the operating frequencies are high (therefore, $R \ll \omega L$).

For controlled impedance conductor interconnections, the electrical and dielectric properties of the board materials have increased importance and greater care must be taken with the design and termination of the circuit.

3.4.7 Propagation in a Transmission Line The propagation of an electromagnetic wave in a uniform continuous transmission line is described by its propagation function, $\Gamma(\omega)$, which is given by:

$$\Gamma(\omega) = e^{-\gamma(\omega)L} \quad [3-11]$$

where ω is the angular frequency, L is the propagation distance, and $\gamma(\omega)$ is the propagation coefficient give by:

$$\begin{aligned} \gamma(\omega) &= \sqrt{(R + j\omega L)(G + j\omega C)} \\ &= \alpha(\omega) + j\beta(\omega) \end{aligned}$$

where $\alpha(\omega)$ and $\beta(\omega)$ are the attenuation (or loss) and phase functions of the transmission line.

3.4.7.1 Attenuation Attenuation is a critical parameter for preserving the integrity of a signal propagating in the transmission line and for the performance of high-speed circuits. High-speed electronic systems generate and require fast transition (risetime, falltime) electrical pulses. These systems may respond unpredictably to pulses having transitions slower than a critical duration or amplitudes less than a critical voltage. Because attenuation in the transmission line is a frequency dependent phenomenon, attenuation may cause the pulse transition to increase to a value greater than some critical value thereby causing the circuit to malfunction. Attenuation will also cause the pulse amplitude to decrease.

Losses in a transmission line are given by:

$$\alpha = \alpha_c + \alpha_d + \alpha_r \quad [3-13]$$

Where α_c , α_d , and α_r are the conductor, dielectric, and radiative losses. Signal attenuation and distortion in a uniform continuous transmission line are caused by resistive losses in the conductors and dissipative losses in the dielectric. The effects of signal attenuation and distortion can best be understood if the pulse is described as consisting of many frequency components, a spectrum (see 3.4.5.1). The faster the pulse transition, the higher the frequency content of the pulse's spectrum. For the low frequency spectral components of the signal, the resistive losses are described by the DC resistance of the conductor. The DC losses affect pulse amplitude. For the high frequency components, the resistive losses are dependent on the penetration of the current into the conductors, which is a function of the metal conductivity and the frequency; these losses are called skin-effect losses. Skin effect losses increase with increasing frequency. The skin effect loss is also increased by rough conductor surfaces; the rough-surfaced conductors effectively have a longer electrical path length than a smooth-surfaced conductor.

The dissipative losses of the signal in the dielectric increase with increasing frequency for a constant loss tangent. Consequently, the higher frequency components of the signal will experience greater dielectric losses and thus cause the transition duration of the pulse to increase.

For an example of loss in a transmission line, consider a stripline structure. The dielectric contribution, α_d , to the attenuation is not affected by signal line width. The attenuation, in dB/m, due to dielectric losses is given by (2, Equation 7):

$$\alpha_d = 8.68589\pi \frac{f}{c} \sqrt{\epsilon_r} \tan \delta \quad [3-14]$$

where c is the speed of light. From this equation, it can be seen that the dielectric loss increases with increasing fre-

quency and increasing loss tangent. The conductor losses are dependent on the penetration of the electrical current into the conductors. The attenuation in the conductors, α_c , is complicated for planar structures (see IPC-2252), but it is proportional to the surface resistivity. For smooth conductors the surface resistivity in ohms/square is given by:

$$R_s = \sqrt{\frac{\pi f \mu}{\sigma}} \quad [3-15]$$

Corrections to this equation for surface roughness should be made (see IPC-2252), especially for high frequencies where the surface roughness approaches the skin depth. The skin depth is the depth into a conductor for which e^{-1} of the current associated with a propagating electromagnetic signal is flowing (see IPC-2252). The skin depth becomes less as frequency increases and so resistive loss also increases. The skin depth, δ , is given by:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad [3-16]$$

where μ is the magnetic permeability of the conductor and σ is the electrical conductivity of the conductor. Since α_c is proportional to R_s , α_c will increase with increasing frequency, decreasing conductivity, and/or increasing permeability.

3.4.7.2 Dispersion Dispersion occurs when the propagation speed (see 3.4.7.3) changes with frequency. The propagation speed is affected by frequency through a frequency dependence in the relative permittivity of the dielectrics of the transmission line. Dispersion will cause the transition of the pulse to broaden and this broadening may cause the circuit to malfunction.

3.4.7.3 Propagation Speed Propagation speed is the speed at which an electromagnetic wave propagates in a given medium. For a transmission line, the propagation speed is affected by the effective permittivity (see 3.4.2.2). From Maxwell's equations, it can be shown that the propagation speed, v , for a signal in a transmission line is:

$$v = \frac{c}{\sqrt{\epsilon_{r,eff}}} \quad [3-17]$$

where c is the speed of light in a vacuum (3×10^8 m/s) and $\epsilon_{r,eff}$ is the real part of the effective relative permittivity. The propagation speed of a pulse in a transmission line is affected by the frequency-dependent phase and attenuation characteristics of the transmission line. The attenuation (see 3.4.7.1) is caused by conductor, dielectric, and radiative losses in the transmission line. The phase response is affected by the permittivities of the dielectrics.

The propagation speed is important, for example, in determining the delays in a transmission line and the time

these delays, the skew (see 3.4.14.1). 4.2 lists equations for several transmission line configurations from which the propagation speed of the transmission line can be calculated.

Signal (pulse or sinusoidal) propagation speed is also affected by the surface roughness of the conductors. Surface roughness of the conductor increases the effective path length that a signal must propagate and, thereby, increases the signal propagation time for a given length of conductor (1).

Pulse propagation speeds in transmission lines may appear different for different device technologies. However, this apparent difference in propagation speed is a consequence of several factors. For one, the device technologies are limiting the bandwidth (see Table 3-1) and, thus, the propagating frequencies of the pulse. Secondly, a given transmission line structure (such as microstrip or strip line), will exhibit frequency dependent attenuation (see 3.4.7.1) and dispersion (see 3.4.7.2), both of which will cause the pulse transition to increase. Lastly, propagation speed is typically defined from the propagation delay (see 3.4.10.1) which may be affected by broadening of the pulse transition caused by attenuation and dispersion.

3.4.8 Critical Signal Speed The critical signal speed is related to the signal rise time, not the clock frequency. The bandwidth of a digital system is determined by the leading edge of the pulse (which has the shortest transition time). This edge must be permitted to rise (or fall) as quickly as possible. High speed signals have bandwidths in the 100 MHz to 1 GHz range, corresponding to rise/fall times ranging between 3.5 ns to 350 ps (see 3.4.5). The general rule is that transmission line effects (wave effects) become an important design consideration when the length of the interconnection (including conductors and plated-through holes) approaches some fraction of the wavelength (see 3.4.9) of the -3 dB frequency of the signal's power spectrum. The wavelength at a given frequency can be obtained using:

$$\lambda = \frac{v}{f} \quad [3-18]$$

where λ is wavelength. Successful controlled impedance design requires the use of materials where ϵ_r is relatively constant over the 100 MHz to 1 GHz frequency range. Table 3-1 shows the rise times for some families of the ICs. For example, ECL has a 0.45 ns rise time and this rise time corresponds to a 3 dB frequency bandwidth of 777 MHz.

3.4.9 Critical Line Length The critical length is the length above which a conductor exhibits the characteristics of a transmission line, that is, when propagation effects of the conductor should be considered. The critical length, a

parameter widely cited within the printed board wiring community, is determined from the rise time of the pulse and the propagation speed of the pulse in the transmission line. The critical length can be determined in different ways. For example, using the effective permittivity of the transmission line, the pulse propagation speed in the transmission line can be estimated (see 3.4.7.3). From this speed, the electrical length of the transmission line is calculated from the product of the pulse rise time, t_r , and the pulse propagation speed, v , where v is defined in 3.4.7.3 and t_r is described in 3.4.5. The critical length is then defined as being a multiple of electrical lengths ($t_r v$). Typically the critical length is between $2t_r v$ and $10t_r v$, where $10t_r v$ is a conservative value.

For a general "rule of thumb," if the line length is less than $3t_r v$, then the line should be treated as a lumped (or discrete) circuit element. Similarly, for a general "rule of thumb," if the line length is greater than $3t_r v$, then the line should be treated as a distributed circuit element (or transmission line).

An alternative, but less commonly used definition of critical line length is based on the wavelength of the 3 dB frequency, λ_{3dB} , which is the frequency at which the power spectrum of the pulse has dropped -3 dB relative to its DC power. The critical line length, in this case, is equal to $0.5\lambda_{3dB}$. Any circuit conductor greater than or equal to $0.5\lambda_{3dB}$ is considered a transmission line.

For conductors longer than the critical length, reflections from a mismatched load impedance may be received back at the source after the pulse has reached its maximum value; this may lead to false triggering of a device. For conductors shorter than the critical length, reflected pulses are received back at the source before the pulse has reached its maximum value. Therefore, any modification of the pulse shape will only be to the leading edge, which is less likely to produce false device triggering.

3.4.10 Propagation Time Propagation time is the time it takes a signal to travel from node to another node along a given interconnect. Propagation time is in units of seconds. For a system to perform correctly at high speeds, controlled propagation time between nodes may be required. Adjustments in the propagation time of the line may be achieved by controlling the length of the line from source to load. As shown in sec. 3.4.7.3, the real part of the effective relative permittivity affects the propagation speed. Because propagation delay (see 3.4.10.1) is the reciprocal of propagation speed, the effective permittivity affects propagation time and delay. In some situations, ϵ'_r will be dependent on the orientation of the electric field of the propagating pulse with respect to the material axes (such as FR4). To calculate the propagation speed for a specific conductor, the equation in 3.4.7.3 must be used where ϵ'_r is the permittivity

$\epsilon'_{r,eff}$, where $\epsilon'_{r,eff}$ is the effective relative permittivity, which was described in 3.4.2.2.

The measurement of propagation time in a transmission line may be affected by frequency-dependent attenuation (see 3.4.7.1), dispersion (see 3.4.7.2), and pulse amplitude attenuation. Dispersion and frequency-dependent attenuation typically will cause the rise time of the pulse to increase with propagation distance in a transmission line and this in turn will cause an observed increase in propagation time. Pulse amplitude attenuation will affect propagation time calculations if a fixed amplitude is used as a reference level. For example, if the input pulse has an amplitude of 2 V, the reference level is chosen to be 1 V, and after propagation in the transmission line the pulse amplitude is reduced to 1.5 V, an erroneous increase in propagation time may be computed.

3.4.10.1 Propagation Delay Propagation delay is the time it takes a pulse to travel a given length of transmission line (that is, propagation delay is the propagation time per unit length), typically given in units of ps/cm. Because the propagation time is directly proportional to the square root of $\epsilon'_{r,eff}$, so is the propagation delay.

3.4.11 Signal Loading Effects When a conductor is connected to several loads (devices), signal loading must be considered. When connected in serial fashion and where the impedance of the load is low or a near match to the characteristic impedance of the line, there will be a decrease in signal amplitude as each load is reached. High impedance loads relative to the line impedance will result in a smaller decrease in amplitude. An impedance-matched load at the end signal line may be necessary to prevent a reflection that could send an aberrant pulse (resulting in a false triggering) on the line

Radial or star connections to loads may result in complex reflections from the open ends of each line that add to each other. This method of connecting should be avoided in high speed design.

3.4.12 Crosstalk Crosstalk is the transfer (coupling) of energy between conductors by mutual inductance and/or capacitance. In crosstalk, the energy from an active line becomes superimposed on a passive line (also called a quiet line, victim line, or a receptor conductor), leading to spurious switching and circuit dropouts. Crosstalk is a result of the electromagnetic fields of the signal propagating on the active line extending outward to and enveloping the quiet line. The magnitude of coupling to the passive line is dependent on the length over which the fields envelop the passive line and the magnitude of those fields.

The terms “near end” and “far end” are used to indicate the direction of signal propagation on a line. The near end refers to the signal originating end, and the far end refers

to the signal receiving end. The coupled signals that travel toward the far end of the line constitute forward crosstalk, and the coupled signals that travel back to the near end constitute backward crosstalk. The crosstalk coupling coefficients found in references differentiate between the forward and backward coefficients.

The coupling to the passive line by capacitive effects causes a low level replica of the active signal to be sent to both the far and near ends of the passive line, with the same polarity as the active signal. The coupling due to the inductive effects also sends signals to both the near and the far ends of the passive line, but the signal observed at the far end is inverted (reversed polarity) relative to that of the active signal. The signals from the both inductive and capacitive crosstalk sum at the far and near ends of the passive line. Consequently, backward crosstalk is the sum of the inductive and capacitive coupling, whereas forward crosstalk is the difference between the two signals. Forward crosstalk is usually smaller than backward crosstalk. Backward crosstalk reaches a maximum in short parallel runs and is of major concern in circuit design.

The magnitude of the coupled signal decreases with shorter parallel line segments, wider line separations, thinner dielectrics, and longer pulse rise times. Conductors that are parallel for long lengths either on the same signal plane or on adjacent signal planes are susceptible to induced crosstalk. A passive line can also run parallel for short distances to several other lines. If a certain combination and timing of pulses occurs, this combination can induce a signal on the passive line that is equal in amplitude to the active signal. Thus, there are design requirements that state that the crosstalk between lines be kept below some specified level.

Typically, crosstalk is a concern when high-speed devices are used because of their fast rise time. Mixing logic families may also cause problems because of the mixture of various voltage swings, noise margins, and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL switches 3 volts and the ECL family has only a 100 mV DC noise margin, significant undesired coupling can occur to an ECL device in a TTL circuit.

3.4.13 Termination of Nets Termination of nets may be necessary to satisfy signal integrity, timing, and voltage requirements of drivers and receivers and impedance matching. Terminations prevent reflections of the propagating pulse by either providing an impedance match for the transmission line at the device I/O port or by absorbing the energy reflected from the device I/O port. Common termination types are detailed in the following paragraphs and are shown in Figure 3-4.

