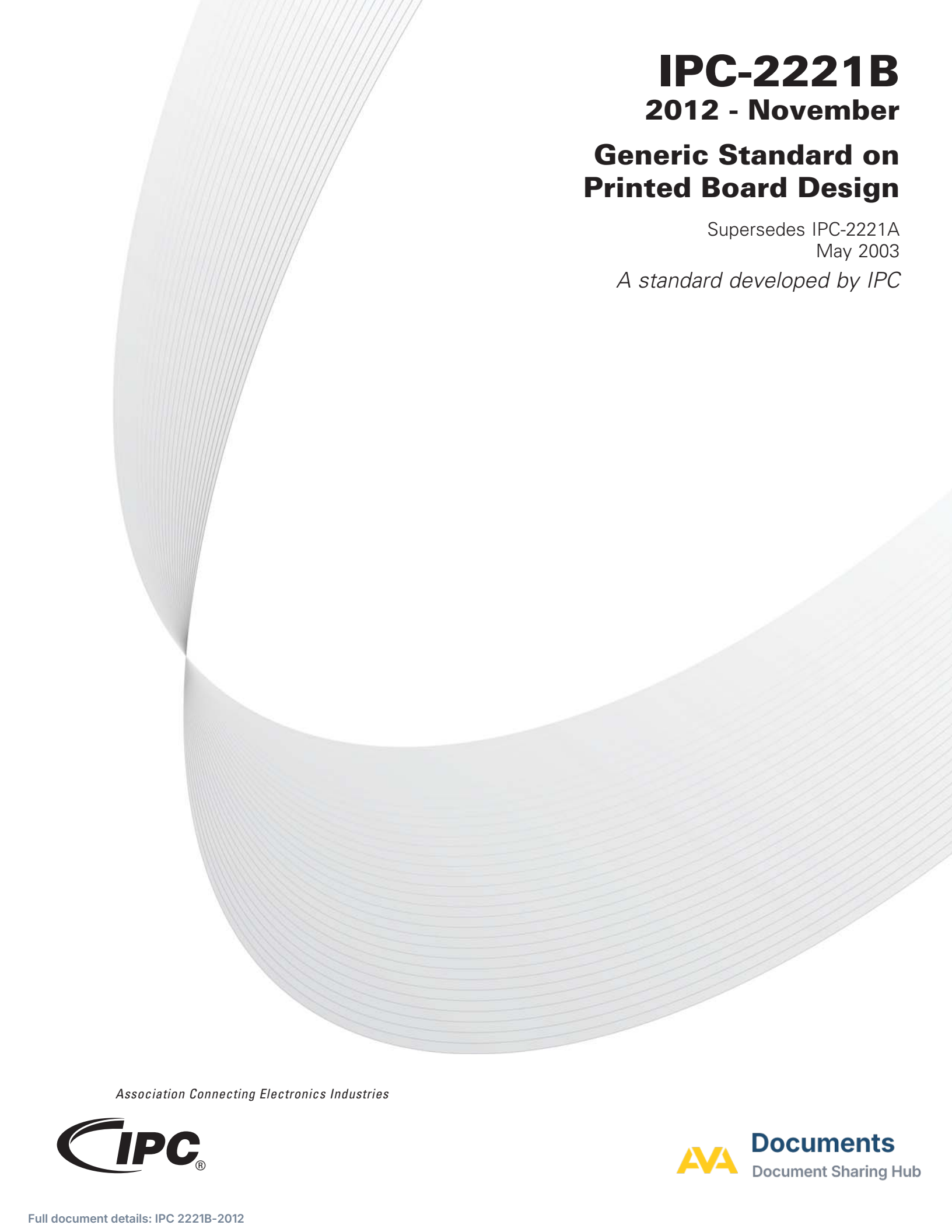




IPC-2221B

2012 - November

Generic Standard on Printed Board Design

Supersedes IPC-2221A
May 2003

A standard developed by IPC

Association Connecting Electronics Industries



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IPC-2221B

Generic Standard on Printed Board Design

Developed by the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of IPC

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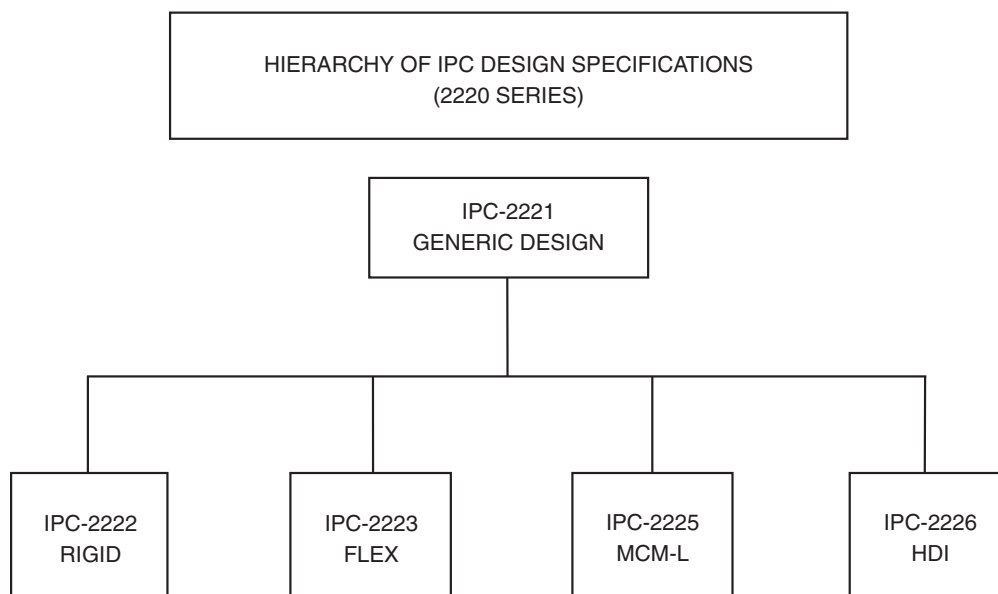
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Users of this publication are encouraged to participate in the development of future revisions.

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FOREWORD

This standard is intended to provide information on the generic requirements for organic printed board design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the broad spectrum of those designs that use organic materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting electronic, electromechanical, and mechanical components. It is crucial that a decision pertaining to the choice of product types be made as early as possible. Once a component mounting and interconnecting technology has been selected the user should obtain the sectional document that provides the specific focus on the chosen technology.

It may be more effective to consider alternative printed board construction types for the product being designed. As an example the application of a rigid-flex printed wiring board may be more cost or performance effective than using multiple printed wiring boards, connectors and cables.

IPC's documentation strategy is to provide distinct documents that focus on specific aspect of electronic packaging issues. In this regard document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0).

Included in the set is the generic information which is contained in the first document of the set and identified by the four digit set number. The generic standard is supplemented by one or many sectional documents each of which provide specific focus on one aspect of the topic or the technology selected. The user needs, as a minimum, the generic design document, the sectional of the chosen technology, and the engineering description of the final product.

As technology changes specific focus standards will be updated, or new focus standards added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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Generic Standard on Printed Board Design

1 SCOPE

This standard establishes the generic requirements for the design of organic printed boards and other forms of component mounting or interconnecting structures, including PC card form factors. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials; the interconnections may be single, double, or multilayered.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of a specific interconnecting structure sectional standard (see 1.2) to produce detailed designs intended to mount and connect components. This standard is not intended for use as a performance specification for finished printed boards nor as an acceptance document for electronic assemblies.

1.2 Documentation Hierarchy This standard identifies generic physical design principles, and is supplemented by various sectional standards that provide sharper focus on specific aspects of printed board technology. These include:

IPC-2222 Rigid organic printed board design
IPC-2223 Flexible printed board design
IPC-2225 Organic, MCM-L, printed board design
IPC-2226 High Density Interconnect (HDI) printed board design

The documents are a part of the Family of Design Documents which is identified as IPC-2220. The number IPC-2220 is for ordering purposes only and includes this standard and the four listed above.

Note: IPC-2224, a sectional design standard for PC card form factors, was cancelled by the IPC. Relevant PC form factor design information has been transferred to this revision of IPC-2221 and to IPC-2222.

1.3 Presentation All dimensions and tolerances in this standard are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this standard are expected to use metric dimensions. All dimensions greater than or equal to 0.1 mm [0.0039 in] will be expressed in millimeters and inches. All dimensions less than 0.1 mm [0.0039 in] will be expressed in micrometers and microinches.

1.3.1 Dimensional Units The following is taken from National Institute of Standards and Technology - Metric Information and Conversions: "Beginning January 1, 2010, the European Union Council Directive 80/181/EEC (Metric Directive) allowed the use of only metric units, and prohibited the use of any other measurements for most products sold in the European Union (EU). The Metric Directive made the sole use of metric units obligatory in all aspects of life in the European Union, extending to areas such as product literature and advertising."

Most component datasheets are provided in metric units. Many printed board designers spend a lot of time converting between imperial (inch) and SI (metric). Round-off errors, when converting units, can result in inaccuracies that result in marginal or failed designs. However, the printed board fabrication vendors often default to imperial units. Electronic Computer Aided Design (ECAD) tools accommodate both metric and imperial library components being placed on the same printed board because dimensional precision is large enough to describe most standard components accurately.

Problems arise when importing information from third party software or trying to mix units during printed board layout. For example, if a portion of the printed board design is an imported Drawing Exchange Format (.DXF) file with metric units that needs to interface with a digital portion done in imperial units, a problem can occur where the data from the two grids are mixed. Unlike importing from libraries, a conversion to printed board units is not always done when importing DXF.

While a user can convert printed board units from metric to imperial in modern day tools without problems, this should not be done too often during the design phase as repeated conversions can introduce unexpected errors. A single set of units should be used in the layout of the printed board. If imported data is in metric units, the layout portion of the process should use metric units. Once the layout is complete and verified, the designer can convert the printed board to imperial units for documentation, if necessary.

1.4 Interpretation "Shall," the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a "shall" requirement may be considered if sufficient data is supplied to justify the exception.

The words “should” and “may” are used whenever it is necessary to express nonmandatory provisions. “Will” is used to express a declaration of purpose.

To assist the reader, the word “**shall**” is presented in bold characters.

1.5 Definition of Terms The definition of all terms used herein **shall** be in accordance with IPC-T-50 and as defined in 1.5.1.

1.5.1 Microvia A microvia is defined as a blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 1-1, terminating on or penetrating a target land, with a total length of no more than 0.25 mm [0.00984 in] measured from the structure’s capture land foil to the target land.

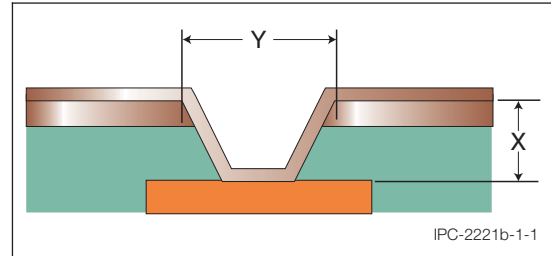


Figure 1-1 Microvia Definition

Note: X/Y = Microvia Plating Aspect Ratio, with $X \leq 0.25$ mm [0.00984 in] and aspect ratio $\leq 1:1$.

1.6 Classification of Products This standard recognizes that printed boards and printed boards assemblies are subject to classifications by intended end item use. Classification of producibility is related to complexity of the design and the precision required to produce the particular printed board or printed board assembly.

Any producibility level or producibility design characteristic may be applied to any end-product equipment category. Therefore, a high-reliability product designated as Class “3” (see 1.6.2), could require level “A” design complexity (preferred producibility) for many of the attributes of the printed board or printed board assembly (see 1.6.3).

1.6.1 Printed Board Type This standard provides design information for different printed board types. Printed board types vary per technology and are thus classified in the design sectionals.

1.6.2 Performance Classification This standard recognizes that electrical and electronic products are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of product between classes.

The user is responsible for defining the product class. The procurement documentation package **shall** state the product class and any exceptions to specific parameters, where appropriate.

Criteria defined in this document reflect three classes, which are as follows:

Class 1 General Electronic Products – Includes limited life products suitable for applications where the requirement is function of the completed product.

Class 2 Dedicated Service Electronic Products – Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical.

Class 3 High Reliability Electronic Products – Includes products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, and the product must function when required.

1.6.3 Producibility Level When appropriate, this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

- Level A General Design Producibility-Preferred
- Level B Moderate Design Producibility-Standard
- Level C Least Design Producibility-Reduced

The producibility levels **shall not** to be interpreted as a design requirement, but rather as a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the numerous tables are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that **shall** be controlled on the end item **shall** be specified on the master drawing of the printed board or the printed board assembly drawing.

1.7 Revision Level Changes Changes made to this revision of the IPC-2221 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the Figure or Table header.

2 APPLICABLE DOCUMENTS

The following documents form a part of this document to the extent specified herein. If a conflict of requirements exists between IPC-2221 and those listed below, IPC-2221 takes precedence.

2.1 IPC¹

IPC-TR-001 An Introduction to Tape Automated Bonding Fine Pitch Technology

IPC-A-43 Ten-Layer Multilayer Artwork

IPC-A-47 Composite Test Pattern Ten-Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-322 Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

IPC-D-356 Bare Substrate Electrical Test Data Format

IPC-D-422 Design Guide for Press Fit Rigid Printed Board Backplanes

IPC-TM-650 Test Methods Manual²

2.4.22 Bow and Twist

2.5.5.7 Characteristic Impedance Lines on Printed Boards by TDR

2.5.6 Dielectric Breakdown of Rigid Printed Wiring Material

2.5.7 Dielectric Withstanding Voltage, PWB

2.5.7.2 Dielectric Withstand Voltage (HiPot Method) - Thin Dielectric Layers for Printed Boards

2.6.8 Thermal Stress, Plated-Through Holes

2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

IPC-CM-770 Printed Board Component Mounting

IPC-SM-780 Component Packaging and Interconnecting with Emphasis on Surface Mounting

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-MC-790 Guidelines for Multichip Module Technology Utilization

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Boards

IPC-HDBK-840 Solder Mask Handbook

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-2141 Controlled Impedance Circuit Boards and High Speed Logic Design

IPC-2251 Design Guide for High Speed/High Frequency Electronic Packaging

1. www.ipc.org

2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/html/testmethods.htm)

- IPC-2316** Design Guide for Embedded Passive Device Printed Boards
- IPC-2511** Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer Methodology
- IPC-2611** Generic Requirements for Electronic Product Documentation
- IPC-2615** Printed Board Dimensions and Tolerances
- IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards
- IPC-4103** Specification for Base Materials for High Speed/High Frequency Applications
- IPC-4202** Flexible Base Dielectrics for Use in Flexible Printed Circuitry
- IPC-4203** Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring and Flexible Bonding Films
- IPC-4204** Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry
- IPC-4552** Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
- IPC-4553** Specification for Immersion Silver Plating for Printed Boards
- IPC-4554** Specification for Immersion Tin Plating for Printed Circuit Boards
- IPC-4562** Metal Foil for Printed Wiring Applications
- IPC-4563** Resin Coated Metal Foil for Printed Boards
- IPC-4761** Design Guide for Protection of Printed Board Via Structures
- IPC-6011** Generic Performance Specification for Printed Boards
- IPC-6012** Qualification and Performance Specification for Rigid Printed Boards
- IPC-7094** Design and Assembly Process Implementation for Flip Chip and Die Size Components
- IPC-7095** Design and Assembly Process Implementation for BGAs
- IPC-7351** Generic Requirements for Surface Mount Design and Land Pattern Standard
- IPC-7525** Stencil Design Guideline
- IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
- IPC-9252** Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards
- IPC-9631** Users Guide for IPC-TM-650, Method 2.6.27, Thermal Stress, Convection Reflow Assembly Simulation

2.2 Joint Industry Standards³

- J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies
- JP002** Current Tin Whiskers Theory and Mitigation Practices Guideline
- J-STD-003** Solderability Tests for Printed Boards
- J-STD-005** Requirements for Soldering Pastes
- J-STD-006** Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

3. www.ipc.org

2.3 Society of Automotive Engineers⁴

SAE-AMS-QQ-A-250 Aluminum Alloy, Plate and Sheet

SAE-AMS-QQ-N-290 Nickel Plating (Electrodeposited)

2.4 American Society for Testing and Materials⁵

ASTM-B-152 Copper Sheet, Strip and Rolled Bar

ASTM-B-488 Standard Specification for Electrodeposited Coatings of Gold for Engineering Use

ASTM-B-579 Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)

2.5 Underwriters Labs⁶

UL-94 Test for Flammability of Plastic Materials for Parts in Devices and Appliances

UL-746E Standard Polymeric Materials, Material used in Printed Wiring Boards

2.6 IEEE⁷

IEEE 1149.1 Standard Test Access Port and Boundary-Scan Architecture

2.7 ANSI⁸

ANSI/EIA 471 Symbol and Label for Electrostatic Sensitive Devices

2.8 ANSI/ESD⁹

ANSI/ESD-S-20.20 Protection of Electrical and Electronic Parts, Assemblies and Equipment

2.9 PCMCIA¹⁰

PC Card Standard Physical Specification

4. www.sae.org

5. www.astm.org

6. www.ul.org

7. www.ieee.org

8. www.ansi.org

9. www.esda.org

10. www.pcmcia.org

3 GENERAL REQUIREMENTS

The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle.

Designing the physical features and selecting the materials for a printed board involves balancing the electrical, mechanical and thermal performance as well as the reliability, manufacturing and cost of the printed board. The tradeoff checklist (see Table 3-1) identifies the probable effect of changing each of the physical features or materials. The items in the checklist need to be considered if it is necessary to change a physical feature or material from one of the established rules. Cost can also be affected by these parameters as well as those in Table 5-1.

How to read Table 3-1: As an example, the first row of the table indicates that if the dielectric thickness to ground is increased, the lateral crosstalk also increases and the resultant performance of the printed board is degraded (because lateral crosstalk is not a desired property).

Table 3-1 PCB Design/Performance Tradeoff Checklist

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Dielectric Thickness to Ground	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
Line Spacing	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk		X	X	
	MP	Physical Size/Weight	X			X
	M/Y	Electrical Isolation	X		X	
Coupled Line Length	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk	X			X
Line Width	EP	Lateral Crosstalk		X	X	
	EP	Vertical Crosstalk	X			X
	EP	Characteristic Impedance		X	Design Driven	
	MP	Physical Size/Weight	X		Design Driven	
	R	Signal Conductor Integrity	X		X	
	M/Y	Electrical Continuity	X		X	
Line Thickness	EP	Lateral Crosstalk	X			X
	R	Signal Conductor Integrity	X		X	
Vertical Line Spacing	EP	Vertical Crosstalk		X	X	
Z ₀ of PCB vs. Z ₀ of Device	EP	Reflections		X	X	
Distance between Via Walls	R	Electrical Isolation	X		X	
Annular Ring (capture and target land to via)	M/Y	Producibility	X		X	
Signal Layer Quantity	MP	Physical Size/Weight	X			X
	M/Y	Layer-to-Layer Registration		X		X

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R) Manufacturability/ Yield (M/Y)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Component I/O Pitch Board Thickness	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	M/Y	Via Plating Thickness		X		X
Copper Plating Thickness	R	Via Integrity	X		X	
Aspect Ratio	R	Via Integrity		X		X
	M/Y	Producibility		X		X
Overplate (Nickel -Kevlar only)	R	Via Integrity	X		X	
Via Diameter	M/Y	Via Plating Thickness	X		X	
	R	Via Integrity	X		X	
Laminate Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	MP	Flatness Stability	X		X	
Prepreg Thickness (Core)	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	EP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
Dielectric Constant	EP	Reflections	X			X
	EP	Characteristic Impedance		X	Design Driven	
	EP	Signal Speed		X	Design Driven	
CTE (out-of-plane)	R	Via Integrity		X		X
CTE (in-plane)	R	Solder Joint Integrity		X		X
	R	Signal Conductor Integrity		X		X
Resin T _g	R	Via Integrity	X		X	
	R	PTH Solder Joint Integrity	X		X	
Copper Ductility	R	Via Integrity	X		X	
	R	Signal Conductor Integrity	X		X	
Copper Peel Strength	R	Component Land Adhesion to Dielectric	X		X	
Dimensional Stability	M/Y	Layer-to-Layer Registration	X		X	
Resin Flow	M/Y	PWB Resin Voids		X	X	
Rigidity	MP	Flexural Modulus	X		Design Driven	
Volatile Content	M/Y	PWB Resin Voids	X			X

3.1 Information Hierarchy

3.1.1 Order of Precedence In the event of conflict, the following order of precedence **shall** apply:

1. The procurement contract.
2. The master drawing or assembly drawing (supplemented by an approved deviation list, if applicable).
3. This standard.
4. Other applicable documents.

3.1.2 End-Product Performance Requirements The end-product performance requirements **shall** be defined prior to design start-up. Maintenance and serviceability requirements are important factors which should be addressed during the design phase. Frequently, these factors affect layout and conductor routing. Finished printed boards **shall** meet the performance requirements of IPC-6011 and its applicable sectional specification (i.e., IPC-6012, IPC-6013, IPC-6018, etc.).

3.2 Design Considerations The design process should include a formal design review of details by as many affected disciplines within the company as possible, including fabrication, assembly and testing. The approval of the layout concepts by representatives of the affected disciplines will ensure that these production-related factors have been considered in the design.

The success or failure of an interconnecting structure design depends on many interrelated considerations. From an end-product usage standpoint, the impact on the design by the following typical parameters should be considered:

- Equipment environmental conditions, such as ambient temperature, heat generated by the components, ventilation, shock and vibration.
- If an assembly is to be maintainable and repairable, consideration **shall** be given to component/circuit density, the selection of printed board/conformal coating materials, and component placement for accessibility.
- Installation interface that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement, and the placement of brackets and other hardware.
- Testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- Process allowances such as etch factor compensation for conductor widths, spacings, land fabrication, etc. (see Sections 5, 9 and 10).
- Manufacturing limitations such as minimum etched features, minimum plating thickness, printed board shape and size, etc.
- Coating and marking requirements.
- Assembly technology used, such as surface mount, through hole, and mixed.
- Printed board performance class (see 1.6.2).
- Materials selection (see Section 4).
- Producibility of the printed board assembly as it pertains to manufacturing equipment limitations. This includes:
Flexibility (Flexural) Requirements
- Electrical/Electronic
- ESD sensitivity considerations.
- Copper density per layer.
- Balanced Construction.
- Partitioning of design for signal integrity, test and ease of design reuse, etc.

Partitioning is performed in the preliminary printed board design phase. It includes trade-off studies, usually including several design concepts that could solve the problem. These design concepts are functionally block diagrammed and, as with any trade-off, a set of advantages and disadvantages is formulated and evaluated by the designer to make his decision on which solution is optimal for this design. It is at this point important to ensure all functional requirements, test connections, and any known growth requirements are being considered. These should flow from the project requirements as documented in the design requirements. The test requirements and growth requirements may not need to be implemented during the electrical design phase, but the interfaces, including printed board wiring, Field Programmable Logic (FPL), and memory assets, should be allocated.

The design partitioning for each concept needs to evaluate what can be implemented on the printed board. The following questions should be answered:

- What are the control requirements?
- What are the memory requirements?
- What are the data path requirements?
- What are the I/O requirements?

It is difficult to convey all the considerations that should be evaluated. The few here have been included to provoke the thought process. Users are encouraged to consult with experienced printed board designers if there is a need for assistance.

3.3 Schematic/Logic Diagram The initial schematic/logic diagram designates the electrical functions and interconnectivity to be provided to the designer for the printed board and its assembly. This schematic should define, when applicable, critical circuit layout areas, shielding requirements, grounding and power distribution requirements, the allocation of test points, and any preassigned input/output connector locations. Schematic information may be generated as hard copy or computer data (manually or automated).

3.4 Density Evaluation A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper), and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute in that they route signals through conductors.

There are also limits to how much routing each can accommodate. The factors that define the limits of their wire routing ability as a substrate are:

- Pitch/distance between vias or holes in the substrate.
- Number of wires that can be routed between those vias.
- Number of signal layers required.

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the wire routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However area array components are more space conservative and allow coarser I/O pitches to be used (see Figure 3-1).

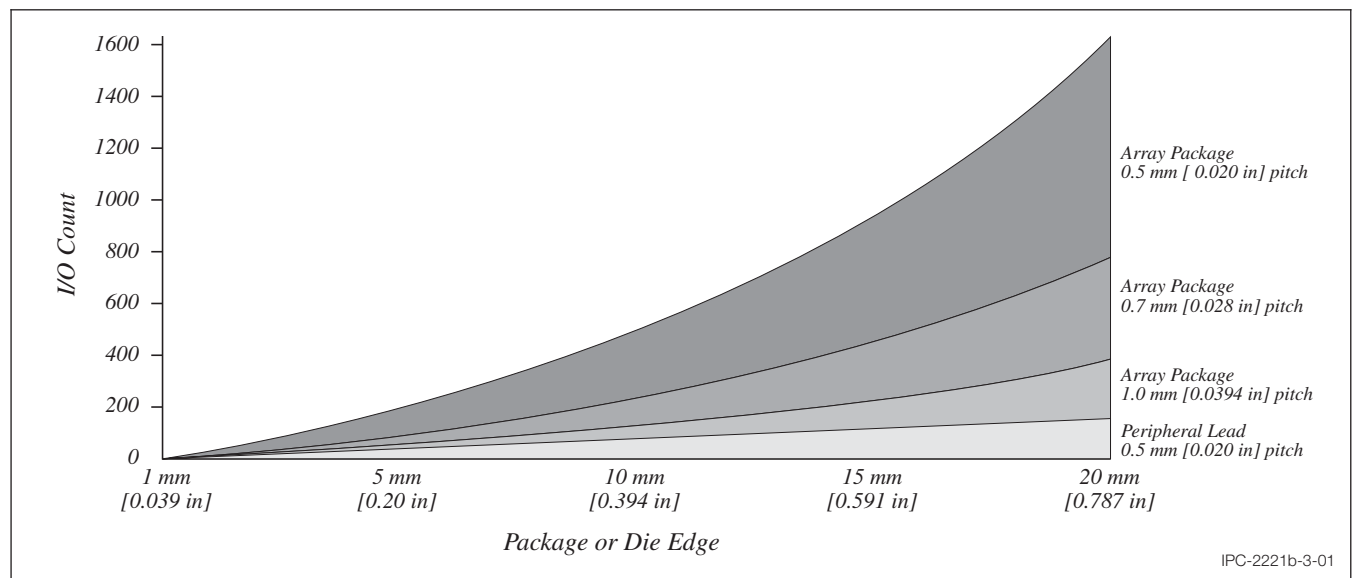


Figure 3-1 Package Size and I/O Count

3.5 Parts List A parts list, or bill of materials (BOM), is a tabulation of parts and materials used in the construction of a printed board assembly. All end item identifiable parts and materials **shall** be identified in the parts list or on the field of the drawing. Excluded are those materials used in the manufacturing process, but may include reference information; i.e., specifications pertinent to the manufacture of the assembly and reference to the schematic/logic diagram.

All mechanical parts appearing on the assembly pictorial **shall** be assigned an item number which **shall** match the item number assigned on the parts list.

Electrical components, such as capacitors, resistors, fuses, ICs, transistors, etc., **shall** be assigned reference designators, (Ex. C5, CR2, F1, R15, U2, etc.). Electrical reference designators **shall** match the assignments given to the same components on the Logic/schematic diagram.

It is advisable to group like items; e.g., resistors, capacitors, ICs, etc., in some sort of ascending or numerical order.

The parts list may be handwritten, manually typed on to a standard format, or computer generated.

3.6 Test Requirement Considerations Normally, prior to starting a design, a testability review meeting should be held with fabrication, assembly, and testing. Testability concerns, such as circuit visibility, density, operation, circuit controllability, partitioning, and special test requirements and specifications are discussed as a part of the test strategy. See Appendix C for an example of a testability design checklist.

During the design testability review meeting, tooling concepts are established, and determinations are made as to the most effective tool-cost versus printed board layout concept conditions. See 3.7.1 for layout recommendations relative to testability.

During the layout process, any printed board changes that impact the test program, or the test tooling, should immediately be reported to the proper individuals for determination as to the best compromise. The testing concept should develop approaches that can check the printed board for problems, and also detect fault locations wherever possible. The test concept and requirements should economically facilitate the detection, isolation, and correction of faults of the design verification, manufacturing, and field support of the printed board assembly life cycle.

3.6.1 Electrical

3.6.1.1 Bare Printed Board Testing When electrical testing is required it **shall** be specified in accordance with IPC-9252 including the assignment of a “Test Level” and including any user defined “AABUS” (As Agreed Between User and Supplier) test options. It is the responsibility of the user to define test requirements appropriate to the end use of the printed board. The selection of requirements should be carefully considered as these will at least in part determine the relative effectiveness of any test procedure. For example, electrical testing methods optimized for higher productivity may be less capable of detecting certain defects. The user is encouraged to discuss available test options with the supplier so that the appropriate requirements can be developed, which will provide the appropriate level of quality while allowing the greatest freedom in the supplier’s use of available tools.

User defined options may include the following:

- Isolation Test Voltage for “Resistive Testing” (Maximum rated voltage should be specified; if not specified, it will be 40 volts minimum, which may not be sufficient to detect leakage failures).
- Continuity Test Current for “Resistive Testing.”
- Horizontal Adjacency (AABUS for Class 3).
- Vertical Layer Adjacency (AABUS for all three Performance Classes).
- Indirect Isolation And Continuity Testing By “Signature Comparison” (AABUS for Class 3).
- “Hi-Pot” testing of dielectric integrity.
- Impedance testing of specialized circuitry.
- Embedded capacitance and or embedded resistance (test requirements for this technology are not covered by IPC-9252). Refer to IPC-2316 for guidance.

If test requirements are not otherwise defined IPC Performance Class 1, Class 2, and Class 3 **shall** be tested to default IPC-9252 Test Level A, Level B, and Level C respectively.

3.6.1.2 Test Methods The following electrical test methods are available or optional to the supplier in accordance with IPC-9252. Not all test methods have an equal potential for effectiveness. Because of the variations in equipment, training, and practice no method should be considered as “100-percent” effective.

- a) *Resistive Continuity Testing:* This type of test measures the resistance of the net under test. If the resistance is lower than the specified threshold, the network under test passes. If resistance is higher than the specified threshold, the network under test fails and an open is reported. Minimum test thresholds are in accordance with IPC-9252. The test current applied **shall not** exceed that allowed for the smallest conductor in that circuit and should be stated on the master drawing. Resistive Continuity Testing may be performed on a fix-grid or a fixtureless moving-probe (flying-probe) or moving grid test system.
- b) *Resistive Isolation Testing:* This type of testing verifies that electrically isolated networks meet the minimum resistive threshold. If the isolation resistance measured is higher than the minimum specified in IPC-9252, the network passes. Faults detected are defined as either shorts or leakages. Resistive Isolation Testing may be performed on a fix-grid or a fixtureless moving-probe (flying-probe) system. However, the use of a moving-probe test system for resistive isolation testing may be considered impractical unless the supplier is permitted to use one of the adjacency sorting protocols to increase productivity the details of which (including adjacency distance) should be developed between user and supplier.
- c) *Indirect Isolation & Continuity Testing by Signature Comparison:* This type of testing indirectly verifies electrical isolation and continuity by measuring and recording electrical properties (such as capacitance, RF, impedance, etc.) of a printed board under test and comparing them to a measured or calculated reference value which is capable of distinguishing between manufacturing and design faults. When faults by the indirect method are verified by the resistive method, they are classified as shorts, leakages, or opens. Otherwise network resistance values are not measured and should not be specified without exception where the intent is to allow the use of indirect testing. Indirect test methods are used with moving probe test systems running proprietary test software.
- d) *Insulation Resistance Test* This test is used to provide a quantifiable resistance value for all of a product’s insulation. A Direct Current (DC) test voltage is applied. The voltage and measured current value are used to calculate the resistance of the insulation.

3.6.1.2.1 HiPot Testing A HiPot test (also called a Dielectric Withstanding Voltage Test) verifies that the insulation of a product or component is sufficient to protect the hardware. In a typical HiPot test, high voltage is applied between a product’s current-carrying conductors and its metallic chassis. The resulting current that flows through the insulation, known as leakage current, is monitored by the HiPot tester. The theory behind the test is that if a deliberate over-application of test voltage does not cause the insulation to break down, the product will be safe to use under normal operating conditions. Three common high voltage tests include:

- Dielectric breakdown test (IPC-TM-650, Method 2.5.6) – The test voltage is increased until the dielectric fails, or breaks down, allowing too much current to flow. This test is performed on an Acceptable Quality Level (AQL) sample basis by the laminate material supplier. This test allows designers to determine the breakdown voltage of a product’s design. This value is often provided in the material supplier’s laminate specification sheet.
- Dielectric withstanding voltage (DWV) test (IPC-TM-650, Method 2.5.7) – A standard test voltage is applied (below the established Breakdown Voltage) for a specific length of time to determine any occurrence of flashover, spark over or breakdown. This test is routinely done on a monthly basis (see coupon “E” in 12.4.2).
- Dielectric withstanding voltage (IPC-TM-650, Method 2.5.7.2) – thin dielectric layers and planar capacitance layers - The test voltage, voltage ramp rate, hold time at peak voltage, and current threshold are pre-programmed into the HiPot tester. This test allows designers to determine the breakdown voltage of a product’s design. This value is often provided in the material supplier’s laminate specification sheet.

Note: Capacitance effect within the printed board may affect testing procedures.

The following are design considerations and documentation requirements for designs requiring high pot testing:

a. Design Considerations

- 1) Inadequate (current) creepage distance between holes (copper migration).
- 2) Inadequate clearance distances between conductive geometries in both the horizontal and vertical directions. Consideration should be given to laminate anomalies such as “eyebrow” cracks, which may affect the test result.
- 3) Solder mask or coating characteristics and thickness.
- 4) Dielectric characteristics.

b. Documentation requirements

- 1) Peak voltage desired. Typically user specified.
- 2) Specific circuit locations identified, if board testing is required.
- 3) Voltage ramp rate.
- 4) Hold time at peak voltage.
- 5) Sampling plan for testing.

3.6.1.2.2 Impedance Considerations

- Conductor width and spacing is determined by modeling electrical impedance values in conjunction with printed board layer stack-up using a reliable industry accepted impedance calculator. Due to material and fabrication process variations, fabricator calculations will provide more accurate results.
- Should differentiate conductors with impedance requirements from other conductors. As an example, if conductors are routed at 0.15 mm [0.006 in], the conductor width should be increased or decreased by 2.54 μm [100 μin]. This will make it easier for the printed board fabricator to identify which conductors to test.
- Each impedance controlled conductor should be identified with its associated reference plane(s).
- Avoid routing across any empty spaces in the reference layer.
- Testing per IPC-TM-650. Coupons may be specified for evaluation of impedance requirements.

The following are *examples* of sample notes for impedance considerations and are not requirements of this standard:

• XX. Impedance testing (IPC-TM-650, Method 2.5.5.7)

XX.1 Single ended: (Conductor widths [0.0059 in] on Layer X with respect to Layer Y)

*The printed board **shall** exhibit a characteristic impedance of 52.5 ohms ($\pm 15\%$) as measured using a Time Domain Reflectometer (TDR) which **shall** be verified by measurement of impedance coupons supplied by the fabricator.*

XX.2 Differential pairs: (Conductor widths [0.0059 in] on layer X with respect to Layer Y)

*The printed board **shall** exhibit a characteristic impedance of 105 ohms ($\pm 15\%$) as measured using a Time Domain Reflectometer (TDR) which **shall** be verified by measurement of impedance coupons supplied by the fabricator.*

- **ALL 0.023 in WIDE CONDUCTORS ON LAYER X ARE IMPEDANCE CONTROLLED (TYPE XXXXXXXX) TO XXX OHMS $\pm 10\%$ WITH RESPECT TO REFERENCE PLANE LAYERS Y AND Z. THE PRINTED BOARD MANUFACTURER HAS THE OPTION OF ADJUSTING THE DIELECTRIC MATERIAL THICKNESS AND THE CONDUCTOR WIDTH AS REQUIRED TO MEET THE IMPEDANCE REQUIREMENT. THE ADJUSTED CONDUCTOR WIDTH **SHALL NOT EXCEED A TOLERANCE OF ± 0.0015 in. THIS REQUIREMENT TAKES PRECEDENCE OVER OTHER CONDUCTOR WIDTH REQUIREMENTS. THE MANUFACTURER **SHALL** VERIFY IMPEDANCE REQUIREMENTS BY TIME DELAY REFLECTOMETRY (TDR) TEST ON MANUFACTURER SUPPLIED COUPON.****

3.6.1.3 Test Data (Source Data) The fabricator **shall** be provided with CAD Netlist data for use as electrical test source data. When Netlist data cannot be provided or is not available, Level C testing can be performed using CAM (Gerber) data. Certain test methods (e.g., adjacency, capacitance, etc.) require graphical circuitry data which may not be available within the CAM data. In this event, only the product of Gerber netlist extraction created by the supplier's proprietary software will be compatible.

3.6.2 Printed Board Assembly Testability Design of a printed board assembly for testability normally involves systems level testability issues. In most applications, there are system level fault isolation and recovery requirements such as mean time to repair, percent up time, operate through single faults, and maximum time to repair. To meet the contractual requirements, the system design may include testability features, and many times these same features can be used to increase testability at the printed board assembly level. The printed board assembly testability philosophy also needs to be compatible with the overall integrations, testing and maintenance plans for the contract. The factory testers to be used, how integration and test is planned, when printed board assemblies are conformal coated, the depot and field test equipment capabilities and personnel skill level are all factors that should be considered when developing the printed board assembly test strategy. The test philosophy may be different for different phases of the program. For example, the first unit debug philosophy may be much different than the test philosophy for spares when all the systems have already been shipped.

Before the printed board design starts, requirements for the system testability functions should be presented at the conceptual design review. These requirements and any derived requirements should be partitioned down to the various printed board assemblies and documented. The system and program level test criteria and how they are partitioned down to the printed board assembly requirements are beyond the scope of this document.

The two basic types of printed board assembly test are functional test and in-circuit test. Functional testing is used to test the electrical design functionality. Functional testers access the printed board under test through the connector, test points, or bed-of-nails. The printed board is functionally tested by applying pre-determined stimuli (vectors) at the printed board assembly's inputs while monitoring the printed board assembly outputs to ensure that the design responds properly.

In-circuit testing is used to find manufacturing defects in printed board assemblies. In-circuit testers access the printed board under test through the use of a bed-of-nails fixture which makes contact with each node on the printed board assembly. The printed board assembly is tested by exercising all the parts on the printed board individually. In-circuit testing places fewer restrictions on the design. Conformal coated printed board assemblies and many Surface Mount Technology (SMT) and mixed technology printed board assemblies present bed-of-nails physical access problems which may prohibit the use of in-circuit testing. Primary concerns for in-circuit test are that the lands or pins (1) should be on grid (for compatibility with the use of bed-of-nails fixture) and (2) should be accessible from the secondary side (a.k.a. noncomponent or solder side of through-hole technology printed boards) of the printed board assembly.

A Manufacturing Defects Analyzer (MDA) provides a low cost alternative to the traditional in-circuit tester. Like the in-circuit tester, the MDA examines the construction of the printed board assembly for defects. It performs a subset of the types of tests, mainly only tests for shorts and opens faults without power applied to the printed board assembly. For high volume production with highly controlled manufacturing processes (i.e., Statistical Process Control techniques), the MDA may have application as a viable part of a printed board assembly test strategy.

Vectorless Test is another low cost alternative to in-circuit testing. Vectorless Test performs testing for finding manufacturing process-related pin faults for SMT printed boards and does not require programming of test vectors. It is a powered-off measurement technique consisting of three basic types of tests:

- a. *Analog Junction Test* – DC current measurement test on unique pin pairs of the printed board assembly using the ESD protection diodes present on most digital and mixed signal device pins.
- b. *RF Induction Test* – Magnetic induction is used to test for device faults utilizing the printed board assembly's devices protection diodes. This technique uses chips power and ground pins to make measurements for finding solder opens on device signal paths, broken bond wires, and devices damaged by ESD. Parts incorrectly oriented can also be detected. Fixturing containing magnetic inducers are required for this type of test.
- c. *Capacitive Coupling Test* – This technique uses capacitive coupling to test for pin opens and does not rely on internal device circuitry but instead relies on the presence of the metallic lead frame of the device to test the pins. Connectors and sockets, lead frames and correct polarity of capacitors can be tested using the technique.

3.6.3 Boundary Scan Testing As printed board assemblies become more dense with fine pitch devices, physical access to printed board assembly nodes for in-circuit testing may not be possible. The boundary scan standard for integrated circuits (see the IEEE 1149 series of standards) provides the means to perform virtual in-circuit testing to alleviate this problem. Boundary scan architecture is a scan register approach where, at the cost of a few I/O pins and the use of special scan registers in strategic locations throughout the design, the test problem can be simplified to testing of simpler, mostly combinational circuits.

In many applications, the inclusion of scan registers on the inputs and outputs of the printed board assembly allows the printed board to be tested while installed. If the circuit is more complex, additional sets of scan registers can be included in the design to capture intermediate results and apply test vectors to exercise portions of the design.

A full description of the standard access port and boundary scan architecture can be found in the IEEE 1149 series of standards. The full test access port capabilities are not needed to gain significant testability via the scan registers.

The decision to use boundary scan test as part of a test strategy should consider the availability of boundary scan parts and the return on investment for capital equipment and software tools required for implementing this test technique. Boundary scan testing can be conducted using a low cost PC-based tester which requires access to the printed board assembly under test through the edge connector or an existing functional, in-circuit, or hybrid tester that may be adapted to perform boundary scan testing. The printed board interface (e.g., JTAG connector, etc.) can also be used to facilitate on-printed board programming of programmable memory devices.

3.6.4 Functional Test Concern for Printed Board Assemblies There are several concerns for designing the printed board assembly for functional testability. The use of test connectors, problems with initialization and synchronization, long counter chains, self diagnostics, and physical testing are topics which are discussed in detail in the following subsections and are not meant to be tutorials on testability but rather ideas of how to overcome typical functional testing problems.

3.6.4.1 Test Connectors Fault isolation on conformal coated printed boards or most SMT and mixed technology designs can be very difficult because of the lack of access to the circuitry on the printed board.

If strategic signals are brought out to a test connector or an area on the printed board where the signals can be probed (test points), fault isolation may be much improved. This lowers the cost of detection, isolation and correction.

It is also possible to design the circuit so that a test connector can be used to stimulate the circuit (such as taking over a data bus via the test connector) or disable functions on the printed board assembly (such as disabling a free running oscillator and adding single step capability via the test connector).

3.6.4.2 Initialization and Synchronization Some designs or portions of a design do not need any initialization circuitry because the circuit will quickly cycle into its intended function. Unfortunately, it is sometimes very difficult to synchronize the tester with this type of circuit because the tester would need to be programmed to stimulate the circuit until a predetermined signature is found on the outputs of the circuit. This can be difficult to achieve.

With relatively little difference in the design, initialization capability can usually be designed into the circuitry allowing the printed board assembly to be quickly initialized and the circuit and the tester can follow the expected outputs of the printed board assembly.

Free running oscillators also present a problem in testing because of the synchronization problem with the test equipment. These problems can be overcome by (1) adding test circuitry to select a test clock instead of the oscillator; (2) removing the oscillator for test and injecting a test clock; (3) overriding the signal; or (4) designing the clock system so that the clocking can be controlled via a test connector or test points.

3.6.4.3 Long Counter Chains Long counter chains in the design with signals used from many stages of the counter chain present another testability problem. Testability can be very bad if there is no means to preset the counter chain to different values to facilitate testing of the logic that is driven from the high order stages of the counter chain.

Testability is much improved if the counter chain is either broken into smaller counter chains (perhaps no more than 10 stages) which can be individually controlled or if the counter chain can be loaded via the test software. The test software can then verify the operation of the logic that is driven from the counter stages without wasting the simulation and test time that would be required to clock through the complete counter chain.

3.6.4.4 Self Diagnostics Self diagnostics are sometimes imposed either contractually or via derived requirements. Careful consideration should be given to determine how to implement these requirements.

Many times a printed board assembly does not contain functions that lend themselves to self diagnostics at the printed board assembly level but a small group of printed board assemblies, when taken as a unit, do lend themselves to good diagnostics. For example, a complex Fast Fourier Transform (FFT) function may be spread across multiple printed board assemblies. It may be very difficult for any one printed board assembly to self diagnose a problem but it may be very easy to design-in circuitry that self diagnoses the whole FFT function.

The depth of self diagnostics that are needed is usually driven by the line replaceable unit (LRU) which varies with requirements. It may be an integrated circuit or it may be a drawer of electronics depending on the contract, the function of the design, or the system level maintenance philosophy.

For self diagnostics at a printed board assembly level, the printed board assembly is usually put into a test mode and then the printed board assembly applies a known set of test inputs and compares the results with a stored set of expected responses. If the results do not match the expected responses, the printed board assembly signals the test equipment indicating the printed board assembly failed the self-test. There are many variations on this scheme. Some examples are:

- The printed board assembly is placed in a feedback loop with the results checked after a predetermined number of cycles.
- A special test circuit or the Central Processor Unit (CPU) applying the stimuli and comparing the signature of the responses against a known pattern.
- The printed board assembly performing self-checks when idling and then supplying the results to another (or diagnostic) printed board assembly for verification of the responses, etc.



3.6.4.5 Physical Test Concerns Printed board assembly functional test equipment is usually very expensive and requires highly skilled personnel to operate. If printed board assembly testability is poor, the printed board assembly test operation can be very expensive. There are some simple physical considerations that can decrease the debug time and therefore the overall test costs.

The orientation of polarized parts should be consistent so that the operator does not get confused with parts being oriented 180° out of phase with other parts on the printed board assembly. Nonpolarized parts still need to have the pin #1 identified so that the test operator knows which end to probe when guided probe software says to probe a specific pin.

Test connectors are much preferred over test points which require the use of test clips or test hook-up wires. However, test points such as riser leads are preferred over clipping on to the lead of a part. If riser leads are used for temporary testing, such as determining a select-by-test resistor, it is suggested that the risers remain after the installation of the selected component. This allows verification of the selected item without re-fixturing the assembly.

Signals that are not accessible for probing (such as can happen with leadless parts) can greatly increase fault isolation problems. If scan registers are not used, it is recommended that every signal have a land or other test point somewhere on the printed board assembly where the signal can be probed. It is also recommended that lands used for test points be located on grid and placed so that all the probing can be done from the secondary side of the printed board assembly. If it is not feasible to provide capability for probing every signal, then (1) only the strategic signals should have special probing locations and (2) the test vectors need to be increased or other test techniques need to be utilized to assign fault isolation to one component or a small set of components.

Many faults are often due to shorts between the leads of adjacent parts, shorts between a part lead and an external layer conductor on the printed board or shorts between two printed board conductors on the external layers of the printed board. The physical design should consider these normal manufacturing defects and not impair the isolation of the faults due to lack of access or inconvenient access to signals. As with design for in-circuit testability, probe land test points should be on grid to allow automated probing to be used in the future.

Partitioning of the design into functions, perhaps digital separated from analog, is sometimes required for electrical performance. Testing concerns also are helped with physical separation of dissimilar functions. Separation of not just the circuitry but also the test connectors or at least grouping the pins on the connectors can help improve testability. Designs that mix digital design with high performance analog design may require testing on two or more sets of test equipment. Separating the signals will not only help the test fixturing but will help the operator in debugging the printed board assembly.

As with in-circuit test fixturing, functional test fixturing can have a significant cost impact. Normally a standard printed board size or only a few printed board sizes are used for all designs on a program. Similarly one, or at most a few, test fixtures are typically used for a program. Generating test fixtures can be costly and debugging noise problems in the fixtures or tuning the fixtures to the tester can be expensive. If the test fixturing is not adequately engineered, it may not be possible to accurately measure the printed board under test. Typically much effort is expended in generating a few test fixtures and it is expected that the fixtures will be used for all the printed board assembly designs. Therefore the test fixturing restrictions **shall** be considered in the printed board assembly design. The fixturing restraints can be significant. Such as (1) requiring ground and voltage supplies on specific connector pins, (2) limiting which pins can be used for high speed signals, (3) limiting which pins can be used for low noise applications, (4) defining power switching limitations, (5) defining voltage and current limitations on each pin, etc.

3.6.5 In-Circuit Test Concerns for Printed Board Assemblies In-circuit testing is used to find shorts, opens, wrong parts, reversed parts, bad devices, incorrect assembly of printed board assemblies and other manufacturing defects. In-circuit testing is neither meant to find marginal parts nor to verify critical timing parameters or other electrical design functions.

In-circuit testing of digital printed board assemblies can involve a process that is known as backdriving (see IPC-T-50). Backdriving can also cause devices to oscillate and the tester can have insufficient drive to bring a device out of saturation. Backdriving can be performed only for controlled periods of time, or the junction of the device (with the overdriven output) will overheat.

The two main concerns for designing the printed board and printed board assembly for in-circuit testability are design for compatibility with in-circuit test fixturing and electrical design considerations. These topics are discussed in detail in the following subsections.

3.6.5.1 In-Circuit Test Fixtures In-circuit test fixtures are commonly called bed-of-nails fixtures. A bed-of-nails fixture is a device with spring contact probes which contact each node on the printed board under test. The following guidelines should be followed during printed board assembly layout to promote in-circuit testability in bed-of-nails fixtures.

- a. The diameter of lands of plated-through holes (PTHs) and vias used as test lands are a function of the hole size (see 9.1.1). The diameter of test lands used specifically for probing should be no smaller than 0.9 mm [0.0354 in]. It is feasible to use 0.6 mm [0.0236 in] diameter test lands on printed boards under 7700 mm² [11.935 in²].
- b. Clearances around test probe sites are dependent on assembly processes. Probe sites should maintain a clearance equal to 80% of an adjacent component height with a minimum of 0.6 mm [0.0236 in] and a maximum of 5.0 mm [0.20 in] (see Figure 3-2).
- c. Part height on the probe side of the printed board should not exceed 5.7 mm [0.224 in]. Taller parts on this side of the printed board will require cutouts in the test fixture. Test lands should be located 5.0 mm [0.20 in] away from tall components. This allows for test fixture profiling tolerances during test fixture fabrication (see Figure 3-3).
- d. No parts or test lands should be located within 3.0 mm [0.118 in] of the printed board edges.
- e. All probe areas should be solder coated or covered with a conductive nonoxidizing coating. The test lands should be free of solder mask and markings.
- f. Probe the test lands or vias, not the termination/castellations of leadless surface mount parts or the leads of leaded parts (see Figure 3-4). Contact pressure can cause an open circuit or make a cold solder joint appear good.
- g. Avoid requiring probing of both sides of the printed board. Use vias, to bring test points to one side, the bottom side (noncomponent or solder side of through-hole technology printed board assemblies) of the printed board. This allows for a reliable and less expensive fixture.
- h. Test lands should be on 2.5 mm [0.0984 in] hole centers, if possible, to allow the use of standard probes and a more reliable fixture.
- i. Do not rely on edge connector fingers for test lands. Gold plated fingers are easily damaged by test probes.
- j. Distribute the test lands evenly over the printed board area. When the test lands are not evenly distributed or when they are concentrated in one area, the results are printed board flexing, probing faults, and vacuum sealing problems.
- k. A test land should be provided for all nodes. A node is defined as an electrical connection between two or more components. A test land requires a signal name (node signal name), the x-y position axis in respect to the printed board datum point, and a location (describing which side of the printed board the test land is located). This data is required to build a fixture for SMT and mixed technology printed board assemblies. The quantity of required test lands may be reduced when Boundary Scan test is used.
- l. Mixed technology printed board assemblies and pin grid component printed boards provide test access for some nodes at the solder side pins. Pins and vias used at test lands should be identified with node signal name and X-Y position in reference to the printed board datum point. Use solder mount lands of parts and connectors as test points to reduce the number of generated test lands.

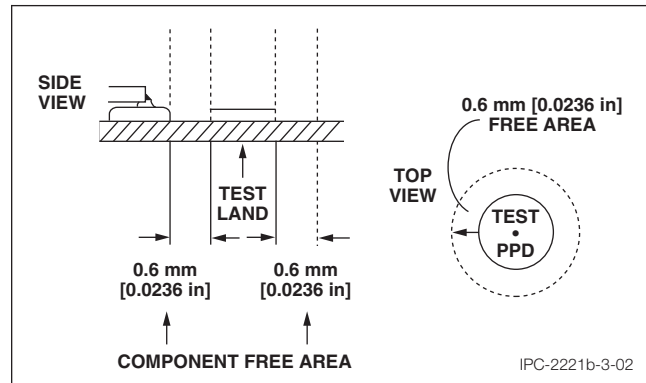


Figure 3-2 Test Land Free Area for Parts and Other Intrusions

Note 1. PPD is short for "Probe Point Diameter"

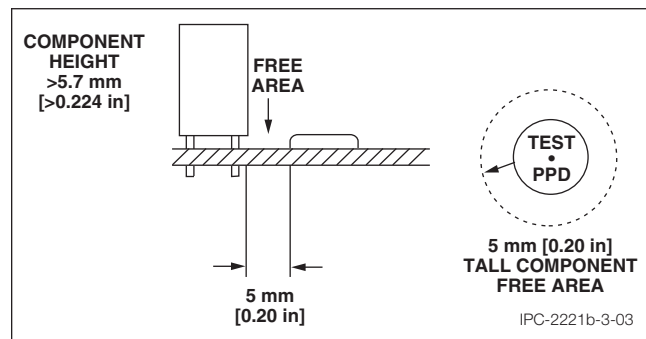


Figure 3-3 Test Land Free Area for Tall Parts

Note 1. PPD is short for "Probe Point Diameter"

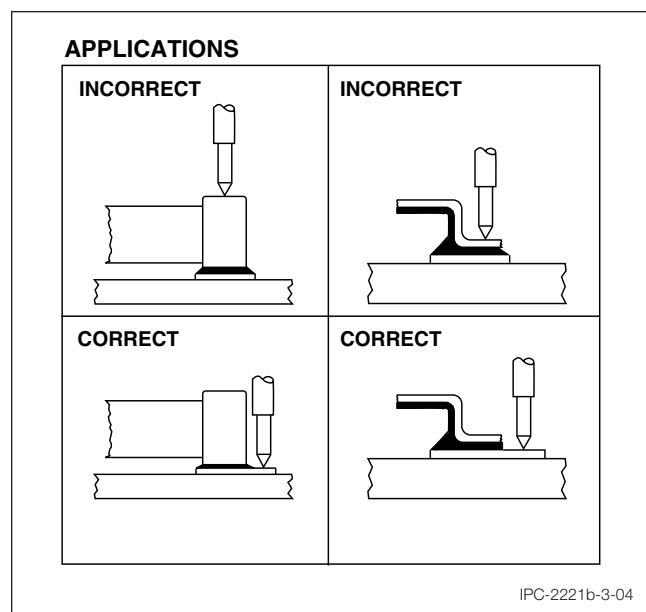


Figure 3-4 Probing Test Lands

3.6.5.2 In-Circuit Test Electrical Considerations The following electrical considerations should be followed during printed board assembly layout to promote in-circuit testability:

- a. Do not wire control line pins directly to ground, V_{cc} , or a common resistor. Disabled control lines on a device can make it impossible to use the standard in-circuit library tests. A specialized test with reduced fault coverage and higher program cost is the normal result.
- b. A single input vector for tri-stating a device's outputs is preferable for in-circuit testing. Reasons for tri-statable outputs are (1) testers have a limited amount of vectors, (2) the backdrive problems will disappear, and (3) it simplifies the generation of test programs. An example of this which would reduce program cost is tri-statable Programmable Array Logic (PAL) outputs. Use a spare input to a pull-up resistor plus an equation that would enable a normal function in a high state and the device outputs to be tri-stated in a low state.
- c. Gate arrays and devices with high pin counts are not testable using an in-circuit tester. Backdrive may not be a problem per pin but the large numbers of pins limit backdrive restrictions. A control line or a single vector to tri-state all device outputs is recommended.
- d. Node access and the inability to cover all nodes using standard in-circuit testers is a growing problem. If standard test techniques cannot be applied to detect surface mounted part faults, an alternative method should be developed.

Alternative test strategies **shall** be developed for SMT printed board assemblies with limited nodes. An example of this is a test that will partition the printed board into groups of clustering components. Each group should have control lines (for testability) and test lands to electrically isolate the cluster from the other devices or groups during test.

Another alternative test method for opens, shorts, and correct devices is boundary scan. This built-in-test-circuitry (electronic bed-of-nails) is gaining momentum in the surface mount printed board assembly area. See the IEEE Standard 1149 series of specifications for more information on boundary scan.

3.6.6 Mechanical

3.6.6.1 Uniformity of Connectors Test fixtures are most often designed for automatic or semiautomatic engagement of edge type or on-printed board connectors. Connectors should be positioned to facilitate quick engagement and should be uniform and consistent (standardized) in their relationships to the printed board from one design to another. Similar types of connectors should be keyed, or printed board geometry used, to ensure proper mating, and prevent electrical damage to the circuitry.

3.6.6.2 Uniformity of Power Distribution Arrangement and Signal Levels on Connectors The connector contact position should be uniform for AC and DC power levels, DC common and chassis ground, e.g., contact number 1 is always connected to the same relative circuit power point in each printed board design. Standardizing contact positions will minimize test fixture cost and facilitate diagnostics.

Signals of widely different magnitude should be isolated to minimize crosstalk.

Logic levels should be located in pre-designated connector contacts.

3.7 Layout Evaluation

3.7.1 Printed Board Layout Design The design layout should be such that designated areas are identified by function, e.g., power supply section confined to one area, analog circuits to another section, and logic circuits to another, etc. This will help to minimize crosstalk, simplify bare printed board and assembly test fixture design, and facilitate troubleshooting diagnostics. In addition, the design should:

- Ensure that components have all testable points accessible from the secondary side of the printed board to facilitate probing with single-sided test fixtures.
- Have vias and component holes placed away from printed board edges to allow adequate test fixture clearance.
- Require the printed board be laid out on a grid which matches the design team testing concept.
- Allow provision for isolating parts of the circuit to facilitate testing and diagnostics.
- Test points that will be used for manual testing should be placed for ease of accessibility.
- The use of sockets may reduce overall reliability and result in socket related issues such as intermittent circuits, spread socket contacts, etc. Therefore, the potential risk for use of sockets needs to be carefully considered.

- Provide optic targets (fiducials) for surface mount designs to allow the use of optic positioning and visual inspection equipment and methods (see 5.4.3).

Surface mounted components and their patterns require special consideration for test probe access, especially if components are mounted on both sides of the printed board and have very high lead counts.

3.7.1.1 Layout Concepts The printed board layout depicts the physical size and location of all electronic and mechanical components, and the routing of conductors that electrically interconnect the components in sufficient detail to allow the preparation of documentation and artwork.

3.7.2 Feasibility Density Evaluation After approved documents for schematic/logic diagrams, parts lists, and end-product and testing requirements are provided, and before the actual drawing of the layout is begun, a feasibility density evaluation should be made. This should be based on the maximum size of all parts required by the parts list and the total space they and their lands will require on the printed board, exclusive of interconnection conductor routing.

The total printed board geometry required for this mounting and termination of the components should then be compared to the total usable printed board area for this purpose. Reasonable maximum values for this ratio are 70% for Level A, 80% for Level B, and 90% for Level C. Component density values higher than these will be a cause for concern. The lower these values are, the easier it will be to design a cost-effective functional printed board.

Figure 3-5 provides the usable printed board area for the standardized printed board sizes.

Printed Board Size (Fig. 5-1)	Overall Dimensions		Usable Dimensions		Usable Area		
	Height mm [in]	Width mm [in]	Length mm [in]	Width mm [in]	mm ²	Grid Elements 0.5 mm Grid	cm ²
A1	80 [3.15]	60 [2.36]					
B1	170 [6.692]						
C1	260 [10.25]						
D1	350 [13.78]						
A2	80 [3.15]	120 [4.724]					
B2	170 [6.692]						
C2	260 [10.25]						
D2	350 [13.78]						
A3	80 [3.15]	180 [7.087]					
B3	170 [6.692]						
C3	260 [10.25]						
D3	350 [13.78]						
A4	80 [3.15]	240 [9.449]					
B4	170 [6.692]						
C4	260 [10.25]						
D4	350 [13.78]						

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Figure 3-5 Example of Usable Area Calculation, mm [in] (Usable area determination includes clearance allowance for edge printed board connector area, printed board guides, and printed board extractor.)

Table 3-2 gives the area (in 0.5 mm [0.020 in] grid elements) a component will occupy on the printed board for a variety of components. As an example, the 14 lead dual in-line package for through-hole technology occupies a total of 84.0 grid elements. The package outline that encloses the component and land pattern has a grid matrix of 20 x 42 grid elements on 0.5 mm [0.020] centers. The 20 grid elements establish an outline dimension of 10.0 mm [0.394 in] while the 42 grid elements account for 21.0 mm [0.827 in]. This component area would use up a portion of the printed board usable area. The component outline does not include grid elements for conductor routing outside the land area. Total component area compared to total usable area provides the conductor routing availability and thus the density percentage.

Table 3-2 Component Grid Areas

Component Description	Type ¹	Number of Grid Elements ² 0.5 mm [0.020 in] Grid	
D07 (without stress relief loop)	THT	6 x 24	144
D07 (with stress relief loop)	THT	6 x 28	168
T05	THT	20 x 20	400
T024	THT	10 x 10	100
CK05	THT	6 x 12	72
CM05, 13000pF	THT	20 x 44	880
CM06, 400pF	THT	12 x 26	312
RC07	THT	6 x 20	120
RC20	THT	10 x 26	260
RN60	THT	10 x 30	300
CQFP-10 T090	SMT	16 x 12	192
CQFP-28	SMT	34 x 34	1156
CQFP-144	SMT	68 x 68	4624
3216 (1206)	SMT	4 x 10	40
4564 (1825)	SMT	14 x 12	168
6032	SMT	8 x 18	144
DIP-14	THT	20 x 42	840
DIP-14	SMT	22 x 42	924
DIP-24	SMT	22 x 60	1320
DIP-24L	SMT	26 x 64	1664
SOD87/MLL-41	SMT	6 x 14	84
SOT23	SMT	8 x 8	64
SOT89	SMT	12 x 10	120
SOT143	SMT	8 x 8	64
SQFP 7x7-40	SMT	22 x 22	484
SOIC-20W	SMT	28 x 24	672
SOIC-36X	SMT	48 x 24	1152
TSOP 10x20	SMT	22 x 44	968
SOJ 26/350	SMT	24 x 34	816

¹THT = Through-Hole Technology, SMT = Surface Mount Technology

²Grid area includes physical component outlines and land areas. It does not include space for conductor routing.

An alternative method of feasibility density evaluation expresses printed board density in units of square centimeters per equivalent SOIC. A 16-pin SOIC occupies approximately one cm² of printed board area. Figure 3-6 shows a table for determining the SOIC equivalent for a variety of components and the total SOIC equivalents used on the printed board. This number is then divided into the total square centimeters of usable printed board area. Reasonable maximum density values are 0.55 cm² per SOIC for Level A, 0.50 for Level B, and 0.45 for Level C. Density values can increase with additional circuit layers. Also, when using surface mount technology, the potential usable printed board area is theoretically doubled.

PRINTED BOARD DENSITY EVALUATION			Date of issue	No. Revised
DESCRIPTION: SOICs per square centimeter				
Comp. Name	# of comp.	or	IC equiv	Comments
8 SOIC		.50		
14 SOIC		1.00		
16 SOIC		1.00		
16L SOIC		1.00		
20 SOIC		1.25		
24 SOIC		1.50		
18 PLCC		1.13		
18L PLCC		1.13		
20 PLCC		1.25		
28 PLCC		1.75		
44 PLCC		2.75		
SOT 23		0.19		
SOT 89		0.19		
SOMC 1401		1.00		
SOMC 1601		1.00		
2012 (0805)		0.13		
3216 (1206)		0.13		
3225 (1210)		0.13		
4564 (1812)		0.13		
Others (specify)				
Total IC equivalent _____				
Total Printed Board Area	(X)	=	cm ² cm ²	
Usable Printed Board Area	(X)	=	Usable Printed Board Area Design C~riteria	
			☐ Analog	☐ Digital
			Etch & Spac.	/
			PWB & GYD Sz	/
Devel. by		Date	App'd by	Date

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Figure 3-6 Printed Board Density Evaluation

4 MATERIALS

4.1 Material Selection A designer of printed boards has several material choices to consider, ranging from standard to highly sophisticated and specialized. When specifying materials, the designer first determines what requirements the printed board needs to meet. These requirements include temperature (soldering and operating), electrical properties, interconnections (soldered components, connectors), structural strength, and circuit density. It should be noted that increased levels of sophistication may lead to increased material and processing costs.

When constructing a composite from materials with different temperature characteristics, the maximum end-use temperature allowable **shall** be limited to that of the lowest rated material.

Other items that may be important in the comparison of various materials include:

- Resin Formula
- Flame Resistance
- Thermal Stability
- Structural Strength
- Electrical Properties
- Flexural Strength
- Maximum Continuous Safe Operating Temperature
- Glass Transition Temperature (T_g)
- Reinforcing Sheet Material
- Nonstandard Sizes and Tolerances
- Machinability or Punchability
- Coefficients of Thermal Expansion (CTE)
- Dimensional Stability
- Overall Thickness Tolerances
- Temperature of Decomposition (T_d)

4.1.1 Material Selection for Structural Strength The first design step in the selection of a laminate is to thoroughly define the service requirements that need to be met, i.e., environment, vibration, “G” force, shock (impact), physical and electrical requirements.

The choice of laminate should be made from standard materials to avoid costly and time consuming proof-out tasks. Several laminates may be candidates, and the choice should be optimized to obtain the best balance of properties.

Materials should be easily available in the form and size required. Special laminate may be costly, and have long lead times. Special laminates should be analyzed against all of the parameters discussed in this section.

Items to be considered are such things as machining, processing, processing costs, and the overall specification of the raw material.

In addition to these parameters, the structural strength of the printed board should be able to withstand the assembly and operational stresses.

4.1.2 Material Selection for Electrical Properties Some of the critical properties to consider are electrical strength, dielectric constant, moisture resistance, and hydrolytic stability. Table 4-1 lists properties of some of the more common systems. Consult the laminate manufacturer utilized by the fabricator for specific values.

4.1.3 Material Selection for Environmental Properties Table 4-1 shows the properties affected by the environment for some of the more common resin systems. The stated values are typical and will vary among different material suppliers. Consult the laminate manufacturer utilized by the fabricator for specific values.

4.2 Dielectric Base Materials (Including Prepregs and Adhesives) Bonding materials described in the following paragraphs **shall** be used to bond layers of copper foil, bare laminate, copper clad laminate or heat-sinking plates and conductors.

4.2.1 Preimpregnated Bonding Layer (Prepreg) Prepreg **shall** conform to the types listed in IPC-4101 or UL 746E. In most cases, the prepreg should be of the same resin and reinforcement type as the copper clad laminate. The reinforcement style, nominal resin flow, nominal scaled flow thickness, nominal gel time, and nominal resin content are process parameters normally dictated by the printed board manufacturing process.

Unless design constraints dictate, these values **shall not** be included on master drawings, but **shall** only be specified and used in procurement specifications by the printed board manufacturer.

4.2.2 Adhesives Adhesives used in printed board assemblies are drawn from at least five basic resin types covering a wide range of properties. In addition to adhesion quality or bond strength, criteria for adhesive selection include hardness, CTE, service temperature range, dielectric strength, cure conditions and tendency for outgassing. In some cases structural adhesives may be sufficient for thermal bonding applications, see 4.2.5. Each adhesive type has both strong and weak points.

Selection of a resin system for an adhesive or encapsulant is to be based on the characteristics of the materials being bonded and their compatibility. Special treatments, such as primers or activators, may be required to suitably activate surfaces for bonding. The selection process should also consider the exact purpose of the adhesive bond and its use environment. Fungus inert materials are also a consideration. Not all adhesives are suitable for direct application on or near electronic products due to either their chemical or dielectric properties. Incorrect selection of materials may result in product degradation or failure.

In actual application, most adhesive needs can be addressed by a few carefully selected materials. Storage and shelf life limitations apply to most of these materials.

4.2.2.1 Epoxies Epoxy resin formulations are among the most versatile adhesives for electrical insulating and mechanical bonding applications. They offer a wide range of physical and electrical properties, including adhesive and cohesive strengths, hardness, chemical resistance, thermal conductivity and thermal vacuum stability. They are also available with a wide range of cure methods and times. A thorough review of the material is warranted, based on its intended use. Thermal coefficient of expansion and glass transition temperatures should be considered, in addition to other properties, to preclude problems. Epoxies are available with a variety of modifiers, fillers and reinforcements for specific applications and extended temperature ranges.

4.2.2.2 Silicone Elastomers Silicone elastomers are generally noted for being resilient materials with very good electrical and mechanical properties at ambient and extreme temperatures. Several curing methods are available, including moisture, metallic salts and others. Silicone elastomers which evolve acetic acid during their cure should be avoided in electronic applications. Bond strength, tensile strength, and hardness properties tend to be considerably lower than epoxies. Silicones will swell and dissolve with prolonged exposure to some chemicals. Some of the metallic salts curing silicones will react with TFE and PTFE materials. Conformal coatings other than silicones generally will not adhere to cured silicone materials. Silicones are often used as a cushioning overcoat for articles which will be encased in hard potting compounds later.

A number of high purity grades of silicones are available which offer good thermal vacuum stability. Silicone gels are also available, which offer enhanced properties as encapsulants. These materials generally require physical restraint, such as a potting cup or enclosure to maintain their form, once applied.

4.2.2.3 Acrylics Acrylic resins generally provide rapid cures, good electrical and adhesive properties and hardness. Chemical resistance and thermal vacuum stability tend to be considerably lower than the epoxies. The glass transition temperature of these materials also tends to be low.

4.2.2.4 Polyurethanes Polyurethanes are available in almost as many variations as the epoxies. These materials generally offer toughness, high elasticity, a wide range of hardness, and good adhesion. Some of the urethane compounds are outstanding as vibration and shock damping materials. Moisture and chemical resistance is relatively high, but varies with the individual product. Thermal vacuum stability will also vary by the individual product formulation. Many of the urethanes can be used in a relatively thick application as a local vibration damping compound.

4.2.2.5 Specialized Acrylate-Based Adhesives This category includes the cyanoacrylates (instant cure) and anaerobic adhesives (cure without air). The cyanoacrylates form strong bonds within seconds without catalysts when only a trace amount of moisture is present on a surface. The anaerobic adhesives cure in the absence of oxygen when a peroxide additive can be decomposed by certain transition metal ions. Both adhesive types can give high initial bond strengths.

Table 4-1 Typical Properties of Common Dielectric Materials¹

Property	Material						
	Difunctional/ Multifunctional Epoxy (IPC-4101/21)	Epoxy/Multi- functional Epoxy (IPC-4101/24)	Epoxy/Multi- functional Epoxy (IPC-4101/26)	Epoxy Triazine (IPC-4101/29)	Bismaleimide Triazine Epoxy (IPC-4101/30)	Polyimide E-glass (IPC-4101/41)	Polyimide Nonwoven Aramid (IPC-4101/53) ²
Electric Strength ² (kV/mm)	47	50	53	47	46	51	51
Moisture Absorption (wt%)	0.17	0.15	0.15	0.1	0.15	0.44	0.6
Dissipation Factor (Loss Tangent) @1 MHz	0.022	0.022	0.021	0.008	0.011	0.012	0.015
Thermal Expansion xy-plane (ppm/°C)	12-16	12-16	11-16	10-14	10-15	12-17	6-9
Thermal Expansion z-axis below T _g ⁵ (ppm/°C)	50-80	50-55	50-55	—	55-70	40-60	80-90
Glass Transition Temp. T _g (°C) (IPC-4101)	110 - 150	150 - 200	170 - 220	170 - 220	170 - 220	200- 250	220 minimum
Glass Transition Temp. T _g (°C) (DSC)	140	170-175	175 - 180	210	185-200	250 - 260	240
Flexural Modulus (Pa)	Fill ³ Warp ⁴	1.86 x 10 ¹⁰ 1.20 x 10 ¹⁰	1.93 x 10 ¹⁰ 2.20 x 10 ¹⁰	1.93 x 10 ¹⁰ 2.20 x 10 ¹⁰	2.07 x 10 ¹⁰ 2.41 x 10 ¹⁰	2.69 x 10 ¹⁰ 2.89 x 10 ¹⁰	4.8 x 10 ⁸
Tensile Strength (Pa)	Fill ³ Warp ⁴	4.13 x 10 ¹⁰ 4.82 x 10 ¹⁰	4.13 x 10 ¹⁰ 5.24 x 10 ¹⁰	4.13 x 10 ¹⁰ 5.24 x 10 ¹⁰	3.93 x 10 ¹⁰ 4.27 x 10 ¹⁰	4.82 x 10 ¹⁰ 5.51 x 10 ¹⁰	3.14 x 10 ⁷

Note 1. For values of dielectric constant, see Table 6-2.

Note 2. The stated electrical strength values are commonly evaluated under test conditions with a 0.125 mm [0.00492 in] core laminate thickness. These values should not be considered linear for high voltage designs with a minimum dielectric separation, i.e., less than 0.09 mm [0.00354 in].

Note 3. Fill-yarns that are woven in a crosswise direction of the fabric.

Note 4. Warp (cloth)-yarns that are woven in the lengthwise direction of the fabric.

Note 5. Z-axis expansion above T_g can be as much as four times greater. For FR-4 it is 240-390 ppm. Contact supplier for specific values of the other materials.

Note 6. Values for fill and warp do not apply for a random fiber.

be beneficial for wire staking and temporary bonding applications. The instant cure adhesives generally have poor impact resistance and are susceptible to degradation from exposure to moisture and temperatures over 82 °C [179.6 °F]. The anaerobic adhesives have the capability of withstanding higher temperatures but can lose strength with prolonged exposure to chemicals.

4.2.2.6 Other Adhesives Many other types and forms of adhesives are available, including polyesters, polyamides, polyimides, rubber resins, vinyl, hot melts, pressure sensitive, etc. Where they are used is determined by the needs of the design and its performance requirements. Selection of specialized items, such as chip bond adhesives, should be done in conjunction with the using facility, in order to ensure full compatibility of the equipment and process.

4.2.3 Adhesive Films or Sheets Adhesive films or sheets used for bonding heatsinks, stiffeners, etc., or as insulators, are generally in accordance with IPC-4203 or IPC-4101.

Film type adhesives find many uses in laminated structures. The ability to pre-cut a film adhesive to fit given shapes or dimensions is a distinct advantage in the fabrication of some laminated parts. Epoxy based film adhesives provide very good bond strength but require elevated temperature cure. Film adhesives are commonly used to bond printed board heatsinks to printed boards.

Through-hole technology (THT) printed boards and heatsinks may be bonded together with a dry epoxy sheet adhesive to improve heat transfer or resist vibration. These adhesives consist of an epoxy impregnated glass cloth which is cut to the heatsink configuration, assembled between printed board and heatsink, then cured with heat and pressure. The cured adhesive is strong and resists vibration, temperature extremes, and solvents. Thicknesses of 0.1 mm [0.0039 in] should be adequate for most applications. If necessary, specify two sheets.

4.2.4 Electrically Conductive Adhesives This class of adhesives consists, generally, of a conductive filler, such as graphite (carbon) or silver, embedded in a polymeric resin adhesive system, which is loaded into the material to achieve conductivity. Volume resistivity, a measure of the electrically conductive property of the material, may be varied over a range of values consistent with the intended application. This is accomplished by the type of filler used and the loading. Bonding strength of these materials can be compromised by the filler material.

Epoxies, silicone elastomers and urethanes are the resin systems commonly used to formulate conductive adhesives. The strongest bonds are generally achieved with conductive epoxy. Silicone elastomers follow, with urethanes a close third. Cure conditions and filler content have a pronounced effect upon tensile strength of these materials. The choice of conductive adhesive for a particular application should consider the strength of bond, the service temperature, the effect of CTE on the bond and the volume resistivity or conductivity required.

4.2.5 Thermally Conductive/Electrically Insulating Adhesives Thermally conductive adhesives are filled versions of epoxy, silicone, urethane and some acrylic base materials. The filler is normally dried aluminum oxide or magnesium oxide powder.

4.2.5.1 Epoxies The epoxies offer the greatest bond strength and best solvent resistance, along with good thermal conductivity and electrical resistance. As with most two part systems, the choice of catalyst has an impact on cure conditions and ultimately could affect the glass transition temperature, since it is somewhat dependent upon cure conditions.

4.2.5.2 Silicone Elastomers The silicone elastomers are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy and are two part systems with other variable properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

Silicone elastomers may be obtained as humidity curing or heat curing, the latter offering accelerated cure with applied heat. They cure well in contact with most materials except butyl and chlorinated rubbers, some RTV silicone elastomers and residues of some curing agents. Some bonding applications may require a primer.

4.2.5.3 Urethanes Urethanes can be varied through a wide range of hardness, tensile and electrical properties by varying the proportions of curing agent to resin. Consistency can be varied from a soft, rubbery state to a hard, rigid condition by this method. The latitude for formulation optimization over a range of application conditions is an advantage offered by the filled urethanes.

The urethanes are characterized by relatively low bond strengths and less rigidity (lower hardness) than epoxies. They are less resistant to solvent attack than epoxy; are two part systems with variable other properties dependent upon formulation. Thermal conductivity and electrical resistance properties are good.

4.2.5.4 Use of Structural Adhesives as Thermal Adhesives In design circumstances where thermal conduction properties are not critical, the use of structural adhesives (see 4.2.2) in place of thermal adhesives may be acceptable as determined by thermal analysis and may be a more cost effective alternative.

4.3 Laminate Materials Laminate materials **shall** be selected from material listed in IPC-4101, IPC-4103 or IPC-4202, as applicable.

When the Underwriters Laboratories Inc. (UL) recognized component mark is required, the designer should ensure that the specified laminate is certified to the required flammability rating. Typically FR-4 materials are “94 V-0” certified, where “94” refers to the specification UL-94, the letter(s) refers to the test performed and the number refers to the results grade. Other materials such as some polyimides may have “94 HB”; some high frequency materials have no rating. The flammability rating of the material can typically be found on the laminate’s datasheet which can usually be found on the manufacturer’s web site.

The fabricator of the printed board should also have their product, the combination of that material and their fabrication processes, be UL certified to be able to mark the printed board with the flammability rating. Constructions using more than one laminate type, such as rigid-flex or hybrids, which combine epoxy fiberglass with polyimide or PTFE, require that the fabricator be certified for that combination even if they are certified for each individually.

The printed board design **shall** be such that internal temperature rise due to current flow in the conductor, when added to all other sources of heat at the conductor/laminate interface, will not result in an operating temperature in excess of that specified for the laminate material or maximum sustained operating temperature of the assembly.

Since heat dissipated by parts mounted on the printed boards will contribute local heating effects, the material selection **shall** take this factor, plus the equipment’s general internal rise temperature, plus the specified operating ambient temperature for the equipment into account for maximum operating temperature.

Hot spot temperatures **shall not** exceed the temperatures specified for the laminate material selected. See IPC-2222 for maximum operating temperature specified for laminate materials. Materials used (copper-clad, prepreg, copper foil, heatsink, etc.) **shall** be specified on the master drawing.

4.3.1 High T_g Laminates High temperature laminates include those made from resins, and blends of resins, such as Epoxy, Cyanate Ester, Bismaleimide-Triazine, Modified Thermoplastics, and Polyimide. High temperature laminates offer the advantages of increased chemical resistance and thermal stability. They are commonly used to improve the reliability of a device where extremes of thermal cycles and temperatures are expected during assembly or use. Disadvantages may include the need for specialized processing and/or higher material cost.

4.3.2 Color Pigmentation Natural colored stock is preferred, because whenever a pigment is added to change a color, the possibility exists for the pigment to retard the ability of the impregnating resin to completely wet each and every glass fiber. Without complete wetting, moisture can be trapped.

Colored stock should not be used because the material usually costs more. Production delays may also be incurred because of lack of availability of the colored stock. If colored stock is required, it **shall** be specified on the procurement documentation.

4.3.3 Dielectric Thickness/Spacing The minimum dielectric thickness/spacing **should** be specified on the master drawing. When raw materials are specified on the master drawing, classes and tolerances **shall** be selected compatible with end item dielectric thickness requirements. Recognize that when material is called out as nominal thicknesses, such as 0.1 mm [0.0039 in.] IPC-4101 Class M core for example, tolerance or process variation can take the thickness below the minimum, which is 87 µm [3,425 µin].

4.3.4 Thermally Conductive Laminates Several composite laminates have been developed to increase heat dissipation. These laminates should be selected from IPC-4101. If the laminate requirements are not in the IPC specifications, the requirements **shall** be as specified on the master drawing and AABUS.

4.3.5 Minimum Base Material Thickness for PC Card Form Factors The minimum base material thickness associated with PC card form factor printed boards is generally much thinner than conventional printed board technology, with a single ply of dielectric material between conductive layers. Copper cladding used with these materials may require a low profile foil to ensure the insulating properties of clad base materials. This can be implemented by specifying IPC-4562 with foil profile type “L.”

4.4 Conductive Materials The primary function of metallic coatings is to contribute to the formation of the conductive pattern. Beyond this primary function, specific platings offer such additional benefits as corrosion prevention, improved long term solderability, wear resistance, and others.

The thickness and integrity requirements for metallic platings and coatings on as-produced printed boards **shall** be in accordance with the requirements of Table 4-2 through Table 4-5 for the appropriate class of equipment (see also IPC-6012, IPC-6013, IPC-6018, etc.). Unless otherwise specified on the master drawing, metallic platings and coatings **shall** meet the requirements specified in 4.4.1 through 4.4.11. Attention should be paid to the effects of dissimilar metals in areas such as connectors, sockets, and other interfaces. The result of a poor material selection could be a reduction in function, either mechanical or electrical. Table 4-6 provides guidance on these metallic platings and coatings for use in lead-free soldering environments and should be tempered by evaluation of each individual application.

Table 4-2 Final Finish and Coating Requirements

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code ¹
S	Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-003 J-STD-006	b0
b1	Lead-Free Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-003 J-STD-006	b1
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable	J-STD-003 J-STD-006	b3
X	Either Type S or T	As indicated by code		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	J-STD-003 J-STD-006	b3
G	Gold for edge printed board connectors and areas not to be soldered - minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	None	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered - maximum ³	0.45 µm [17.72 µin]	None	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) - minimum	0.05 µm [1.97 µin]	None	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3 µm [118 µin]	None	b4
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	Class 1 and Class 2 0.3 µm [11.8 µin]	None	b4
		Class 3 0.8 µm [31.5 µin]		
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3 µm [118 µin]	None	b4
N	Nickel - Electroplate for edge printed board connectors - minimum	Class 1 2.0 µm [78.7 µin]	None	N/A
		Class 2 and Class 3 2.5 µm [98.4 µin]		
NB	Nickel-Electroplate as a barrier ⁴ - minimum	1.3 µm [51.2 µin]	None	N/A
OSP	Organic Solderability Preservative	Solderable ⁵	None	b6
HT OSP	High Temperature OSP	Solderable ⁵	None	b6
ENIG	Electroless Nickel - minimum	3 µm [118 µin]	IPC-4552	b4
	Immersion Gold - minimum	0.05 µm [1.97 µin] ⁶		b4

Code	Finish	Thickness	Applicable Acceptability Specification	Marking Code ¹
ENEPIG	Electroless Nickel - minimum	3 µm [118 µin]	IPC-4552	b4
	Electroless Palladium - minimum	0.05 µm [2 µin]	None	N/A
	Immersion Gold - minimum	Coverage and Solderable ⁶	None	b4
DIG	Direct Immersion Gold (Solderable Surface)	Solderable ⁶	None	b4
IS	Immersion Silver	Solderable ⁷	IPC-4553	b2
IT	Immersion Tin	Solderable ⁸	IPC-4554	b3
C	Bare Copper	AABUS	AABUS	N/A

Note 1. These marking and labeling codes represent the codes for surface finish categories established in IPC/JEDEC-J-STD-609.

Note 2. No finish thickness requirement is needed to be specified on drawing. See also 4.4.10.1.

Note 3. Industry investigations have shown that a gold-tin intermetallic phase forms under normal soldering process parameters when the weight percent of gold in the solder joint reaches the 3-4% range. Refer to IPC-J-STD-001 and IPC-HDBK-001 for further information on gold removal to prevent the formation of brittle solder joints resulting from high concentrations of gold dissolving into the solder joint.

Note 4. Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

Note 5. See 4.4.7.

Note 6. See 4.4.4.1 through 4.4.4.3.

Note 7. See 4.4.5.

Note 8. See 4.4.6.

Table 4-3 Surface and Hole Copper Plating Minimum Requirements for Buried Vias >2 Layers, Through-Holes, and Blind Vias¹

	Class 1	Class 2	Class 3
Copper - average ²	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
Thin areas	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
Wrap ³	AABUS	5 µm [197 µin]	12 µm [472 µin]

Note 1. Does not apply to microvias (see 1.5.1).

Note 2. Copper plating thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for filled PTHs and vias **shall** be in accordance with IPC-6012.

Table 4-4 Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)¹

Copper - average ²	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap ³	AABUS	5 µm [197 µin]	6 µm [236 µin]

Note 1. See 1.5.1 for definition of microvia.

Note 2. Copper plating thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for filled microvias **shall** be in accordance with IPC-6012.

Table 4-5 Surface and Hole Copper Plating Minimum Requirements for Buried Via Cores (2 Layers)

Copper - average ¹	13 µm [512 µin]	15 µm [592 µin]	15 µm [592 µin]
Thin areas	11 µm [433 µin]	13 µm [512 µin]	13 µm [512 µin]
Wrap ²	AABUS	5 µm [197 µin]	7 µm [276 µin]

Note 1. Copper plating (1.3.4.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 2. Wrap copper plating for filled buried via cores **shall** be in accordance with IPC-6012.

Table 4-6 Surface Finishes

Application	Lead-Free Hot Air Solder Level	Organic Solderability Preservative	Electroless Nickel/ Immersion Gold	Electroless Nickel/ Immersion Palladium/ Immersion Gold	Electroless Nickel/ Immersion Palladium/ Immersion Gold	Electroless Nickel/ Electroless Palladium/ Electroless Gold ¹	Electrolytic Nickel/ Electrolytic Gold ¹	Electroless Nickel/ Immersion Gold ¹	Immersion Tin	Immersion Silver
Finish Code	LF-HASL	OSP	ENIG	ENEPIG	ENIPIG	ENEPEG	Ni/Au	ENIG/EG	ISn	IAg
Soldering	●	●	●	●	●	●	●	●	●	●
Gold Embrittlement	●	●	●	●	●	●	●	●	●	●
Switch Contacts	○	○	●	●	●	●	●	●	○	●
Wire Bonding	○	○	●	●	●	●	●	●	○	○
Press Fit	●	○	●	●	●	●	●	●	●	●
Compliant Pin	●	○	●	●	●	●	●	●	●	●
Edge Board Connector	○	○	●	●	●	●	●	●	○	○
Shelf Life (1 year)	●	●	●	●	●	●	●	●	●	●
Oxidation Resistance	●	○	●	●	●	●	●	●	●	●
Solderable After Multiple Reflow Cycles	●	●	●	●	●	●	●	●	○	●
Coplanarity	○	●	●	●	●	●	●	●	●	●
Radio Frequency (RF)	●	●	●	●	●	●	●	●	●	●
Special Packaging ²	●	●	●	●	●	●	●	●	●	●

Note 1. Embrittlement becomes a concern when the gold thickness is in excess of 0.45 µm [17.72 µin]. Embrittlement is a function of gold thickness and not of gold type.

Note 2. Refer to IPC-1601.

● = Preferred ● = Functional ○ = Not Recommended

4.4.1 Electroless Copper Plating Electroless copper is deposited on the surface and through holes of the printed board as a result of processing the drilled panel through a series of chemical solutions. Typically, this is the first step in the plating process and is usually 0.6 to 2.5 μm [24 to 98.4 μin] thick. Electroless copper can also be used to fully build the required copper thickness, which is referred to as additive plating.

4.4.2 Semiconductive Coatings Semiconductive coatings for direct metallization are used as a conductive starter coating prior to electrolytic copper plating and are applied to the hole wall. The coating should be of sufficient quality for subsequent metallic deposition and **shall** be non-migrating. This process is typically fabricator dependent and is not specified on the master drawing. Palladium and tin are commonly used materials. A thin layer is deposited on exposed surfaces, especially inside drilled holes. This provides a surface for auto-catalyzing the electroless copper deposition.

4.4.3 Electrolytic Copper Plating Electrolytic copper can be deposited from several different electrolytes, including copper fluoroborate, copper cyanide, copper sulfate, and copper pyrophosphate. Copper sulfate and copper pyrophosphate are the most commonly used electrolytes for building the copper deposition on the surface and through the holes to the required thickness. This type of plating usually produces the final copper thickness requirement.

4.4.4 Gold Plating A variety of gold platings are available for depositions on printed boards. These may be electrolytic, electroless, or immersion deposits. The electrolytic deposition may come in 24k soft gold, 23+k hard gold (hardening uses trace amounts of cobalt, nickel, or iron which are co-deposited with the gold), or the plating may be a lower karat alloy (14 - 20k) for some applications. Gold plating serves several purposes:

- To act as a self lubricating and tarnish resistant contact for edge printed board connectors (see Table 4-2). Hard electrolytic gold plating is most often used for this application.
- To prevent oxidation of underlying plating such as nickel and electroless nickel so as to enhance solderability and extend storage life. Electrolytic, immersion and electroless gold are most often used for this purpose (see Table 4-2 for thickness).
- To provide a wire bonding surface. This application employs a soft 24k electrolytic gold, see Table 4-2 for thickness.
- To provide an electrically conductive surface on printed boards when electrically conductive adhesives are used. A minimum thickness of 0.25 μm [9.84 μin] is recommended.
- To act as an etch resist during printed board fabrication, a minimum thickness of 0.13 μm [5.12 μin] is recommended.

Electrolytically deposited gold is often specified as required to meet ASTM-B-488 with the type and grade selected to satisfy the different applications. A low-stress nickel or electroless nickel **shall** be used between the gold overplating and the basis metal when gold finish is to be used for electrical or wire bonding.

Table 4-7 will help clarify some of the uses for the various alloys.

Table 4-7 Gold Plating Uses

Minimum Purity	Knoop Hardness	Contacts	Wire Bonding	Soldering
99.0	130-200	S	C*	C**
99.0	90 max	NR	S	C**

S - Suitable use NR - Not recommended C - Conditional use

* May be used, but will depend on type of wire bonding being used. Run Test prior to wire bonding.

** More than 0.45 μm [17.72 μin] gold on printed boards or leads may cause embrittled solder joints.

4.4.4.1 Electroless Nickel/Immersion Gold (ENIG) ENIG (Electroless Nickel/Immersion Gold) is widely used as a surface finish for high density SMT designs. The surface is coplanar and is compatible with eutectic and lead-free solders. It is widely considered an ideal contacting surface. It is also aluminum wire bondable and its shelf life can exceed 12 months.

The thickness of the deposit **shall** comply with IPC-4552 which specifies Ni between 3 - 6 μm [118 - 236 μin] and a gold thickness of 0.05 μm [1.97 μin] minimum. Attempting to put more than 0.125 μm [4.92 μin] of gold using the ENIG process could result in corrosion and loss of solderability of the underlying Ni and give rise to the phenomenon of "Black Pad." Black pad is a deterioration of the pad surface finish. See IPC-4552 for a complete discussion.

The bare printed board requirements for deposit thickness of the ENIG should be verified using X-Ray Fluorescence (XRF), or similar, measurement. Class 1 and Class 2 products require, as a minimum, five measurements per lot. Class 3 product measurements are AABUS, and the procurement documentation **shall** specify the minimum frequency of thickness verification. For consistency, all measured pad sizes **shall** have an area approximately 1.5 x 1.5 mm [0.060 x 0.060 in]. The advantages and limitations of ENIG are outlined in Table 4-8.

Table 4-8 ENIG Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Moderately higher cost to OSP or HASL
Excellent wettability, with eutectic and lead-free solder	Multi-step process
Multiple lead-free reflow cycles	Requires good process control
Ideal contacting surface	Poor process control may lead to Black Pad
Aluminum wire bondable	Not recommended for gold wire bonding
Shelf-Life - capable of J-STD-003 Category 3 durability	Limited re-workability at the printed board level
Improved PTH reliability	Solder mask shall be fully cured before ENIG plating
Nickel barrier reduces copper dissolution during lead-free solder assembly and/or rework	

Note: In spite of ENIG's potential for "black pad" or nickel corrosion, it remains a widely used surface finish, particularly for lead-free soldering. Nickel corrosion occurs during the gold deposition step. It only occurs on a compromised Ni deposit coupled with extended dwell in an aggressive gold bath. Focus on ENIG pre-treatment and control of the Ni bath will produce the desired nickel deposit that is not susceptible to corrosion. Limiting the gold thickness and hence dwell time in the gold deposition step has come a long way in eliminating the defect.

4.4.4.2 Electroless Nickel/Immersion Gold/Electroless Gold (ENIG/EG) The finish is used for gold wire bonding and in compression connections. Some gold wire bonding requires a thicker gold than ENIG or ENEPIG can supply. The immersion gold serves as an initiator for electroless gold deposition, as electroless gold does not initiate directly on electroless nickel. The surface is coplanar and has excellent shelf life, in excess of 12 months.

The thickness of the deposit is designed to meet the requirements of the intended use. For gold wire bonding, the minimum thickness per Table 4-2 would be sufficient to ensure proper bonding and shelf life stability. Thicker gold in the order of 1.0 μm [40 μin] may be needed for compression connections.

ENIG/EG is not ideal for soldering, as the thicker gold layer may embrittle the solder joint, depending on the volume of solder used in the joint.

The bare printed board requirements for deposit thickness of the nickel and gold should be verified with an appropriate instrument, such as, X-Ray Fluorescence (XRF) Spectrometry.

The advantages and limitations of ENIG/EG are outlined in Table 4-9.

Table 4-9 ENIG/EG Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	Limited applicability for soldering
Gold wire bondable	Multi-step process
Compression connection surface	More stringent process control of electroless gold required
Improved PTH reliability	Moderately higher cost to OSP or HASL
Shelf-Life - capable of J-STD-003 Category 3 durability	Limited re-workability at the bare printed board level
No copper sidewalls, No overhang or slivers, pad completely encapsulated	

4.4.4.3 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) ENEPIG is a very versatile surface finish with a wide range of applications. It has gained popularity as a surface finish for high density SMT designs. The surface is coplanar and is compatible with eutectic and lead-free solders. ENEPIG forms a very robust solder joint with copper bearing lead-free solders, such as, SAC alloys. It is a surface finish that is both aluminum and gold wire bondable with a shelf life that can exceed 12 months. ENEPIG is suitable to replace multiple finishes used for soldering, wire bonding and/or contact surfaces on the same printed board.

Most users specify nickel thickness between 3 - 6 μm [118 - 236 μin], palladium thickness in the range of 0.05 - 1.0 μm [1.97 - 40.0 μin] and immersion gold layer **shall** have coverage and be solderable (Common gold plating results in a thickness from 0.025 to 0.1 μm [0.984 - 4.0 μin]). If the finish is going to be used for both soldering and wire bonding, then, the thinner palladium thickness (0.1 μm [4.0 μin]) is recommended. If the finish will not be used for soldering, a higher palladium thickness may be specified. As of the publication to this revision of IPC-2221, the IPC-4556 specification for ENEPIG is under development.

The bare printed board requirements for deposit thickness of the nickel and palladium should be verified with an appropriate instrument, such as X-Ray Fluorescence (XRF) Spectrometry. For consistent data, all measured land sizes should have an area approximately 1.5 x 1.5 mm [0.060 x 0.060 in]. Class 1 and Class 2 products require, as a minimum, five measurements per lot. Class 3 product measurements are AABUS. It is, therefore, recommended that an inspection plan be established for the quantity and extent of XRF measurements for Class 3 product. A pull test may be desirable for some wire bond applications. A custom coupon may be utilized.

The advantages and limitations of ENEPIG are outlined in Table 4-10.

Table 4-10 ENEPIG Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Moderately higher cost to OSP or HASL
Excellent wettability, with eutectic and lead-free solder	Multi-step process
Multiple lead-free reflow cycles	Requires good process control
Ideal contacting surface	Limited re-workability at the bare printed board level
Shelf-Life - capable of J-STD-003 Category 3 durability	Solder mask shall be fully cured before ENEPIG plating.
Aluminum and gold wire bondable	Difficult to build thicker gold finishes over palladium
Improved PTH reliability	High palladium thicknesses combined with solders containing lead have the potential of generating embrittled solder joints
No probability of "Black Pad"	
Alleviates copper dissolution from hole walls	

4.4.5 Immersion Silver Immersion silver is a viable solderable surface finish for all categories of printed boards. The surface is coplanar and is compatible with eutectic and lead-free solders. It may be the preferred finish for very high frequency RF applications because it avoids the skin effect problem that may arise with nickel-gold finishes. The immersion silver coating consists of pure silver and a small amount of organic additives. At assembly, the silver is dissolved in the solder and a Cu/Sn intermetallic (IMC) is formed.

As this surface finish has established itself in the marketplace, its advantages and weaknesses have become better understood. Instances of interfacial voiding reported by early users have been resolved. Immersion silver is susceptible to creep corrosion in humid environments that contain sulfur compounds. Solder mask defined lands are more susceptible to creep corrosion, as compared to pattern defined lands.

The IPC immersion silver specification, IPC-4553, specifies the minimum thickness.

Appropriate packaging and storage of immersion silver finishes is important to preserve solderability. See IPC-4553.

The advantages and limitations of Immersion Silver Surface Finish are outline in Table 4-11.

Table 4-11 Immersion Silver Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Limited re-workability at the bare printed board level
Excellent wettability, with eutectic and lead-free solder	Solder mask shall be fully cured before Immersion silver plating
Low loss finish compatible with RF design requirements	Reduced Shelf Life - in environments containing sulfur compounds or chlorides
	Excessive thickness of IAg combined with lead-free silver bearing solder, has the potential to create an embrittled solder joint
	No Nickel barrier allows copper dissolution during lead-free solder assembly and/or rework

4.4.6 Immersion Tin Immersion tin is a viable solderable surface finish for all categories of printed boards. The surface is coplanar and is compatible with eutectic and lead-free solders. It has been used for very high frequency RF applications because it avoids the skin effect problem that may arise with nickel-gold finishes.

The immersion tin coating consists of pure tin, some formulations contain small quantities of silver for whisker mitigation and a small amount of organic additives. At assembly, the deposit is dissolved in the solder and a Cu/Sn IMC is formed.

IPC-4554 covers this surface finish and it is the one finish currently that has been broken into 3 categories of coating durability - this is a function of copper migration through the deposit and the number of thermal cycles in use.

will see. Thicknesses should be specified as a function of coating durability categories, in accordance with IPC-J-STD-003, and may be found in IPC-4554. It is imperative that the correct thickness of tin, devoid of copper, be specified for a particular assembly process. Failure to do so, or receiving product that does not meet the specified requirements, will result in solderability defects. The same 1.5 x 1.5 mm [0.060 x 0.060 in] pad size is used for XRF measurements, as this is the standard pad size for all surface finish measurements.

Appropriate packaging and storage of immersion tin finishes is important to preserve solderability. See IPC-4554 and IPC-1601. Unlike other finishes, heat is a key driver in the degradation of performance of this finish. Heat facilitates the migration of copper through the tin finish to the surface, resulting in oxidation and loss of solderability.

The advantages and limitations of Immersion Tin Surface Finish are outlined in Table 4-12.

Table 4-12 Immersion Tin Surface Finish Advantages and Disadvantages

Advantages	Limitations
Uniform coplanar surface	Rapid diffusion of copper through the deposit can impact shelf life - specify coating durability
Forms CuSn IMC's - predictable solder joints	Deposit is "dirty" requiring special cleaning post plating
Easy to measure by XRF	Deposit is soft and mars easily
Low loss finish compatible with RF design requirements	Very aggressive chemistry on solder masks, especially around annular rings
Excellent wettability with eutectic and lead-free solder	Tin whiskers have been reported in some instances - some chemistries offer mitigation strategies (i.e., silver)
	No Nickel barrier allows copper dissolution during lead-free solder assembly and/or rework
	Limited re-workability at the bare printed board level
	Not suitable as a surface finish for either aluminum or gold wire bonding due to the instability and metallurgical incompatibility of the deposit

4.4.7 Organic Solderability Preservative (OSP) OSP is a general term that describes a variety of water based surface treatments containing organic compounds that are designed to serve the same function. They coat the copper surface by forming an organo-metallic complex, whose thickness and chemical composition may range from a molecular monolayer, to complex films with thicknesses up to 0.5 µm [19.7 µin]. OSPs are copper surface specific and are often designed specifically to minimize film formation on gold or other surfaces. The coatings protect the underlying copper from oxidation, thus preserving its solderability.

Some examples of classes of organic compounds used in OSPs are benzotriazoles, imidazoles and benzimidazoles. The ability of a particular OSP to withstand thermal excursions at assembly can be affected by a variety of formulation factors including the choice of organic compound. The simpler types may only withstand a single eutectic thermal excursion, while the more sophisticated ones can withstand multiple thermal excursions even at lead-free soldering temperatures, with or without a nitrogen atmosphere.

When selecting OSP as a surface finish, it is advisable to work with the assembler to confirm that the assembly conditions (for example, number and type of reflow cycles, in-process hold times) are compatible. Some designs are not suitable for OSP. Fabricators often process a single OSP proprietary product, so specifying an OSP may limit the choice of suppliers.

If the paste print screen openings are smaller than the land, there may be exposed copper after assembly, because OSP finishes provide only very limited solder spread.

During assembly, the OSP coating is removed when it comes in contact with soldering flux. The intermetallic formed at the solder joint/land interface is a Cu/Sn compound. The OSP coating, itself, does not become part of the solder joint.

Shelf life of OSP coated printed boards may be as high as 12 months, but will vary depending on the type of OSP, the packaging and storage conditions and the application/assembly process conditions. Printed boards that have exceeded their shelf life may become oxidized which will then require rework by stripping and recoating.

The advantages and limitations of OSP are outlined in Table 4-13.

4.4.8 Nickel Plating Nickel plating serves a dual function in contact plating: 1) It provides an anvil effect under the gold providing an essential extra hardness to the gold; 2) It is an effective barrier layer (when its thickness exceeds 2.5 µm [98.4 µin]) which prevents the diffusion of copper into gold. This diffusion process can result in a room temperature alloying of the gold, degrading the electrical and corrosion resistance characteristics of the contact.

Table 4-13 OSP Surface Finish Advantages and Limitations

Advantages	Limitations
Uniform coplanar surface	May require an aggressive flux
Some OSPs do not deposit on gold	Boards with OSP coating requires careful handling
Reworkable, aqueous process	Not easy to inspect or measure
Controllable, automated process	Exposed copper areas may be vulnerable to corrosion
No process thermal shock during application	Not a suitable contact surface
Preferentially coats copper	Soldering of Class 3 holes with aspect ratios greater than 10:1 are not achievable
Consistent compliant pin insertion and rework	May have limited in-process hold times
Least expensive of all final finishes	As there is no Nickel barrier, copper dissolution may occur during lead-free solder assembly and/or rework
	OSP's may be damaged by baking prior to soldering

All electrolytically deposited nickel plating **shall** be low-stress and conform to AMS-QQ-N-290, Class 2, except that the thickness **shall** be as specified in Table 4-2.

Reasons for using a nickel underplate include:

- *Diffusion Barrier* – To inhibit diffusion of copper from the basis metal (and of zinc from brass) to the surface of the precious metal plating, or to inhibit interdiffusion between the basis metal and the gold top coat (for example, silver and copper), which might produce a weak alloy or intermetallic compound at the interface.
- *Levelling Layer* – To produce a smoother surface than the basis metal in order to ensure a lower porosity gold top plate (for example, levelling nickel over a rough substrate).
- *Pore Corrosion Inhibitor* – A nickel underplate under the gold top coat will form passive oxides at the base of pores in humid air, provided the environment does not contain significant amounts of acidic pollutants (such as SO₂ or HCl).
- *Tarnish Creepage Inhibitor for Gold* – Non-copper base metals will inhibit creepage of copper tarnish films over the gold—where the tarnish originates from pores and bare copper edges.
- *Load-Bearing Underlayer for Contacting Surfaces* – A hard nickel underplate can serve as a load-bearing foundation for the gold top coat to prevent cracking of hard golds and reduce the wear of the precious metal during sliding of the contacting surfaces. For all these purposes, the nickel underplating should be intact (that is, not cracked) and should have sufficient thickness to achieve the particular function for which it was intended. As a general rule, the minimum thickness should be 1.2 µm [47.2 µin], preferably greater. For some levelling purposes, a far greater thickness may be required.

4.4.9 Tin/Lead Plating Tin/Lead Plating is applied in the subtractive fabrication process to provide a copper etch resist and a solderable coating, when required. Typical thickness sufficient for etch resist on 2 oz. copper is 8.0 µm [315 µin], but it is a fabrication process parameter, not a design requirement. The electrodeposit is generally fused by one of several techniques (hot oil immersion, infrared exposure, exposure to hot vapors or inert liquids). The fusing operation results in the formation of a true alloy on the surface and in the through holes of the printed board. Fusing is required unless the unfused option is selected to maintain flatness. It also promotes improved long-term solderability.

Tin lead plating does not apply to buried PTHs which are internal to the printed board and do not extend to the surface.

Tin-lead plating **shall** meet the composition requirements of ASTM-B-579.

4.4.9.1 Tin Plating Tin Plating is applied in the subtractive fabrication process to provide a copper etch resist.

4.4.10 Solder Coating Solder coating is generally applied by immersing the printed board into molten solder and removing the excess by blowing hot, pressurized air, fluid or vapors over the surface of the printed board in a specially designed machine.

Solder coating does not apply to buried or tented PTHs which are internal to the printed board and do not extend to the surface.

Unless otherwise specified on the master drawing, the solder used for solder coating **shall** be in accordance with J-STD-006. Solder coating thickness may be specified for particular applications. The performance of solder coating is evaluated, not by a mechanical thickness measurement, but by the ability of the printed board to pass solderability testing per J-STD-003 (see Table 4-2). The user has the responsibility to determine if steam aging, prior to solderability testing, is required.

4.4.10.1 Hot Air Solder Leveling (HASL) The current surface finish of long standing is hot air solder leveling (HASL). In this process, the finished circuit board is dipped either vertically or horizontally into a molten solder bath and the excess solder is blown away and leveled with hot air, giving the process its name. The HASL process is the first soldering stress that the printed board experiences. Some material combinations may be prone to delamination or reduced product life cycle due to multiple thermal excursions.

When done properly, the HASL finish process generates visual assurance of solderability. The quality of the product regarding solderability can be confirmed using an approved test method as specified in IPC-J-STD-003. Any evidence of non-wetting or dewetting is immediately apparent as the printed board exits the process.

HASL finish has good solderability and has limited shelf life. It can withstand multiple thermal excursions for double sided assembly. HASL processes, however, are considered to have a degree of difficulty in their control. This, coupled with pad sizes and geometries placing additional challenges on such processes, places the creation of a practical minimum thickness outside the scope of this design standard.

4.4.10.1.1 Tin Lead HASL Although the tin lead surface finish was the main solution for printed boards, one concern with the HASL process is coating thickness uniformity. Often in the process, the solder thickness varies widely from 0.75 - 35 μm [29.5 - 1,378 μin]. Thinner solder finishes, such as <1.2 mm [0.0472 in], reduce shelf life due to formation of inter-metallics. As a result, acceptance criteria for the solderability of printed boards should include or be entirely based on functional testing of sample boards or coupons.

The wide variation seen in solder thickness in HASL affects the coplanarity of solder termination on the printed board and hence the coplanarity of SMT components, and uniform solder paste stencil contact.

The increase in the use of thin printed boards (< 0.5 mm [0.0197 in] in thickness) may preclude the use of HASL because of warping of the printed boards during processing.

4.4.10.1.2 Lead-free HASL The lead-free hot air solder leveling process can provide both quality and reliability of the surface finish in providing long shelf life solderability. Like most of lead-free technology, the process for lead-free HASL is maturing as more printed board fabrication facilities implement its use.

The most likely candidates for lead-free HASL are Sn-Cu eutectic (227 °C [441 °F] melting point), or Sn-Ag-Cu eutectic (217 °C [423 °F] melting point). The Sn-Ag-Cu alloy has a lower melting point, but the tin-copper is lowest cost. The Sn-Cu solder pool is easy to manage and recycle, because there are only two constituents. The solder bath is not too aggressive, has low copper dissolution, and is relatively tolerant of common impurities. In contrast, the Sn-Ag-Cu has a much higher copper dissolution rate.

Some proprietary formulas have application for specific uses, such as, carbon paste.

Lead-free HASL finishes are more expensive because tin and silver cost more than lead. The finish is smooth and bright and less domed than eutectic tin/lead HASL (see Figure 4-1).

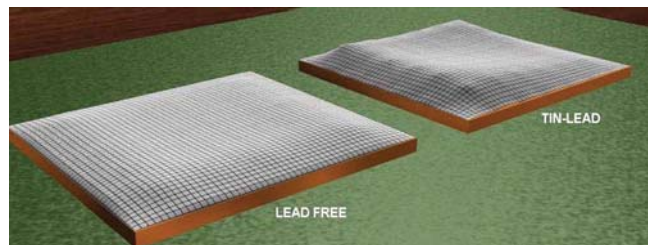


Figure 4-1 HASL Surface Topology Comparison

4.4.11 Other Metallic Coatings for Edge Printed Board Contacts In addition to the coatings cited previously, there are several other options that the designer may want to consider:

- Rhodium – a low resistance contact coating for flush circuits, switches or where a high number of insertions is expected. Expense has precluded its general use.
- Tin/Nickel Alloy – an abrasion resistant coating.
- Palladium/Nickel Alloy – a low resistance contact coating. May be particularly useful for flush circuits.

4.4.12 Metallic Foil/Film

4.4.12.1 Copper Foil There are two types of copper foil available: (W) – wrought (or rolled), and (ED) – electrodeposited. There are also several copper foil grades. For rigid printed boards, electrodeposited copper foil is generally used. For flexible printed boards, wrought foil is generally used. Whichever type is used, the copper foil shall conform to the requirements of IPC-4562.

The thickness of starting copper conductors **shall** be as defined in Table 4-14 for the appropriate class of equipment (a reduction in copper thickness of inner layers may be expected after processing). See Appendix A of IPC-4562 for details of foil properties.

Thinner foils are generally used by the printed board manufacturer for “fine line” designs to reduce the amount of under-cutting of circuit conductors that occurs during the etch operation and meet the requirements of flip chip and chip scale packages. The final after-plating copper thickness is nominally 25.0 - 35.0 μm [984.0 - 1,378 μin] greater than the base foil. For multilayer constructions, the copper thickness should be specified for each layer of the printed board.

If thinner foils are specified and greater after-process copper thicknesses are required, the following should be kept in mind. Using thinner copper foil means that more copper plating is required to reach the final requirement. Thus there will also be more plating in the holes, which means that the vendor should start out with larger hole diameters. This in turn will decrease the annular ring and increase the chance of hole breakout if a larger size land is not used. If larger land sizes cannot be used, the greater copper thickness requirement should be reconsidered or met by other means such as increasing the width of conductors.

4.4.12.2 Copper Film Copper film **shall** be in accordance with Table 4-14.

Table 4-14 Copper Foil/Film Requirements¹

Copper Type	Class 1-3
Minimum Starting Copper Foil - external	1/8 oz/ft ² (5 μm) [197 μin]
Minimum Starting ² Copper Foil - internal	1/4 oz/ft ² (9 μm) [354 μin]
Starting Copper Film (semi-additive)	5 μm [197 μin]
Final Copper Film (fully-additive)	15-20 μm [591-787 μin]

1. All dimensional values are nominal and derived from weight measurements.

2. 1/8 oz/ft² (5 μm) [197 μin] may be used for buried via applications.

It should be noted that the minimum material properties for electrodeposited copper foils given in IPC-4562 are inadequate for many printed board designs and applications. This is particularly the case for IPC-4562/1 (CV-E1), IPC-4562/2 (CV-E2), and IPC-4562/3 (CV-E3). While the vast majority of foil product sold under these slash sheet specifications far exceed the minimum property values, some product sold barely meets these specifications. Thus, it is prudent to obtain actual material properties for critical product.

4.4.12.2.1 Resin Coated Copper Foil Metal foils coated with a resin or composite of resins on one side which are used for the fabrication of printed boards. Coated copper foils when used **shall** be as specified in IPC-4563.

4.4.12.2.1.1 Copper Foil With Single Layers of Resin Copper foil with a single coating of thermosetting resin can be used to improve the surface uniformity, flatness, and chemical resistance of the outer dielectric layers of a printed board.

4.4.11.2.1.2 Copper Foil With Two Layers of Resin Copper foil with two layers of thermosetting resin coated onto one side, such that the layer against the foil is cured to a “C” stage to provide a fixed minimum dielectric thickness and the outer layer of resin partially cured to a “B” stage to provide an adhesive layer, can be used to provide a very thin, flat, dielectric layer between conductors. One layer of resin with a gradient of cure, with the extent of cure being highest against the copper, can be used to simulate the two layer resin coated product. The dielectric and mechanical characteristics of the resin layer between the conductors will be consistent with those of the cured resin. These dielectric layers, produced without reinforcement, are commonly used to facilitate production of high density micro via layers by laser and plasma ablation techniques.

4.4.12.3 Other Foils/Film When other foils or films (nickel, aluminum, etc.) are used, their characteristics **shall** be specified on the master drawing.

4.4.12.4 Metal Core Substrates Substrates for metal core printed boards **shall** be in accordance with Table 4-15.

Table 4-15 Metal Core Substrates

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As specified on master drawing
Steel	QQ-S-635	As specified on master drawing
Copper	ASTM B-152 / IPC-4562	As specified on master drawing
Copper-Invar-Copper Copper-Moly-Copper	IPC-CF-152	As specified on master drawing
Other	User defined	As specified on master drawing

4.5 Electronic Component Materials The following subsections provide a generic overview of embedded passive device materials, including resistors, capacitors and inductors. For more detailed guidance on the incorporation of embedded components in printed boards, see IPC-2316.

4.5.1 Embedded (Buried) Resistors Incorporating embedded resistance technology is considerably more expensive than standard multilayer printed board fabrication. This is due to the special material copper foil purchasing, additional imaging and etching, and resistance (ohm) value verification.

One of the main printed board attributes that requires embedded resistance technology is the availability of component real estate. Some high-density designs do not permit discrete resistors. In these cases, buried resistors are viable because they are considerably smaller and when buried allow surface mount components or surface circuitry to pass over them.

An annular resistor is a polymer resistor that can be formed in the empty annulus or “antipad” which surrounds each via hole which passes through the plane or circuit layer. The annular design allows the resistor to be screened with a minimum number of factors which will affect the final resistor value. The primary use of this type of resistor is to replace pull up or pull down resistors that have an acceptable tolerance of 10% or greater. This resistor may be produced much less expensively than a surface resistor and does not require any room on the printed board surface. The larger resistor tolerance and limited number of resistor types that can be replaced are the primary design limitations.

4.5.2 Embedded (Buried) Capacitors Distributed capacitance is a design feature which places the power (VCC - voltage common carrier) and ground plane directly facing and in close proximity to each other. A separation of the two planes by 0.1 mm [0.0039 in] or less will produce a “sandwich” that will provide a low inductance, high capacitance connection to the active devices on the printed board. This fast switching, low current bypass is most useful in high speed digital applications in which the desire to remove surface capacitors or EMI are key considerations. In most designs two power/ground sandwiches are used to replace the existing power and ground plane layers presently in the printed board. In many cases the bypass capacitors 0.1 μ F and smaller may be removed from the printed board.

Because of the construction of PC card form factors, minor natural capacitance will be achieved with these types of printed board constructions. Buried discrete technologies are available and can be applied.

4.5.3 Embedded (Buried Inductors) Embedded inductors are typically fabricated by imaging the copper on one or more layers within the printed board in spiral patterns. Inductors are also made by applying a ferromagnetic material above, below or between the spiral conductor patterns.

At the time of publication of this revision to IPC-2221, there were no known commercially available embedded inductance materials.

4.6 Organic Protective Coatings

4.6.1 Solder Mask Coatings Coatings and markings **shall** be compatible with each other and with all other parts and materials used in the printed board, and the printed board assembly process, including the printed board preparation/cleaning required prior to their application. IPC-SM-840 assigns determination of this compatibility to the printed board fabricator and assembler.

The use of solder mask coatings **shall** be in accordance with the requirements of IPC-SM-840. When required, Class 3 printed boards **shall** use IPC-SM-840, Class H or FH solder mask. When Underwriters Laboratories (UL) requirements are imposed, the coatings used **shall** be approved by UL for use by the printed board manufacturer’s process.

When solder mask is used as an electrical insulator the dielectric properties of the coating **shall** be sufficient to maintain electrical integrity. There **shall** be no solder mask in areas of the printed board that make contact with the printed board guides.

If the application or design mandates, the minimum and/or maximum solder mask thickness **shall** be specified on the Master Drawing. The minimum thickness specification is required to meet insulation resistance requirements and **shall** be calculated from solder mask material specifications. The maximum thickness specification is required for component assembly process issues, such as solder paste applications.

Solder mask coating adhesion to melting metal surfaces (solder coating, tin/lead plating, etc.) cannot be assured, as printed boards are subjected to temperatures that cause redistribution of the melting metals. When solder mask coating is required over melting metal surfaces, the maximum recommended conductor width, where the coating completely covers the conductor, **shall** be 1.3 mm [0.0512 in].

When conductors of melting metal have a width larger than 1.3 mm [0.0512 in], the design of the conductor **shall** provide a relief through the metal to the base laminate substrate. The relief should be at least 0.625 mm² [0.001 in²] in size and located on a grid no greater than 6.35 mm [0.25 in]. When conductor areas of melting metal are to be left uncovered, the design for all class printed board **shall** provide that the solder mask **shall not** overlap the melting metal by more than 1.0 mm [0.0394 in].

Design requirements may dictate that via holes are protected from access by processing solutions during soldering, cleaning, etc.

The occurrence of solder balls at the assembly level may be related to the surface finish of the solder mask, e.g., matte, glossy, etc.

Additional design guidance and coverage of application processes for solder mask are described in IPC-HDBK-840.

4.6.1.1 Mask Adhesion and Coverage Adhesion between solder mask and laminate and between solder mask and conductor **shall** be complete for the total coverage area. Oxide treatment, double-treated copper, protective chemical treatment, or other adhesion promoter may be used. The use of an adhesion promoter may need user approval.

When circuit designs include unrelieved copper areas greater than 625 mm² [0.9688 in²], the use of a mask adhesion promoter is advisable.

When polymer coatings are required over nonmelting metals, such as copper, the design should provide that conductors not covered by the mask **shall** be protected from oxidation, unless otherwise specified.

4.6.1.2 Mask Clearances and Dams Mask clearances and dams should be in accordance with Table 4-16. Clear areas may have to be provided for assembly fiducials.

Table 4-16 Typical Minimum Solder Mask Clearances and Dams

Mask Type	Clearance	Dam
Liquid Screenable	0.25 mm [0.010 in]	0.25 mm [0.010 in]
Photoimageable Dry Film ≤0.0635 mm [≤0.0025 in]	0.051 mm [0.002 in]	0.127 mm [0.005 in]
Photoimageable Dry Film 0.066 - 0.1 mm [0.0026 - 0.0039 in]	0.051 mm [0.002 in]	0.25 mm [0.010 in]
LPI	0.051 mm [0.002 in]	0.1 mm [0.0039 in]

Data files usually will contain openings equal to the lands. This will allow the printed board fabricators to adjust the clearance to meet his process capabilities while meeting minimum design clearance requirements specified on the master drawing.

Solder mask-to-land relationship **shall** meet the registration requirements stated on the master drawing.

4.6.2 Conformal Coatings When conformal coating is required, it **shall** meet the requirements of IPC-CC-830 and **shall** be specified on the master drawing or master assembly drawing. When UL requirements are imposed, the coatings **shall** be approved by UL for use by the printed board manufacturer. The designer should be cognizant of compatibility issues. Conformal coating is an electrical insulation material which conforms to the shape of the circuit printed board and its components. It is applied for the purpose of improving surface dielectric properties and protecting against the effects in a severe environment.

Unless otherwise specified on the drawing/documentation, conformal coating is not required on surfaces or in areas that have no electrical conductors. Conformal coating **shall not** be applied on printed board surfaces that interface with card guides or printed board mounting hardware. Conformal coating need not be present on printed board edges (i.e., the vertical surface) unless otherwise specified on the drawing/documentation.

4.6.2.1 Conformal Coating Types and Thickness Conformal coating may be any one of the types indicated. The thickness of the conformal coating **shall** be in accordance with Table 4-17 for the type specified, when measured on a flat unencumbered surface:

Table 4-17 Conformal Coating Types and Thickness Range

Conformal Coating Type	Thickness Range
Type AR - Acrylic Resin	0.03 - 0.13 mm [0.00118 - 0.00512 in]
Type ER - Epoxy Resin	0.03 - 0.13 mm [0.00118 - 0.00512 in]
Type UR - Urethane Resin	0.03 - 0.13 mm [0.00118 - 0.00512 in]
Type SR - Silicone Resin	0.05 - 0.21 mm [0.00197 - 0.00828 in]
Type XY - Paraxyllylene Resin	0.01 - 0.05 mm [0.000394 - 0.00197 in]

There are three primary chemical categories in use for conformal coating materials: silicone elastomers, organics, and parylene. All three types provide various levels of protection from solvents, moisture, corrosion, arcing, and other environmental factors that can jeopardize the circuit's operational performance (see Table 4-18). Many surface mount technologies cannot perform adequately without the use of a conformal coating due to the tight spacing of leads and conductors.

Conformal coatings may be used in greater thicknesses as shock and vibration dampening agents. This type of application brings with it the risk of mechanical stress to glass and ceramic sealed parts during cold temperature excursions, which may require the use of buffer materials. Heavy build up of conformal coatings under DIPs may also result in mechanical stress of soldered connections during thermal cycling, unless precautions are taken.

Conformal coatings, in particular Type UR, are sometimes used to help mitigate tin whiskers as a means of reducing the potential for an electrical short circuit. However, when used for this purpose, it is recommended that a second method of tin whisker mitigation be used since tin whiskers can grow under the coating or may penetrate the coating, depending on its thickness. See IPC/JEDEC-JP002 for additional information.

Table 4-18 Conformal Coating Functionality

Type	Advantages	Disadvantages
Silicone elastomers	Resistant to extreme temperature cycling. Good intermittent solvent splash resistance. Low modulus, easily removed, flexible. Works well over most solder resists and no clean fluxes. Easily reworked.	Low mechanical abrasion resistance. Half the dielectric strength of organics. Can impair solderability after coating.
Organics	High dielectric strength. Excellent mechanical abrasion resistance. Excellent solvent resistance. Excellent moisture resistance.	Can only be used to 125 °C [257 °F]. Difficulty of rework varies. Coefficient of thermal expansion needs to be matched. Required compatibility check with solder resist. Required compatibility check with flux chemistry.
Parylene	Extremely high dielectric strength. Excellent conformability around parts. Excellent penetration of polymer. Excellent moisture/chemical resistance.	High raw material cost. Applied in a vacuum chamber (batch process). Masking seals must be air-tight. Thin film leakage difficult to visually detect.

4.6.3 Tarnish Protective Coatings Protective coatings may be applied to bare copper on the unassembled printed board in order to maintain solderability or appearance for extended periods. These coatings may be dispersed during the soldering operation or may require a separate removal process prior to the soldering operation. The coating requirement **shall** be designated on the master drawing.

4.7 Marking and Legends When specified on the master drawings, printed boards and assemblies **shall** be marked with their full identification by appropriate nonconductive inks, labels, etched characters, or other methods. Marking should be used to provide reference designators, part or serial numbers, revision level, orientation or polarization symbols, bar codes, electrostatic discharge (ESD) status, etc.

The marking locations should be such to avoid placing information under components, in hidden locations after assembly or installation, or on conductive surfaces. Marking should not be placed on surfaces covered with melting metals or opaque coatings. Etched markings may affect electrical characteristics such as capacitance.