



ASSOCIATION CONNECTING  
ELECTRONICS INDUSTRIES

---

# IPC-2224

## Sectional Standard for Design of PWBs for PC Cards

**IPC-2224**

January 1998

A standard developed by IPC

---

2215 Sanders Road, Northbrook, IL 60062-6135

Tel. 847.509.9700 Fax 847.509.0700

[www.ipc.org](http://www.ipc.org)



**Documents**

Document Sharing Hub

## The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

### Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for Engineering (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

### Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

## Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

## IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee (TAEC) that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC standard/guideline is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.

Adopted October 6, 1998

## Why is there a charge for this standard?

Your purchase of this document contributes to the ongoing development of new and updated industry standards. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low in order to allow as many companies as possible to participate. Therefore, the standards revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit [www.ipc.org](http://www.ipc.org) or call 847/790-5372.

Thank you for your continued support.



ASSOCIATION CONNECTING  
ELECTRONICS INDUSTRIES

IPC-2224

# Sectional Standard for Design of PWBs for PC Cards

Developed by the PCMCIA Subcommittee (1-21) of the Electronic  
Packaging Design Committee of IPC

Users of this standard are encouraged to participate in the  
development of future revisions.

Contact:

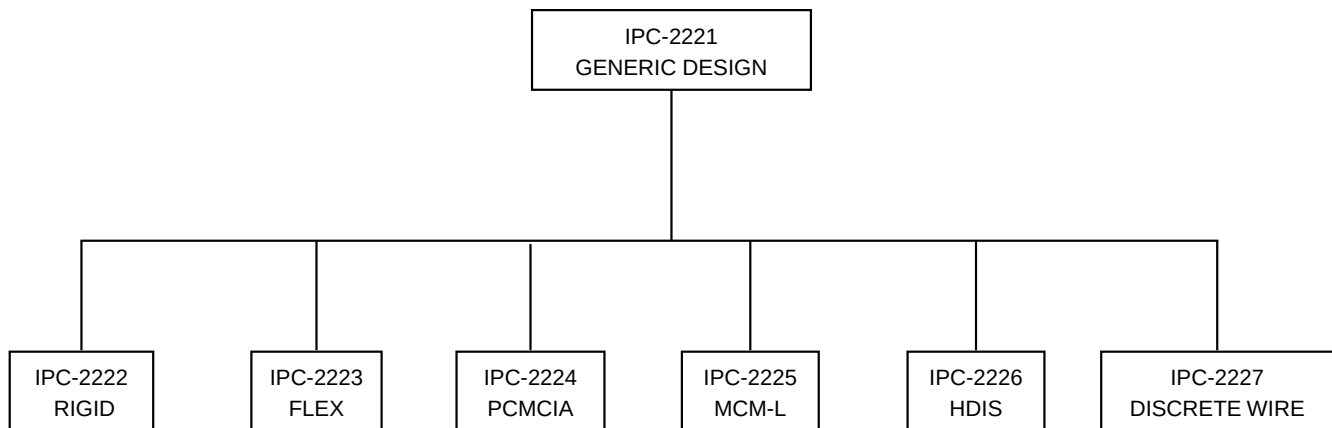
IPC  
2215 Sanders Road  
Northbrook, Illinois  
60062-6135  
Tel 847 509.9700  
Fax 847 509.9798



**Documents**  
Document Sharing Hub

---

## HIERARCHY OF IPC DESIGN SPECIFICATIONS (2220 SERIES)



### FOREWORD

This standard provides information on the generic requirements for PC Card printed board design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the broad spectrum of those designs that use organic materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting electronic, electromechanical, and mechanical components.

The information contained herein is intended to be compared to the generic design requirements specified in IPC-2221. When coupled with the aforementioned inputs this comparison will provide a complete standard and facilitate the appropriate selection process of the materials, fabrication, and assembly technology necessary to meet the engineering design objectives.

IPC's documentation strategy is to provide distinct documents that focus on specific aspect of electronic packaging issues. In this regard document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0).

Included in the set is the generic information which is contained in the first document of the set and identified by the four digit set number. The generic standard is supplemented by one or multiple sectional documents, each of which provide specific focus on one aspect of the topic or the technology selected. The designer of the printed board, needs as a minimum, the generic, the sectional of the chosen technology and the engineering description of the final product.

As technology changes specific focus standards will be updated, or new focus standards added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

## Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the PCMCIA Subcommittee (1-21) of the Electronic Packaging Design Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

| <b>Electronic Packaging Design Committee</b>                    | <b>PCMCIA Subcommittee</b>                       | <b>Technical Liaison of the IPC Board of Directors</b> |
|-----------------------------------------------------------------|--------------------------------------------------|--------------------------------------------------------|
| Chairman<br>Foster Gray<br>PC Interconnects                     | Chairman<br>Leonard Roach<br>Lucent Technologies | Larry Bergman<br>Advanced Flex, Inc.                   |
| <b>PCMCIA Subcommittee</b>                                      |                                                  |                                                        |
| Marshall Andrews, Interconnection Technology Research Institute | Martin Freedman, Amp Inc.                        | Julio Mendoza, Nelco Technology Inc.                   |
| Paul Baker, Encore Computer Corp.                               | Thomas Gardeski, ICI Americas Inc.               | James Mumby, Ciba                                      |
| Rich Barnett, Compaq Computer Corporation                       | J. Gonterman, Owens-Corning Fiberglass Corp.     | Bob Neves, Microtek Laboratories                       |
| David Boyle, Northrop Grumman Corporation                       | James Grasso, Circuitest Services Inc.           | Thomas Newton, Ibiden Circuits of America Corp.        |
| Jack Bramel, Jack Bramel & Associates                           | Ralph Hersey, Ralph Hersey & Associates          | Leonard Roach, Lucent Technologies Inc.                |
| Clifford Chaif, Circo Craft Co. Inc.                            | Robert Hodges, Rogers Corporation                | Peter Rucinski, SAS Circuits Inc.                      |
| Thomas Coyle, Hadco Corp.                                       | David Iguchi, Nelco International Corporation    | Thilo Sack, Celestica                                  |
| Tom Davison, Celestica                                          | Dan Jacobus, Sheldahl Inc.                       | Terry Shepler, Sheldahl Inc.                           |
| Steven Doepke, AlliedSignal Laminate Systems                    | John Kelly, Motorola GSTG                        | Robert St. Pierre, New England Laminates               |
| C. Don Dupriest, Lockheed Martin Vought Systems                 | Cynthia King, Nelco Technology Inc.              | Max Thorson, Compaq Computer Corporation               |
| Werner Engelmaier, Engelmaier Associates Inc.                   | George Kotecki, Northrop Grumman Corporation     | Fred Verdi, Lucent Technologies Inc.                   |
| Jim Ennis, Adtran Inc.                                          | Jack Krispin, Orbotech Inc.                      | Terry Wright, Details Inc.                             |
| Michael Flatt, Michael O. Flatt Ltd.                            | Brian Lough, U.S. Navy                           | Michael Yuen, Plexus Corp.                             |
|                                                                 | William McManus, Raytheon Company                |                                                        |



# Table of Contents

|                                                                                      |   |                                                              |    |
|--------------------------------------------------------------------------------------|---|--------------------------------------------------------------|----|
| <b>1.0 SCOPE</b> .....                                                               | 1 | 5.1 Fabrication Requirements.....                            | 6  |
| 1.1 Purpose .....                                                                    | 1 | 5.1.1 Panel Design.....                                      | 7  |
| 1.2 Documentation Hierarchy .....                                                    | 1 | 5.1.2 Fabrication Notes .....                                | 7  |
| 1.3 Presentation.....                                                                | 1 | 5.2 Product/Board Configuration .....                        | 7  |
| 1.4 Interpretation.....                                                              | 1 | 5.2.1 Board Geometries.....                                  | 7  |
| 1.5 Classification of Products.....                                                  | 1 | 5.2.2 Bow and Twist.....                                     | 9  |
| 1.5.1 Board Types.....                                                               | 1 | 5.2.3 Constraining Core Boards.....                          | 9  |
| <b>2.0 APPLICABLE DOCUMENTS</b> .....                                                | 1 | 5.2.4 Support.....                                           | 9  |
| 2.1 Reference Documents.....                                                         | 1 | 5.3 Assembly Requirements.....                               | 9  |
| 2.1.1 Institute for Interconnecting and Packaging<br>Electronic Circuits (IPC) ..... | 1 | 5.3.1 Tooling Rails .....                                    | 9  |
| 2.1.2 Underwriter's Labs.....                                                        | 2 | 5.4 Dimensioning Systems .....                               | 9  |
| 2.1.3 PCMCIA/JEIDA.....                                                              | 2 | 5.4.1 Cutouts and Notches .....                              | 9  |
| 2.1.4 Joint Industry Standards.....                                                  | 2 | 5.5 Structural Strength.....                                 | 10 |
| <b>3.0 GENERAL REQUIREMENTS</b> .....                                                | 2 | <b>6.0 ELECTRICAL PROPERTIES</b> .....                       | 10 |
| 3.1 Test Requirement Considerations .....                                            | 2 | <b>7.0 THERMAL MANAGEMENT</b> .....                          | 10 |
| 3.1.1 Mechanical.....                                                                | 2 | 7.1 Convection.....                                          | 10 |
| <b>4.0 MATERIALS</b> .....                                                           | 2 | 7.2 Heat Dissipation Considerations.....                     | 10 |
| 4.1 Material Selection.....                                                          | 2 | 7.2.1 Enclosed Housing.....                                  | 10 |
| 4.2 Bonding Material.....                                                            | 2 | 7.2.2 Ventilated Housing .....                               | 11 |
| 4.2.1 Flexible PC Cards (bond ply).....                                              | 2 | <b>8.0 COMPONENT AND ASSEMBLY ISSUES</b> .....               | 11 |
| 4.2.2 Adhesive Films.....                                                            | 2 | 8.1 General Placement Requirements .....                     | 11 |
| 4.3 Laminate Materials.....                                                          | 2 | 8.2 Plated-Through Hole Requirements.....                    | 11 |
| 4.3.1 Rigid Laminates .....                                                          | 2 | 8.3 Mounting Methods for Connectors.....                     | 11 |
| 4.3.2 Epoxy Laminates .....                                                          | 4 | 8.4 Stiffeners .....                                         | 11 |
| 4.3.3 High Performance Laminates.....                                                | 4 | 8.5 Fine Pitch SMT (Peripherals) .....                       | 11 |
| 4.3.4 High Temperature Laminates.....                                                | 4 | 8.6 Array SMT (BGA, µBGA, etc.).....                         | 11 |
| 4.3.5 High Speed and Low Loss Laminates.....                                         | 4 | 8.7 Bare Die .....                                           | 11 |
| 4.3.6 Double-Clad Laminates.....                                                     | 4 | 8.7.1 Wire Bond.....                                         | 11 |
| 4.3.7 Special Clad Materials .....                                                   | 5 | 8.7.2 Flip Chip .....                                        | 11 |
| 4.4 Flexible Substrates .....                                                        | 5 | 8.7.3 Chip Scale.....                                        | 11 |
| 4.4.1 Flexible Laminate Materials (Flexible<br>Metal Clad Dielectrics) .....         | 5 | 8.8 Tape Automated Bonding.....                              | 11 |
| 4.4.2 Coverlayer.....                                                                | 5 | 8.9 Castellations.....                                       | 11 |
| 4.5 Conductive Materials .....                                                       | 5 | 8.10 Bottom Only Terminations.....                           | 11 |
| 4.5.1 Copper Foil/Film .....                                                         | 5 | <b>9.0 HOLES/INTERCONNECTIONS</b> .....                      | 11 |
| 4.5.2 Other Foils/Film .....                                                         | 6 | 9.1 General Requirements for Lands<br>with Holes.....        | 11 |
| 4.5.3 Metal Core Substrates .....                                                    | 6 | 9.1.1 Clearance Areas in Planes.....                         | 12 |
| 4.5.4 Electronic Component Materials (Buried<br>Resistors and Capacitors).....       | 6 | 9.1.2 Conductive Pattern Feature<br>Location Tolerance ..... | 13 |
| 4.5.5 Conductive Dielectric Composites.....                                          | 6 | 9.2 Holes .....                                              | 13 |
| 4.6 Organic Protective Coatings .....                                                | 6 | 9.2.1 Quantity .....                                         | 13 |
| 4.7 Marking and Legends.....                                                         | 6 | 9.2.2 Spacing of Adjacent Holes.....                         | 13 |
| 4.8 Thickness Class Tolerance .....                                                  | 6 | 9.2.3 Hole Pattern Variation .....                           | 13 |
| <b>5.0 MECHANICAL/PHYSICAL PROPERTIES</b> .....                                      | 6 | 9.2.4 Blind/Buried Vias .....                                | 13 |
|                                                                                      |   | 9.2.5 Unsupported Holes .....                                | 13 |

|        |                                                       |           |
|--------|-------------------------------------------------------|-----------|
| 9.2.6  | Minimum Hole Sizes for Plated-Through Hole Vias ..... | 13        |
| 9.2.7  | Etchback .....                                        | 13        |
| 9.3    | Drill Size Recommendations for Printed Boards .....   | 13        |
| 10.0   | <b>GENERAL CIRCUIT FEATURE REQUIREMENTS .....</b>     | <b>13</b> |
| 10.1   | Conductor Characteristics .....                       | 13        |
| 10.1.1 | Conductor Width and Thickness .....                   | 15        |
| 10.1.2 | Edge Spacing .....                                    | 15        |
| 10.1.3 | Large Conductive Areas .....                          | 15        |
| 10.1.4 | Balanced Conductors .....                             | 15        |
| 10.2   | Land Characteristics .....                            | 15        |
| 10.2.1 | Lands for Interfacial Connection Vias .....           | 15        |
| 10.2.2 | Vias in Lands .....                                   | 15        |
| 11.0   | <b>DOCUMENTATION .....</b>                            | <b>15</b> |
| 11.1   | Artwork .....                                         | 15        |
| 11.1.1 | Component Pedestal Artwork .....                      | 15        |
| 12.0   | <b>QUALITY ASSURANCE .....</b>                        | <b>15</b> |

Figures

|             |                                              |    |
|-------------|----------------------------------------------|----|
| Figure 4-1  | Dielectric layer thickness measurement ..... | 4  |
| Figure 5-1  | Panel borders .....                          | 8  |
| Figure 8-1  | Horizontal part mouting .....                | 12 |
| Figure 8-2  | Lead-in chamfer configurations .....         | 12 |
| Figure 9-1  | Clearance area in planes, mm .....           | 12 |
| Figure 10-1 | Etched Conductor Characteristics .....       | 14 |

Tables

|            |                                                                                                                                                         |    |
|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Table 4-1  | Clad Laminate Maximum Operating Temperatures .....                                                                                                      | 3  |
| Table 4-2  | Guide to Laminate Thickness, mm .....                                                                                                                   | 3  |
| Table 5-1  | Fabrication Capability Assessment .....                                                                                                                 | 6  |
| Table 5-2  | Panel Size to Manufacturing Operation Relationships .....                                                                                               | 6  |
| Table 5-3  | Substrate Dimensions, mm .....                                                                                                                          | 7  |
| Table 5-4  | Maximum Interconnect Warpage Area .....                                                                                                                 | 9  |
| Table 5-5  | Maximum PC Card Warpage (by type) .....                                                                                                                 | 9  |
| Table 5-6  | Tolerance Cutouts, Notches, and Keying Slots, as Machined, mm .....                                                                                     | 10 |
| Table 9-1  | Feature Location Tolerances (Lands, Conductor Pattern, etc.), mm .....                                                                                  | 13 |
| Table 9-2  | Minimum Unsupported Holes Tolerance Range .....                                                                                                         | 13 |
| Table 10-1 | Typical Values to be Added or Subtracted for the Desired Nominal Conductor Width in Order to Arrive at the Nominal Width on the Production Master ..... | 16 |

.....

This page intentionally left blank

# Sectional Standard for Design of PWBs for PC Cards

## 1.0 SCOPE

This standard establishes the requirements for the design of printed boards for PC card form factors. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials; the interconnections may be single, double, or multilayered.

**1.1 Purpose** The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with IPC-2221 (see 1.2) to produce detailed designs intended to mount and attach passive and active components.

The components may be through-hole, surface mount, fine pitch, ultra-fine pitch, array mounting or unpackaged bare die. The materials may be any combination able to perform the physical, thermal, environmental, and electronic functions.

**1.2 Documentation Hierarchy** Document hierarchy **shall** be in accordance with the generic standard IPC-2221.

**1.3 Presentation** Presentation **shall** be in accordance with the generic standard IPC-2221.

**1.4 Interpretation** Interpretation **shall** be in accordance with the generic standard IPC-2221.

**1.5 Classification of Products** Classification of Products **shall** be in accordance with the generic standard IPC-2221 and as follows:

**1.5.1 Board Types** Board types are classified as:

- Type 1 — Single-sided printed board
- Type 2 — Double-sided printed board
- Type 3 — Multilayer board without blind or buried vias
- Type 4 — Multilayer board with blind and/or buried bias
- Type 5 — Multilayer metal core board without blind or buried vias
- Type 6 — Multilayer metal core board with blind and/or buried vias

## 2.0 APPLICABLE DOCUMENTS

The following documents form a mandatory part of this standard and all requirements stated therein apply, unless modified in the section in which they are invoked.

**IPC-2221** Generic Standard on Printed Board Design

**2.1 Reference Documents** The following documents form a part of this document to the extent specified herein. If a conflict of requirements exist between IPC-2224 and those listed below, IPC-2224 takes precedence.

The revision of the document in effect at the time of solicitation **shall** take precedence.

### 2.1.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)<sup>1</sup>

**IPC-DD-135** Qualification for Deposited Organic Inter-layer Dielectric Materials for Multichip Modules

**IPC-MF-150** Metal Foil for Printed Wiring Applications

**IPC-L-125** Specification for Plastic Substrates, Clad or Unclad, for High Speed/High Frequency Interconnections

**IPC-FC-231** Flexible Bare Dielectrics for Use in Flexible Printed Wiring

**IPC-FC-232** Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Wiring

**IPC-FC-241** Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Wiring

**IPC-D-300** Printed Board Dimensions and Tolerances

**IPC-D-310** Guidelines for Phototool Generation and Measurement Techniques

**IPC-D-322** Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

**IPC-D-325** Documentation Requirements for Printed Boards, Assemblies, and Support Drawings

**IPC-TM-650** Test Methods Manual

Method 2.1.1 Microsectioning

Method 2.1.6 Thickness, Glass Fabric

**IPC-SM-782** Surface Mount Design and Land Pattern Standard

**IPC-SM-785** Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

**IPC-MC-790** Guidelines for Multichip Module Technology Utilization

1. Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062

**IPC-2223** Sectional Design Standard for Flexible Printed Wiring and Flexible Wiring Assemblies  
Laminate/Prepreg

**IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards

**IPC-7074** Sectional Requirements for Fine Pitch & High Pin Count Component Mounting

**IPC-7075** Sectional Requirements for High Pin Count Area Array Component Mounting

**SMC-TR-001** An Introduction to Tape Automated Bonding Fine Pitch Technology

### 2.1.2 Underwriter's Labs<sup>2</sup>

**UL 746E Standard** Polymeric Materials, Materials Used in Printed Wiring Boards

### 2.1.3 PCMCIA/JEIDA<sup>3</sup>

**PC Card Standard** Physical Specification

### 2.1.4 Joint Industry Standards<sup>1</sup>

**J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies

**J-STD-012** Implementation of Flip Chip and Chip Scale Technology

**J-STD-013** Implementation of Ball and Array and Other High Density Technology

## 3.0 GENERAL REQUIREMENTS

General requirements **shall** be in accordance with the generic standard IPC-2221 and as follows:

**3.1 Test Requirement Considerations** Testing of substrates for PC cards may require individual board tooling. A minimum of two tooling holes should be provided on each board.

**3.1.1 Mechanical** Tooling holes may also be used for mechanical operations such as shearing, punching, routing, or repair of individual boards.

## 4.0 MATERIALS

Artwork compensation may be required to enhance registration.

**4.1 Material Selection** Material selection **shall** be in accordance with the generic standard IPC-2221 and as follows:

Materials should meet the requirements of IPC-L-125, IPC-FC-231, IPC-FC-232, IPC-FC-241 and IPC-4101. Special considerations for selection of substrates to be used for mounting of devices on to a PC card, or using a PC card as part of the packaged device may exceed the existing printed board standards. These may include:

- High Temperature and Pressure Moisture Resistance
- Substrate Hardness or Compliance at Joining Temperatures
- Thermal Conductivity
- Dielectric Breakdown resistance
- Compatability of the Metallurgy on the Device and Printed Board

**4.2 Bonding Material** Bonding materials **shall** be in accordance with the generic standard IPC-2221 and as follows:

Bonding materials described in the following paragraphs **shall** be used to bond layers of copper foil, bare laminate, copper clad laminate or heat-sinking planes to each other. Single ply and flex materials are widely used for bonding.

**4.2.1 Flexible PC Cards (bond ply)** Flexible adhesive bonding films are typically used in the bonding multiple flexible layers and attachments used for thermal management or structural support. These materials offer high bond strength to the flexible dielectrics. These bonding films may be formulated from low  $T_g$  resins to enhance adhesion and flexibility.

When flexible adhesive bonding films are used on PC cards, the material **shall** be in accordance with IPC-FC-232. The areas which require adhesive and those to be free of adhesive **shall** be defined on the master drawing.

**4.2.2 Adhesive Films** Adhesive films used for bonding heatsinks, stiffeners, etc., or as insulators, **shall** be in accordance with IPC-FC-232.

**4.3 Laminate Materials** Laminate materials **shall** be in accordance with the generic standard IPC-2221 and as follows:

**4.3.1 Rigid Laminates** Printed boards **shall** be fabricated from the laminate materials specified in Table 4-1 or UL 746E, or the applicable specification. When Underwriter's Labs (UL) requirements are imposed, the material used

2. Underwriter's Labs, 333 Pfingsten Avenue, Northbrook, IL 60062

3. PCMCIA, 1030 East Duane Avenue, Suite G, Sunnyvale, CA 94086