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ELECTRONICS INDUSTRIES

IPC-2225

Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

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A standard developed by IPC

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Developed by the MCM-L Design Standard Task Group (D-31c) of the
Rigid Printed Board Committee of IPC

APPROVED APRIL 14, 1999 BY



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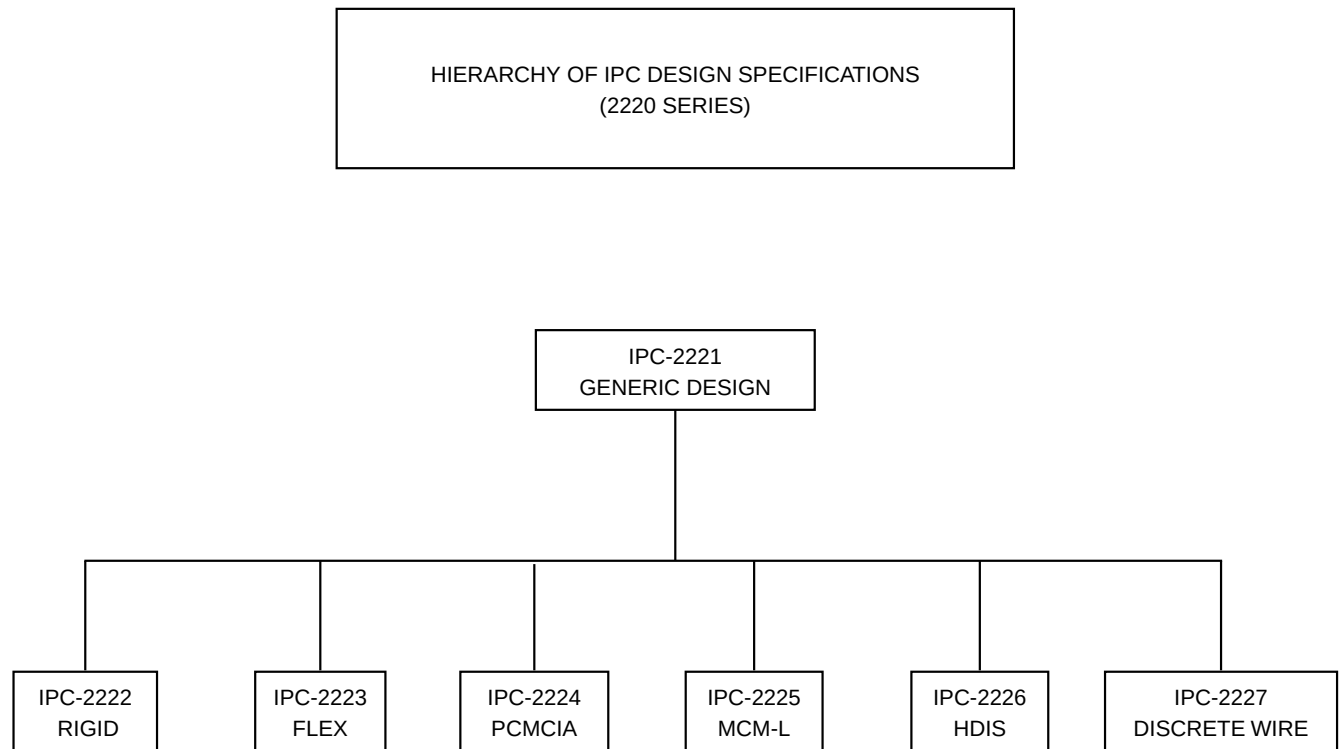
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FOREWORD

This standard is intended to provide information on the detailed requirements for organic Laminated Multichip Module (MCM-L) design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the unique requirements of those designs that use organic rigid (reinforced), organic flexible (unreinforced) materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting unpackaged die.

The information contained herein is intended to supplement generic design requirements identified in IPC-2221. When coupled with the generic design input, it should facilitate the selection process of the materials and the detailed organic structure fabrication technology necessary to meet the engineering design objectives.

The selected component mounting and interconnecting technology for the physical Mounting and Interconnection Structure (MIS) should be commensurate with the requirements provided and the specific focus of this sectional document.

A description of what is an MCM-L and what permutations can be accomplished by mixing other MCM technologies is important to understand to ensure proper design. A detailed description is also provided on the identification of the product in terms of the materials and processes used to manufacture the MCM-L. Other forms of multichip modules are identified in order to establish the relationship with

these technologies (i.e., MCM-C, MCM-D), and the design principles contained herein.

Differences between semiconductors, modules and boards relate to their application and are defined as:

ASIC Application Specific Integrated Circuit represents a semiconductor device intended to satisfy a unique complete circuit function.

ASEA Application Specific Electronic Assembly represents printed board assemblies consisting of electronic components attached to an interconnecting substrate, intended to perform a complete circuit or electronic function.

ASEM Application Specific Electronic Module represents a grouping of components intended as a subassembly or super-part that will be interconnected on an ASEA.

Because of the similarity between various techniques, an attempt to describe the variation between Chip-on-Board (COB) and Multichip Modules (MCM) is described to reflect that:

COB products are ASEAs intended as a complete electronic assembly, using unpackaged chips in whole or in part, which will perform a total electronic function. COB assemblies usually plug into a mother board. For example a PC card can be a COB assembly.

MCM products are ASEMs intended as a super-part or subassembly that will be mounted on an interconnecting structure or substrate.



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The processes and technologies used to fabricate multichip modules fall into three categories. These are described in many industry documents and are identified as MCM-L, MCM-C, and MCM-D. As the industry matures the need for mixing and matching of the processes have resulted in products being manufactured as interconnecting substrates for MCMs that combines the capabilities of each MCM type.

It is important to understand the similarities and differences of the three module types. These characteristics relate to the physical properties of the module (materials, conductor, vias, etc.) The processes used to manufacture the various modules are defined in the following:

MCM-L Multichip modules primarily using standard printed board manufacturing processes and materials, specifically dielectrics that are purchased from a supplier (laminator).

MCM-C Multichip modules primarily using ceramic base materials onto which the dielectric and conductor layers are applied either sequentially or co-fired.

MCM-D Multichip modules in which the materials, both dielectric and conductive, are added sequentially by the supplier to a mounting structure or substrate. Dielectric materials may be deposited in sheet or liquid form.

MCM-L PROCESSES

Material

Materials, specifically dielectrics, are purchased from a supplier (laminator). They may be clad or unclad, they may be unreinforced, reinforced with a separate material coated with resin, or reinforced through molecular cure.

Conductive Pattern

Both conductors and metallization in the vias may be formed by the following means:

- Chemical techniques (plating and etching)
- Screening techniques (conductive polymers)
- Sputtering (thin film metal deposition)

Hole Formation

Hole formation for through holes may use:

- Drilling
- Punching
- Lasers
- Etching (both ion and chemical)

Depending on the method of layering, some of the techniques may be used for blind or buried vias.

Layering

Layering is accomplished through lamination, either in a single operation or sequentially.

Surface Finish

Finishes may be applied to the surfaces of the conductive pattern for protection of the surface or for bonding of the unpackaged chips. Potential finishes include: gold, nickel, copper, tin-lead, solderability protective coating (OSPs), palladium or palladium alloy.

Additives

Special heat sinks or solid structures are added to the interconnecting structure to improve the Coefficient of Thermal Expansion (CTE) characteristics. The finished MCM-L may be conformal coated or otherwise encapsulated in order to protect the unpackaged chips.

MCM-C PROCESSES

Material

Materials are ceramic or glass-filled ceramic. Usually started in a green condition, the substrate and conductive paste are fired together. There are instances in which these materials are sequentially fired over fired ceramics.

Conductive Pattern

Conductors and vias are formed using conductive polymers (thick film) and fired.

Hole Formation

Holes are formed in the green condition by punching or using laser technology.

Layering

Layering is accomplished through co-firing or sequential firing of the original dielectric and conductive materials.

Surface Finish

The conductive surfaces are printed and then fired. Some potential metals are copper, gold, silver, palladium, tungsten, molybdenum.

Additives

Passivation is applied to the conductive surfaces opening the bonding sites for chip attachment. Chip protection is accomplished through hermetic case seals or a combination of gels and coatings.

MCM-D PROCESSES

Material

Materials, both dielectric and conductive, are added sequentially by the supplier to a mounting structure or substrate. Dielectric materials are deposited in sheet or liquid form.

Conductive Pattern

The conductive pattern may be created through sputtering, evaporation or electroless deposition.

Hole Formation

Holes are created using the following techniques:

- Ion etching (reactive)
- Laser piercing
- Photochemical etching

Layering

Layering is accomplished in a sequential manner, alternating the layers of dielectric with layers of conductive patterns interconnected with interstitial vias.

Surface Finish

Surface finishes contain the characteristics of the conductive pattern method of application.

Additives

Coatings may or may not be applied to protect the unpackaged chips.

MIXING TECHNOLOGIES

Mixing and matching of the three technologies and processes embodies the use of the letters that define the details

of the process. In order to relate the manufacturing sequence, a technique for identification has been defined that builds on the industry concepts used to describe chip on board (COB) methodology. Just as COB defines an assembly technique, using MCM-L processes on which MCM-D processes are added can be defined as MCM-D on MCM-L. A simplification of this principle is to replace the words “on” with a “/” and identify such a product as MCM-D/L. Other examples are MCM-L/C where a laminate is used on an MCM-C ceramic structure or MCM-D/C which uses deposited dielectric processes on ceramic materials and processes. See Figure A-1.

Future identification may include the structure of the MCM by providing an indication of the techniques involved in a fabrication sequence. An example could be an MCM-D/C/D, or DCD which would imply using the processes of deposited dielectric and conductive materials to both sides of a co-fired ceramic interconnection substrate. In this example the processes of MCM-C were completed. It is not a case of using MCM-D processes on a ceramic base. Standardization of these principles will be addressed in the future.

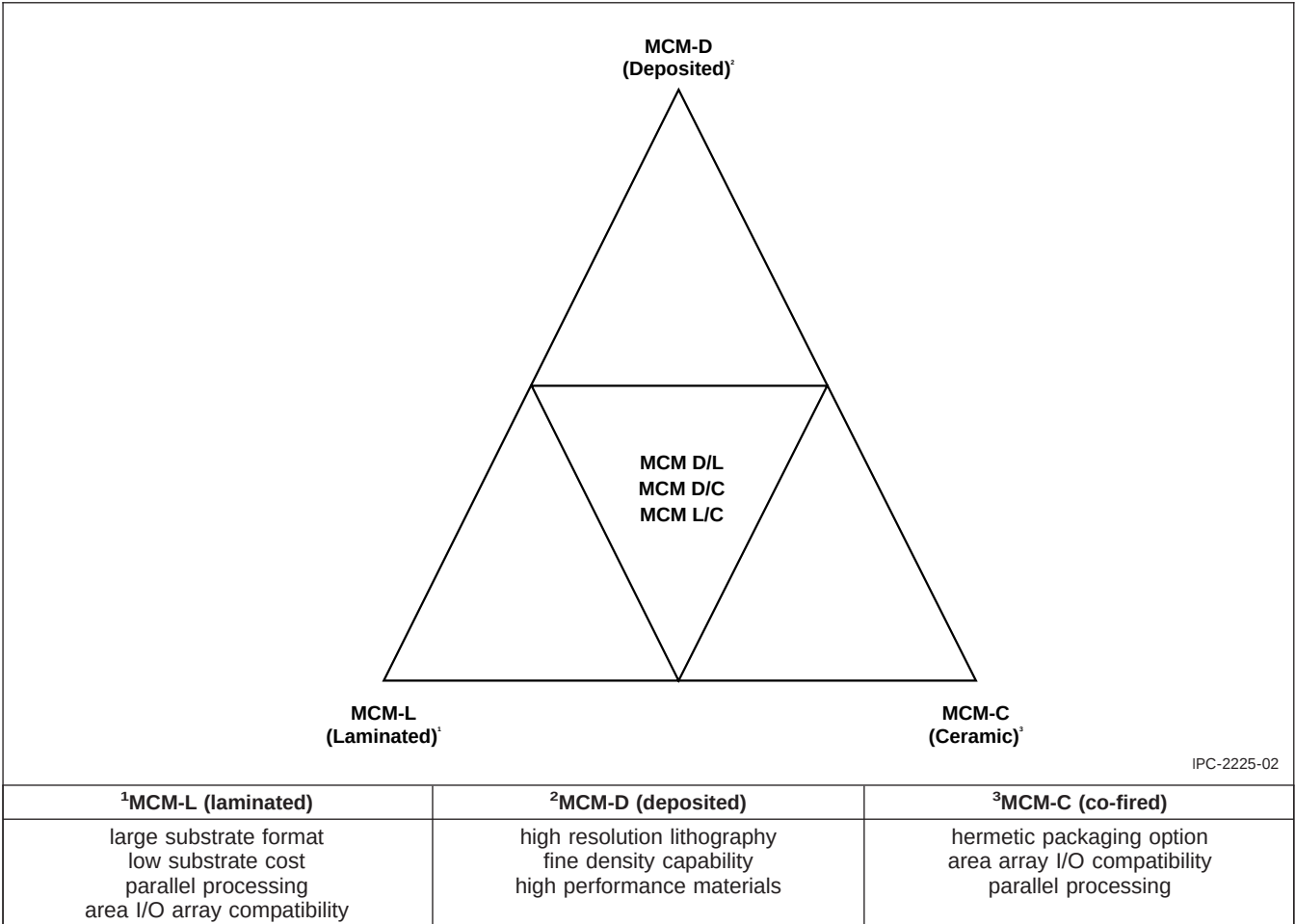


Figure A-1 Evolution of MCM Technologies

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Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

1.0 SCOPE

This standard establishes requirements and other considerations (thermal, electrical, electromechanical and mechanical) for the design of organic mounting structure used to interconnect chip components, which in combination form the completed functional Single Chip Module (SCM-L), MCM, or MCM-L assemblies.

1.1 Purpose The purpose of this standard is to establish design principles and recommendations that **shall** be used to produce the appropriate class of multichip module or assembly. Unique design requirements for multichip modules and multichip module assemblies intended for military electronic equipment applications will be noted as such, and **shall** be fabricated by a supplier that has been qualified by the appropriate agency unless otherwise agreed to contractually.

1.2 Documentation Hierarchy Document hierarchy shall be in accordance with generic standard IPC-2221.

1.3 Presentation Presentation shall be in accordance with the generic standard IPC-2221.

1.4 Interpretation Interpretation shall be in accordance with the generic standard IPC-2221.

1.5 Classification of Products Classification of products shall be in accordance with the generic standard IPC-2221 and as follows:

1.5.1 Assembly Types Assembly types are defined as:

Single-sided/Double-sided — Multiple bare and/or chip scale packaged die assemblies analogous to single and double sided printed board assemblies.

Cavity Structures — Multiple bare and/or chip scale packaged die assemblies in which the components are placed into cavities fabricated in the interconnecting structure.

Stacked Structure (includes 3-D memory packages) — Multiple bare and/or chip scale packaged die assemblies in which components are placed one on top of another.

Embedded Structures — Multiple bare and/or chip scale packaged die assemblies in which components are embedded within the interconnecting structure requiring lamination over bare die and subsequently interconnected.

Multi-Mounting Structure — Combination of any above assembly types.

1.5.2 Packaging Density The assembly of uncased or bare chips on substrates has become popular mostly due to the ability of such assemblies to reduce the area needed for interconnecting substrates. The ideal limit for such assembly would be to place all the chips tightly together, without any space in between. This would result in 100% of Packaging Efficiency, a ratio of silicon area to the substrate area. Naturally, 100% efficiency is not achievable, but this ratio is still useful in ranking various substrate construction of bare chip attachment methods.

Table 1-1 shows the different feature resolution capabilities, i.e., line widths and spacings, for the MCM-L mounting structure construction and their respective wiring density capability.

Table 1-1 MCM-L Wiring Capability

Typical wiring capability cm/cm ² layer	Typical signal plane	Total wiring capability cm/cm ²
Standard 15	4S 8S	60 30
Extended 25	4S 8S	100 200
Sequential 30-50	2S 4S	60/100 120/200

Table 1-2 tabulates the total substrate area needed to place 16 chips (10 mm x 10 mm) on a MCM-L mounting structure using four typical chip wiring methods.

Table 1-2 MCM-L Area (mm²) for 16 Chips (10 mm x 10 mm)

	Flip Chip	Wire Bond	Flip TAB	Reg TAB
MCM-L S/S	2500	6200	7000	8400
MCM-L D/S	1800	4300	4900	5900

1.5.3 Producibility Level Although multichip modules are usually high density interconnecting structures of bare chips, there are times when only a few bare chips are necessary to accomplish the goal of the multichip module designer. In these instances interconnection area relates to the amount of area of silicon die occupied on the module. Thus a general approximation has been made in the three levels as to the percentage of silicon area occupied on the interconnecting substrate.

The three MCM levels and their associated silicon area densities are:

Level A General Design Complexity—Preferred (<40% area density)

Level B Moderate Design Complexity—Standard (40 - 70% area density)