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IPC-2226

Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC-2226

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A standard developed by IPC

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Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

Developed by the HDI Design Subcommittee (D-41) of the HDI
Committee (D-40) of IPC

Users of this standard are encouraged to participate in the
development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the HDI Design Subcommittee (D-41) of the HDI Committee (D-40) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

1 SCOPE

This standard establishes requirements and considerations for the design of organic and inorganic high density interconnect (HDI) printed boards and its forms of component mounting and interconnecting structures.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of IPC-2221. In addition, when the core material reflects requirements identified in the sectional standards (IPC-2222, IPC-2223, IPC-2224 and IPC-2225), that information becomes a mandatory part of this standard.

The standard provides recommendations for signal, power, ground and mixed distribution layers, dielectric separation, via formation and metallization requirements and other design features that are necessary for HDI-advanced IC interconnection substrates. Included are trade-off analyses required to match the mounting structure to the selected chip set.

1.2 Document Hierarchy Document hierarchy **shall** be in accordance with the generic standard IPC-2221.

1.3 Presentation All dimensions and tolerances in this standard are represented in SI (metric) units with Imperial units following as a hard conversion for reference only (e.g., 0.01 cm [0.0039 in]).

1.4 Interpretation Interpretation **shall** be in accordance with the generic standard IPC-2221.

1.5 Classification of HDI Types Classification **shall** be by category in accordance with the requirements based on end use and as stated in 1.5.1 and 1.5.2 of this standard.

1.5.1 Core Types When HDI products utilize core interconnections, the core type(s) and their materials **shall** be in accordance with IPC-2222 for rigid and IPC-2223 for flexible core interconnections. For passive or constraining core boards the materials **shall** be in accordance with IPC-2221.

1.5.2 HDI Types The design designation system of this standard recognizes the six industry approved design types (see 5.2) used in the manufacture of HDI printed boards.

The designations in this section determine the HDI design type by defining the number and location of HDI layers that may or may not be combined with a substrate (core [C] or passive [P]).

For instance, an HDI printed board with two layers of HDI on one side of the core and one layer of HDI on the other side of the core would be 2 [C] 1.

The following definitions apply to all forms of HDI.

TYPE I 1 [C] 0 or 1 [C] 1 - with through vias connecting the outer layers (see 5.2.1).

TYPE II 1 [C] 0 or 1 [C] 1 - with buried vias in the core and may have through vias connecting the outer layers (see 5.2.2).

TYPE III ≥ 2 [C] ≥ 0 - may have buried vias in the core and may have through vias connecting the outer layers (see 5.2.3).

TYPE IV ≥ 1 [P] ≥ 0 - where P is a passive substrate with no electrical connection (see 5.2.4).

TYPE V Coreless constructions using layer pairs (see 5.2.5).

TYPE VI Alternate constructions (see 5.2.6).

1.6 Via Formation Via formation may be different from that considered in IPC-2221 since additional methods for via formation, in addition to drilled vias, will be used. The methods for via formation, lamination/coating and sequential layer process are covered in 9.1.1.

1.7 Design Features Figure 1-1 provides a color key to be used with all of the figures within this standard.

2 APPLICABLE DOCUMENTS

The following documents form a mandatory part of this standard and all requirements stated therein apply, unless modified in the section where they are invoked.

The revision of the document in effect at the time of solicitation **shall** take precedence over the applicable section of this document.

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

1. www.ipc.org

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Figure 1-1 Color Key

IPC-CF-152 Composite Metallic Materials Specification for Printed Wiring Boards

IPC-TM-650 Test Methods Manual²

2.1.1 Microsectioning, Manual Method

2.1.6 Thickness of Glass Fabric

IPC-SM-782 Surface Mount Design and Land Pattern Standard

IPC-2221 Generic Standard on Printed Board Design

IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC/JPCA-2315 Design Guide for High Density Interconnects (HDI) and Microvias

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC/JPCA-4104 Qualification and Performance Specification for Dielectric Materials for High Density Interconnect Structures (HDI)

IPC-4412 Specification For Finished Fabric Woven From "E" Glass for Printed Board

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Structures

IPC/JPCA-6801 Terms and Definitions, Test Methods and Design Examples for Build-Up/High Density Interconnects

IPC-9252 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-003 Solderability Test Methods for Printed Wiring Boards

J-STD-012 Implementation of Flip Chip and Chip Scale Technology

J-STD-013 Implementation of BGA and fine Pitch Technology

2.2 Underwriters Laboratories³

UL 746E Standard Polymeric Materials, Materials Used in Printed Wiring Boards

3 GENERAL REQUIREMENTS

3.1 Terms and Definitions Terms and definitions shall be as stated in IPC-T-50, IPC/JPCA-6801 and 3.1.1 through 3.1.8.

3.1.1 Microvia (Build-Up Via) A blind or subsequently buried hole that is ≤ 0.15 mm [0.00591 in] in diameter having a pad diameter that is ≤ 0.35 mm [0.0138 in] and formed either through laser or mechanical drilling, wet/dry etching, photo imaging or conductive ink-formation followed by a plating operation.

NOTE: Formed holes > 0.15 mm [0.00591 in] in diameter will be referred to as vias within this standard.

3.1.2 Capture Land (Via Top Land) Land where the microvia originates; varies in shape and size based on use (i.e., component mounting, via entrance and conductor).

3.1.3 Target Land (Via Bottom Land) Land on which a microvia ends.

2. Current and revised IPC Test Methods are available through IPC-TM-650 subscription and on the IPC Web site (www.ipc.org/html/testmethods.html).
3. www.ul.com

3.1.4 Stacked Vias A via formed by stacking one or more microvias on a buried via that provides an interlayer connection between three or more conductive layers.

3.1.5 Stacked Microvias A microvia formed by stacking one or more microvias on a microvia that provides an interlayer connection between three or more conductive layers.

3.1.6 Staggered Vias A microvia on one layer connecting to a via on a second layer, which are offset such that the land diameters are tangential or greater. Figure 3-1 displays an example of staggered vias.



Figure 3-1 Staggered Via

3.1.7 Staggered Microvias A set of microvias, formed on two or more different layers, which are offset such that the land diameters are tangential or greater. Figure 3-2 displays an example of staggered microvias.

3.1.8 Variable Depth Microvia/Via Microvias or vias formed in one operation, penetrating two or more HDI dielectric layers and terminating at one or more different layers.

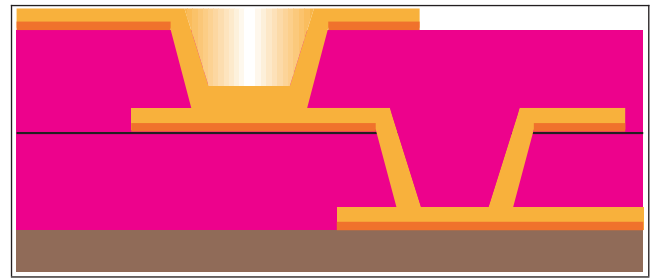


Figure 3-2 Staggered Microvias

3.2 Design Tradeoffs The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle of an HDI substrate.

Designing the physical features and selecting the materials for HDI substrates involve balancing the electrical, mechanical and thermal performance as well as the reliability, manufacturing and cost of the HDI board. The tradeoff checklist (see Table 3-1) identifies the effect of changing each of the physical features or materials. Costs of the board and assembly can be and frequently are affected by these same parameters.

How to read Table 3-1: As an example, the first row of the table indicates that if the dielectric thickness to ground is increased, the lateral crosstalk also increases and the resultant performance of the PCB is degraded (because lateral crosstalk is not a desired property).

Table 3-1 PCB Design/Performance Tradeoff Checklist

Design Feature (Increased)	Performance Parameter/Class ¹	If Design Feature is Increased	
		● = Increase ○ = Decrease Performance Parameter is	■ = Enhanced □ = Degraded Resulting Performance or Reliability Is
Dielectric Thickness to Ground	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	●	□
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/MP	●	□
Line Spacing	Lateral Crosstalk/EP	○	■
	Vertical Crosstalk/EP	○	■
	Physical Size/Weight/MP	●	□
	Electrical Isolation/MY	●	■
Coupled Line	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	●	□
Line Width	Lateral Crosstalk/EP	○	■
	Vertical Crosstalk/EP	●	□
	Characteristic Impedance/EP	○	Design Driven
	Physical Size or Weight/MP	●	Design Driven
	Signal Conductor Integrity/R	●	■
	Electrical Continuity/MY	●	■

Design Feature (Increased)	Performance Parameter/Class ¹	If Design Feature is Increased	
		● = Increase ○ = Decrease Performance Parameter is	■ = Enhanced □ = Degraded Resulting Performance or Reliability Is
Line Thickness	Lateral Crosstalk/EP	●	□
	Signal Conductor Integrity/R	●	■
Vertical Line Spacing	Vertical Crosstalk/EP	○	■
Z _o of PCB vs. Z _o of Device	Reflections/EP	○	■
Distance between Via Walls	Electrical Isolation/R	●	■
Annular Ring (capture and target land to via)	Producibility/MY	●	■
Signal Layer Quantity	Physical Size or Weight/MP	●	□
	Layer-to-Layer Registration/MY	○	□
Component I/O Pitch	Physical Size or Weight/MP	●	□
Board Thickness	Via Integrity/R	○	□
	Via Plating Thickness/MY	○	□
Copper Plating Thickness	Via Integrity/R	●	■
Aspect Ratio	Via Integrity/R	○	■
	Producibility/MY	○	■
Overplate (Nickel -Kevlar only)	Via Integrity/R	●	■
Via Diameter	Via Plating Thickness/MY	●	■
	Via Integrity/R	●	■
Laminate Thickness (Core)	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	○	■
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/MP	●	□
	Via Integrity/R	○	□
	Flatness Stability/MP	●	■
Prepreg Thickness (Core)	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	○	■
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/EP	●	□
	Via Integrity/R	○	□
Dielectric Thickness (HDI) Layer(s)	Lateral Crosstalk/EP	●	□
	Vertical Crosstalk/EP	○	■
	Characteristic Impedance/EP	●	Design Driven
	Physical Size or Weight/MP	●	□
	Via Integrity/R	○	□
	Flatness Stability/MP	○	□
Dielectric Constant	Reflections/EP	●	□
	Characteristic Impedance/EP	○	Design Driven
	Signal Speed/EP	○	Design Driven
CTE (out-of-plane)	Via Integrity/R	○	□
CTE (in-plane)	Solder Joint Integrity/R	○	□
	Signal Conductor Integrity/R	○	□
Resin T _g	Via Integrity/R	●	■
	Solder Joint Integrity/R	●	■
Copper Ductility	Via Integrity/R	●	■
	Signal Conductor Integrity/R	●	■



Design Feature (Increased)	Performance Parameter/Class ¹	If Design Feature is Increased	
		● = Increase ○ = Decrease Performance Parameter is	■ = Enhanced □ = Degraded Resulting Performance or Reliability Is
Copper Peel Strength	Component Land Adhesion to HDI Dielectric/R	●	■
Dimensional Stability	Layer-to-Layer Registration/MY	●	■
Resin Flow	PCB Resin Voids/MY	○	■
Rigidity	Flexural Modulus/MP	●	Design Driven
Volatile Content	PCB Resin Voids/MY	●	□

1. EP = Electrical Performance, MP = Mechanical Performance, MY = Manufacturability/Yield, R = Reliability.

3.3 Design Layout The layout generation process for HDI constructions should include a formal design review of layout details by as many affected disciplines within the company as possible, including fabrication, assembly, testing and those charged with thermal management. The approval of the layout by representatives of the affected disciplines will ensure that these production related factors have been considered in the design.

NOTE: Special consideration should be given to methods for ensuring the integrity of the electrical performance since the feature sizes are smaller than the capability of the presently available electrical continuity probing equipment. It is recommended that an electrical testing strategy be established for both prototype and production quantities before designing the HDI board.

3.3.1 Design Considerations The success or failure of any HDI construction depends on many interrelated design considerations, including:

- Materials selection (see Section 4).
- Manufacturing limitations are magnified for HDI substrates and restrict the capability to image, etch, form holes, plate and register. Screened or embedded components add to the complexity of the manufacturing process.
- Assembly technology used for attaching bare chips, related components and mixed technology for HDI substrates increase the complexity of the assembly operations.
- If an assembly is to be maintainable and repairable, consideration must be given to component land size and density, the selection of board and conformal coating materials and component placement for accessibility. Components with underfill typically can't be reworked.
- Finished product testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- End product assembly considerations that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement and the placement of brackets and other hardware.

- End product environmental conditions, such as ambient temperature, humidity, heat generated by the components, ventilation, shock and vibration.

3.4 Density Evaluation A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper) and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute in that they must route signals through conductors.

There are also limits to how much routing each process can accommodate. The factors that define the limits of their trace routing ability as a substrate are:

- Pitch/distance between vias or holes in the substrate.
- Number of traces that can be routed between those vias.
- Number of signal layers required.

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the trace routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However, area array components are more space conservative and allow coarser I/O pitches to be used (see Figure 3-3). See 10.4, which shows that very high I/O devices will require very dense substrate routing in order to interconnect the devices.

3.4.1 Routability Prediction Methods

3.4.1.1 Substrate Wiring Capacity Analysis After the approved schematic/logic diagrams, parts lists and end-product and testing requirements are provided and before the actual layout design is started, a wiring analysis-density evaluation should be conducted. This is based on all the parts contained in the parts list but excludes the interconnection conductors. The area usage is calculated by the

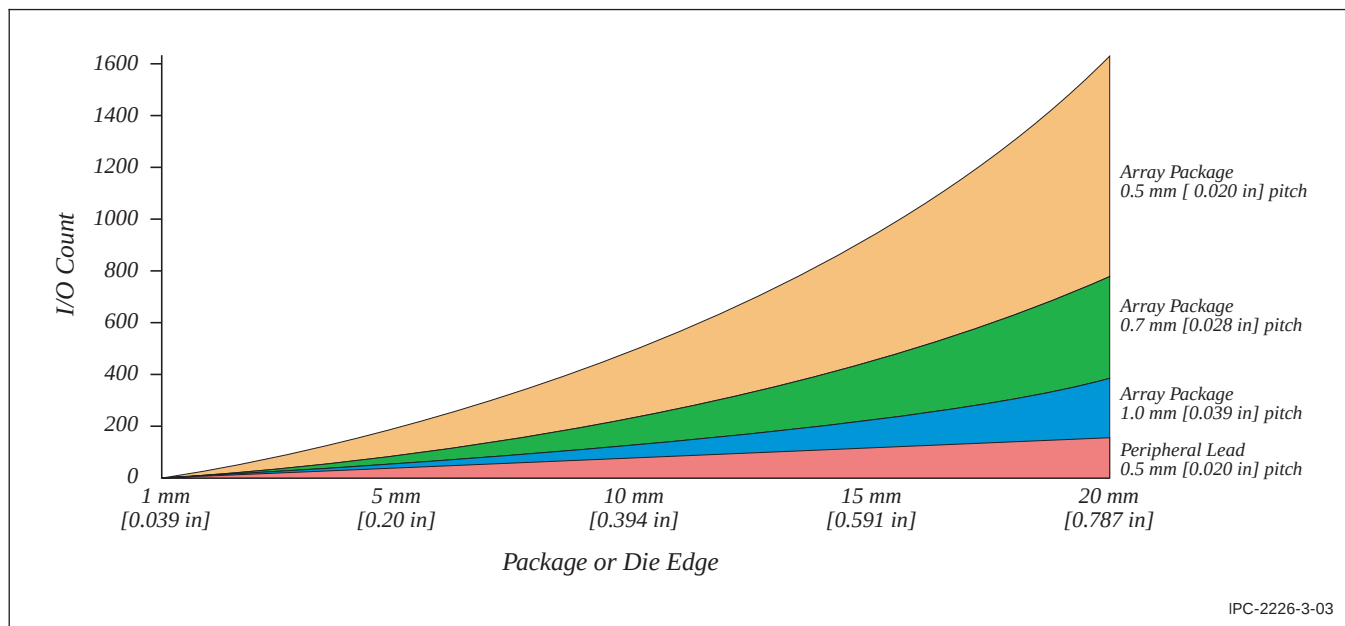


Figure 3-3 Package Size and I/O Count

largest space each part occupies, including the land pattern for mounting the components on the board and “keep out” areas for “step downs” of solder.

3.4.1.2 Wiring Capacity (W_C) Wiring capacity (W_C) is the most common definition of PCB density. This connectivity definition expresses the interconnection capability of a substrate type. It is established by determining the total length of conductors per square area of substrate (cm/cm^2 [in/in^2]) and is the total length of all conductors in all layers of the substrate divided by the area.

3.4.2 Design Basics Channel width and conductors per channel are design layout terms that refer to the distance between vias and/or component lands (channel width) and the maximum number of conductors that can be routed through each channel (conductors per channel). The feature pitch (center-to-center distance) and the size of the feature (annular ring or land size) define the channel width (see Figure 3-4 for these dimensions). The number of conductors per channel is determined by the channel width and conductor width and spacing required to meet the electrical performance of the circuit(s).

A more difficult package to include within the basic substrate design is a BGA package. The difficulty involves fan-out conductors as well as routing and via grids. Figure 3-5 provides a routing diagram as well as defining the relevant segments of the diagram.

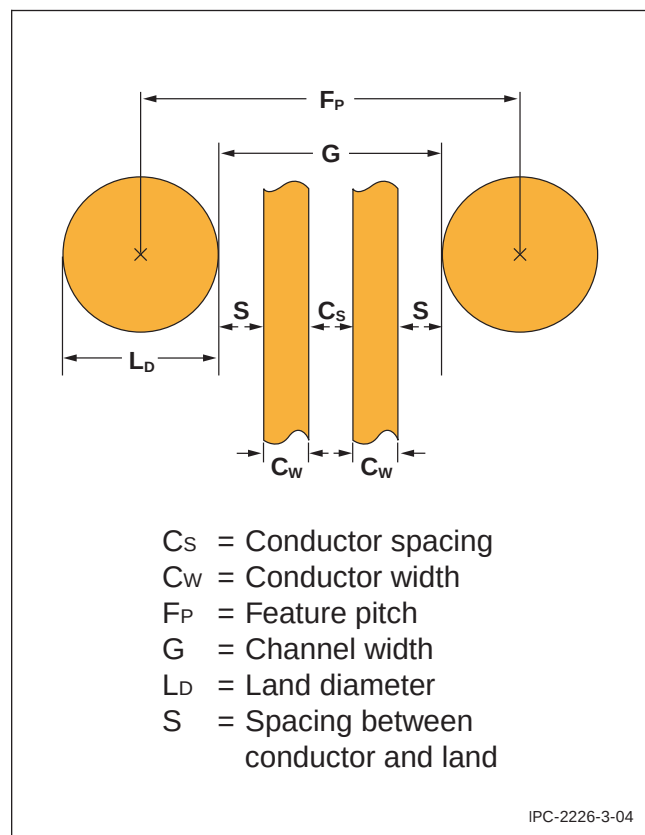


Figure 3-4 Feature Pitch and Feature Size Defining Channel Width

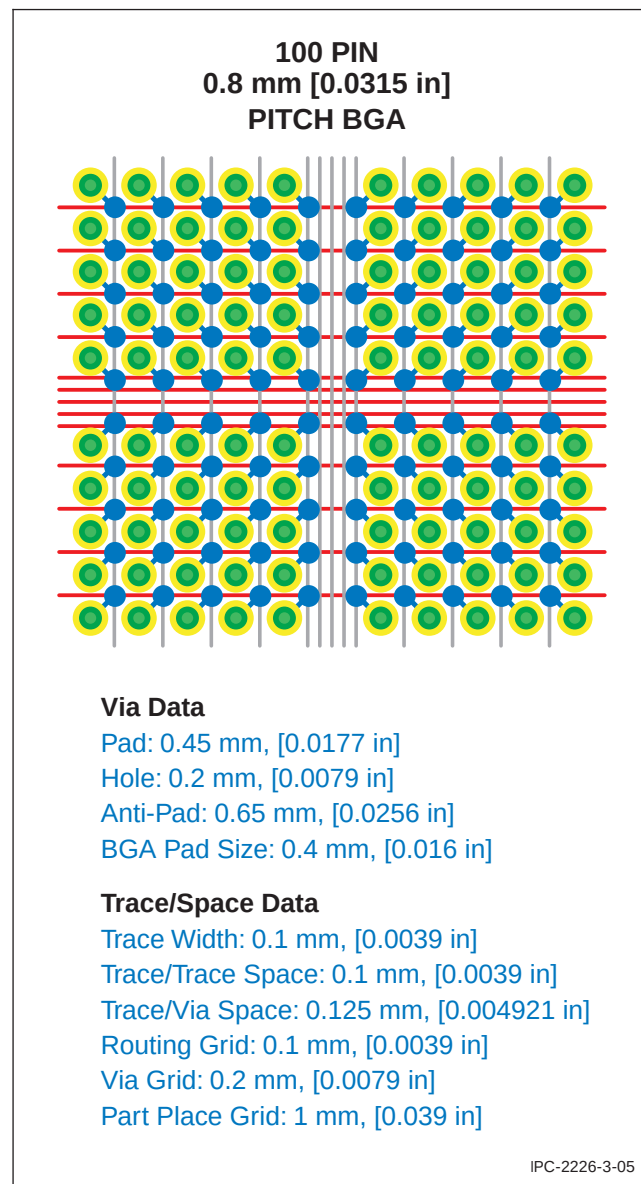


Figure 3-5 Routing and Via Grid for BGA Package

It is important to note that the land size for a microvia feature is determined, rather than simply selected, as discussed in the following.

Manufacturers successfully use a wide variety of dielectrics for microvia boards, ranging from conventional glass-reinforced epoxy to ultra-thin unreinforced materials such

as resin coated copper foil. The product's end-use environment and expected operating life, plus certain needed board-level attributes (e.g., dielectric withstand voltage, resin content to fill buried vias or avoid resin starvation, etc.) may require a particular dielectric type and/or thickness for the microvia layer. However, before the microvia diameter can be determined, the designer must select the thickness and type of dielectric for the microvia layer of the board to be built.

In addition, a suitable value for the aspect ratio of the blind microvia is also needed. The aspect ratio is the ratio of the length of the hole to the diameter of the hole (L/D). Acceptable values for aspect ratio are somewhat board vendor dependent and indicative of the hole configuration the vendors can form and plate reliably and consistently. At the time this document was prepared, typical aspect ratios range from about 0.5 to 0.85, although much effort is being expanded to push this value above 1.0 (see Section 5).

Outer foil thickness should be known or estimated.

The required as-formed diameter of the microvia is calculated as shown in Equation 1.

$$\text{Microvia Diameter} = (j + f)/(A_r) \quad [\text{Equation 1}]$$

Where:

j = Dielectric thickness on outer layer

f = Outer foil thickness

A_r = Aspect ratio

The target pad and capture pad diameters are determined by adding two annular ring widths and a fabrication allowance to the as-formed diameter of the microvia. The required fabrication allowance is a function of material behavior and fabrication process tolerances. See Section 5 for further explanation.

It is important to consider these factors before conducting the wiring assessment to ensure realistic results for the type of board to be fabricated. Also note that conductor width and spacing (and required dielectric thickness) discussed in sections 4 and 5 may not be the same for Type I and Type II boards, due to plating performed on layer 2 and layer n-1 in the Type II board (see 5.2.2).

Examples of various feature pitch and conductors per channel combinations are shown in Figure 3-6.

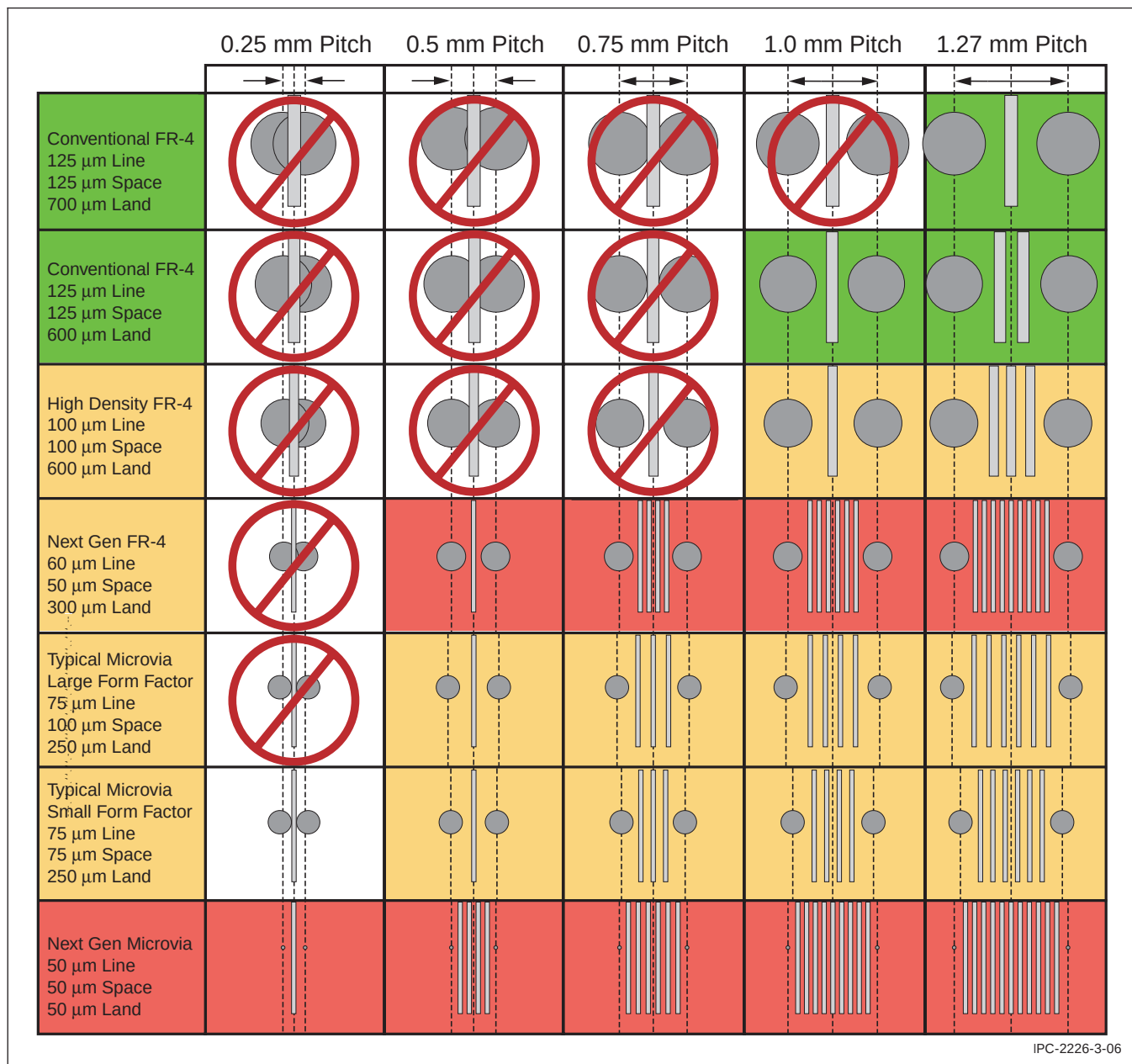


Figure 3-6 Feature Pitch and Conductor Per Channel Combinations

4 MATERIALS

4.1 Material Selection Material type and construction is extremely important in designing and manufacturing HDI boards.

If a core substrate is required for the HDI board, selection of the material(s) **shall** be as stated in IPC-2221. The selection of HDI materials **shall** adhere to the end product requirements. Established materials and their end product requirements are specified in IPC/JPCA-4104 which groups materials into slash sheets that are generic in nature. Due to the changing nature of this technology, there may be acceptable materials that are not yet specified in IPC/JPCA-4104.

4.1.1 HDI Material Options It is important to research the various products to choose the one best meeting the design requirements. The attributes that should be considered are:

- Moisture absorption
- Fire retardancy
- Electrical properties
- Mechanical properties
- Thermal properties

The designer and fabricator should concurrently review material selection for cost, performance and producibility.

New materials or desired combinations of materials should be reviewed with the substrate fabricator to ensure the end product will meet the requirements of the relevant certification body (e.g., UL, CSA, CE, etc.).

4.1.2 Designation System The following system identifies materials used for HDI substrates. This is a general identification system and does not in any way imply that all the permutations of properties and forms exist. Each specification sheet in IPC/JPCA-4104 outlines engineering and performance data for materials that can be used to manufacture HDI substrates. These materials include dielectric insulators, conductors and dielectric/conductor combinations.

The materials contained in IPC/JPCA-4104 represent general material categories. As new materials become available, they can be added to future revisions. Users and material developers are encouraged to supply information on new materials for review by the IPC Microvia/High Density Interconnect Materials Subcommittee (D-42). Users who wish to invoke IPC/JPCA-4104 for materials not listed **shall** list a zero for the specification sheet number (IPC-4104/0).

The designation system recognizes three general material types used in manufacturing HDI:

- Dielectric insulators only
- Conductors only
- Combinations of conductors and insulators

The first level of the designation system is the material type:

Level 1 Material Type

Dielectric Insulator = IN

Conductor = CD

Conductor and Insulator = CI

The other levels used to designate a particular material depend upon Level 1. Table 4-1, Table 4-2 and Table 4-3 illustrate the designation system for each of the material types. The designation listed in the specification sheets can be used to determine the exact material construction by first looking at the Level 1 designation (IN, CD or CI) and then looking in the correct section (4.1.2.1, 4.1.2.2. or 4.1.2.3) for that material type. These sections contain the description of the remaining designation levels with an example table to aid in deciphering the designation.

The default designations are nonphotoimageable and unreinforced. They will not be used as descriptors for simplicity (see Table 4-1, Table 4-2 and Table 4-3).

4.1.2.1 Dielectric Insulator Designations

Example: The sample from Table 4-1 will be written as IN F 1 N 1.

Note: The letter “X” **shall** be entered into the designation where an item is not specified and does not matter.

Level 1 Material Type = IN

Level 2 Form of Dielectric

Liquid = L

Paste = P

Film = F

Reinforced (Prepreg) = R

Adhesive Coated Film = C

Level 3 Photosensitivity

Nonphotoimageable = 1

Photoimageable = 2

Level 4 Reinforcement

Woven Glass = G

Nonwoven Matte Glass = M

Nonwoven Aramid = A

Table 4-1 Sample Dielectric Insulator Designation

IPC-4104	Level 1	Level 2	Level 3	Level 4	Level 5
4104 / S	IN	F	1	N	1
Where S is Specification (Slash) Sheet Number	Material Type	Form of Dielectric	Photosensitivity	Reinforcement	Chemical Composition

Table 4-2 Sample Conductor Designation

IPC-4104	Level 1	Level 2	Level 3
4104 / S	CD	P	3
Where S is Specification (Slash) Sheet Number	Material Type	Form of Conductor	Type of Form

Table 4-3 Dielectric with Conductor Designations

IPC-4104	Level 1	Level 2	Level 3	Level 4	Level 5	Level 6	Level 7
4104 / S	CI	F	1	N	1	CF	1
Where S is Specification (Slash) Sheet Number	Material Type	Form of Dielectric	Photo-sensitivity	Reinforce-ment	Chemical Composition	Type of Metal/Conductor	Type of Conduction

e-PTFE (Expanded PTFE) = E

None = N

Other = O

Level 5 Chemical Composition

Epoxy = 1

Epoxy Blends = 2

Polyimide = 3

Polyester = 4

Acrylics = 5

BT Resins = 6

Cyanate Ester = 7

BCB (Benzocyclobutene) = 8

PEEK (polyetheretherketone) = 9

FEP (fluorinated ethylene propylene) = 10

LCP (liquid crystal polymer) = 11

PPE (Polyphenylene Ether) = 12

PNB (Polynorborene) = 13

Other = O

4.1.2.2 Conductor Designations

Note: The letter “X” **shall** be entered into the designation where an item is not specified and does not matter.

Level 1 Material Type = CD

Level 2 Form of Conductor

Metal Foil = F

Solution Plate = S

Printable/Paste = P

Vacuum Deposit = V

Other = O

Level 3 Type of Form

Copper = 1

Nickel = 2

Other = 3

Solution Plate (S):

Electrolytic Cu = 1

Electroless Cu = 2

Direct Plate Initiation = 3

Other Metal Plate = 4

Printable Paste (P):

Silver Particle Loaded = 1

Other Conductive Particle Loaded = 2

Transient Liquid Phase Sintering = 3

Organometallic = 4

Conductive Polymers = 5

Vacuum Deposited (V):

Evaporative = 1

Sputtering = 2

Other = 3

4.1.2.3 Dielectric with Conductor Designations

Note: The letter “X” **shall** be entered into the designation where an item is not specified and does not matter.

Level 1 Material Type = CI

Level 2 Form of Dielectric

Liquid = L

Paste = P

Film = F

Reinforced = R

Adhesive Coated Film = C

Level 3 Photosensitivity

Nonphotoimageable = 1

Photoimageable = 2

Level 4 Reinforcement

Woven Glass = G

Nonwoven Matte Glass = M

Nonwoven Aramid = A

e-PTFE (Expanded PTFE) = E

None = N

Other = O

Level 5 Chemical Composition

Epoxy = 1

Epoxy Blends = 2

Polyimide = 3

Polyester = 4

Acrylics = 5

BT Resins = 6

Cyanate Ester = 7

BCB = 8

PEEK = 9

FEP = 10

LCP = 11

PPE = 12

PNB = 13

Other = 0

Level 6 Type of Metal/Conductor

Copper Foil = CF

Copper Particle/Post = CP

Silver Particle/Post = SP

Nickel Particle/Post = NP

Alloy Particle/Post = AP

Other Particle/Post = OP

Level 7 Type of Conduction

In Plane (x-y) = 1 (e.g., Copper Foil)

Through Plane (z-axis) = 2 (Anisotropic
Conductive Adhesive)

Both = 3 (e.g., Post)