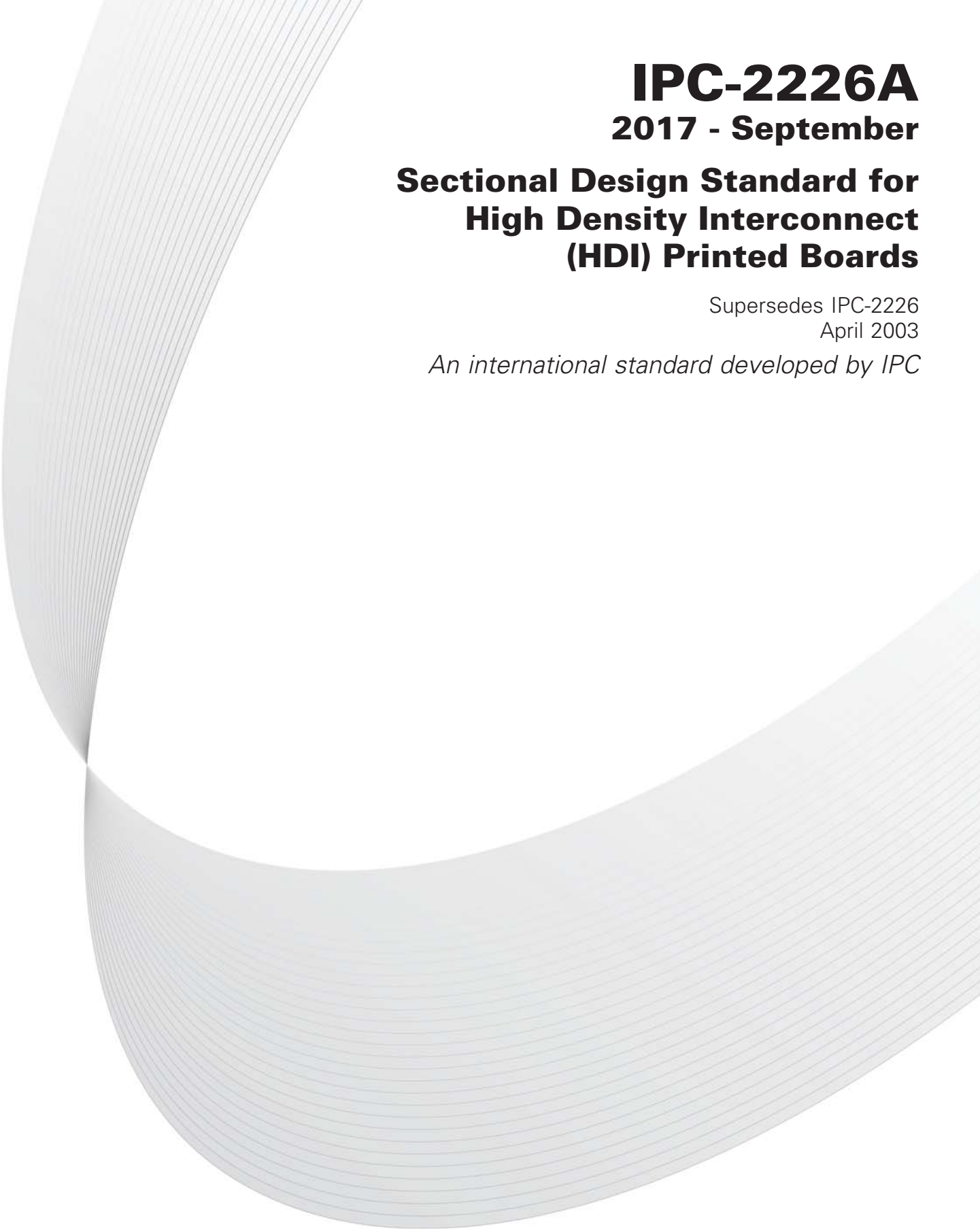




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Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

Supersedes IPC-2226

April 2003

An international standard developed by IPC

Association Connecting Electronics Industries



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IPC-2226A

Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

Developed by the IPC-2221/2222 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of IPC

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Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

1 SCOPE

This standard establishes requirements and considerations for the design of organic and inorganic high density interconnect (HDI) printed boards and structures for component mounting and interconnections.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of IPC-2221. In addition, when the core material reflects requirements identified in the sectional standards (IPC-2222, IPC-2223, and IPC-2225), that information becomes a mandatory part of this standard.

The standard provides recommendations for signal, power, ground, and mixed distribution layers, dielectric separation, via formation and metallization requirements and other design features that are necessary for HDI substrates.

1.2 Document Hierarchy Document hierarchy **shall** be in accordance with the generic standard IPC-2221.

1.3 Presentation All dimensions and tolerances in this standard are represented in SI (metric) units with Imperial units following as a hard conversion for reference only (e.g., 0.01 cm [0.0039 in]). In instances of metric based components, dimensions in this standard are represented in SI (metric) units only to prevent an accumulation of errors in rounding with Imperial units. When using predominately metric components, IPC highly recommends doing design layout in a metric environment.

1.4 Interpretation Interpretation **shall** be in accordance with the generic standard IPC-2221.

1.5 Classification of HDI Types Classification **shall** be by category in accordance with the requirements based on end use and as stated in 1.5.1 and 1.5.2 of this standard.

1.5.1 Core Types When HDI products utilize core interconnections, the core type(s) and their materials **shall** be in accordance with IPC-2222 for rigid and IPC-2223 for flexible core interconnections. For passive or constraining core boards the materials **shall** be in accordance with IPC-2221.

1.5.2 HDI Types The design designation system of this standard recognizes the six industry approved design types (see 5.2) used in the manufacture of HDI printed boards. The designations in this section determine the HDI design type by defining the number and location of HDI layers that may or may not be combined with a substrate (core [C] or passive [P]).

For instance, an HDI printed board with two layers of HDI on one side of the core and one layer of HDI on the other side of the core would be 2 [C] 1.

The following definitions apply to all forms of HDI. Blind vias may exist in all types.

TYPE I 1 [C] 0 or 1 [C] 1 – with through vias connecting the outer layers (see 5.2.1).

TYPE II 1 [C] 0 or 1 [C] 1 – with buried vias in the core and may have through vias connecting the outer layers (see 5.2.2).

TYPE III ≥ 2 [C] ≥ 0 – may have buried vias in the core and may have through vias connecting the outer layers (see 5.2.3).

TYPE IV ≥ 1 [P] ≥ 0 – where P is a passive substrate with no electrical connection (see 5.2.4).

TYPE V Coreless constructions using layer pairs (see 5.2.5).

TYPE VI Alternate constructions (see 5.2.6).

1.6 Producibility Level When appropriate, this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Producibility-Preferred
 Level B Moderate Design Producibility-Standard
 Level C Least Design Producibility-Reduced

The producibility levels **shall not** to be interpreted as a design requirement, but rather as a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the numerous tables are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that **shall** be controlled on the end item **shall** be specified on the master drawing of the printed board or the printed board assembly drawing.

1.7 Via Formation Via formation may be different from that considered in IPC-2221 since additional methods for via formation, in addition to drilled vias, will be used. The methods for via formation, lamination/coating, and sequential layer process are covered in 9.1.1.

1.8 Design Features Figure 1-1 provides a color key to be used with all of the figures within this standard.

2 APPLICABLE DOCUMENTS

The following documents form a mandatory part of this standard and all requirements stated therein apply, unless modified in the section where they are invoked.

The revision of the document in effect at the time of solicitation **shall** take precedence over the applicable section of this document.

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-2152 Standard for Determining Current Carrying Capacity in Printed Board Design

IPC-2221 Generic Standard on Printed Board Design

IPC-2222 Sectional Design Standard for Rigid Organic Printed Boards

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

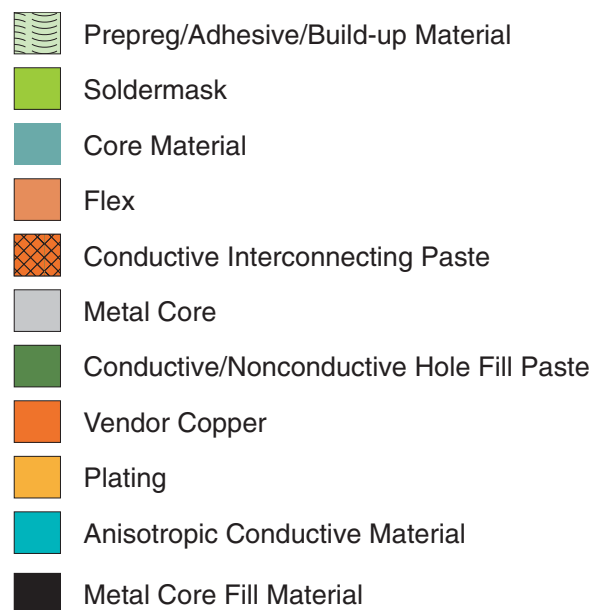
IPC/JPCA-4104 Qualification and Performance Specification for Dielectric Materials for High Density Interconnect Structures (HDI)

IPC-4204 Flexible Metal-Clad Dielectrics for Use in Fabrication of Flexible Printed Circuitry

IPC-7092 Design and Assembly Process Implementation for Embedded Components

IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7351 Generic Requirements for Surface Mount and Land Pattern Design Standard



IPC-2226a-1-01

Figure 1-1 Color Key

1. www.ipc.org

3 GENERAL REQUIREMENTS

3.1 Terms and Definitions Terms and definitions **shall** be as stated in IPC-T-50 and 3.1.1 through 3.1.6.

3.1.1 Microvia Defined as a blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 3-1, terminating on or penetrating a target land, with a total depth (X) of no more than 0.25 mm [0.0098 in] measured from the structure's capture land foil to the target land.

3.1.2 Capture Land (Via Top Land) The external land portion during formation of a blind or buried microvia. (See Figure 3-2).

3.1.3 Target Land (Via Bottom Land) The internal land portion during formation of a blind or buried microvia. (See Figure 3-2).

3.1.4 Stacked Microvias A structure formed by vertically aligning microvias directly on top of each other (or on top of a buried via). Refer to cautionary statement in 9.2.2. See Figure 9-6 and Figure 9-7 for examples of stacked structures.

3.1.5 Staggered Microvias A structure formed by offsetting microvias laterally off each other in the vertical direction (or off a buried via). See Figure 3-3 and Figure 3-4 for examples of staggered structures.

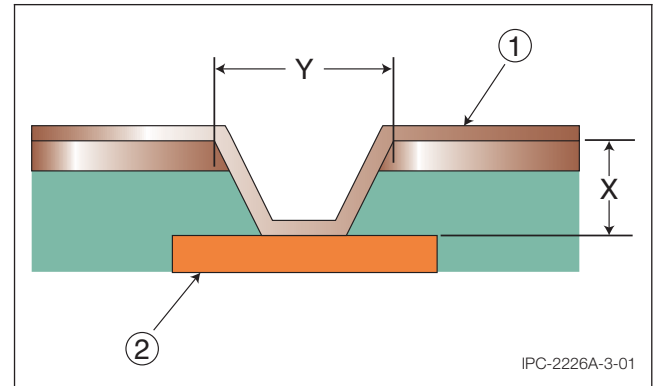


Figure 3-1 Microvia Definition

Note 1. Capture Land.

Note 2. Target Land.

Note 3: X/Y = Microvia Plating Aspect Ratio, with $X \leq 0.25$ mm [0.00984 in] and aspect ratio $\leq 1:1$.

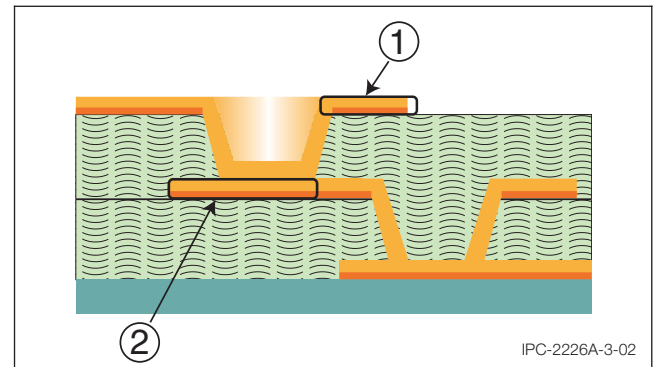


Figure 3-2 Capture and Target Land (Microvia)

1. Capture Land

2. Target Land

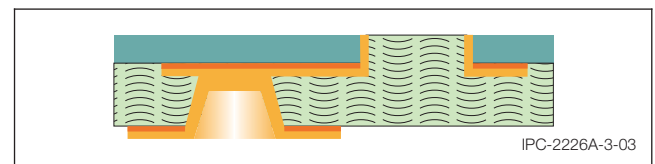


Figure 3-3 Staggered Via

Note 1. Additional layers for the buried via not shown.

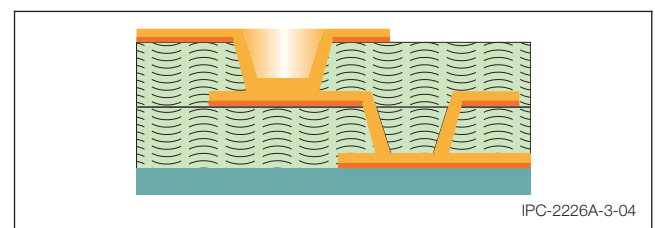


Figure 3-4 Staggered Microvias

3.1.6 Variable Depth Microvia Microvias formed in one operation, spanning two or more dielectric layers as shown in Figure 3-5. This structure may be blind or buried.

3.2 Design Tradeoffs The information contained in this section describes the general parameters to be considered by all disciplines prior to and during the design cycle of an HDI substrate.

Designing the physical features and selecting the materials for HDI substrates involve balancing the electrical, mechanical, and thermal performance as well as the reliability, manufacturing, and cost of the HDI board. The tradeoff checklist provided in Table 3-1, intended to supplement the corresponding table in IPC-2221 for HDI printed boards, identifies the effect of changing each of the physical features or materials. Costs of the board and assembly can be and frequently are affected by these same parameters.

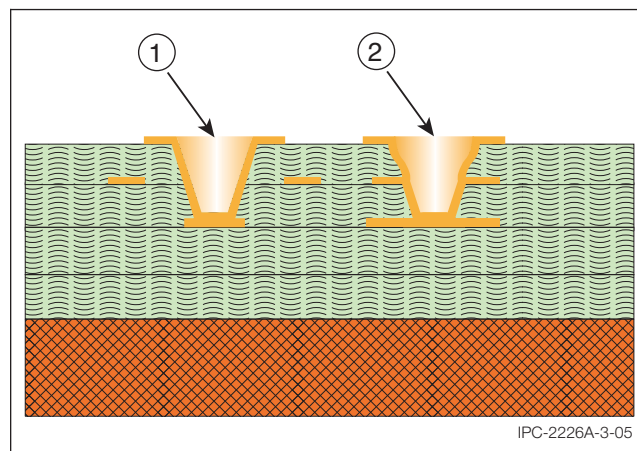


Figure 3-5 Variable Depth Microvias

Note 1. Skip Via.

Note 2. Variable Depth Microvia.

How to read Table 3-1: As an example, the first row of the table indicates that if the microvia dielectric thickness is increased, the lateral crosstalk also increases and the resultant performance of the printed board is degraded (because lateral crosstalk is not a desired property).

Table 3-1 PCB Design/Performance Tradeoff Checklist¹

Design Feature	Class Electrical Performance (EP) Mechanical Performance (MP) Reliability (R)	Performance Parameter	Impact if Design Feature is Increased			
			Performance Parameter is:		Resulting Performance or Reliability is:	
			Increased	Decreased	Enhanced	Degraded
Microvia Dielectric Thickness ²	EP	Lateral Crosstalk	X			X
	EP	Vertical Crosstalk		X	X	
	EP	Characteristic Impedance	X		Design Driven	
	MP	Physical Size/Weight	X			X
	R	Via Integrity		X		X
	MP	Flatness Stability		X		X

Note 1: This table is to be used in conjunction with Table 3-1 of the base IPC-2221 standard.

Note 2: There is a trade-off between thin dielectrics preferred when using microvias and the volume that needs to be resin filled on plated layers.

3.3 Design Layout The layout generation process for HDI constructions should include a formal design review of layout details by as many affected disciplines within the company as possible, including fabrication, assembly, testing, and those charged with thermal management. The approval of the layout by representatives of the affected disciplines will ensure that these production related factors have been considered in the design.

Note: Special consideration should be given to methods for ensuring the integrity of the electrical performance since the feature sizes are smaller than the capability of the presently available electrical continuity probing equipment. It is recommended that an electrical testing strategy be established for both prototype and production quantities before designing the HDI board.

3.3.1 Design Considerations The cost or producibility of any HDI construction depends on many interrelated design considerations, including:

- Materials selection (see Section 4).
- Manufacturing limitations are magnified for HDI substrates and restrict the capability to image, etch, form holes, plate, and register. Screened or embedded components add to the complexity of the manufacturing process.
- Assembly technology used for attaching bare chips, related components, and mixed technology for HDI substrates increase the complexity of the assembly operations.
- If an assembly is to be maintainable and repairable, consideration must be given to component land size and density, the selection of board and conformal coating materials, and component placement for accessibility. Components with underfill typically can't be reworked.
- Finished product testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- End product assembly considerations that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement, and the placement of brackets and other hardware.
- When microvias are placed in pads intended to be soldered (via-in-pad), the holes should be filled. Vias can be filled and plated over or filled with copper to yield an acceptable solderable surface. If the vias are not filled, the volume of the microvia will "steal" solder from the intended solder joint. The air, which is entrapped after solder paste has been applied, is also likely to out gas during the reflow process and create voids in the solder joints.
- End product environmental conditions, such as ambient temperature, humidity, heat generated by the components, ventilation, shock, and vibration.

3.4 Density Evaluation A wide variety of materials and processes have been used to create substrates for electronics over the last half century, from traditional printed circuits made from resins (i.e., epoxy), reinforcements (i.e., glass cloth or paper), and metal foil (i.e., copper), to ceramics metallized by various thin and thick film techniques. However, they all share a common attribute in that they must route signals through conductors.

There are also limits to how much routing each process can accommodate. The factors that define the limits of their conductor routing ability as a substrate are:

- Pitch/distance between vias or holes in the substrate
- Number of conductors that can be routed between those vias
- Number of signal layers required.

In addition, the methods of producing blind and buried vias can facilitate routing by selectively occupying routing channels. Vias that are routed completely through the printed board preclude any use of that space for routing on all conductor layers.

These factors can be combined to create an equation that defines the conductor routing ability of a technology. In the past, most components had terminations along the periphery on two or more sides. However, area array components are more space conservative and allow coarser I/O pitches to be used. See 3.4.3, which shows that very high I/O devices will require very dense substrate routing in order to interconnect the devices.

3.4.1 Routability Prediction Methods

3.4.1.1 Substrate Wiring Capacity Analysis After the approved schematic/logic diagrams, parts lists, and end-product and testing requirements are provided, and before the actual layout design is started, a wiring analysis-density evaluation should be conducted. This is based on all the parts contained in the parts list but excludes the interconnection conductors. The area usage is calculated using the largest space each part occupies, including the land pattern for mounting the components on the printed board and "keep out" areas for "step downs" of solder.

3.4.1.2 Wiring Capacity (W_C) Wiring capacity (W_C) is the most common definition of printed board density. This connectivity definition expresses the interconnection capability of a substrate type. It is established by determining the total length of conductors per square area of substrate (cm/cm^2 [in/in^2]), and is the total length of all conductors in all layers of the substrate divided by the area.

3.4.2 Design Basics Channel width and conductors per channel are design layout terms that refer to the distance between vias and/or component lands (channel width) and the maximum number of conductors that can be routed through each channel (conductors per channel). The feature pitch (center-to-center distance) and the size of the feature (annular ring or land size) define the channel width (see Figure 3-6 for these dimensions). The number of conductors per channel is determined by the channel width and conductor width and spacing required to meet the electrical performance of the circuit(s).

It is important to note that the land size for a microvia feature is determined, rather than simply selected, as discussed in the following.

Manufacturers successfully use a wide variety of dielectrics for microvia printed boards, ranging from conventional glass-reinforced epoxy to ultra-thin unreinforced materials such as resin coated copper (RCC) foil. The product's end-use environment and expected operating life, plus certain needed board-level attributes (e.g., dielectric withstanding voltage, resin content to fill buried vias or avoiding resin starvation, etc.), may require a particular dielectric type and/or thickness for the microvia layer. However, before the microvia diameter can be determined, the designer must select the thickness and type of dielectric for the microvia layer of the printed board to be built.

In addition, a suitable value for the aspect ratio of the blind microvia is also needed. The aspect ratio is the ratio of the length of the hole to the diameter of the hole (L/D). Acceptable values for aspect ratio are somewhat printed board fabricator dependent and indicative of the hole configuration the fabricator can form and plate reliably and consistently.

Outer foil thickness should be known or estimated.

The aspect ratio is derived by the formula as shown in Equation 1.

$$A_r = (j + f) / \text{Microvia diameter} \quad [\text{Equation 1}]$$

Where:

j = Dielectric thickness on outer layer

f = Outer foil thickness

A_r = Aspect ratio

Note: Microvia diameter is measured at the capture land.

Typical microvia aspect ratios range from 0.5 - 0.85:1, to a maximum of 1:1. Aspect ratios greater than 1:1 fall outside the definition in IPC-T-50 for microvias; acceptance requirements **shall** be defined in procurement documentation or As Agreed Between User and Supplier (AABUS).

Note: As of the publication date of this document, there is insufficient reliability data to recommend aspect ratios greater than 1:1 for Class 2 and Class 3 products.

The target pad and capture pad diameters are determined by adding two annular ring widths and a fabrication allowance to the as-formed diameter of the microvia. The required fabrication allowance is a function of material behavior and fabrication process tolerances. See Section 5 for further explanation.

It is important to consider these factors before conducting the wiring assessment to ensure realistic results for the type of printed board to be fabricated. Also note that conductor width and spacing (and required dielectric thickness) discussed in Section 4 and Section 5 may not be the same for Type I and Type II HDI printed boards, due to plating performed on layer 2 and layer n-1 in the Type II HDI printed board (see 5.2.2).

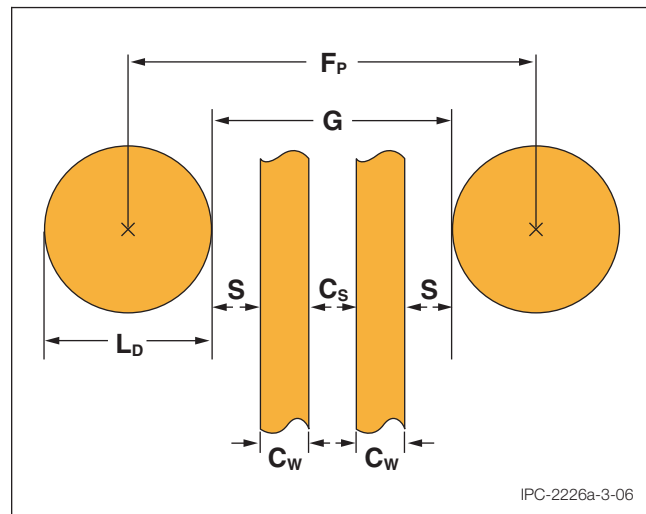


Figure 3-6 Feature Pitch and Feature Size Defining Channel Width

C_s = Conductor spacing

C_w = Conductor width

F_p = Feature pitch

G = Channel width

L_d = Land diameter

S = Spacing between conductor and land

Examples of various feature pitch and conductors per channel combinations are shown in Figure 3-7. Figure 3-7 shows examples of conductor and space widths that will fit between adjacent lands with various pitches and land diameters. Note that as the solder ball pitch decreases, the conductor width and spacing for a given number of conductors per channel also decreases, and it becomes more difficult and costly to produce the printed board.



Figure 3-7 Feature Pitch and Conductor per Channel Combinations

3.4.3 HDI Routing Density Factors As IC pin counts increase, the corresponding packaging sizes along with feature sizes such as lands are decreasing. At the same time the distance between pins, also known as the pin pitch, are decreasing.

When considering routing density for HDI circuits, three major perspectives as provided below must be considered. They all have an interdependent relationship, and therefore all must be considered together:

- Routing solvability refers to the volume of all signal conductors, voltages and ground that need to pin escape a μ BGA, and then satisfy overall connectivity. With Z-axis type routing using microvias, the physical feature sizes and routing volume must be considered in a 3D perspective. The size of conductors and microvias will also be relative to the signal's electrical performance and the manufacturing capabilities