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Design Guide for the Packaging of High Speed Electronic Circuits

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Developed by the IPC-2251 Task Group (D-21a) of the High Speed/
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Design Guide for the Packaging of High Speed Electronic Circuits

1 GENERAL

1.1 Purpose The object of this document is to provide guidelines for the design of high-speed circuitry. The subjects presented here represent the major factors that may influence a high-speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope The goal in electronic packaging is to transfer a signal from one device to one or more other devices through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties affect circuit function and require consideration. Every electrical concept has relevant physical implementation data and limitations provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more detailed supplemental data. Since most high speed design requires signal integrity and EMI techniques, often field solvers, signal integrity simulation tools, EMI/EMC simulation programs may be required for resolving design challenges. Many PWB layout design tools include these tools as options to their programs. These simulators are driven by SPICE, IBIS, or other models. References to manufacturers of these tools may be found on the IPC Web site (www.ipc.org).

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

Symbol	Description
ABT	Advanced Bipolar-CMOS Technology
AC	Advanced CMOS
AC	Alternating Current (Time varying current)
ACQ	Advanced CMOS Quiet
ACT	Advanced CMOS TTL Compatible
ACTQ	Advanced CMOS TTL Compatible Quiet
AGP	Advanced Graphics Port Logic
AHC	Advanced High-Speed CMOS
AHCT	Advanced High-Speed CMOS TTL Compatible

ALS	Advanced Low Power Schottky Technology
AS	Advanced Schottky Technology
BCT	Bipolar-CMOS Technology
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE _{XY}	X and Y-Axis Coefficient of Thermal Expansion
CTE _Z	Z-Axis Coefficient of thermal expansion
CTT	Center Tap Terminated Logic
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
dV/dT	Delta Voltage/Delta Time (Edge Slew Rate)
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
F	Fast Bipolar Logic Technology
FR-4	Flame Retardant Level 4, Epoxy Glass Dielectric Material
GaAs	Gallium Arsenide Technology
GTL	Gunning Transceiver Logic
GTL+	Gunning Transceiver Logic Plus
HC	High-Speed CMOS Technology
HCT	High-Speed CMOS TTL Compatible
HL	High-to-Low Signal Edge Transition
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
IBuf	Input Buffer
IC	Integrated Circuit
K _B	Backward Crosstalk
K _F	Forward Crosstalk
L _G	Ground Plane Inductance
L _H	Low-High Signal Edge Transition
L _P	Power Plane Inductance
LVDS	Low Voltage Differential Signalling
LVEL	Low Voltage ECL
LVPECL	Low Voltage PECL
LVC MOS	Low Voltage CMOS Technology
LVT	Low Voltage Technology

ALS	Advanced Low Power Schottky Technology
AS	Advanced Schottky Technology
BCT	Bipolar-CMOS Technology
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE _{XY}	X and Y-Axis Coefficient of Thermal Expansion
CTE _Z	Z-Axis Coefficient of thermal expansion
CTT	Center Tap Terminated Logic
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
dV/dT	Delta Voltage/Delta Time (Edge Slew Rate)
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
F	Fast Bipolar Logic Technology
FR-4	Flame Retardant Level 4, Epoxy Glass Dielectric Material
GaAs	Gallium Arsenide Technology
GTL	Gunning Transceiver Logic
GTL+	Gunning Transceiver Logic Plus
HC	High-Speed CMOS Technology
HCT	High-Speed CMOS TTL Compatible
HL	High-to-Low Signal Edge Transition
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
IBuf	Input Buffer
IC	Integrated Circuit
K _B	Backward Crosstalk
K _F	Forward Crosstalk
L _G	Ground Plane Inductance
L _H	Low-High Signal Edge Transition
L _P	Power Plane Inductance
LVDS	Low Voltage Differential Signalling
LVEL	Low Voltage ECL
LVPECL	Low Voltage PECL
LVC MOS	Low Voltage CMOS Technology
LVT	Low Voltage Technology

LVTTTL	Low Voltage TTL Technology
LVX	Low Voltage CMOS Translation
OBuf	Output Buffer
PCI	Peripheral Component Interconnect
PDN	Power Distribution Network
PDS	Power Distribution System
PECL	Positive ECL Technology
PWB	Printed Wiring Board
R_C	Series Lead Resistance
R_G	Ground Plane Resistance
R_p	Power Plane Resistance
RSECL	Reduced Swing ECL
R_T	Sheet Resistance
Si-Ge	Silicon-Germanium
SM	Surface Mount
SPICE	Simulation Program with Integrated Circuit Emphasis
SSTL	Stub Series Terminated Logic
TAB	Tape Automated Bonding
Tan δ	Dissipation Factor (Loss Tangent)
TDR	Time Domain Reflectometer
t_f	10%-90% Edge Transition Time (Fall Time)
t_p	Total Signal Line Propagation Delay Time
t_{PD}	Propagation Delay Per Unit Length
t_r	10%-90% Edge Transition Time (Rise Time)
TTL	Transistor Transistor Logic
Z_O	Characteristic Line Impedance (Unloaded)
Z_O'	See 5.6.4
ϵ_r	Real Part of Relative Permittivity
$\epsilon_{r,eff}$	Real Part of Effective Relative Permittivity
δ	Skin Depth

1.3.2 Terms and Definitions The terms listed below are used in this document. Their definitions are given in order to help the new reader. These definitions are also found in IPC-T-50, "Terms and Definitions for Interconnecting and Packaging Electronic Circuits." Where possible, definitions that appear in the body of this document are referred to as follows: "Bus - 5.6.7.2." This indicates that a definition for "Bus" appears in 5.6.7.2, and will not be repeated here.

AC Impedance – The combination of resistance, capacitive reactance, and inductive reactance experienced by time-varying voltage.

Alternating Current (AC) – A current that varies with time. This label is commonly applied to a power source that switches polarity many times per second, such as the

power supplied by utilities. An AC signal may take a sinusoidal shape, but could be a square or triangular wave shape.

Amplitude – The difference between the high level and the low level of a voltage or current signal.

Analog Ground Plane – A solid copper or electrically conductive plane or plane-shape within a layer of a PWB. It provides a low inductive Analog ground signal reference (return path) for analog signal conductors on adjacent or buried layers. It also provides ground interconnect for analog active and passive analog devices.

Asymmetrical Dual-Strip Stripline – A stripline where the signal conductor that is embedded between two ground planes is not centered between them.

Attenuation – Reduction in the amplitude of a signal due to losses in the media through which it is transmitted.

Backward Crosstalk – Noise induced into a quiet line by an adjacent active line as seen at the end of the quiet line that is closest to the signal source. Typically, backward crosstalk is an inductive form of Crosstalk.

Broadside Coupled Pair – Signal conductors on adjacent layers that are routed parallel to each other, exhibits mutual trace-width coupled impedance between them, typically 50 to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Bulk Decoupling Capacitor – A capacitor that provides low frequency charge storage. Typically a tantalum or aluminum electrolytic dielectric capacitor placed at the power input of a circuit board and others distributed throughout the printed wiring board to reduce noise power and provide energy storage for high frequency decoupling capacitors.

Bus – See 5.6.7.2.

Busbar – A large copper or brass bar used to carry high power supply currents onto a printed wiring board (PWB) or backplane.

Capacitance – A measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them. Measured in Farads.

Characteristic Impedance – The vector sum of the impedance and reactance of a parallel conductor structure to the flow of AC current. Usually applied to transmission lines in printed boards and to cables carrying high-speed signals. Normally the characteristic impedance is a constant value over a wide range of frequencies and typically is referred to as Z_O .

Chassis Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference (return path) for signal conductors on adjacent or buried conductors. The chassis ground plane may also be placed on the top and bottom layers of a

printed wiring board to reduce electromagnetic emissions emanating from internal layers.

Circuit Board – For the purposes of this guideline the term circuit board covers both printed circuit board and discrete wiring boards where a circuit function is performed.

Clock – A gated synchronous or continuous digital periodic signal that provides timing for logic circuits.

Coaxial Transmission Line (Coax) – A transmission line structure where a round signal conductor is centered coaxially within a hollow cylindrical return (ground) conductor. The inside diameter of the return conductor is greater than the outside diameter of the signal conductor.

Crossover – Intersection of two conductors separated by dielectric.

Crosstalk – See 3.2 of Appendix B.

Current – The rate at which electrons travel in a conductor as a result of a voltage difference between the ends of the conductor. The unit of measure for current is the ampere, A.

Decoupling – Absorption or isolation of the noise that is induced in the power supply lines by switching logic devices. Decoupling prevents switching logic devices from disturbing other logic devices on the same power supply circuit. Decoupling is usually accomplished using capacitors (see 5.1.3).

Differential Impedance – The resistance of a dual parallel conductor structure to the flow of AC current. Usually applies to broadside coupled or edge coupled transmission lines in printed wiring boards and cables carrying high-speed signals. Differential impedance is normally a constant value over a wide range of frequencies and is typically referred to as Z_{DIFF} .

Differential Pair – Parallel routed signal lines exhibiting mutual coupled impedance between them that is typically between 50 ohms to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Direct Current (DC) – A current produced by a voltage source that does not vary with time. Normally provided by power supplies to power electronic circuits.

Discrete Wiring Board – Circuit board using round insulated wire to form signal paths that is terminated at both ends by a plated through hole.

Dissipation Factor – A parameter used to express the tendency of insulators or dielectrics to absorb some of the energy in an AC signal.

Dual Asymmetrical Stripline – A stripline signal conductor(s) that is embedded between two ground planes, and is not centered between them (closer to one ground plane than the other).

Edge Coupled Pair – Signal conductors routed parallel to each other on the same layer that exhibit mutual edge coupled impedance between both lines, typically between 50 ohms to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Edge Rate – The rate of change in voltage with time of a logic signal transition. Usually expressed in volts per nanosecond.

Edge Transition Attenuation – The reduction in the edge rate of a pulse caused by absorption of the higher frequency components of the pulse by the transmission line.

Effective Permittivity (Dielectric Constant) – See 5.2.2.

Effective Relative Permittivity – See 5.2.2.

Electromagnetic Interference (EMI) – Degradation of the performance of a device, equipment or system caused by an electromagnetic disturbance. Government regulating agencies control the allowable limits for radiated and conducted emissions surrounding electronic devices. Self-compatibility controls the allowable limits for internal radiated and conducted emission limits.

EMI Conducted Emissions – Conducted electromagnetic energy from digital, power, analog or components which is injected onto traces, power line conductors, or cables that cause interference to external or internal electronic circuitry. Often conducted EMI that is present on cables causes radiated EMI emissions in a system. Government regulating agencies control the allowable limits for radiated and conducted emissions surrounding electronic devices. Self-compatibility controls the allowable limits for internal radiated and conducted emission limits.

EMI Radiated Emissions – EMI that is the result of electromagnetic energy radiated from an electrical or electronic device, circuit or system. The Federal Communications Commission (a U.S. regulatory agency) and international technical and scientific organizations (such as the European Union - EU) limit the power of emissions radiated from electronic systems. Self-compatibility controls the allowable limits for internal radiated and conducted emission limits.

EMI Susceptibility – The sensitivity or vulnerability of an electronic device, circuit, or system to become adversely affected by radiated or conducted electromagnetic emissions. International and national technical and scientific organizations set upper limits on the energy or power levels (usually as a function of frequency) below which performance degradation of the device, circuit, or system should not occur. Self-compatibility of a system sets the maximum power levels for internally generated conducted and radiated emissions.

Electrostatic Discharge (ESD) – The resulting current field created when a high-voltage is discharged through a

return. An ESD may follow multiple coupling paths (including sensitive circuitry) to ground creating radiated EMI emissions. ESD may cause circuit malfunction, failure, or damage depending on the circuit's ESD or EMI susceptibility.

ESD Damage – The damage caused to an electronic circuit when an unwanted high-voltage short-duration electrical pulse discharges into a static sensitive device. ESD damage often causes latent defects in semi-conductors. Generally, all semiconductors and some passive devices are ESD sensitive.

ESD Susceptibility – The vulnerability of a circuit to be affected by ESD. Typical ESD susceptibility tests are direct discharge and indirect discharge test based on the ESD established models.

Fall Time – Time required for a logic signal to switch from its high state to its low state. Commonly measured between the 90% and 10% amplitude levels. Transition duration is the term preferred and accepted by both international (IEC) and national (Institute of Electronic and Electrical Engineers, or IEEE) standards setting bodies to describe fall time. See IEC-469-1. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels. See Transition Duration.

Flat Conductor – A rectangular conductor that is wider than it is high. Usually refers to signal conductors in a printed wiring board.

Forward Crosstalk – Noise induced into a quiet line placed next to an active line as seen at the end of the quiet line, which is farthest from the signal source. Typically Forward Crosstalk is a capacitive form of Crosstalk.

Ground – A term used to describe the terminal of a voltage source that serves as a measurement reference for all voltages in the system. Ground is often, but not always, the negative terminal of the power source.

Ground Bounce – A term used to describe the effect when multiple simultaneously switched outputs change from one state to another and which subsequently causes a quiet (undriven) input or output to follow the edges of the driven outputs (see 3.2.1.7). This effect is a difference of voltage drop between the die pad and the package-pin pad or lead-frame.

Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance ground reference (return path) for signal conductors on adjacent or buried lines. The ground plane also provides a ground connection for active and passive devices.

High-Frequency Decoupling Capacitor – A Capacitor that can charge/discharge high-frequency energy. Typically the high-frequency decoupling capacitor is a ceramic dielectric capacitor placed between the power pin and ground of an

IC or discrete circuit to supply high frequency switching edge energy for the device or circuit. Multiple capacitors and/or values may be required for large IC packages.

IBIS Model – A model used for Signal Integrity analysis that defines a device's package parasitics, input characteristics, internal clamps, output characteristics, measurement thresholds, and edge rates. IBIS is not usually a proprietary model.

Impedance – The resistance to the flow of current represented by an electrical network. May be resistive or reactive, or both.

Inductance – The property of an electrical device or circuit that describes how well a time-varying current can induce an electromotive force in that or a nearby device or circuit. Inductance is proportional to the total magnetic flux and current through the device or circuit and its unit of measure is the Henry(H). Inductors store energy in a magnetic field.

Line Coupling – Coupling between two transmission lines caused by their mutual inductance and the capacitance between them.

Load Capacitance – The capacitance seen by the output of a logic circuit or other signal source. Load Capacitance is usually the sum of distributed line capacitance and input of the load circuits.

Logic – A general term used to describe the functional circuits used in computers and other digital electronics to perform computational or control functions.

Logic Family – A collection of logic functions or ICs using the same form of electronic circuit technology. Examples: ECL-Emitter Coupled Logic; TTL-Transistor-Transistor Logic; CMOS-Complimentary Metal Oxide Semiconductor logic; GTL-Gunning Transceiver Logic.

Microstrip – Microstrip, microstripline, and microstrip line are used interchangeably (see 5.5.1).

Net – See 5.6.7.1.

Nonmonotonic Edge (Transition) – A term used to describe an unwanted signal integrity “double edge” effect that occurs during a rising or falling edge, where two edges are generated (sometimes referred to as a double clock) (see 3.2.1.4).

Overshoot – The amount by which a pulse exceeds its nominal amplitude after its transition from one state to another. Overshoot is a signal aberration and is usually given as a percentage of the nominal pulse amplitude. Overshoot can be caused by pulse reflections from impedance discontinuities in a transmission line. Typically, the discontinuities that contribute to overshoot are from a low to high impedance. For example, the signal amplitude may temporarily rise to 6.5 V because of reflections even though the supply voltage is only 5.0 V (see 3.2.1.4).

Parallel Pair – Two conductors that are routed side by side on the same or on adjacent layers and are at a controlled separation.

Permeability – A general term used to express various relationships between magnetic induction and magnetizing force.

Permittivity (Dielectric Constant) – See 5.2.

Plane – A solid copper or electrically conductive layer or plane-shape within a layer of a PWB. Planes are typically used for power and ground distribution, impedance control, and circuit isolation. Planes may be voltages, grounds, digital, analog, RF circuitry, or whatever is required for the design. A PWB will generally have multiple plane layers or plane-shapes.

Power Distribution Network (PDN) – The network of power distribution elements on a PWB or system that delivers power from one location (source) to destination devices. The network is composed of inductive and capacitive elements. The PDN is designed to provide a low impedance source across applicable frequency range to destination devices. Also referred to as Power Distribution System (PDS).

Power Distribution System (PDS) – See Power Distribution Network (PDN).

Power Dissipation – Energy used by an electronic device in the performance of its function.

Power Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference for signal conductors on adjacent or buried layers and a power interconnect for active devices.

Power Plane Inductance – See 5.1.2.1.

Power Plane Coupled Noise – An unwanted signal integrity effect when edge-switching noise is transferred from one circuit to another through the power planes.

Printed Wiring Board – A circuit board utilizing etched copper traces for signal interconnections.

Propagation Delay – The time from output to input required for a signal to travel along a transmission line, or the time required for a logic device to receive an input stimulus, perform its function, and present a signal at its output.

Pulse – A logic signal that switches from one state to another and back in a short period of time, and remains in the original state most of the time. Usually used as timing strobe signals for logic devices.

Reflection – Energy from a high-speed signal edge that is sent back toward the source as a result of encountering a change in impedance in the transmission line on which it is traveling.

RF Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance RF reference for analog signal conductors on adjacent or buried layers. The RF ground plane also provides a ground connection for active and passive RF devices.

Rise Time – Time required for a logic signal to switch from its low state to its high state. Commonly measured between the 10% and 90% voltage levels. Transition duration is the term preferred and accepted by international (IEC) and national (IEEE) standards setting bodies to describe rise time. See IEC-469-1. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels. See Transition Duration.

Routed Signal Line Delay – See 3.2.1.6.

Signal Ground – The common ground return reference for logic signals. Typically one or more signal ground planes in a PWB.

Signal Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference for digital signal conductors located on adjacent or buried layers. The signal ground plane also provides a ground connection for active and passive devices.

Signal Integrity Degradation – Signal aberrations that degrade system performance or cause mis-operation. These signal aberrations may be Overshoot, Undershoot, Crosstalk, Nonmonotonic edges, Ground bounce, Power plane coupled noise, or Routed signal line delay skew.

Signal Line – Any conductor used to transmit an electrical signal from one circuit to another.

Skin Effect – See 5.8.1.

SPICE Model – A model used for Signal Integrity analysis that defines a device's package parasitics, input characteristics, and output characteristics.

Stripline – See 5.5.3.

Stub – A branch of the main line of a signal net usually used to reach a load that is not on the direct signal path.

Matched Termination – A term used to describe the matching of the driving source, transmission media, and destination load to minimize signal integrity degrading effects.

Transition Duration – The difference between the instants on the same transition that the waveform crosses specified reference levels. Unless otherwise specified, the two *reference levels* are the 10% and 90% *reference levels*. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels.

Deprecated Terms: Risetime, Falltime, Leading Edge, Rising Edge, Trailing Edge, Falling Edge, Transition Time – The terms *risetime*, *falltime*, *leading edge*, *rising edge*, *trailing edge*, *falling edge*, *transition time*

although widely used, are deprecated because they are ambiguous and confusing. First, the use of the word *time* in this standard refers exclusively to an *instant* and not an *interval*. Also, if the *first transition* of a *waveform* within a *waveform epoch* happens to be a *negative transition*, some users may refer to its *transition duration* as its *risetime*, and some others may refer to its *transition duration* as its *falltime*. If the use of these deprecated terms is required, then *risetime* is synonymous with the *transition duration* of a *positive-going transition*, and *falltime* is synonymous with the *transition duration* of a *negative-going transition*. If the upper and lower *state boundaries* of the two *states* are not the user-defined *reference levels* (for example, the 10% and 90% *reference levels*), then the *duration* of a *transition* is not equal to the *transition duration*. IBIS Models commonly use dV/dT measured between the 20% and 80% voltage levels.

Transmission Line – A signal-carrying circuit with controlled conductor and dielectric material physical relationships such that its electrical characteristics are suitable for the transmission of high frequency or narrow pulse electrical signals.

Undershoot – A term used to describe an unwanted signal integrity effect that occurs after successive reflections causing a short additional pulse within the supply or ground rails after the original transition (see 3.2.1.3).

Waveguide – A rectangular or round tube used to transmit RF energy in the form of an electromagnetic wave rather than as a current in a wire.

1.4 Units All dimensions and tolerances in this standard are expressed in hard metric (SI) units and parenthetical soft imperial (inch) units.

2 APPLICABLE DOCUMENTS¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-DW-424 General Specification For Encapsulated Discrete Wire Interconnections Boards

IPC-DW-425 Design End Product Requirements for Discrete Wiring Boards

IPC-2141 Controlled Impedance Circuit Boards and High Speed Logic Design

IPC-2221 Generic Standard on Printed Board Design

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC-4103 Specification for Base Materials for High-speed/High Frequency Applications

IPC-4562 Metal Foil for Printed Wiring Applications

3 OVERVIEW

Packaging of electronic equipment has traditionally been an area for mechanical considerations. An assortment of active and passive devices need to be adequately provided with physical support, environmental protection, heat removal, electrical interconnections where specified, and electrical insulation where interconnections are not specified, all by a cost-effective means.

Packaging design is becoming more complex. Switching devices typical of digital electronics technology are continually increasing in both switching speed and in the number of devices per chip. Individual chips are being provided with greater numbers of connections that are in smaller individual chip package sizes. The competitive need to take maximum advantage of device density and speed has forced packaging designers to pay much more attention to the problems of electromagnetic wave-propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. This document is intended to help meet this need and this overview section will introduce in broad terms what is covered.

3.1 Decision Making Process Determine at the start of a project which packaging concerns need early introduction into the design process. Performance of older systems was limited by the devices available at the time and therefore packaging design could often be left for the end of the design activity. High performance systems are limited in speed by packaging, so if the project is concerned with speed, start by considering how to get the most out of the packaging today.

There are numerous design options to consider, and the designer will have to compromise between thermal, mechanical and electrical requirements of the package (see Figure 3-1). For a proposed system, a choice among types of electronic devices has to be made. This will have an influence on the kinds of packaging materials to be selected. It will become apparent that the design is a collection of compromises to get the best overall performance. Effort early in a program to evaluate many sets of options and their interactions is recommended.

The decision making cycle will consist of proposing a design with selection of devices, packaging materials, and interconnection schemes. The system preferably will be modeled and its deficiencies and limitations identified. This should result in some alterations in the design and the start

1. www.ipc.org

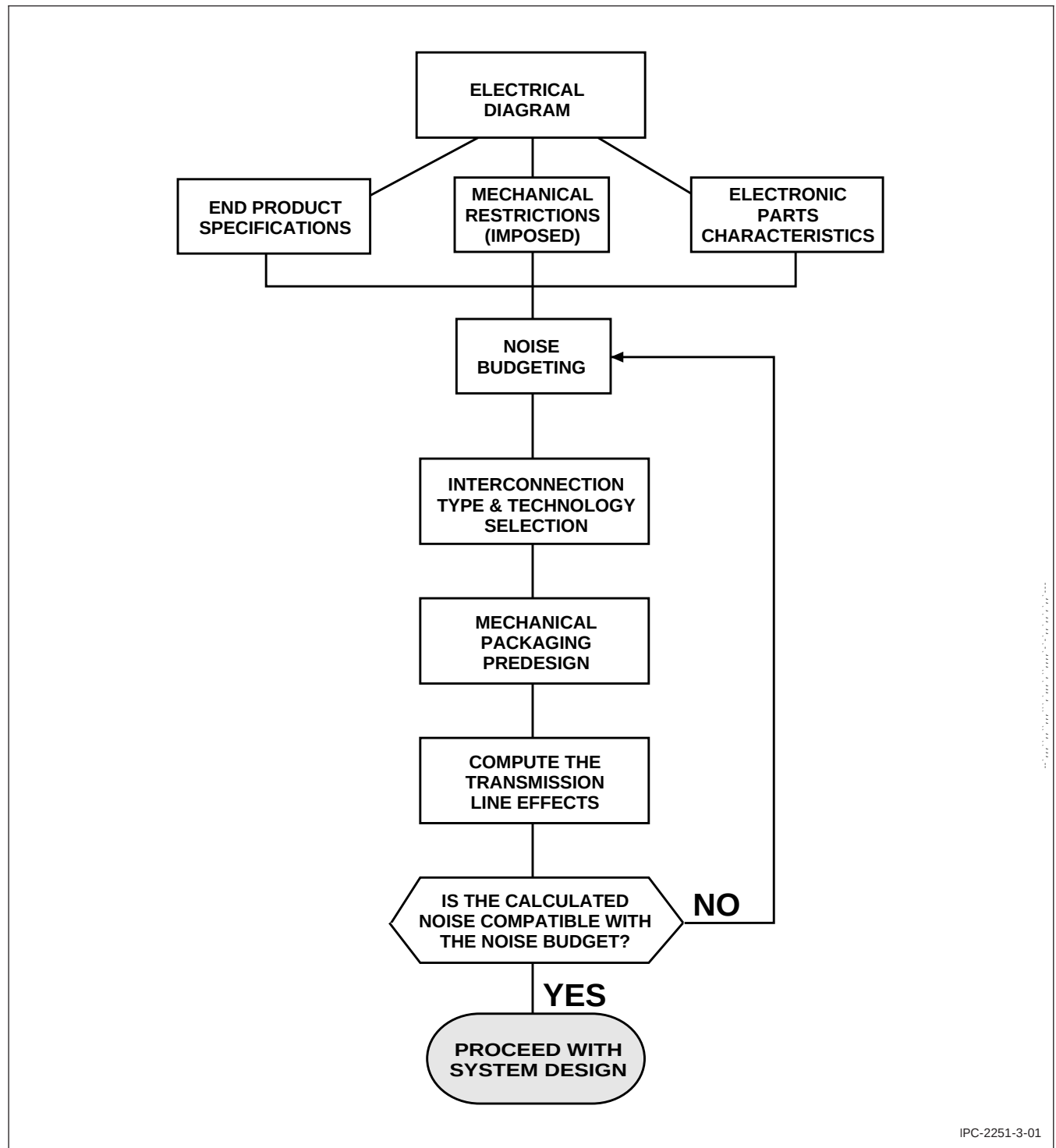


Figure 3-1 High-Speed Packaging Design Concept

of another modeling cycle. The process is repeated until further improvement is minimal. If the projected performance is far short of the target then the designer should consider attempting a different design approach.

These guidelines should be helpful to the designer in providing awareness of the options available and the principles needed in modeling. There is plenty of room for innovative advances in high-speed packaging.

3.2 Design Options Let us consider some of the options to be exercised by the designer, realizing that each selection interacts with the others. These options are listed in this section and are followed (see 3.3 and 3.4) by a list of corresponding requirements.

3.2.1 System Electrical/Mechanical Constraints What type of active switching devices will be used? Example options include TTL, Schottky TTL, CMOS, ECL, BiCMOS,

GTL, GTL+, and GaAs, each with its own set of power requirements, operating temperature range, density on a chip, input impedance, output impedance, signal threshold levels, noise sensitivity, response time and output pulse rise/fall time.

How will the selected electronic devices be organized in the final assembly? Chip devices can be prepackaged and individually mounted on a large board or assembled into small boards or Multichip Modules, which will in turn be mounted onto large boards. Large systems will require several large board assemblies and there is yet another option of how this level of interconnection will be applied. Reflection noise and signal degradation will accompany transitions from one packaging level to the next. Organization will have an impact on manufacturability and repairability of the system.

What transmission line geometry on boards will be used for signal interconnections between devices? Options include coplanar coupled pairs, microstrip over a single ground plane, striplines between ground planes, orthogonal striplines sharing a common pair of ground planes, wire over ground plane, and wire between ground plane. For a given geometry, the selection of substrate thickness and conductor width will depend on the required characteristic impedance, and the relative permittivity (dielectric constant) and thickness of the substrate.

What interconnect schemes for signal transmission will be used? One could choose single connections from one device output to another device input. A single output could be connected to several inputs and the multiple connections could be accomplished either by branching or by continuing from one input to the next in daisy-chain fashion. The scheme will affect transmission time, noise, settling-time and signal pulse degradation.

3.2.2 Signal Integrity Design Constraints If the design of the system and circuit card assemblies are not controlled Signal Integrity cannot be achieved. These effects degrade noise margins, cause mis-operation and are indicated by overshoot, undershoot, nonmonotonic edges, signal line crosstalk, routed signal line induced skew, ground bounce, poor power quality, poor output drive due to loading effects, and EMI problems. These effects are usually controlled up front during the design phase, with component placement, PWB layer stack-up, and during the route.

3.2.2.1 Overshoot Signal line overshoot is caused by a reflection due to an impedance mismatch. Generally, the mismatch is caused when the source impedance of the driver is lower than the impedance of the trace conductor and destination load(s). During a transition, the rising or falling edge goes beyond the supply or ground reference voltages. For example: if a signal is transitioning from 0 Volts to 5 Volts, a reflection may “overshoot” the 5.0 Volt

supply reference to a value of 6.5 Volts. While minor levels of overshoot may be acceptable, it degrades system noise margin budgets and may cause instability in ICs. Overshoot is controlled by proper signal line termination, logic family selection, driver slew rate or drive strength control, route topology, and managing the layer stack-up impedance.

3.2.2.2 Undershoot Signal line undershoot is caused by a reflection due to an impedance mismatch. Generally, undershoot is the result of an overshoot problem. It occurs after successive reflections causing a short additional pulse within the supply or ground rails after the original. For example: if a signal is transitioning from 4 Volts to 0 Volts, a successive reflection may “undershoot” the 0 Volt supply reference and generate a short additional pulse after the falling edge of 0.8 Volts. While minor levels of undershoot may be acceptable, the magnitude may exceed logic levels and cause an additional delayed logic state resulting in circuit mis-operation. Since undershoot is generally caused by overshoot, the same techniques used to control overshoot apply.

3.2.2.3 Nonmonotonic Edge A nonmonotonic edge is a “double transition” effect that occurs during a rising or falling edge, where two edges are generated (sometimes referred to as a double clock). For example during a rising edge, the signal rises and during the transition, falls for a short period of time then finishes the rising edge. Typically caused by poor route topology with a driver branching to more than one load of unmatched lengths of conductors. The short trace reflection and long trace reflection combine at the nearest receiver causing the effect. Where the non-monotonicity occurs on the edge is important. If it occurs in the logic threshold region, it may cause a false logic condition resulting in mis-operation. Nonmonotonic edges are controlled by proper signal line termination, managing the route topology, and matching conductor lengths.

3.2.2.4 Signal Line Crosstalk Signal line crosstalk is discussed in 3.4.7 and 5.7 and 3.2 of Appendix B. Signal line crosstalk is managed by proper conductor placement and spacing.

3.2.2.5 Routed Signal Line Induced Skew Routed signal line induced skew is caused when additional unplanned delay or skew is introduced in the route of signal conductors. For example: A clock or data strobe is routed too long or too short for a data latch and the data is not stable (still settling) before the qualifying clock or strobe is presented. Incorrect data may be latched causing an error. Routed signal Line skew is managed by directing the router to match the lengths of signals in a group and matching loading delay. Critical timing lines should be identified and skew predetermined (route path and route length).

PWB is routed. Most layout tools are able to route to conductor length or delay matching rules to a predetermined tolerance. Some skew is acceptable and the amount is constrained by clock rate, set-up and hold times, edge rate, route layer definition, routing space, and crosstalk management.

3.2.2.6 Ground Bounce Ground Bounce is caused by a combination of problems. Ground Bounce is the effect when multiple outputs simultaneously switch from one state to another, which causes another “quiet” (non-switched) input or output to follow (bounce), the edges of the driven outputs. Most integrated circuits have inductance associated with bond wires (or carrier traces in high density IC interconnects) for inputs, outputs, power, and grounds. At high switching speeds, the inductive reactance may become significant particularly on the power and ground interconnects; this effect is a difference of voltage drop between the die pad and the package-pin pad or lead frame. When wide high-speed busses simultaneously switch from high to low or low to high, large amounts of instantaneous current is required to drive the bus load. The current must be supplied by the power and ground interconnects (bond wires or carrier interconnect). The resulting dI/dT required by the driven bus lines across the interconnect creates a voltage drop across the interconnect. This creates localized voltage shifts on the IC die, which allows a quiet line in that localized area to bounce. The amplitude of the bounce varies with the number of simultaneously switching outputs and the inductance of the IC power interconnects. Many vendors have reduced susceptibility to ground bounce by using multiple power and ground wires or interconnect (paralleled wires reduce inductance similar to resistors in parallel), or use shorter wires or interconnect (shorter length reduces inductance), or use the flip chip techniques instead of wire bonding (shorter length, controlled impedance, ground plane referenced results in less inductance). Another problem that aggravates ground bounce is bus loading. Generally, wide busses go to many bus elements (processors, cache ram, ram, memory controllers, etc.). Each I/O pin and its associated interconnect (trace capacitance) between each I/O is a capacitive load. The resultant capacitive load of the switched outputs is impressed on the driving IC power and ground bond wires or carrier interconnect. Reducing this load may reduce ground bounce. Sometimes, series resistors on the bus elements help limit the current but present other problems with component count, rise / fall time, and timing margins. Proper component placement (even distribution of routing stubs from the bus) and short interconnect helps reduce the capacitive loading, thereby reducing the risk of ground bounce. The power and ground plane inductance being too high may aggravate ground bounce. If the power or ground planes have too many localized via clearances, its inductance may be too high. This creates a poor source of power

to the devices driving wide busses. The power and ground interconnects (vias or traces) should provide a low inductive source to ICs.

3.2.2.7 Poor Power Quality Poor power quality is generally caused by a lack of power decoupling, circuit isolation, and poor power regulation. Poor power quality degrades noise margins, is aggravated by environmental changes, causes timing problems, degrades edge rates, and is difficult to locate. Power decoupling and circuit isolation are covered in 5.1.4. Power regulation is covered in 5.1.

3.2.2.8 Poor Output Drive Poor output drive is caused by a device's output impedance being much higher than the load impedance. It is generally characterized by severely rounded off edges or poor noisy edges on the waveform. It causes poor timing margins due to the longer transitioning edges consuming a larger than anticipated percentage of the duty cycle. Poor drive erodes set-up and hold times. Careful attention must be paid to impedance matching, PWB layer stack-up, loaded line capacitance, stub distribution (see 5.6.3 through 5.6.6), minimizing trace lengths, and power quality.

3.2.2.9 EMI Problems EMI problems are covered in 5.11.1 through 5.11.3.7.

3.2.3 System Electrical/Mechanical Requirements The decision on the number of signal layers in multilayer boards or discrete wiring boards to be used will be influenced by the density of interconnections within the board. There will be a compromise on the degree of isolation of one interconnection from another versus the need to get a large number of interconnections in a given board area.

Determine the degree of crosstalk or coupling between signal lines that can be tolerated. This can have a major effect on acceptable interconnection densities.

Relative permittivity (ϵ_r) influences board substrate selection. While a low ϵ_r value means faster signal propagation it also increases the conductor width needed at a given substrate thickness for a given characteristic impedance, thus reducing room for conductors.

Power requirements of the devices will also need to be met. Often the choice is made to provide power planes in circuit boards that serve the dual roles of ground plane for signal conductors and power supply for the electronic devices. An alternative is to provide a power bus system to the array of devices on the board.

3.3 Mechanical Requirements The mechanical requirements listed within this section is given to help the designer maintain the integrity and performance of electrical interconnections among electronic devices in the system.



3.3.1 Circuit Board Circuit boards are required to provide mechanical support and interconnection of components mounted on them. Space constraints, number and complexity of interconnections, thermal management, power distribution, and cost of manufacture are some factors to be considered when determining requirements of how many layers to use, the thickness of dielectric layers, the composition and thickness of ground/power plane layers, the dielectric composition and the overall length, width, and thickness of the board.

3.3.2 Hybrid This term is often used to refer to assemblies of thin/thick film chip devices mounted directly on thin/thick film ceramic interconnection boards to form a multichip module. Other technologies using polymeric substrates in place of the thin/thick film ceramic could also be used to build multichip modules. Hybrid boards and multichip modules are usually required to provide protection of sensitive chip components from adverse effects of any environmental or operating conditions that may be encountered in service. They also must be able to withstand thermal and mechanical shock during manufacturing and assembly as well as in service.

3.3.3 Component Packaging Unless chip devices are packaged in multichip modules or hybrid subassemblies they are usually prepackaged individually. The component package can be polymeric or ceramic depending on the degree of atmospheric protection required. The package is required to provide protection to the chip and electrical connections from the chip to the board on which it will be mounted. The package also provides a means for connecting to the chip for automated testing of the package prior to its being used in a board assembly.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated through holes provided in the board, as in dual in-line package, to a series of metallized regions along the edge or arrayed over the base of a surface mount device. What type of connection is selected will depend on, among other things, the requirements for electrical performance of the connections.

Requirements for component packaging will be dependent on many factors including space available, economics, electrical performance requirements, reliability, life expectancy, and thermal conditions.

3.3.4 Thermal Management The system must withstand thermal cycling and temperature differences during service. Temperature differences arise, especially in startup, between packaged electronic devices and the interconnecting board. This temperature difference will cause mechanical strain between the packaged devices and the board because of their different coefficients of thermal expansion.

The greater the difference in the coefficient of thermal expansion (CTE) of the devices and the boards, the greater will be the mechanical strain.

The packaging materials must handle the heat generated by operating the system. Mechanical properties sufficient to provide mechanical integrity of the system must not change at the elevated temperatures expected to be encountered during system operation. Packaging must provide for removal of excess heat to keep the temperature below the point where impairment of electronic performance would occur.

3.3.5 Component Mounting The component must be provided in a physical format that is convenient to attach to the circuit board. Mechanical requirements imposed on the board by a component include the feature tolerances required for attaching the component to the board and the susceptibility to damage during attachment of the component. Some device packaging categories include:

- a. COB mount device
- b. TAB mount device
- c. Single chip package (DIP, PLCC)
- d. Multichip package

3.4 Electrical Considerations Electromagnetic wave propagation theory must be considered in evaluating the performance of interconnecting conductors and their substrates. High-speed devices are characterized by the fast rise time of the electrical pulses. The pulse waveform may be represented using the Fourier transform as the series of sinusoidal signals with certain phase and amplitude relationships. As the rise time of the pulse decreases, the frequency of the important components increases.

3.4.1 Power Distribution For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in electrical current from the power supply. If several devices are demanding current changes at or near the same instant, the power distribution system is required to meet these demands while simultaneously maintaining voltage within specified limits to all devices being supplied. Meeting this requirement demands low inductance connections to devices, with high capacitance among various voltage levels in the distribution system.

3.4.2 Permittivity The relative permittivity (ϵ_r) of the dielectric substrate of an interconnecting device, whether it be a printed board, discrete board and a multichip module, or a chip package, will affect electrical performance of the interconnection on or embedded in it. An assumed ϵ_r is used in the design of the interconnection to meet the impedance, capacitance and propagation time requirements as will be discussed later. The tolerances of these requirements, along with manufacturing tolerance

dimensions, impose a tolerance requirement on ϵ_r if the system is to perform as designed. Since ϵ_r of many substrate materials varies with composition, frequency, and environmental conditions, these variations also impact the allowable tolerances on ϵ_r .

The permittivity that actually affects transmission line electromagnetic wave propagation characteristics is what is called the effective permittivity, or $\epsilon_{r,eff}$. The effective permittivity is affected by the geometry of the transmission line and by the dielectrics of and near the transmission line that is influenced by electromagnetic energy from the propagating wave or pulse. For a given transmission line geometry, propagation time and capacitance will vary directly by the square root of $\epsilon_{r,eff}$. Impedance will vary inversely as the square root of $\epsilon_{r,eff}$.

There are trade-offs in the selection of high or low $\epsilon_{r,eff}$ values for the substrate that will be discussed later.

3.4.3 Capacitive Versus Transmission Line Environment For an interconnection from one device to another, the connecting line can be treated either as a transmission line or a capacitive line. For transmission lines, the design concept is to provide a known characteristic impedance that is terminated at the destination with a matching impedance to minimize reflections that result from fast rise time pulses. For a capacitive line, the concept is that of a line whose stored charge requires a certain amount of current flow to result in a change in the voltage that is present at the destination. The critical design parameters and requirements will depend on which concept is appropriate.

3.4.4 Propagation Time In high-speed systems, it is not unusual for the clock cycle time to be shorter than the propagation time for a signal from one device to another, especially where a signal might originate on one board and be received on a device on another board. For the system to perform correctly at high-speeds, a well-controlled propagation time is required and in some cases adjustments in the propagation time for certain signal paths (lines) may be required.

3.4.5 Characteristic Impedance The Characteristic Impedance typically used will range from 50 to 70 Ohms. This range of characteristic impedance is often used because lower impedance values cause excessive crosstalk between nearby signal lines and power consumption by impedance-matched electronic devices. Higher impedance provide lower crosstalk values for a given signal amplitude but produce circuits with greater EMI/ESD susceptibility, and greater EMI radiated emissions. Typical signal paths will have a characteristic impedance of 50 Ω for most printed wiring boards. Examples where 50 Ω is not used are: PCI, 100 Ω but is dependent on signal path length and load impedances (32 Ω is the minimum load impedance);

Compact PCI, 65 Ω ; RS-422/RS-485/LVDS differential traces, 50 Ω to 75 Ω for signal-line-to-ground impedance and 100 Ω to 120 Ω for signal-line-to-signal-line impedance; analog, 25 Ω to 100 Ω ; and radio frequency, 50 Ω , 75 Ω , and 100 Ω , 75 Ω characteristic for RS-170 and RS-343 video traces. The impedance selected may be higher than 50 Ohms for large bus structures with multiple terminations to reduce driver loading and Ground Bounce. The characteristic impedance of a lossless uniform transmission line is equal to the square root of the ratio of inductance per unit length to capacitance per unit length. The impedance of a transmission line can be mathematically modeled as a complex function of several parameters:

- Conductor width/diameter-impedance decreases with increasing signal line width or diameter.
- Type of transmission line-Microstrip, Embedded Microstrip, Centered Stripline, Dual Asymmetrical Stripline, Edge Coupled Differential Pairs, Broadside Differential Pairs, and Coplanar (see IPC-2141). With equal ϵ_r , spacing and conductor width, impedance ranking will be, from highest to lowest: Differential Pairs, Coplanar, Microstrip, Embedded Microstrip, Dual Asymmetrical Stripline, and Centered Stripline. Refer to Figure 5-8.
- ϵ_r of dielectric-impedance decreases with increasing values of ϵ_r .
- Spacing between signal and ground-impedance decreases for decreasing spacing.
- Proximity to other conductors-impedance decreases as distance increases.

3.4.6 Signal Loading Effects When a signal line terminates into several electrical loads and if the power supply is not an ideal voltage source (which is usually the case), the issue of signal loading must be considered.

First, consider loads connected along the length of the signal line. If the impedance of the load is low or a near match to the characteristic impedance of the line, there will be a decrease in signal amplitude as each successive load in the signal path is encountered. High-impedance loads relative to the line will result in less decrease in amplitude. A matched load at the end signal line is needed to prevent a reflection that could affect circuit function. If the distance between loads along the signal line is approximately equal to or longer than the wavelength of the highest frequency component of the signal, the signal propagation along the transmission line must be considered when calculating loading effects. On the other hand, if the spacing between electrical loads is much less than a wavelength, then for practical purposes the loads appear to be connected at a common location or node. Consequently, the node will have low impedance and the signal amplitude to the loads will be diminished. The impedance at this node can be approximated using lumped-element analysis.

3.4.7 Crosstalk In general, an interconnecting board is populated as densely as possible with devices and conductors to minimize the size of the system and reduce propagation time along the signal lines. The result is that conductors must be placed close to each other and usually the designer must resort to multilayer boards or discrete wiring boards to accommodate the high interconnect density and the crossover situations in the wiring plan.

Crosstalk is the transfer of electromagnetic energy from a signal on an aggressor (source or active) line to a victim (quiet or inactive) line. The magnitude of the transferred (coupled) signal decreases with shorter adjacent line segments, wider line separations, lower line impedance, and longer pulse rise and fall times (transition durations).

A victim line may run parallel to several other lines for short distances. If a certain combination and timing of pulses on the other lines occurs, it may induce a spurious signal on the victim line. Thus, there are requirements that the crosstalk between lines be kept below some level that could cause a noise margin degradation resulting in malfunction of the system.

3.4.8 Signal Attenuation High-speed systems have devices that generate fast rise and/or fall time pulses and the devices may respond ambiguously to pulses exceeding a certain maximum rise time. This is best explained by considering the Fourier transform of a signal. The Fourier transform decomposes the signal into a series of harmonically related frequency components. This is best explained in terms of the model of a pulse as a sum of even and odd harmonic signals, where the harmonics are of greater frequency than the fundamental frequency. The high frequency components of the pulse attenuate more rapidly than lower frequency components. This is due to the skin effect in the conductor as well as the dissipation effect in the dielectric. Furthermore, for thin copper, the pretreatment may raise the copper resistance, which will increase skin effect losses. The skin effect losses may also depend on the finish of the copper surface.

The resistance of the copper may reduce the steady state voltage levels below the levels needed for adequate noise immunity. This is especially true of ECL circuits where a voltage divider is formed by the terminating resistor and the line resistance.

The DC resistance of a line can be calculated using the copper resistivity and the geometries of the line. The effects of surface finish (skin effects) may have to be determined experimentally. The smooth surface of a drawn wire used in discrete wiring boards has lower skin effect losses and other advantages over etched conductors.

4 MECHANICAL CONSIDERATIONS

In addition to meeting the predicted performance criteria, circuit board designs must be manufacturable if the system

is ever to become a reality. Performance versus cost also factors into the choice of the optimum system design. Yield at manufacture and end product reliability may be, at times, even greater contributors to cost than the obvious costs of raw materials and fabrication. For this reason, the designer should be familiar with the material options available, their properties, capabilities, and tolerances and have a reasonably good understanding of process capabilities and tolerances that may impact not only performance, but also manufacturing yield and reliability.

The development of a close working relationship with the manufacturing engineering group of the captive or vendor board fabrication facility is highly useful to avoid excessive prototype iterations which are both costly, and time consuming. Designing “based on what worked before” is certainly valid but may be limiting at times if full advantage of advances in both materials and fabrication is to be taken. Therefore, the development of a relationship with in-house advanced materials and manufacturing groups as well as outside industry sources is advisable.

The following is intended to serve as a cursory overview of some of the interactions between raw materials, performance, and manufacturing capabilities. This summary should by no means be considered exhaustive of the technologies available for the production of circuit boards.

4.1 Printed Board

4.1.1 Substrate Materials Laminates and bonding material and their properties are detailed in IPC-4103.

4.1.1.1 Resin Systems The resin systems used for circuit board laminates are classified into two basic categories: thermosetting and thermoplastic. Thermosetting resins are cross-linked matrices of smaller, polymeric units. The polar nature of materials generally contributes to higher relative permittivity, loss tangent (dissipation factor) and water absorption. The cross-linked structure of the thermosets generally provides better dimensional and thermal expansion characteristics than thermo plastics. Water absorption becomes an issue because its relative permittivity is so high (approximately 75) compared to these resin systems. Therefore, relatively small changes in humidity in the environment may drastically impact performance (i.e., capacitance and Z_0) and necessitate strict environmental controls. Likewise, each resin system has a characteristic response of relative permittivity and loss tangent to temperature and operating frequency.

4.1.1.2 Reinforcements, Supports, and Fillers Although some of the available materials are comprised of resin only, routinely various reinforcements, supports, and/or fillers are incorporated with the various resin systems to enhance the physical or electrical properties of the composite laminate. A typical example is the incorporation of

E-glass into a resin matrix to enhance dimensional stability and reduce the X-Y coefficient of thermal expansion (CTE_{XY}), which may be unacceptable or undesirable in the unsupported resin. Fillers may be added to modify the relative permittivity and/or to exclude resin and thereby reduce the overall CTE in X, Y, and Z dimensions.

The thicknesses of woven glass reinforced materials are typically even multiples of the reinforcement thickness plus resin.

4.1.1.3 Claddings Copper is by far the most common cladding material around which most circuit board processes have been designed. Copper foils are sold by weight, with 1/2 (153), 1 (305), and 2 (610) oz/ft² (gm/m²) being common. These weights roughly translate to 0.018 mm, 0.035 mm, and 0.07 mm [0.0007 in, 0.0014 in, and 0.0028 in] in thickness respectively. Thinner foils are available.

For high-speed circuitry it may become necessary to provide special cladding material:

- With reduced (inner) surface roughness ($\leq 2 \mu\text{m}$ [78.7 μin]) in order to minimize line resistance.
- Permitting advanced interconnection techniques (e.g., ultrasonic bonding).

Copper foils are available in rolled annealed or electro-deposited forms. Other properties of copper foils relate to their ductility and elongation characteristics, which may impact through-hole reliability. For more information on foils, consult IPC-4562. Untreated copper foils shall have the following maximum resistivity at 20 °C [68 °F].

For deposited foil:

Weight Designator

E	0.181 ohm-grams/meter ²
Q	0.171 ohm-grams/meter ²
T	0.170 ohm-grams/meter ²
H	0.166 ohm-grams/meter ²
M	0.164 ohm-grams/meter ²
1 oz. and over (305 gr/m ²)	0.162 ohm-grams/meter ²

For wrought foil (all weights):

Type 5, 8	0.158 ohm-grams/meter ²
Type 6	0.153-0.157 ohm-grams/meter ² according to temper
Type 7	0.152 ohm-grams/meter ²

4.1.1.4 Discrete Wiring The wire resistivity of insulated wires for high-speed circuitry utilizing discrete wiring boards is shown in Table 4-1.

Table 4-1 Wire Resistivity

Diameter	AWG	Resistivity @ 20 °C [68 °F]
0.064 mm [0.0025 in]	42	1.80 ohms/ft
0.1 mm [0.004 in]	38	0.648 ohms/ft
0.16 mm [0.0063 in]	34	0.261 ohms/ft

4.1.1.5 Prepregs, Bonding Layers and Adhesives Various thermosetting and thermoplastic materials are available for laminating the multilayer package. Prepregs are woven glass supported resins in their B-stage or partially cured state. They are used to create the dielectric spacing between layers and are cured or cross-linked in the lamination process. Thermoplastic bonding layers may also be used for dielectric spacing and work by fusion bonding in lamination cycles exceeding their melting point. Thermoplastic bonding films and thermosetting adhesive films are thin unsupported materials used in configurations where the dielectric spacing is already provided by another material.

4.1.1.6 Material Tolerances Knowing the raw material tolerances from the outset will go a long way toward predicting the probability that a given design will perform within the desired specifications and form the basis for any sensitivity analysis. Impedance calculations are heavily impacted by thickness (dielectric spacing) and relative permittivity; therefore, these are of primary interest.

1. Relative Permittivity (ϵ_r) – The relative permittivity of the un-reinforced materials should be invariant as these are generally uniform, isotropic materials. The reinforced, supported, and filled materials are combinations of materials of different relative permittivity and will exhibit variations in this value unless the proportions of the combination are strictly controlled.

2. Thickness – Changes in the volume percent of resin will impact both thickness and relative permittivity. Thickness uniformity among materials will vary with the technology and the level of process control employed.

4.1.1.7 Material Impact on Board Fabrication/Assembly The specific details of circuit board manufacture are not discussed here. However, the effects of materials properties on manufacturing issues are listed as they impact design considerations. This list is not exhaustive.

1. CTE_{XY} – The expansion characteristics of the printed board under thermal load will impact the choice of components, the style of leads, and the method of mounting to minimize CTE mismatches that may ultimately reduce joint reliability. The reverse is also true. If the choice of component package and lead has already been made, then the material choice follows. In other cases, other materials may be incorporated into the package to further constrain movement in the X and Y directions.

reducing any CTE mismatch. Various thermal management schemes may also provide some relief in this regard.

2. **CTE_z** – Thermal expansion in the z-axis may impact through-hole (PTH) reliability in fabrication, assembly and in service. Advanced techniques or controls may be required to utilize high z-axis expansion materials. The number of layers or the overall thickness of the package may have to be limited or in some cases may preclude the use of PTHs altogether. Use of discrete wiring for replacing multiple etched signal layers can significantly reduce board thickness and eliminate z-axis expansion concerns.
3. **Young's Modulus** – The ratio of unit stress to unit strain.
4. **Poisons Ratio** – The ratio of lateral strain to longitudinal strain.
5. **Dimensional Stability** – Dimensional changes in the material impact layer-to-layer registration. Advanced techniques or controls may be required to utilize less stable materials.
6. **Thermal Properties T_g** – The glass transition temperature T_g of the material will dictate the thermal processes employed either in fabrication or component attachment.
7. **Chemical and Solvent Resistance** – These properties will dictate chemistries that can and cannot be used for processing and cleaning.
8. **Machinability** – The relative ease with which a material can be drilled, punched, and routed will impact the cost of fabrication.

4.1.1.8 Circuit Board Fabrication and Tolerances A general understanding of the capabilities of board fabrication technologies and the realistic and achievable tolerances is critical to the successful implementation of designs. Areas of particular interest are:

- a. **Hole Location and Diameter** – impacted by drills, material, dimensional stability, drilling practices, and plating.
- b. **Conductor Width and Spacing** – impacted by artwork, imaging, copper foil thickness, etching and plating. The PWB conductor is determined by wire size selection, and can be spaced on a variable XY grid or on the 45-degree diagonal.
- c. **Conductor Geometry** – impacted by imaging technique, cleaning, etching and plating. The DWB inherent wire uniformity is not affected by subsequent fabrication processing.
- d. **Dielectric Spacing** – impacted by choice of prepreg or bonding layer or film and lamination conditions.

Note: Prepreg thickness (and therefore permittivity) may vary with pressing conditions. For calculation purposes, the designer should consider the effective permittivity and thickness of a prepreg after the lamination cycle and account for any permittivity mismatches that may exist between the prepreg and other layers.

4.2 Component Packaging

4.2.1 Device The component package must be considered when selecting high-speed design rules and determining properties. The device package will establish thermal and electrical guidelines. Lead length is the predominate factor for passive components. The leads provide additional inductance and capacitance, which will affect propagation speed and switching transients. To minimize these effects the leads should be trimmed as short as possible or removed. Surface Mount Device packaging can provide leadless devices, which can be directly mounted to the interconnecting substrate. It is important to note that component data sheets often do not provide parasitic values for high-speed noise and propagation speed calculations.

Active devices, such as integrated circuits, are often offered in several package styles that provide various electrical and thermal performances. In general use, DIP packages have been the predominate package in either plastic or ceramic. These typically are the largest packages and provide the worst high-speed operating environment. The next best package style is the Surface Mount Package. These are offered in either Chip Carrier or Small Outline IC packages. These typically will reduce the lead capacitance and inductance. SM packages can easily be automatically assembled and handled. To obtain the optimum performance from the device, assuming operating conditions and reliability standards can be met, the die should be directly mounted to the substrate using either the Chip-on-Board (COB) or Tape Automated Bonding (TAB) approach. These offer the optimum approach since no additional capacitance or inductance is added with the exception of the bond wire (for COB) or copper conductor (for TAB).

4.2.2 Connectors Board to board connections are often the most troublesome high-speed connections because a continuous signal path is not possible due to mechanical constraints. There are two primary approaches to reduce the signal discontinuity.

The first approach assumes that the connector style is fixed, so the pin-out must be modified to provide a good signal path. Nondifferential signals reference between the active signal line and the closest voltage or ground reference plane.

Board to board connections are often troublesome because of mismatches in characteristic impedance. Nondifferential signal conductors rely on controlled geometries and layering.

AC reference planes (either DC voltage or ground planes) for impedance control. These geometries are interrupted in the connector.

Efforts to control signal and reference pin quantity and location in the connector should be made to control electrical performance.

To reduce the noise more reference pins must be added to reduce the distance and sharing problems. Generally a 3:1 signal to reference pin ratio is sufficient. The best ratio is 1:1, but may be too expensive, or consume too much real estate.

The second approach is to modify the connector. The intent is to minimize the discontinuity distance between boards. Either shortening the pin length, or adding reference ground plane within the connector can be used.

4.2.3 Cables High-speed cables must provide a good signal environment. There are three areas that must be considered; signal propagation speed, crosstalk, and induced noise.

Crosstalk can be minimized by several methods. The easiest is to put ground lines between the signal lines to isolate adjacency. A ground plane can be added which lowers the signal line impedance. The best method is to completely isolate signals using a coax line environment. This provides total isolation, but also is the least dense approach.

Putting a shield between the signal line and the radiating source can lower induced noise coupled onto the lines. Using the ground planes mentioned above, or providing an additional shield plane over the entire structure can accomplish this.

4.3 Thermal Considerations Electronic equipment processes information at the expense of electrical energy. The electrical energy fed to the machine is converted into other forms of energy and dissipated into the machine environment. There are two main ways of dissipating this energy;

- Electromagnetic Radiation
- Heat (Thermal Energy)

The electromagnetic radiation is generated because interconnections between two points on a board act as an unintentional antenna. The greater the area enclosed by the loop and the higher the frequency and the input current, the higher the level of energy radiated from the system. Even though the continuous increase of signal speed in equipment increases the amount of radiation, the quantity of energy lost in this way is negligible when compared with the quantity of energy converted to heat. Because industry regulations limit the amount of energy radiated from the system in the form of electromagnetic waves, this form of energy is generally captured by enclosures and eventually transformed into heat before it dissipates to the environment.

In order to understand the new aspects of the problem created by increasing the signal speed, one has to start by considering that with slower technologies the partitioning of the board is independent of the electrical signal characteristics. Under such conditions, the device positioning on the board and routing of the interconnect traces can be done keeping a few considerations in mind, such as thermal requirements. Under the high-speed conditions, the characteristics of the signal will practically dictate the positioning of the device, the routing of the interconnections, and the material to be used as well as the size and characteristics of the device package. All of these determinants will have very strong impact on the selection of the cooling option and the entire thermal design of the system.

4.3.1 System Level Impacts The increasing of the signal speed is necessary because it can increase the quantity of information that is processed per unit of time. As mentioned before, electronic equipment processes information at the expense of energy (electrical), which is absorbed from the source and lastly transformed into heat that must be removed from the system. For example, Figure 4-1 shows a schematic representation of flows of information, electrical energy and heat in a computer room environment.

With electronics becoming more powerful due to the use of high-speed technology, the energy required to operate the whole system of information processing and heat disposal is becoming a matter of great concern to both the manufacturer and customer alike. Translating this issue into thermal terminologies; “high-speed” often means more heat dissipation per unit volume. Ambient air generally is the ultimate heat sink, therefore it is expected that the temperature of this air will increase resulting in a “hotter” environment for any considered device. The possible solutions at the system level are:

- Increasing ventilation in order to reduce the air temperature by injection of cold air from outside.
- Use of heat exchangers (air to water or coolant) in order to evacuate the heat accumulated in the air in such a way as to reduce the ambient air temperature.
- Use of active mechanical systems for air conditioning.

Replace the air as a cooling agent with other fluids which have a higher specific heat capacity and are easier to circulate and refrigerate (such as water, freon and other organic fluids).

4.3.2 Board Level Impacts The effect of heat on high-speed signals can be immense. Electronic signals typically degrade as the temperature increases. Slower signal transition times result and they may become more sensitive to system electrical transients.

The success of any thermal management approach depends mainly on the ability of the designer to find a way to “spread” the concentrated heat over a large area.

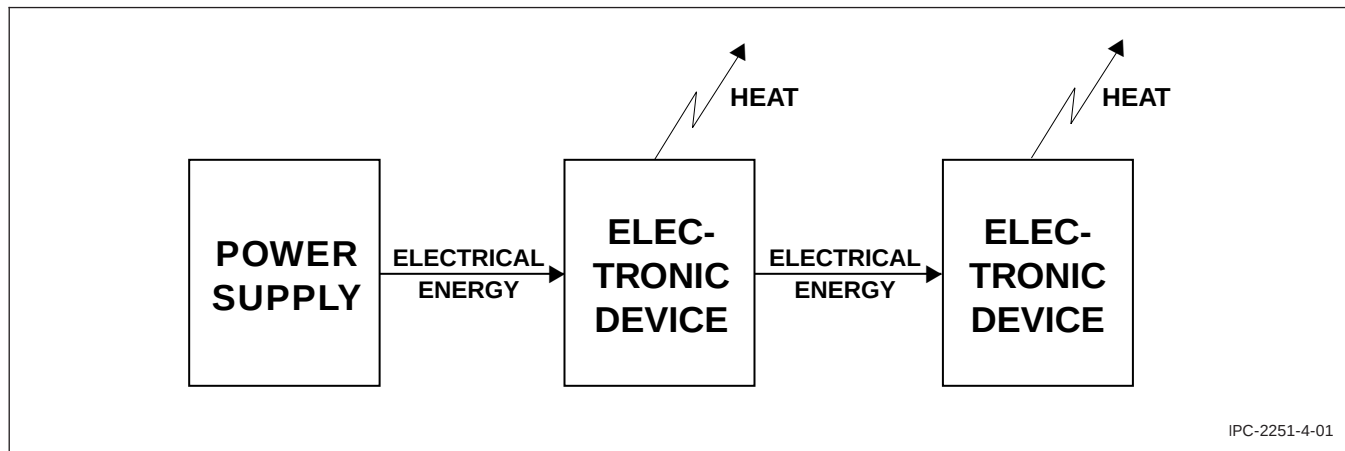


Figure 4-1 Schematic of Information, Electrical Power and Enthalpy (Heat) Flows

to reduce the peaks of the temperature field created by uneven power dissipation. This task is especially difficult today when we consider the properties of the materials involved in high-speed technology: materials with a low permittivity are needed, but these tend to have very poor thermal conductivity as well. For example, in order to spread the heat conducted by an active device, hybrid technology with a ceramic substrate is usually utilized. If the requirements for speed are very high, ceramic substrates may not be a viable option because they have a permittivity two to four times that of FR-4 glass epoxy. Possible solutions to confine this problem are:

- Better air flow management that ensures directing of the air to overheated areas.
- Conduction cooling and thermal spreaders (the heat is conducted to larger areas from which it can be removed).
- Immersion of the electronics in dielectric fluids.

Immersion cooling could be considered a very costly, efficient way of dealing with both high power dissipations as well as uneven dissipations of high concentrations in small volumes.

Beside the capability to spread heat rapidly into the entire volume of the enclosure these fluids can also act as cooling agents by absorbing the heat from the devices and transferring it either to another cooling loop or directly to the environment. The boiling temperature of the immersing fluid can be selected in such a way as to coincide with the maximum temperature admissible in the system. Phase changing of the fluid (boiling and condensation) could practically maintain the temperature of the electronics at a preset constant.

In order to understand the impact that high-speed technology has had on thermal design, one has to consider the multi-chip modules symbolized in Figure 4-2 by double circles. Joining together a certain number of semiconductor chips with controlled impedance transmission lines in order to achieve particular electrical performance creates high-speed multi-chip modules. However, grouping the devices

close together in order to reduce interconnection distance may produce localized hot spots.

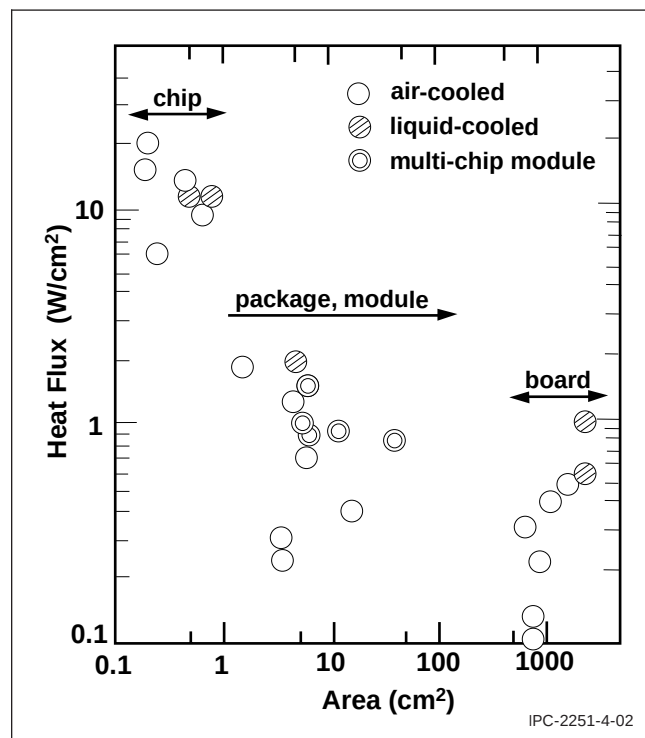


Figure 4-2 Heat Flux vs. Component Area

4.3.3 Device Level Impacts The component package has a direct impact on the performance of the device. At the same time the thermal characteristics of the device package are worsening almost linearly with the decrease of the device size. Generally, a way of improving the device package thermal performance is the use of ceramic materials for enclosures. As specified in the previous discussion ceramic materials have higher electrical permittivity that will negatively impact electrical performance of the package if very high-speed devices are involved. Low permittivity materials that improve the electrical performance tend to be very poor thermal conductors and as a result

inside the semiconductor enclosure. Higher speed is usually associated with a temperature rise in the semiconductor itself and this presents an important challenge when high reliability of the product is required. Reliability decreases as temperature rises.

4.4 Component Placement Component placement is a critical factor in the design of high-speed systems. The effects of improper placement can be significant and include concerns in the following areas.

- Crosstalk Management
- Impedance Control
- Power Distribution
- Thermal Management
- System Cost

4.4.1 Crosstalk Management Typically, crosstalk is a concern when high-speed devices are used because of the high harmonic frequency content. Mixing logic families also causes concern because of the mixture of various voltage swings, noise margins and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL swings 3 volts and the ECL family has only a -100 mV DC noise margin significant undesired coupling can occur.

When copper planes are used to distribute logic levels, crosstalk (coupling) can also occur through the ground return path for these signals. This is called common mode impedance coupling. Essentially, a returning signal causes a ground potential rise due to the DC resistance of the plane. This problem can be very significant especially in analog circuitry when digital logic is present.

Several techniques can be used to control crosstalk in these environments.

- a. Confine logic families geographically.
- b. Restrict signal conductors for each logic family to those areas.
- c. Provide separate return paths for each logic family.
- d. Place components away from I/O connector in ascending order of speed (see Figure 4-3). Taking care to keep the high-speed signals away from the board edge. This will reduce EMI emission and improve EMI immunity.
- e. Terminate controlled impedance conductors to reduce reflections that generate more noise.
- f. Restrict conductor parallelism.
- g. Specify and control conductor-to-conductor spacing.
- h. Place components close together to minimize conductor lengths and parallelism.
- i. Lower the relative permittivity.
- j. Reduce the signal to ground separation.

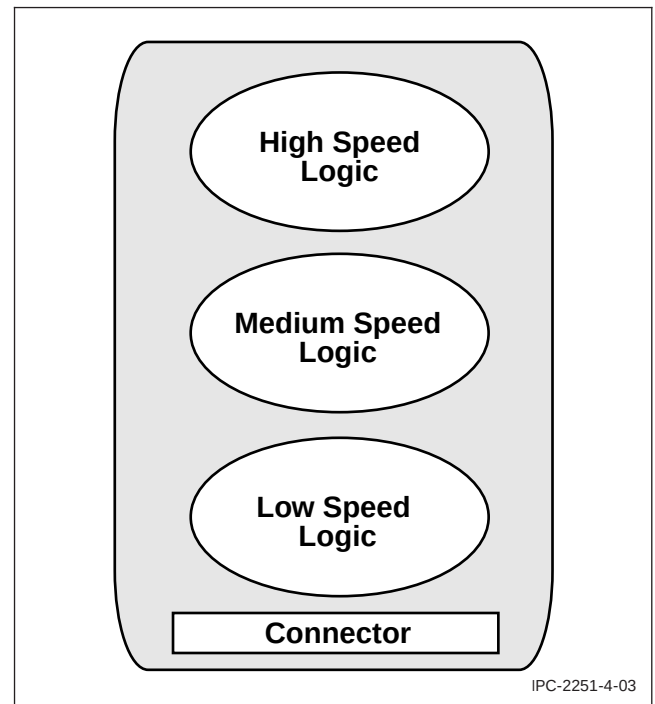


Figure 4-3 Component Placement Guideline

The impact on circuit board design due to these considerations will include:

- a. Circuit board technology must now be capable of managing crosstalk.
- b. Multiple power and ground planes required.
- c. Added density due to the addition of terminations and tight placement.
- d. Selective signal routing criteria.

These can greatly increase complexity and place limitations on the available circuit board technology.

4.4.2 Impedance Control In cases where high-speed signals are being transmitted, the signal conductors may need to be considered as transmission lines. This means, as a minimum, specifying the characteristic impedance of those lines. Since transmission lines should be terminated in their own impedance, a designer must provide for termination resistors.

Specifying a controlled impedance board and providing for termination resistors will add complexity to the design.

- a. Termination resistors (one for each signal line) increase density and complexity.
- b. Placement should be made so that each signal travels the shortest path from source (first point) to termination. Poor placement can result in very dense signal routing.
- c. Circuit board technology must now be capable of controlling impedance.
- d. Minimum component-to-component spacing may eliminate the need for controlled impedance lines but may greatly increase density.

4.4.3 Power Distribution Higher speed devices require the power supply to provide energy quickly. Figure 4-3 illustrates a typical board placement that shows the lowest speed logic near the connector and the highest speed logic away from the connector (This assumes the use of decoupling capacitors to provide the instantaneous power required for high speed devices.) Placement of these devices is not only dependent on performance requirements, but also on thermal requirements and capabilities.

4.4.4 Thermal Management As mentioned, high-speed devices can consume great amounts of power, and consequently dissipate much heat. In the placement of components, the following thermal management techniques should be considered.

- When possible, “hot” components should be spaced apart as greatly as possible.
- Convection Cooling-Components should be placed such that air flows parallel to component orientation.
- Conduction Cooling usually involves the placement of a metal ‘heat sink’ or ‘chill plate’ on the surface or buried within the board. In these applications, placement must allow for sufficient metal surface area (i.e., usually requires greater component spacing).

4.4.5 System Cost Consideration should always be given to the cost of design and manufacturing. Generally, complexity adds density and cost. Cost does not necessarily just mean dollars. Cost can include lead times and reliability. Over-specifying a design “to be sure it will work” can significantly impact total cost.

Designing high-speed circuits is rarely a simple matter. There are many factors to take into consideration that usually act in direct opposition to one another.

Placing high-speed components closely together might reduce the need for transmission line parameters and reduce crosstalk problems, but may result in thermal management problems and increase the number of layers in a circuit board (due to increased density). Increasing the spacing will reduce the thermal problems but could add crosstalk and impedance restrictions. We can see that in high-speed design there are many considerations. It is the job of the circuit designer to understand the system specifications and weigh the alternatives to provide the simplest, cost effective, reliable solution for meeting those specifications.

5 ELECTRICAL CONSIDERATIONS

5.1 Power Distribution This section presents information used for calculating low and high frequency noise characteristics for system power distribution. Factors degrading power distribution may be grouped into two

major categories; metallic losses and parasitic inductance in capacitors, IC lead frames, and planes. Spurious radiation loss is generally negligible.

The DC power distribution system encompasses the system from the output of the power supply to the input of each device. For systems with many cards and supplies, a simulation of the interaction of each component is desirable to verify and assist the design effort.

5.1.1 System DC Model The DC distribution model is comprised of lumped resistance for each element in the system. Figure 5-1 shows the interconnection and the major subsections of the model. This DC model analysis determines the DC voltage drop between the power supply and every integrated circuit location. The major elements in this model are described below.

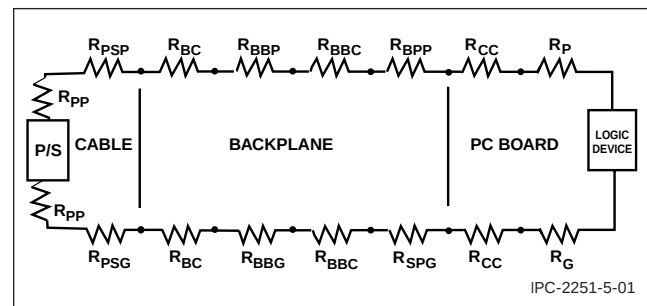


Figure 5-1 DC Distribution Model

5.1.1.1 Power Supply to Power Supply Cable Resistance (R_{PP}) R_{PP} is the contact resistance of the power supply cable to the power supply output. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc., to keep the voltage drop less than 5 mV.

5.1.1.2 Power Supply Cable/Harness Resistance (R_{PSP} , R_{BSG}) This is the resistance due to the interconnection cable or harness from the power supply to the backplane or backplane power distribution busbar. The interconnection can take the form of a cable (circular or flat) or a busbar. R_{PSP} is the resistance of the positive voltage cable. R_{BSG} is the resistance of the power supply ground return cable. Typical resistance for various gauges of copper stranded, rope wound, medium hardness cables at 25 °C [77 °F] are listed in Table 5-1.

5.1.1.3 Power Supply to Busbar Connection Resistance (R_{BC}) This is the contact resistance of the power supply cables to the backplane busbar. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc., to keep the resultant voltage drop less than 5 mV to 10 mV.

Table 5-1 Copper Wire Characteristics

Gauge	Number of Strands	Diameter in.	Area sq. in.	Resistance mΩ/ft.
2/0	19	0.419	0.1045	0.08224
1/0	19	0.373	0.0829	0.10370
1	19	0.332	0.0657	0.13080
2	7	0.292	0.0521	0.16490
3	7	0.260	0.0413	0.20790
4	7	0.232	0.0328	0.26220
5	7	0.206	0.0260	0.33060
6	7	0.184	0.0206	0.41690
7	7	0.164	0.0164	0.52570
8	7	0.146	0.0130	0.66290
9	7	0.130	0.0130	0.83590
10	7	0.116	0.0082	1.05400
12	7	0.092	0.0051	1.67600
14	7	0.073	0.0032	2.66500
16	7	0.058	0.0020	4.23700
18	7	0.046	0.0013	6.73800

5.1.1.4 Busbar Resistance (R_{BBP} , R_{BBG}) This is the resistance of the backplane power distribution busbars from the power supply cable contact to the backplane contact. R_{BBP} is the positive busbar resistance. A busbar is a metal strip that has a lower resistance than the backplane or circuit board. R_{BBG} is the ground return busbar resistance. For multiple backplane connections, this resistance will be modeled as a series of resistances between each backplane connection point. Cross-sectional resistances for copper (99% pure) at 25 °C [77 °F] are listed in Table 5-2.

Table 5-2 Copper Busbar Resistances/ft

Cross-Section Area (sq. in.)	Resistance (mΩ)
0.1662	0.050
0.1318	0.063
0.1045	0.080
0.0829	0.102
0.0657	0.128
0.0521	0.162
0.0413	0.204
0.0328	0.257
0.0260	0.324
0.0206	0.409
0.0164	0.515
0.0197	0.650
0.0103	0.820
0.0082	1.033
0.0065	1.300
0.0051	1.640

5.1.1.5 Busbar to Backplane Connection Resistance (R_{BBC}) This is the contact resistance of the backplane bus-

bar to the backplane. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact.

5.1.1.6 Backplane Resistance (R_{BPP} , R_{BPG}) This is the plane resistance from the busbar contact to the circuit board (daughter card) connector. R_{BPP} is the positive voltage plane resistance. R_{BPG} is the ground return plane resistance. Since most power distribution systems have distributed daughter card contacts R_{BPP} and R_{BPG} will be the resistance between each contact point.

5.1.1.7 Backplane to Daughter Board Connector Resistance (R_{CC}) This is the backplane to daughter board connector pin and contact resistance. This resistance should be the value at the end of life. For a multiple backplane to daughter board interconnect scheme the resistance will be broken down into each contact. For lumped connector pin locations, the pin resistances can be paralleled. For two-piece connector systems R_{CC} is the total resistance for both connectors.

5.1.1.8 Daughter Board Resistance (R_P , R_G) This is the power plane or line resistance for the daughter board. R_P is the positive voltage plane resistance. R_G is the ground return plane resistance.

5.1.1.9 Paralleling of Power and Ground Conductors It is recommended that multiple cable conductors and/or connector pins be provided for power and ground connections. This accomplishes two major goals of power distribution and signal integrity. It reduces the resistance and inductance of the conductors by paralleling them. This is especially important in high-speed designs due to the instantaneous current demands placed on the interconnects. In addition, multiple pins offer long-term protection. As the mated connections age, oxidation occurs and their resistance increases. Multiple pins help keep the resistance low to avoid runaway heating degradation. Occasionally, a pin is mechanically damaged or overheated during its life by multiple insertions or hot plugging, providing multiple pins reduces the resulting failure and/or intermittent problems.

5.1.2 Power Plane Impedance The power distribution planes utilized in backplanes and daughter boards do not have zero impedance. Likewise the power supply does not have a zero source resistance. A circuit diagram of a multilayer power distribution network is shown in Figure 5-2.

The power supply is represented by a voltage source V_S , R_{SP} , and R_{SG} (see Figure 5-2). The distribution impedances are broken out as backplane and daughter board sheet inductances, resistances, and plane-plane capacitance.

5.1.2.1 AC Impedance The power distribution AC impedance is subdivided into three components as shown in Figure 5-3. The first is the switching transient impedance

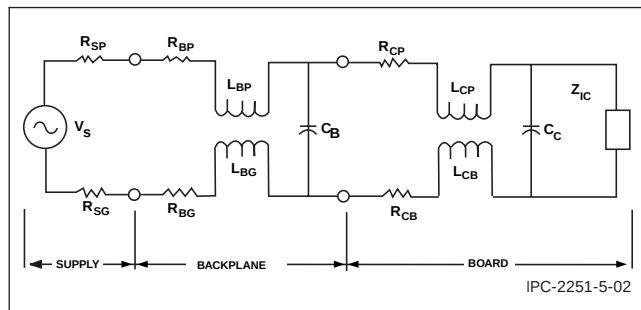


Figure 5-2 DC Power Distribution System (Without Remote Sensing)

(Z_{SW}). This impedance corresponds to the interconnect between the plane capacitance and the component. Using internal power planes that are very closely spaced can increase this capacitance reducing the effective impedance.

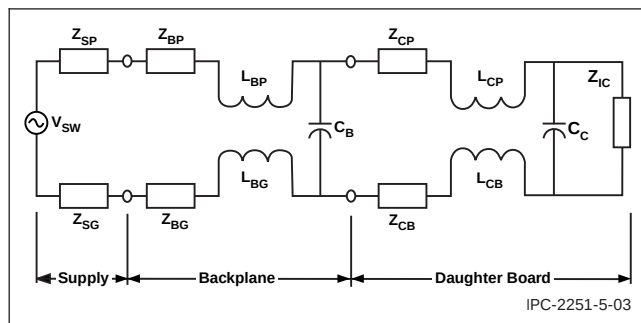


Figure 5-3 Decoupling Impedance Modeling - Power Supply

The second component is the impedance due to the bulk capacitor charging the IC decoupling capacitors (Z_{BC}). The current in this impedance is lower frequency and higher amplitude than the current in the first component. The voltage drop due to the lower impedance because of the lower frequency involved will be less than the above case.

The bulk decoupling capacitance refresh component (Z_{RC}) is the final element of the circuit board decoupling impedance. This current is responsible for recharging the bulk capacitors. It is supplied from the power supply and will usually have the lowest frequency component of the current.

Each of the board impedance components will be modeled as a transmission line plane-over-plane network. This closely models the worst-case configuration because of the regular layout of the printed circuit boards. A brief explanation follows.

The general impedance equation for parallel planes is as follows (reference Figure 5-3):

$$Z_p = \sqrt{R_p^2 + (L_p - C_p)^2} \quad [0.1]$$

where: $L_p = \sqrt{2\pi f L}$
 where L is plane inductance
 R_p = Plane Resistance

$$C_p = \frac{1}{2\pi f C}$$

where C is the plane capacitance

5.1.2.2 DC Resistance The static voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance, R_T .

$$R_T = \frac{679}{T_p \mu\Omega/\text{square}} \quad [0.2]$$

where: T_p = thickness of plane (mils)

A model analysis is used to determine R_T between each integrated circuit location. A computer program can be utilized to simplify the calculations. Each device is modeled as a point load and each connector pin is treated as a point source.

5.1.3 Integrated Circuit Decoupling A packaged device must provide sufficient current for its circuitry to operate. This includes high peak current requirements during output switching. The circuit board power system must provide this current without lowering the input supply voltage below its required minimum level.

When the power supply is too far away or the stored energy in the board is insufficient, capacitors are placed near the devices, connected between the power and ground planes to provide this current. In a sense, these capacitors provide the charge current to the device instead of the power planes. The power plane creates a capacitor that can also provide a small amount of high frequency current. These planes should be spaced very close to maximize their capacitance. When they discharge their current into the device they quickly recharge from energy stored in slower discharging capacitors and power supplies in time for the next required discharge.

5.1.3.1 Decoupling Model Figure 5-4 presents a device-decoupling model. Shown are the decoupling capacitor, power planes, signal load, and device models. The device decoupling system is composed of several elements. Every element can be modeled as a network of resistors, capacitors, and inductors. Figure 5-4 illustrates the interconnection of the following decoupling system components:

- Decoupling Capacitor - (C_D)
- Device Power Lead - (R_p, L_p)
- Device Ground Lead - (R_G, L_G)
- Transmission Line Load - ($Z_O + Z_{LOAD}$)
- Destination Load - (Z_L includes C_{LOAD}, R_L, L_L)
- Power Plane - (C_D, C_{Plane})
- Power and Ground input vias - (L_{P-In}, L_{G-In})
- Trace and via inductance - ($L_{V-Trace}$)

Note: Some parasitics not shown.

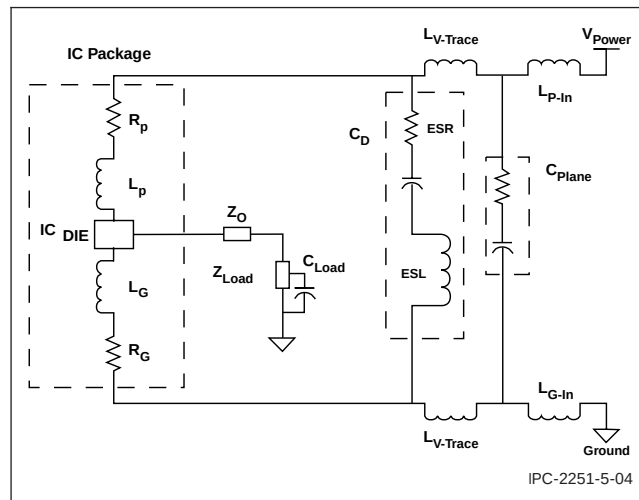


Figure 5-4 Device Decoupling Model

5.1.3.2 Switching Current Frequency Content An integrated circuit has two power supply current components; steady-state bias and output drive. Component data sheets, SPICE models, IBIS models and other proprietary models provide these current specifications.

The steady-state bias current is listed over the full temperature and supply voltage specifications. On large devices, such as microprocessors and memories, an average value is provided for power supply size estimation.

In CMOS devices the frequency dependent output drive current is typically not specified and must be calculated. This is especially true of large programmable devices. Some large programmable devices have multiple supply voltages. Some have one supply voltage for the logic core and another voltage for the I/O drivers. Since these currents are almost always dependent on the operating frequency and/or loaded drive, the vendor's calculations should be used. Most device manufacturers supply calculation approximations for frequency dependent power dissipation on their web sites. Because the signal loads and the device outputs are nonlinear, the current is typically best characterized by a time dependent current waveform.

The frequency response required by the decoupling capacitor system (actually, a network), may be predicted by transforming the time domain waveforms into their frequency components (spectra). The frequency response for the power system should be modeled based on expected activity in locations on the board. This will be generally be dominated by device risen times, not just the primary clock frequency. Many parameters must be considered when designing the Power Distribution System (PDS) of a board or system. The PDS should be considered as individual partitions of circuitry that may include multi-sourced voltage supplies. For example, a modern CPU device will have high frequency core voltage requirements and somewhat lower frequency I/O requirements. Exceptions to this may be with serial I/O schemes or Phase Lock Loop (PLLs) that

may be built into the CPU device, which may have very high frequency requirements. Memory devices will have high frequency current requirements that are often at a different voltage source than the CPU core. I/O devices may have multiple frequency and voltage requirements from simple status monitoring/controlling (very low frequency) to high-speed serial and parallel data rates (very high frequency).

5.1.3.3 Inherent Plane Electrical Model 5.1.2.1 presented the parallel plane impedance of a two plane power distribution system. The power distribution model can be partitioned on a per device basis. In the per device model, the plane inductances (L_P , L_G), parallel-plane capacitance (C_P), parallel-plane impedance (Z_P), and plane resistance (R_P) are:

$$L_P = L_G = 0 \quad [0.3]$$

$$R_G (\text{ohms}) = R_T N \quad \text{from equation [0.2]} \quad [0.4]$$

$$C_P (\text{pF}) = \frac{\epsilon_r \epsilon_0 S}{H} = \frac{0.225 \times 10^{-6} \epsilon_r S}{H} \quad [0.5]$$

where:

R_T = Power plane resistance

N = Number of squares

S = Plane area

H = Plane separation

ϵ_0 = Permeability of Free Space

5.1.3.4 Device Output Load Models The signal line load will have two configurations: capacitive line and transmission line. A capacitive load requires a triangular current pulse at the rate of the output edge transition rate. The current pulse will only occur during the transition.

The transmission line load behaves resistively to the incident signal. The output provides a trapezoidal pulse to the line while the transmission line is active. The I_{CC} requirements have this trapezoidal waveform versus a triangular waveform for a capacitive load. The I_{CC} waveforms for capacitive and transmission line loads are shown in Figure 5-5. Figure 5-6 presents the Fourier Transform for the waveform presented in Figure 5-5.

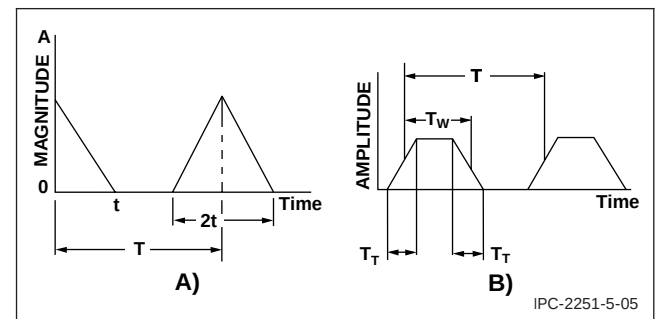


Figure 5-5 Capacitive and Transmission Line Current Pulses – A) is for a very short line and B) is for a long line

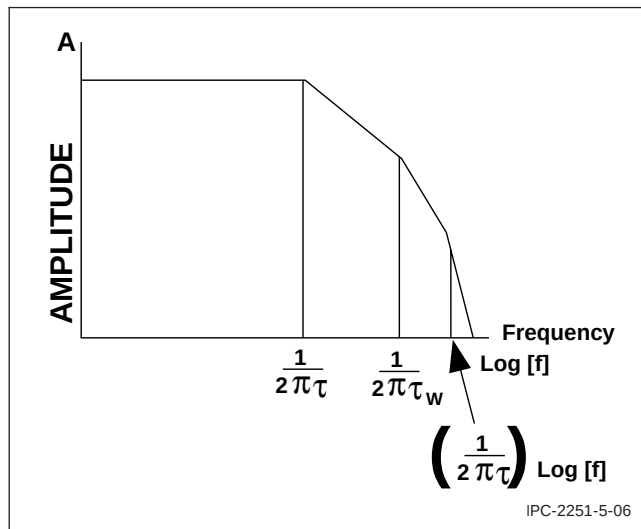


Figure 5-6 Fourier Transform

5.1.4 Decoupling Capacitance and Plane Capacitance

Decoupling capacitors and Plane Capacitance provide current to devices until the power supply can respond. High frequency switching, which is composed of a broad spectrum of very high frequencies, and requires plane capacitance to support them. The discrete capacitors recharge the plane capacitors.

5.1.4.1 Switching Transient Capacitance Switching transient capacitance provides very fast energy to charge the output sections of the device during an output transition. This transient typically contains the highest frequency content of the power to the device but the least amount of energy. With modern devices, this current may be tens to hundreds of amps at the edge rate. Sometimes, this energy requirement is aided by chip capacitance in the form of discrete component capacitors or as part of the package power interconnect (BGA Carrier). Including the decoupling capacitance in the package minimizes the lead inductance between the capacitance and the device that requires the local energy. This capacitance is almost always not enough for the device and additional capacitance must be provided external to the device. If insufficient energy is available, the signal transition time will degrade prior to leaving the device package. The second effect is high frequency ripple currents appear on the Vdd/Vcc rails and planes, which can result in higher levels of EMI.

In high-speed applications, it is necessary to provide a PWB structure where a Power Plane and a Ground Plane are placed adjacent to each other in the stack-up to provide additional capacitance. This structure generally forms a plate capacitor sometimes referred to as buried capacitance. In this structure there is typically less than 0.127 mm [0.005 in] of dielectric thickness between the power and ground planes. The buried capacitance provided by the planes provide high speed switching current prior to the current being supplied by the discrete high frequency

decoupling capacitors. This buried plane capacitance is increased as the planes are spaced closer together or the dielectric constant of the PWB board material is increased. There may be a limit to how close the planes may be placed as far as reliability is concerned. Actual copper plane material is not completely smooth. During the PWB manufacturing process, it is polished for manufacturability, which improves the surface finish. There still remain very small spurs that protrude into the dielectric material between the planes. With smaller dimensions between the planes, a small conductive filament develops that may cause a plane short. This is referred to as Electro migration, Conductive Filament Formation (CFF), or Conductive Anodic Filament (CAF). This starts as a chemical and environmental problem at first and when a voltage bias is applied, the filaments grow from each plane through the dielectric until they complete the shorting filament and cause a short between the planes. Some dielectric materials are less susceptible to the problem. This may also occur with Plated-Through Holes (PTH) as well.

5.1.4.2 Line Charging Capacitance or High Frequency Decoupling

Line charging capacitance provides switching current to charge the signal line after the signal reaches the lines. The charge current is required until the line reaches its quiescent state. If insufficient current is provided to the device, the edge transition time will degrade or become noisy.

5.1.4.3 Low Frequency (Bulk) Capacitance Low frequency capacitance is often termed bulk capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors, and provide switching current for lower frequency requirements. Generally, bulk capacitance is placed at each voltage input to the board. It is also distributed on the board using an “area of influence” method to supply the high frequency decoupling local charge current.

5.1.4.4 Capacitor Model The model for a packaged capacitor is shown in Figure 5-7. R_L and L_L are the resistance and inductance of the capacitor leads, C_C is the ideal capacitance, R_C is loss of the capacitor, and R_{SH} is the resistance of the insulation. R_{SH} and R_C can be added in parallel to give R_P :

$$R_P = \frac{R_C R_{SH}}{R_C + R_{SH}} \quad [0.6]$$

Using R_P , the impedance of the packaged capacitor is given by:

$$Z_C = R_L + j\omega L_L + \left(\frac{1}{R_P} + j\omega C_C \right)^{-1} \quad [0.7]$$

$$= R_L + j\omega L_L + \frac{R_P (1 + j\omega C_C R_P)}{1 + \omega^2 C_C^2 R_P^2}$$

