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IPC-2316

Design Guide for Embedded Passive Device Printed Boards

IPC-2316

March 2007

A standard developed by IPC

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Design Guide for Embedded Passive Device Printed Boards

Developed by the Embedded Devices Design Subcommittee (D-51)
of the Embedded Components Committee (D-30) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

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Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Embedded Devices Design Subcommittee (D-51) of the Embedded Components Committee (D-50) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Special Note of Appreciation

A special note of appreciation goes to the following principal members of the subcommittee who either led the effort or made significant contributions to make this document possible.

Nick Biunno, Sanmina-SCI
William Borland, E. I. du Pont de
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Inc.
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Nemours and Co.

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Joel Peiffer, 3M Company
Virang Shah, Microfab Technologies
Inc.
Richard Snogren, Bristlecone LLC

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Design Guide for Embedded Passive Device Printed Boards

1 SCOPE

1.1 Statement of Scope This document is a guide to established and emerging embedded passive materials and technologies. It should not be used as an endorsement of any particular material or company product.

1.2 Purpose The purpose of this document is to give users and designers of printed boards the necessary information for incorporating embedded passive components into their applications. In addition, it also assists the user in understanding some of the physical and thermal characteristics of the embedded component materials so that their designs can achieve maximum stability and performance.

1.3 Terms and Definitions Terms and definitions shall be in accordance with IPC-T-50 and as stated herein.

Passive Components – Passive components usually refer to resistors, capacitors and inductors but can also include thermistors, varistors, transformers, temperature sensors, and almost any nonswitching analog device that perform the following functions:

- Provide or absorb energy to maintain a constant voltage or current.
- Filter signals to provide safe signals to other circuits.
- Control impedance.
- Sense signals to transmit information to other circuits.
- Delay or synchronize signals to provide timing to other circuits.

Discrete – A single passive element in its own leaded or surface mount technology (SMT) package. Figure 1-1 shows an example of a single resistor, capacitor, or inductor in a 0402 size (generally defined as a 1.0 mm by 0.5 mm [0.040 in by 0.020 in] package). The majority of discrete passives have two electrical contacts that are also used for soldering to the board.

Passive Array – A passive array comprises multiple passive components of like function, which are formed on the surface of a separate substrate and packaged in a single SMT case (see Figure 1-2). The case is then mounted on the primary interconnect substrate of the system. Examples include an array of capacitors or an array of resistors.

Passive Networks – Passive networks comprise multiple passive components of more than one function, which are formed on the surface of a separate substrate and packaged in a single SMT case. The case is then mounted on the pri-

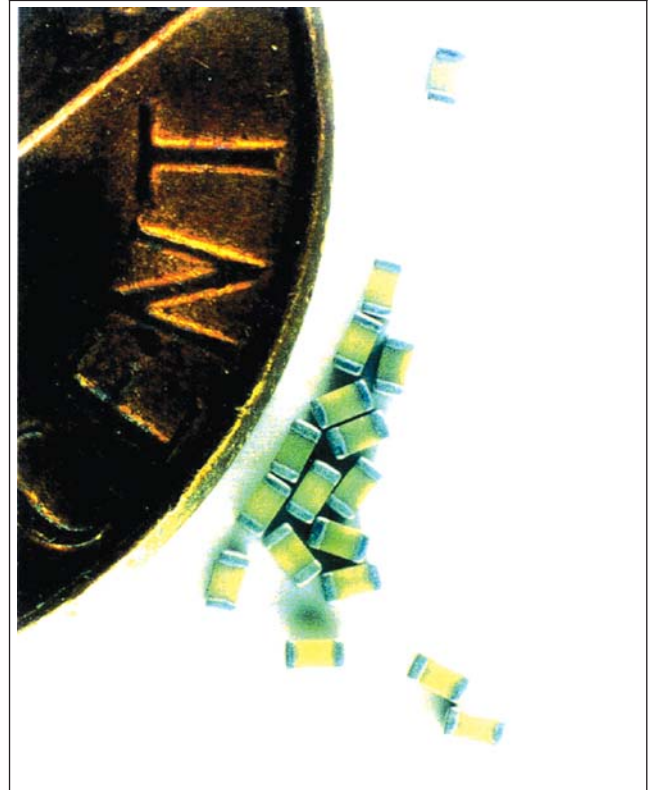


Figure 1-1 Discrete Passives

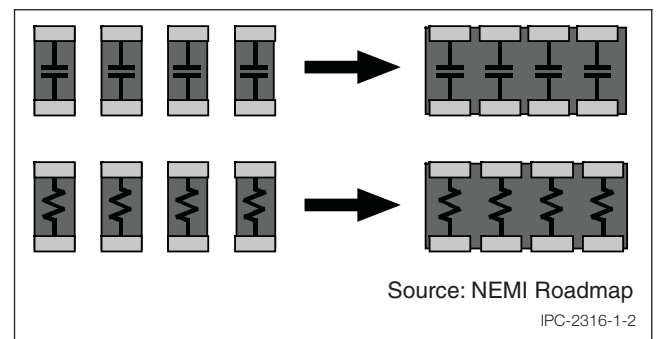


Figure 1-2 Passive Arrays

mary interconnect substrate of the system. These passive networks typically have some internal connections to form simple functions such as terminators or filters.

Integrated Passive Component – Multiple passive components that share a substrate and package. Integrated passive components may be housed inside the layers of the primary interconnect substrate, which would give them the sub-designation of an *embedded passive component*. Alternatively, these components may be on the surface of a separate substrate that is then placed in the end use and

surface mounted on the primary interconnect substrate; in this case, the components would be called *passive arrays* or *passive networks*.

On-Chip Passives – A passive element that is fabricated along with the active elements as part of the semiconductor wafer (die). Since this document is concerned with the passive components that are critical to the interconnect (“glue components”), only the singulated (discrete-like) passives that were eliminated from the system are counted, not the actual passive elements on the active semiconductor die.

Embedded Passive Component – A passive component may be formed or placed, as shown in Figure 1-3, inside the primary interconnect substrate, as opposed to being mounted on the surface. Formed embedded passive components may be singulated (embedded discrete) or embedded

distributed (planar) structures, as shown in Figure 1-4 and Figure 1-5. Embedded passives discussed in this text are formed components. Also, as shown in Figure 1-3, discrete components, passive or active, may also be “placed” in the printed board structure.

Surface Planar Resistors – Resistors manufactured as an integral part of the printed board manufacturing process using the embedded passive resistor materials, except that the resistors are placed on the outer layers of the printed board.

Note: The user’s attention is called to the possibility that utilization of some of the materials described within this design guideline may require use of inventions covered by rights of patents. By publication of this document, no position is taken with respect to the validity of these claims or of any rights of patents in connection therewith. The patent

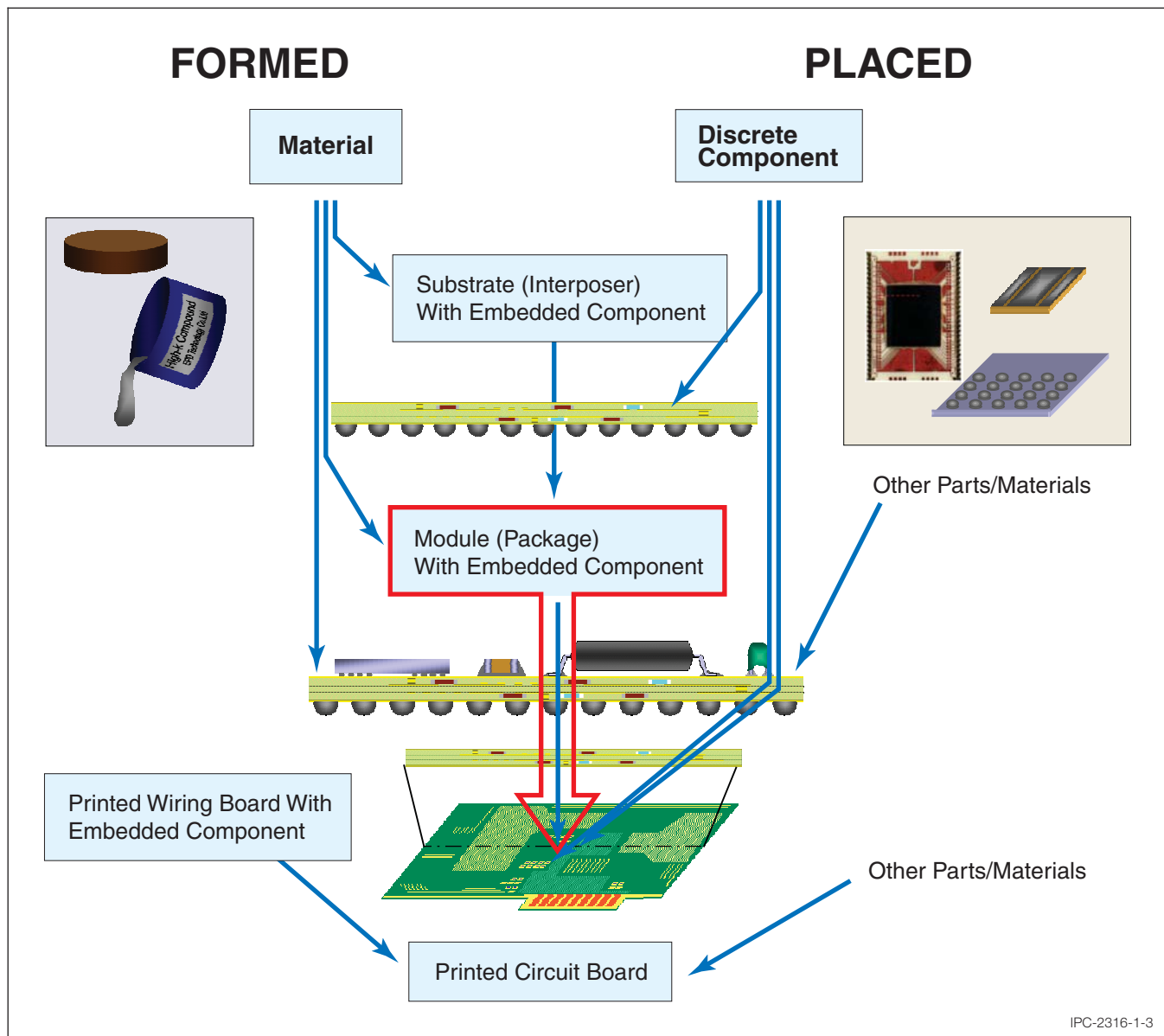


Figure 1-3 IPC, NEMI and JISSO Common Language for Embedded Components

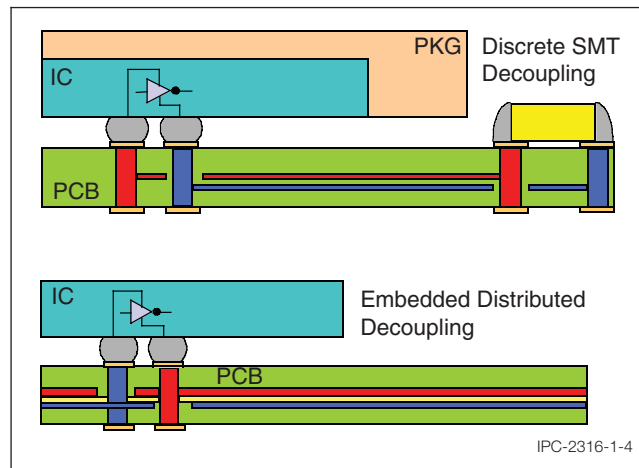


Figure 1-4 Embedded Distributed Capacitor

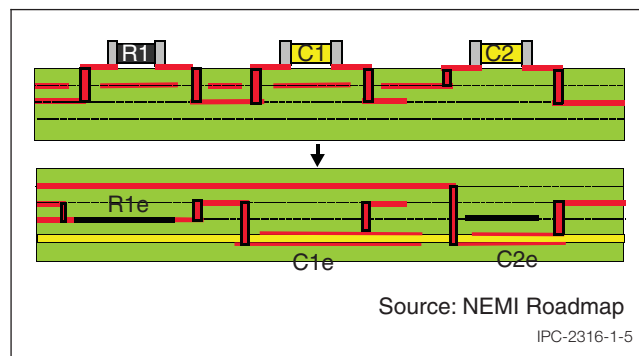


Figure 1-5 Singulated Embedded Passives Construction

holders have, however, filed a statement of willingness to grant a license under the rights of these patents on reasonable and nondiscriminatory terms and conditions to applicants desiring to obtain such a license. Details may be obtained from IPC.

2 APPLICABLE DOCUMENTS

The following documents of the issue in effect at the time of order form a part of this guideline to the extent specified herein. If a conflict exists between IPC-2316 and the listed applicable documents, IPC-2316 does not take precedence.

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-TM-650 Test Methods Manual

IPC-QL-653 Certification of Facilities that Inspect/Test Printed Boards, Components and Materials

IPC-4101 Specification for Base Materials for Rigid and Multilayer Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-4821 Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-9191 General Requirements for Statistical Methods

2.2 National Conference of Standards Laboratories (NCSL)²

ANSI/NCSL Z540-1 General Requirements for Calibration Laboratories and Measuring and Test Equipment.

2.3 International Standards³

ISO 10012-1 Quality Assurance Requirements for Measuring Equipment, Part 1 - Metrological Confirmation System for Measuring Equipment

2.4 International Electrotechnical Commission (IEC) Standards⁴

IEC-61000-4-2 Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test.

3 GENERAL INTRODUCTION

This section reviews both the history of embedded passive components and the economic attributes of a system's design and production including the impact of the decision to use embedded passives and existing models for addressing economic tradeoffs.

3.1 History of Embedded Passive Technologies

3.1.1 History of Additive Polymer Thick-Film Resistor Technology Polymer Thick Film (PTF) resistor technology has been employed in wide tolerance applications for more than 40 years. [1] High volume applications have been varied from simple discrete potentiometers to pull-up and pull-down resistors in hard disk drives. PTF resistors have also been used as strain gauges [2] in mechanical diagnostic applications. At the time of publication for this guideline, the use of PTF materials in high-volume RF applications has also been implemented. [3]

Material and processing costs related to PTF resistors are typically lower than those related to thin-film metal and metal oxide systems. Moreover, the wide availability of PTF sheet resistivities ranging from 1 $\Omega/\square$ (per square) to

1. www.ipc.org
 2. www.ncslinternational.org
 3. www.iso.org
 4. www/iec.ch

1 M Ω /□ that are co-printable on the same layer make the technology compelling for use in printed board technology. However, PTF resistors have not been widely used in modern electronics for three reasons: 1) wide as-printed resistor tolerance, 2) poor resistor stability with environmental exposure, and 3) relatively high temperature coefficient of resistance (TCR) compared to metals and metal oxides.

The first challenge of using PTF resistors is accurate and precise printing. PTF is usually applied to the printed board by screen-printing, which is far less accurate than print and etch methods used for nickel-phosphorus materials. Additionally, the PTF resistors must be cured, and resistivity of the finished material is a small, but significant function of the cure profile. Therefore, tolerances of well-calibrated high-volume PTF resistor processes may be in the range of ± 15 to $\pm 20\%$. Fortunately, many resistor applications in portable products do not require tight tolerances—20% tolerance is often acceptable. Recent advances in thixotropy of PTF inks, especially low value sheet resistivity inks, have resulted in improvements in as-printed tolerances. If these tolerances are not acceptable, multiple companies have demonstrated laser trimming for PTF resistors, trimming resistors to better than $\pm 1\%$, which results in net tolerance (including subsequent processing variation and environmental drifts) of $\pm 5\%$.

The second concern with using PTF for embedded resistors is resistor stability, especially following humidity exposure. PTF termination directly on copper results in relatively poor resistor stability under environmental stress (exposure to 85% relative humidity/85 °C) due to corrosion at the copper/carbon ink interface. This can be ameliorated by printing at fairly large resistor dimensions (widths of several mm), but advanced products require sub-mm resistor widths and high resistor densities to provide significant space (and cost) savings vs. discrete surface mount chip resistors. Silver paste on copper has historically been used as a barrier layer to enable small resistor geometries, but the paste print itself introduced its own errors, including relatively large geometries for the resistor termination pads for paste print registration. Recently, immersion silver on copper has been used as the resistor termination metallurgy. Replacing the traditional silver paste with an interfacial stability promoter deposited directly on the copper terminations substantially mitigates resistor drift under environmental stress while preserving the precise edge definition and density advantages of photolithographically-patterned copper. PTF resistors manufactured with the immersion silver on copper drift less than $\pm 10\%$ following 500 hours of 85% relative humidity/85 °C exposure, and this shift was almost entirely reversed after a 125 °C, three hour bake, indicating that shifts are due to water absorption in the paste rather than termination corrosion.

The third and final hindrance to use of PTF materials is the relatively high TCR as compared to metal films and metal

oxide films. It is true that PTF materials possess TCRs on the order of 100ppm/°C vs. the order of 10ppm/°C for metal films. For many applications, this level of temperature drift is acceptable. However, many PTF material makers are working on improving their PTF temperature performance.

Boundaries preventing wide application of PTF resistors in modern electronics are being traversed. Improvements in paste printing and termination metallurgy have negated many of the potential problems related to tolerance and resistor stability. Improvements by ink suppliers in ink thixotropy and possibly in TCR are also evolving the technology. The benefits of covering more than five decades of resistance practically on a single board with PTF technology have outweighed the remaining barriers in the minds of many modern-day OEMs.

3.1.2 History of Additive Thin-Film Resistor Technology

The concept of plated additive resistors came from two inputs:

- Planar deposited nickel phosphorus resistors had been used commercially for some 15 years when the concept of additive resistors came up. Prior nickel phosphorus resistors had been made, as now, by etching deposited nickel phosphorus sheet layers (carried on copper foil). The cost per square foot of incoming nickel-phosphorus-on-copper foil was considered to be high, so one cost reduction method consideration was to only deposit nickel phosphorus where needed.
- Electroless nickel phosphorus can be selectively plated by immersion of a catalyzed printed board laminate in an electroless nickel bath. The critical step is to block off the bare laminate where no plating is desired. This is done with laminated dry film photoresist. Performance of dry film photoresist through the electroless nickel plating step was a key requirement to make the process work. Also it was recognized that the background catalyst would need to be removed from the laminate areas before pressing.

A North American board fabricator submitted a test artwork they used for etched nickel phosphorus resistors. This etching image was reversed and the precatalyzed inner layer plated in a standard electroless nickel bath. The fabrication showed significant promise after that first experiment. Subsequently, optimization of electroless nickel bath to increase deposit resistance, dry film performance through electroless nickel plating, and improvement of deposit properties during multilayer pressing were added tasks.

In 1998, the Embedded Passives proposal to the NIST Advanced Technology Program was made by 12 companies. Plated additive resistors were included in this proposal, as an alternative to the traditional etched film or PTF technologies. Throughout the four year demonstration (1999 to 2003), incremental work on dry film resistors

compensation for resistor size, and offset of plated value for change in lamination were undertaken.

Also, other compatible technologies were demonstrated that improved the accuracy of the plated additive resistors. Laser trimming is regarded as being easy with the deposited electroless metal resistors. In addition, “trimming down” was demonstrated by inkjet printing of conductive polymers onto the plated additive resistors. No performance issues were detected with either of these accuracy improvement technologies.

3.1.3 History of Subtractive Planar Thin-Film Resistor Technology A study of the history of printed board design shows the impact of planar resistor technology. Driven by ever increasing frequency, component and I/O densities and the need to reduce form factors and costs, embedded resistors have become increasingly more important because they enable miniaturization, improve signal integrity and can reduce costs.

In many ways, embedded resistors are new applications of mature technologies. Modern buried resistors originated with planar resistive materials introduced in the 1970s as a response to tightening substrate and component requirements for microelectronics that were about to exceed the limits of through-hole technology. The resistive materials were nickel alloys, primarily nickel-phosphorous, deposited on copper foil and laminated to epoxy substrates. This was the time when photolithography was beginning to replace silk screen technology for primary imaging of printed circuitry and enabled the subtractive processes (print and etch) used for thin-film resistors.

Early applications were potentiometer circuits, fuses, isolation resistors for burn-in boards and hybrid circuits. These were surface resistors, sometimes trimmed to a nominal resistance value, and always protected by solder mask or conformal coatings. Planar resistors on organic substrates became a low cost alternative to screen-on and fired resistor pastes on ceramic substrates.

Planar resistor technology use was limited during the 1980s because of the introduction of SMT. SMT components replaced through-hole components for high performance applications. The SMT chip resistor and capacitor would become the dominant passive component technology, however, planar resistor use would continue in certain high speed, high density and high reliability applications. Emitter-coupled-logic (ECL) logic and speeds in excess of 100 MHz required terminating resistors. Pull-up/pull-down serpentine resistors also came into use. Thin-film planar resistors were also used in RF applications, primarily as power dividers on PTFE substrates, and currently remain the technology of choice for space applications.

During the 1990s the introduction of array packaging and the need to terminate signals within the footprint of the

array, spurred the growth of buried resistors. Densities in excess of 15 Input-outputs (I/Os) per square centimeter and 150 cm/square cm of wiring required advanced technologies. High density interconnect (HDI) or embedded passives became necessary. Although thought of as enabling technologies, these are alternative technologies. Printed board designers can use either blind microvias and 0201 chip components or buried vias and embedded resistors; however, when compared to the cost of sequentially built printed boards, embedded resistors in conventional printed boards were the low cost alternative.

High power densities, often in excess of 100 watts per square inch, meant that the resistor percent tolerance drove the minimum resistor element size. Historically, sheet resistivities ranged from 25 to 100 $\Omega/\square$ with material tolerances of $\pm 5\%$ and final tolerances, untrimmed, of ten to fifteen percent. Because of low series inductance and the lack of inductive reactance, buried planar resistors of $\pm 15\%$ tolerance provided better impedance matching (less signal discontinuities) than SMT resistors of a one percent tolerance.

By the year 2000, there were several thin-film resistive materials on the market, all based on nickel alloys with a wide span of sheet resistivities. Conventional wisdom expressed in technical roadmaps held that high sheet resistivities would be necessary to embed high valued resistors and sheet resistivities of some thin-film products reached 1000 $\Omega/\square$. However, miniaturization and BGA packaging decreased the channel widths between pads and vias. Decreasing widths meant higher aspect ratios (length versus width) and, therefore, lower sheet resistivities. As a result, built-in-trace resistors using ten $\Omega/\square$ materials were introduced.

Enabling technologies were also improved. These included design and layout tools, electrical test and trim equipment. The most significant improvement in the last twenty years was the evolution of design and test software. In regards to CAD/CAM layout tools, the primary issue is additive versus subtractive technology and not thin film versus thick film. Embedded resistor designs for additive processes more closely resemble SMT substrate patterns and procedures. Subtractive technology reverses the process procedure with the first print determining the resistor width and the second print the length. During the 1980s and most of the 1990s, existing layout tools were used with difficulty and CAD/CAM operators required special training.

For embedded resistors, manual design was required. Resistors were assigned referenced designators and component libraries created. However, CAD generated net lists contained no information about the embedded resistors. Full logic and design rule checking could be done but with some difficulty. More often than not, the problem was passed down to the board shop. Manual designs were similar to “clip art,” meaning that there was no standard

associated with the graphic image. Gerber data was provided to make the phototools but there was no data to drive the electrical test machines needed to test the resistors for ohmic value. Automatic design rules check was not available. CAM operators at the printed shops had to create their own netlists by merging a CAD netlist with a secondary resistor file or the bill of materials. In 1997, IPC introduced a revised data format to support embedded passives, IPC-D-356A. The document was considered ahead of its time as few design bureaus and printed board shops had the necessary software to use the new format.

Improvements in AOI technology allowed visual inspection of planar resistors but did not provide ohmic values. Existing electrical test machines could be used for testing embedded resistors with software upgrades, however, electrical testing of innerlayers was a problem. Fixed grid bed-of-nails testers required large fixtures. Flying probe testers were preferred but were too slow. It wasn't until the test speeds exceeded 100 resistors per minute that flying probe testers became viable for production.

To facilitate design, spreadsheet programs had been in use since the early 1990s. These were off-line programs that used simple algorithms based on power density constants and etch factors to output the resistor element size based on tolerance and power rating of the resistor. This method is called "parametric design."

In 2002, automated layout tools were introduced that used parametric design to create resistor elements in real time. Components libraries were not used. Instead, resistors were recreated at each location by the layout tool. ODB++ files used at preproduction CAM stations enabled design rule checking. Since 2000, the paradigm of the SMT chip resistor has gradually been abandoned and the true potential of the unlimited variety planar resistor designs has become recognized by the printed board designers.

3.1.4 History of Distributed Planar Capacitor Technology Embedded distributed (planar) capacitance is a rather simple concept. It involves using closely spaced power and ground planes as a parallel plate capacitor for power supply decoupling. Closely spaced power and ground planes provide significant capacitance and have very low inductance, ideal for power supply decoupling. This embedded distributed capacitance (EDC) can also be used to replace discrete power supply decoupling capacitors from the board surface. This is especially important at frequencies above a few hundred megahertz where the high inductance of surface mounted capacitors limits their effectiveness. Further, the closely spaced planes provide very effective dampening of high-frequency noise on the planes.

EDC as a concept has been around since the 1920s. The earliest known record of EDC can be found in a 1926 patent application for a radio apparatus in which EDC was used in a power distribution strip [4]. The earliest known

record of EDC in a multilayer printed circuit board can be found in a 1966 patent filing (with a continuation in part filed in 1969) [5]. In this patent, two power-ground layers of embedded distributed capacitance were shown. Each embedded distributed capacitance layer utilized 62.5 μm [0.0025 in] thick copper and 62.5 μm [0.0025 in] thick epoxy - glass as the dielectric.

Some OEMs (including high end workstation and super-computer manufacturers) designed thin FR-4 power-ground cores for embedded distributed capacitance into their multilayer printed boards in the 1970s and 1980s. However, these applications were typically for specific programs and were generally not high volume. One of the first known extremely large application of using EDC in multilayer boards was done in the mid-to-late 1980s by Mupac [6,7]. Mupac shipped millions of dollars worth of wire wrap boards prior to 1989. In 1989, Zycon filed the first of its patents on EDC [8]. These may be some of the better known patents regarding EDC but as can be seen above, they were not the first. Throughout the 1990s, the use of thin FR-4 materials for power-ground cores increased dramatically. Since 2000, the use of thin FR-4 has become common for high speed, digital multilayer boards.

Operating voltages have continued to decrease and operating speeds have continued to increase. Because of this, there was a need for a lower impedance power distribution than thin FR-4 could provide. Additionally, space constrained designs needed materials with a higher capacitance density than thin FR-4 could provide so that a significant numbers of surface mount decoupling capacitors could be removed from the board surface. Work on higher performance embedded distributed capacitance materials (25 μm [0.001 in] or less in thickness), including some filled with high dielectric constant ceramic fillers (such as barium titanate), began in the mid-1990s by companies such as 3M, DuPont and others. The development of some of these high performance materials was facilitated by two industry consortia [9,10]. The details of the work completed in these two industry consortia are summarized in their final project reports, which are available to the public. By 2004, a number of high performance materials, with a dielectric thickness of 25 μm [0.001 in] or less (both with and without ceramic fillers) had been commercialized. Most of these materials were being qualified and/or used in high volume applications by 2005.

3.1.5 History of Polymer Thick-Film Capacitor Technology PTF technology has been available for fabricating discrete embedded capacitors for a number of years. Screen printing techniques have been used to apply PTF dielectrics to etched copper electrodes followed by screen printing a conductive PTF material to form the second electrode. Although materials and techniques have been available, the application of this technology has been limited. Development work is currently underway in a number of areas.

science laboratories. New products are expected to reach the commercial market place in 2007.

3.1.6 History of Ceramic Thick-Film and Thin-Film Capacitor Technology Formed-on-foil ceramic capacitors may embrace a broad range of technologies and materials but a common feature is a first step wherein a ceramic dielectric layer is processed on copper foil. This approach requires relatively high processing temperatures ($>500\text{ }^{\circ}\text{C}$ [$>932\text{ }^{\circ}\text{F}$]) or other processes detrimental to the organic printed board. The ceramic layer may completely cover the copper foil or it may be applied only in selective areas. The ceramic layer may be formed from a thin-film process to yield a dielectric film thickness of less than $1\text{ }\mu\text{m}$ [0.00004 in] or a thick-film process that can be used to form a thicker dielectric layer of between 5 and $20\text{ }\mu\text{m}$ [0.0002 and 0.00079 in]. Dielectric layers that cover the entire area of the foil are typically made with thin-film processes and are supplied as a dielectric layer sandwiched between two copper foils, one of which may or may not be laminated to prepreg. Defining the capacitors requires etching of one or both of the copper foils and may also require an etching step to remove dielectric. Thick-film capacitor approaches typically will be supplied as a paste allowing the printed board fabricator to make their own formed-on-foil capacitor design using selective deposition of the dielectric and electrode paste using screen printing. After capacitors have been formed on the foil, the foil is laminated to prepreg and then standard printed board fabrication processes are utilized to embed the capacitors inside the printed board. Table 3-1 provides some common material properties of both thick and thin-film ceramic capacitor technology.

3.1.7 History of Ceramic Filled Photodielectric Capacitor Technology Ceramic-Filled Photodielectrics (CFP) were commercialized in 2002. These materials enabled creation of a capacitor structure near the outer-layers of the printed board known as the “mezzanine”, which somewhat describes the structure. The evolution of this development is described in [11]. The target of the development effort was to create a material that would provide a capacitance density of 10 to 30 pF/mm^2 and that would be compatible with standard printed board manufacturing processes. The

processes are in production as of the publication of this document and technology licenses are available to printed board manufacturers. Mezzanine capacitors are also used in conjunction with PTF embedded resistor technology, providing both resistors and discrete capacitors in the same board.

3.2 Embedded Passive Component Selection Criteria

The first decision that must be made is whether or not to use a discrete or embedded solution. Depending on the application, cost, performance, or some other metric may be the driving force for the decision. Several materials properties must be considered when making the decision of whether or not to embed a particular component in a circuit:

- Available tolerance of the embedded parts.
- Drift limits following thermal shock or humidity exposure.
- Aging behavior.
- Temperature coefficients of capacitance or resistance (TCC/TCR).
- Power handling capacity (may include geometry of part).
- Breakdown field and leakage currents.
- Q – especially important for RF and filter applications.

Additional concerns must include:

- Parts need for circuit tuning (which would be difficult with embedded components, if the circuit needs to be tuned after complete build).
- Special requirements for some parts (e.g., low noise metal film resistors).
- Available space for embedded parts, especially large caps.
- Density of embedded parts – the cost effectiveness of embedding components may be maximized at some intermediate component density.

Figure 3-1 shows the embedded passive selection process with cost as a driver. The passive component bill of materials (BOM) is first limited by the component values and tolerances versus the available embedded passive technologies. Second, critical components, such as those required for circuit tuning, high Q, or low noise, are screened out.

Table 3-1 Common Thick and Thin-Film Ceramic Technologies

Approach	Product	Deposition Process	Dielectric Material	Dk	Thickness (microns)	Capacitance Density (nF/cm ²)
Thick Film	Paste	Screen Printing	BT*/glass	3000	10 to 20	130 to 270 per layer
Thin Film	Laminate	Solution Deposition	BT/BST** PLZT***	200 to 3000	0.5 to 1.0	200 to 4400
		Sputter	BST	200 to 1000	0.5 to 0.8	200 to 1700
		Modified CVD	Alumina	9	0.1	80
		Anodization	Tantalum pentoxide	50	0.02 to 0.1	440 to 2200

* Barium titanate ** Barium strontium titanate *** Lead zirconate titanate

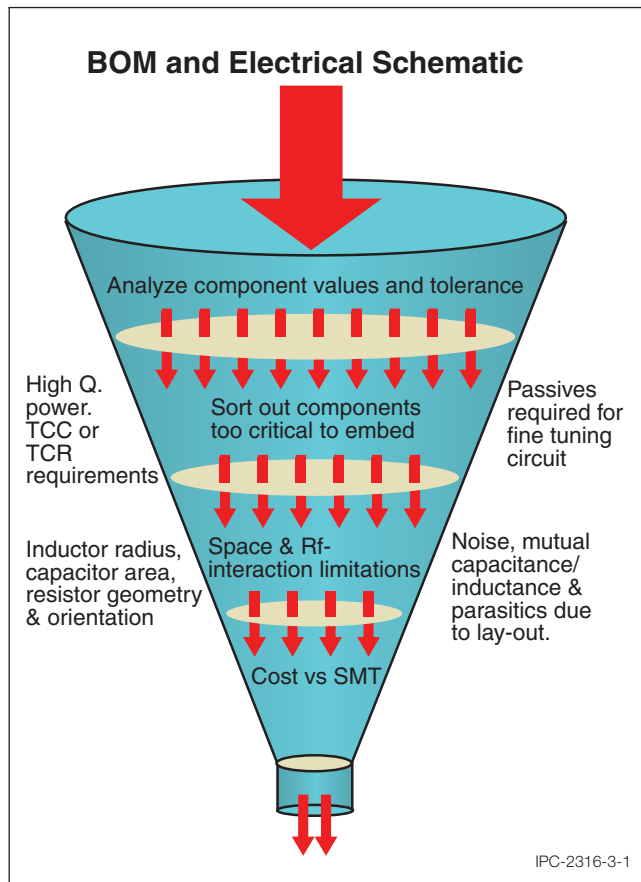


Figure 3-1 Embedded Passive Selection Process with Cost as a Driver

Third, space concerns are examined to be sure all of the embedded parts will fit in the required geometry, choosing a combination of parts that fit both physically and logically. Finally, cost must be considered, as it is the driver in this example. If the resulting cost analysis is lower for the embedded solution as compared to the surface mount alternative, then the process continues.

The above arguments only determine whether or not a set of components should be embedded. Perhaps the more difficult question to answer is “Which embedding type will be used, whether a true embedded passive, an integrated passive device, or another type of device?” Table 3-2 compares and contrasts the various device types by criteria such as cost, size, performance, and reliability. The selection of the appropriate embedded component type is just as critical, or more so, than the selection of the components to embed.

3.3 Cost Analysis Economics encompasses an assessment of the total life cycle cost of a design decision where the life cycle includes the circuit and fabrication process, design, manufacturing, testing, marketing, sustainability, and end-of-life of the product. The decision to convert a design using discrete passives to a design using embedded passives has more ramifications than reducing the cost of part procurement and paying more for the board. In addition,

there is a host of other cost and benefit issues to be considered that translate into life cycle costs at some level.

It is not clear under what conditions applications fabricated using embedded passives will be able to compete economically with discrete passive technology. On the bright side, the use of embedded passives reduces assembly costs, shrinks the required board size, and negates the cost of purchasing and handling the discrete passive components that are replaced. However, these economic advantages must be traded off against the higher cost (per unit area) of boards fabricated with embedded passives (a situation that will not disappear over time) and possible decreases in throughput and yield of the board fabrication process.

The application-specific costs depend on many effects when embedded passives are present in a printed board:

- Decreased printed board area due to a reduction in the number of discrete passive components.
- Decreased wiring density requirements due to the integration of resistors and bypass capacitors into the printed board.
- Increased wiring density requirements due to the decreased size of the printed board.
- Increased number of printed boards fabricated on a panel due to decreased board size.
- Increased printed board cost per unit area.
- Decreased printed board yield.
- Decreased printed board fabrication throughput.
- Decreased assembly costs.
- Increased overall assembly yield.
- Decreased assembly-level rework.

Several other recurring system costs may also be affected by the use of embedded passives, for example: the need to electromagnetically shield the board may be reduced or eliminated when certain passives are embedded (saving on expensive materials and their assembly), and the costs associated with thermal management of the board may also be affected.

Due to the conflicting nature of many of the effects listed above, the overall economic impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. In fact the very nature of tradeoff analysis is one in which *the greater the detail necessary to accurately model a system, the less general and more application-specific is the result.*

3.3.1 Fabrication and Manufacturing Cost Modeling

The most common approach to economic analysis of embedded passives is to:

- 1) Reduce the system cost by the purchase price and conversion costs* associated with the replaced discrete passives,

Table 3-2 Passive Component Selection Criteria

	Discretes	Arrays and Networks	Integrated Passive Devices (IPD)	Embedded Passives
Definition	A single passive element (capacitor, resistor or inductor) in a leaded or surface-mount case.	Passive arrays combine multiple passive elements of like function (i.e., all capacitors or all resistors) in a single surface-mount case. Networks combine passives of more than one function (e.g., capacitors + resistors) in a single surface-mount case. A network typically contains 4 to 12 elements.	Multiple passive elements of more than one function and possibly a few active elements (e.g., resistors + capacitors + diodes) in a single surface-mount or CSP. Typically, an IPD contains more than 20 elements. IPDs may also be referred to as "super components."	Passive devices that are buried in the substrate material (rather than being mounted on top).
Cost	Good—The benchmark for all other technologies.	Better when local densities have four or eight devices close together.	Better when high local densities are application specific.	Better when average component density is above three devices/cm ² . Cost is panel size dependent.
Size	Good—Board area required for each and every device.	Better—50% and greater board area savings over discretes.	Better—Application specific IPDs can replace dozens of components.	Best—No surface board area required because the devices are buried.
Performance	Good—Self-resonates at low frequencies.	Good—Self-resonates at low frequencies.	Better—Qualified out to several gigahertz (GHz).	Best—Ideal components; when buried underneath the integrated circuit (IC), it serves due mainly to decreased lead length and avoidance of the inductance of the connection loops.
Reliability	Good—Heavy use of solder joints.	Better—Reduces solder joints slightly.	Better—Significantly reduced solder joints.	Best—Elimination of solder joints.
Flexibility	Best—Most flexible for both design and manufacturing.	Better than IPDs and embedded passives.	Better than embedded passives.	Good—Requires modeling and simulation.
Time to Market	Best—Flexibility allows quick turns.	Better—Simple quad and octal arrays can be designed in quickly.	Good—IPDs require additional design iterations for wireability.	Fair—Most board shops require at least five to seven days to build an embedded passives board.
Availability	Best—Highly available from multiple sources.	Better—Standard parts from multiple suppliers.	Better—Nonstandard parts from multiple suppliers.	Fair—Few suppliers.
Values	Best—All values available at commodity prices.	Better—Thick film arrays offer high values.	Good—Thin-films have limited capacitor values.	Good—Currently limited to low values.
Tolerances	Best—Tight tolerances available at commodity prices.	Better—Both offer tight tolerances.	Better—Thin-films offer tight tolerances.	Good—Loose tolerance (5 - 10%).

- 2) reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the panel, and
- 3) determine the new board cost based on a higher per unit area cost for the embedded passive panel fabrication and the new number-up computed in step 2.

*Conversion costs are the handling, storage and assembly costs associated with a discrete component.

The results of these three steps determine the new system cost [12,13,14,15,16,17,18]. A representative modeling process that demonstrates the effects that must be considered is given by the following:

- 1) Accumulate the area of the footprints of discrete passives to be embedded.

- 2) Reduce printed board area by the accumulated discrete passive area from step 1, maintaining the aspect ratio of the original printed board. This step is optional, i.e., the printed board area may be fixed.

- 3) Plated or Printed Resistors: Determine the area occupied by each plated or printed embedded resistor on wiring layers. Perform routing analysis, removing nets and vias associated with resistors that are embedded and accounting for area blocked by embedded resistors on wiring layers. Routing is assumed to be unaffected by discrete resistors embedded using subtractive thin-film materials or similar dedicated layer addition approaches. All nets and vias associated with embedded bypass capacitors are removed from the routing problem, and it is expected that embedded singular

affect routing analysis. Using these assumptions, determine the relative change in routing resources due to embedding selected passives.

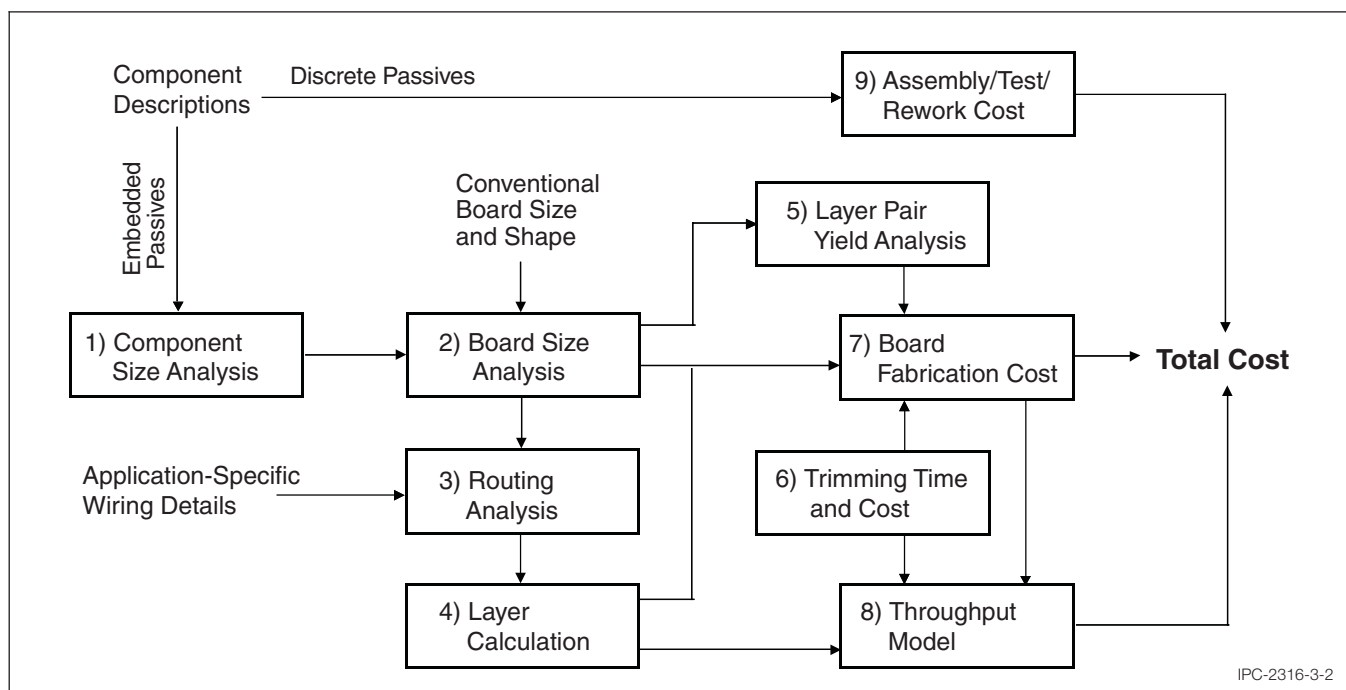
- 4) Compute the number of required layer pairs for the embedded passive implementation using the layer requirements, the relative routing requirements for the embedded substrate and either a fixed measure of the routing efficiency associated with the conventional board or a range of possible efficiencies determined under the assumption that the conventional version of the board did not include any more layer pairs than it needed to route the problem.
- 5) Determine the yield of layer pairs that include embedded passives.
- 6) Determine the trimming cost for embedded resistors. The necessity of trimming is determined by the resistor's tolerance. The application-specific cost per trim is determined by modeling the throughput of a laser trimming process [19].
- 7) Compute the number of printed boards per panel from the board size (number-up) and the effective panel fabrication costs from the layer and material requirements, yields, and resistor trimming costs.
- 8) Determine the relative printed board fabrication profit margin from layer pair throughput modeling. A profit margin model based on throughput is provided in [18], and throughput is modeled in [20].
- 9) Accumulate assembly cost, test, rework, and printed board fabrication costs (with profit margin) to obtain total relative cost.

The analysis in Figure 3-2 focuses on differences in system cost between embedded passive and discrete passive solutions; therefore all cost elements that are approximately equivalent for the embedded and conventional system are effectively ignored, e.g., all functional testing of the system and, procurement and assembly costs associated with non-embeddable parts.

3.3.2 Embedded Resistor Trimming and Rework Economics A key part of the tradeoff analysis is determining under what conditions (application properties and resistor fabrication process) it is economically feasible to perform trimming and possibly rework versus disposal of layer pairs or printed boards that do not meet design specifications.

When resistors are fabricated, their resulting resistance values form a distribution. If the required tolerance is tighter than the as formed distribution, a method of trimming and rework must be chosen.

If the resistors are to be laser trimmed, the fabrication target resistance (peak of the distribution) is below the application target resistance (see Figure 3-3) so that the greatest number of fabricated resistors can be trimmed to values in the specified range. The High Specification Limit (HSL) and the Low Specification Limit (LSL) are determined from the design tolerance associated with the resistor. The area under the curve between the HSL and the LSL represents the yield of the untrimmed resistor. There is a lower limit to the ability to successfully trim a resistor which is approximately 55% of the application target. The area



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Figure 3-2 Embedded Passive Board Cost Tradeoff Model