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2012 - January

Specification for
Immersion Tin Plating for
Printed Circuit Boards

Supersedes IPC-4554
January 2007

A standard developed by IPC

Association Connecting Electronics Industries



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IPC-4554 with Amendment 1

Specification for Immersion Tin Plating for Printed Circuit Boards

Developed by the Plating Processes Subcommittee (4-14) of the
Fabrication Processes Committee (4-10) of IPC

Supersedes:

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Users of this publication are encouraged to participate in the
development of future revisions.

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Specification for Immersion Tin Plating for Printed Circuit Boards

1 SCOPE

This specification sets the requirements for the use of Immersion Tin (ISn) as a surface finish for printed circuit boards. It is intended for use by supplier, manufacturer, contract manufacturer (CM) and original equipment manufacturer (OEM).

1.1 Description ISn is a metallic finish deposited by a chemical displacement reaction that is applied directly over the basis metal of the PCB, that is, copper. ISn is primarily used as a solderable surface. It has been used in press fit connections and as the interface for Zero Insertion Force (ZIF) edge connectors.

The ISn protects the underlying copper from oxidation over its intended shelf life. Copper and tin however have a strong affinity for one another. The diffusion of one species into the other will occur inevitably, directly impacting the shelf life of the deposit and the performance of the finish.

Various ISn formulations designed specifically for use as surface finishes for PCBs utilize various methods of retarding the diffusion process, including the use of co-deposition of organics, the use of another metal as a diffusion barrier or the use of grain structure refining. It is recommended that the user of the deposit clearly understand the different methods of copper migration retardation and that the supplier know the positive and negative impacts of the system chosen.

1.2 Objective This specification sets the requirements specific to ISn as a surface finish. As other finishes require specifications, they will be addressed by the IPC Plating Processes Subcommittee as part of the IPC-4550 specification family. As this and other applicable specifications are under continuous review, the Subcommittee will add appropriate amendments and make necessary revisions to these documents.

1.3 Performance Functions

1.3.1 Solderability The primary function of ISn is to provide a solderable surface finish, suitable for all surface mount and through-hole assembly applications and with an appropriate shelf life. The deposit has demonstrated the ability to meet a Category 3 durability per J-STD-003 when produced per this specification's requirement.

Due to the diffusion of the copper through the tin deposit and its impact on solderability, the ability to meet the greater than six months shelf life is DIRECTLY related to

the deposit thickness. This diffusion also has a negative impact on the correct thickness measurement of the deposit.

The ability to measure and differentiate the tin species in the deposit is imperative to ensure the manufacture and receipt of parts with this useable shelf life. The use of correct XRF standards is imperative. The use of foils over polyester (Mylar® is very common) prevents the impact of basis metal diffusion and should be the XRF "standards of choice" - see Appendix 4 for detailed recommendations.

1.3.2 Contact Surface Immersion tin is not recommended as a finish for soft membrane switch applications.

1.3.3 Electromagnetic Interference (EMI) Shielding A key characteristic for this application is a consistent metal interface between the PCB and the shield material. Due to the dynamic nature of the ISn deposit and the basis metal (Cu) of the PCB, the interface between the EMI shield and the deposit is NOT consistent. The growth of intermetallic compounds (IMCs) will change the electrical characteristics of the interface between the EMI shield and the deposit. It has however been demonstrated to be a suitable interface for EMI shielding for certain specific applications. Testing for suitability is recommended.

1.3.4 Connectors

1.3.4.1 Press-Fit The use of ISn as a deposit suitable for press-fit requirements **shall** meet Telcordia GR-1217-CORE. It should be noted that changing to a thin immersion deposit such as ISn from HASL may require a re-evaluation of the pre-fabrication hole sizes to ensure the correct interference fit required for press-fit applications.

The possibility of tin whisker formation, as a direct consequence of stresses induced on the deposit as a function of press-fit insertion, exists. The end user **shall** determine the impact of whisker formation on the reliability of the module in its end use application.

1.3.4.2 Edge Tab The use of ISn as a surface finish for edge connectors utilizing a zero insertion force (ZIF) connector, i.e., for memory modules, has been successfully demonstrated.

Whisker formation is a concern particularly in fine pitch devices. The end user **shall** determine the impact of whisker formation on the reliability of the module in its end use application.



1.3.5 Wire Bonding ISn is not suitable as a surface finish for either aluminum or gold wire bonding due to the instability and metallurgical incompatibility of the deposit.

1.4 Definition of Terms The definition of all terms used within this specification **shall** be as specified in IPC-T-50 and as defined below:

Solvent Extract Conductivity (SEC) Surface ionic contaminants may be extracted/dissolved by solvents. The bulk ionic cleanliness of an item is then quantified by measuring the solution of extracted contaminants with an ionograph instrument and reported in units of micrograms of sodium chloride equivalent per unit surface area of the tested item.

Useable Tin Tin that has not reacted to form intermetallic compounds.

X-ray Fluorescence (XRF) or Energy Dispersive X-ray Fluorescence (EDS-XRF) Nondestructive chemical analysis techniques that use an X-ray beam aimed at an object's surface. The incident beam causes secondary (fluorescent) X-rays to be generated. These fluorescent X-rays are then measured to determine the identity of metal or other high density elements and their quantity (thickness) present.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

J-STD-003 Solderability Tests for Printed Boards

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-2221 Generic Standard on Printed Board Design

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6013 Qualification and Performance Specification for Flexible Printed Boards

IPC-6018 Microwave End Product Board Inspection and Test

IPC-TM-650 Test Method Manual²

2.3.25 Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract (ROSE)

2.4.1 Adhesion, Tape Testing

2.6.14.1 Electrochemical Migration Resistance Test

2.6.3.5 Bare Board Cleanliness by Surface Insulation Resistance.

2.2 Telcordia^{TM3}

GR-1217-CORE Generic Requirements For Separable Electrical Connectors Used In Telecommunications Hardware

3 REQUIREMENTS

3.1 Visual ISn surfaces **shall** be inspected in accordance with the visual examination sections of the IPC-6011 series, and specifically IPC-6012 which specifies three diopters (a nominal magnification of 1.75X). If confirmation of a suspected defect cannot be made at three diopters, it should be verified at progressively higher magnifications (up to 40X) to confirm that it is a defect. The coverage **shall** be complete and the finish **shall** be uniform on the surface to be plated (see Figures 3-1 and 3-2 for uniform coverage and Figure 3-3 for improper coverage, as visually identified with ISn-plated surfaces).

ISn appearance, like all thin immersion deposits, is directly influenced by the surface preparation of the underlying copper. Depending on the micro-etch chemistry used, the color of the deposit will vary from a white matte appearance to a shiny silver appearance. All colors are acceptable provided that the appearance is uniform through-out the product supplied. The coverage **shall** be complete and the finish **shall** be uniform on the surface to be plated. There **shall** be no extraneous plating, skip plating, edge pull back, dark or discolored pads or mis-registered solder mask on the plated surface for all classes of product.

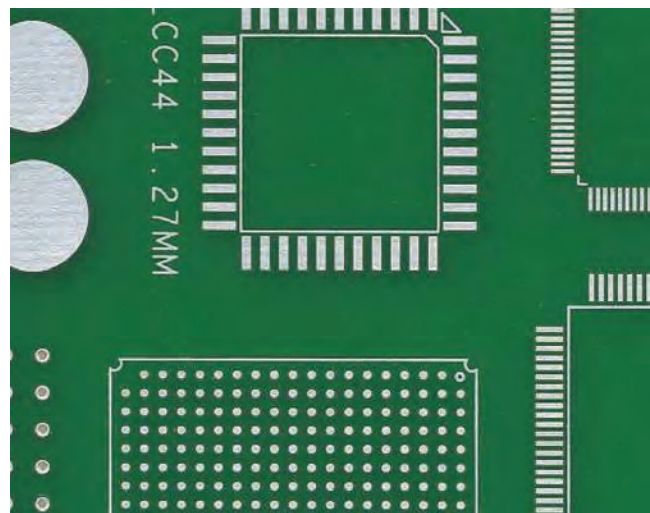


Figure 3-1 Example of Uniform Plating

3.2 Finish Thickness Thickness of the ISn **shall** be measured and verified following the ISn plating step in the PCB fabrication process. The use of X-ray fluorescence methodology for thickness determination **shall** be in accordance with Appendix 4 of this document and **shall** employ

1. www.ipc.org

2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/html/testmethods.htm).

3. www.telcordia.com

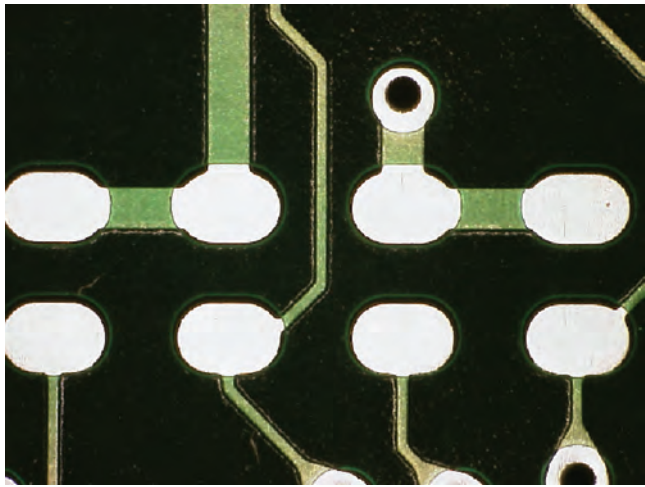


Figure 3-2 Example of Uniform Plating

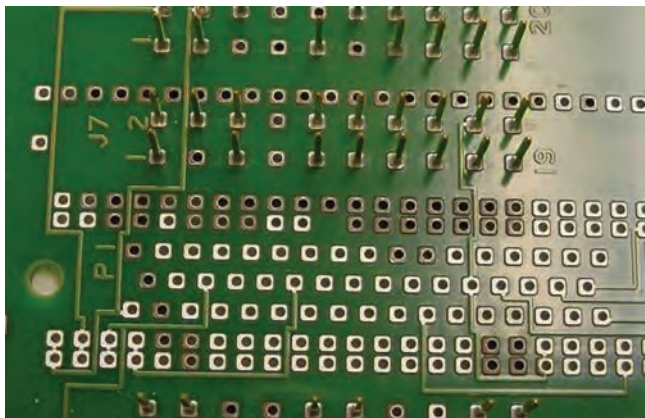


Figure 3-3 Example of Improper ISn Deposit Showing Inconsistent Plating

X-ray fluorescence (XRF) instrumentation equipped with software and hardware specific for ISn measurement. Due to the dynamic nature of the deposit and its interaction with the basis metal, a clear distinction between “useable” tin and total deposit thickness needs to be made. It is recommended that the use of coulometric stripping or similar techniques, e.g., Auger or XPS, be employed at a minimum during qualification and at a regular interval for confirmation as agreed between user and supplier (AABUS). See Appendix 5 of this document regarding the use of coulometric stripping and other accepted techniques.

3.2.1 Immersion Tin Thickness The growth of copper-tin intermetallic compounds (copper-tin IMCs) consume the useable tin in the deposit. Their growth is time- and temperature-dependent. Thermal excursions in assembly advance the growth of the IMCs, thus further consuming the useable tin. If insufficient useable tin is available to survive all thermal process steps in assembly, solderability issues may result, dependent on the flux activation levels used.

In order to insure sufficient useable tin, the minimum ISn deposit thickness **shall** be 1 micron (40 micro inches) at -4 sigma from the process mean when measured on a pad of

1.5 mm X 1.5 mm [0.060 in X 0.060 in] or equivalent area of 2.25 mm² [3.600 E-3 in²] and where the typical values range from 1.15 µm to 1.3 µm. While ISn deposit rates may not be as susceptible to pad geometry/feature size as compared to other immersion metallic finishes, the use of a recommended pad size is to ensure accurate XRF measurement by forcing the 30% rule for collimator size relative to feature size (Appendix 4). Excessively thick deposits, while not impacting solderability, may impact other board fabrication processes negatively, e.g., solder mask and legend adhesion. This minimum deposit thickness is to ensure greater than six months of shelf life (Category 3) and to meet the acceptance criteria of IPC/EIA J-STD-003.

There is sufficient data, both test and anecdotal, to show that ISn deposits below the 1 micron minimum work provided there is either a) sufficient useable tin to meet the assembly processing requirements including expected shelf life or b) the PCBs are consumed in a very short period of time, i.e., below 30 days from manufacturing. The supplier of the ISn-coated PCBs has the option of supplying either to the 1 micron minimum specification OR providing data, via coulometric stripping or Auger, that there is sufficient useable tin in the deposit.

Coating durability categories are defined as follows (per the IPC/EIA J-STD-003). The following categories are **guidelines** for determining the needed coating durability – **These are not product performance classes.**

Category 1 – Minimum Coating Durability

Intended for boards which will be soldered within 30 days from the time of PCB fabrication and will experience minimum-to-moderate thermal exposures. A deposit that contains a minimum **useable tin** of 0.4 microns is recommended.

Category 2 – Average Coating Durability

Intended for boards likely to experience up to 180 days storage from the time of PCB fabrication and will experience minimum-to-moderate thermal exposures. A deposit that contains a minimum **useable tin** of 0.5 microns is recommended.

Category 3 – Maximum Coating Durability

Intended for boards likely to experience long storage (greater than six months) from the time of PCB fabrication and/or severe thermal or solder processing steps. A deposit that contains a minimum **useable tin** of 0.6 microns is recommended. It should be noted that, while the storage duration is specified greater than six months, it is not implied to be solderable forever and that some common sense be used if excessive long term storage has been applied to the PCBs (see Appendix 8).

Note: Coating durability levels other than “Category 3” may be specified AABUS.

3.3 Porosity Porosity testing of ISn is not applicable.

3.4 Adhesion The purpose of adhesion testing for ISn finished boards is two fold. The first is for testing the plating adhesion of the immersion Sn to the underlying copper. The second is for testing the adhesion of the solder mask to both traces and laminate after exposure to the ISn process. In both cases testing should be conducted on regions of high density on the board such as BGA sites, dams between fine pitch leaded devices or over areas of high trace density. The tape testing will be in accordance with IPC-TM-650, Method 2.4.1, using a strip of pressure sensitive tape. There **shall** be no evidence of any portion of the surface finish or the soldermask being removed, as shown by particles of plating/pattern or soldermask adhering to the tape. If tested immediately after ISn plating, there exists the possibility for some mask lifting. If there is mask lifting but no evidence of ISn lifting, it is recommended to allow the product to normalize for four to six hours and repeat the test. If mask lifting is still evident then the parts **shall** be rejected.

If overhanging metal (slivers) or soldermask undercut breaks off and adheres to the tape, it is evidence of overhang or slivers, but not of adhesion failures.

Because of the requirement to test in high density areas, the potential to leave tape residue that could interfere with soldering exists, especially if the wrong type of tape is used. Verification of zero impact to solderability must be demonstrated for the areas tested.

3.5 Solderability This thickness specification contained herein **shall** meet the coating durability requirements of Category 3 in IPC/EIA J-STD-003, i.e., intended for boards likely to experience long storage (e.g. greater than six months). Caution needs to be exercised pertaining to the storage and packing of the ISn boards to ensure that the growth of copper-tin IMC's and surface oxides are minimized and will thus meet the Category 3 requirements. Exposure to high storage temperatures will accelerate the formation rate of copper tin intermetallics. Storage in a high humidity environment with the PCBs removed from their original packaging may increase the oxide thickness and/or species and likewise have a detrimental effect on solderability. Recommended storage conditions should not exceed 25 °C [77.0 °F] and a humidity range of 30 to 70% R.H. Such storage conditions are stated in J-STD-003 as providing a one year coating durability for Class 3 applications.

• Solderability testing using Eutectic SnPb solder **shall** use the Standard Test Flux # 1 as per the IPC/EIA J-STD-003 for four Tests: A, B, C and D with exceptions noted for Tests E and F, below.

- 1) Test A - Edge Dip Test.
- 2) Test B - Rotary Dip Test.
- 3) Test C - Solder Float Test

4) Test D - Wave Solder Test (This Test D may also use a production flux, AABUS.)

5) Test E - Surface Mount Simulation Test will need to use a flux AABUS, because the Standard Test Flux # 1 is not available in a solder paste form.

6) Test F - Wetting Balance Test **shall** only use the Standard Test Flux # 2.

• Solderability testing using Lead Free SAC305 solder **shall** use the Standard Test Flux # 2 as per the IPC/EIA J-STD-003 for five Tests: A1, B1, C1, D1 and F1 with exception noted for Test E1, below.

- 1) Test A1 - Edge Dip Test.
- 2) Test B1 - Rotary Dip Test.
- 3) Test C1 - Solder Float Test
- 4) Test D1 - Wave Solder Test (This Test D1 may also use a production flux, AABUS.)
- 5) Test E1 - Surface Mount Simulation Test will need to use a flux AABUS, because the Standard Test Flux # 2 is not available in a solder paste form.
- 6) Test F1 - Wetting Balance Test

Note #1: The use of steam conditioning is not an applicable accelerated stress method for ISn. The use of 72°C [162 °F] / 85% R.H. for eight hours is the recommended stress condition for this deposit. (See Figure 3-4 for surface mount solderability test coupon.)

Note #2: Baking of boards to remove moisture following the recommendations of IPC-1601 **shall** require the use of the Standard Test Flux # 2 when testing with Eutectic SnPb solder where the default flux had previously been Standard Test Flux # 1.

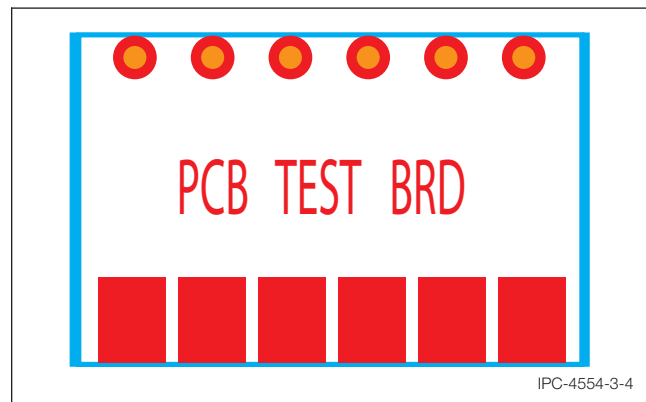


Figure 3-4 Coupon for Surface Mount Solderability Testing

3.5.1 Solder Spread Test The use of a spread test for verifying solderability of ISn using a solder paste has been used since the reintroduction of this deposit as a solderable surface. The committee has evaluated extensively the use of this test method and the results obtained and have deemed it to be an acceptable method for verifying the solderability of the deposit as a function of coating angle.

achieved. The test protocol used by the committee can be found in Appendix 7 along with the coupon design as seen in Appendix 8, Figure A8-6. Results from a series of round robin tests may also be found in Appendix 8.

3.6 Cleanliness The nature of the ISn chemical process and/or board design features may lead to excessive entrapment of process chemistry. This, in turn, may require special post-tin application rinsing/cleaning in order for the deposit to meet current industry requirements for both SEC and SIR testing. The process **shall** be installed and maintained using IPC-TM-650, Method 2.3.25 “Detection and Measurement of Ionizable Surface Contaminants by Resistance of Solvent Extract” and Method 2.6.3.5 “Bare Board

Cleanliness by Surface Insulation Resistance.” The SEC results **shall** meet the values given in IPC-6010 series that requires $1.56 \mu\text{g}/\text{cm}^2$ NaCl equivalent. The SIR results will be as specified in Table 3-1. Failure to meet this cleanliness specification should trigger immediate corrective action.

Note: Good SIR values do not necessarily equate to good SEC values due to the absorption of the contaminants into the board materials. The use of both techniques is recommended until a sufficiently large data base exists to demonstrate process control for cleanliness.

3.6.1 Electrolytic Corrosion The ISn process both contains and produces by-products from the reaction that may be detrimental to long term module reliability as a function

Table 3-1 Requirements of Immersion Tin Plating

Tests	Test Method	Requirement Paragraph	Class 1	Class 2	Class 3
General:					
Visual	Visual	3.1	Uniform plating and complete coverage of surface to be plated.		
Immersion Tin Thickness (as plated)	Appendix 4	3.2.1	1 μm (40 μin) minimum at -4 sigma from the process mean as measured on a pad of 2.25 mm ² [3.600 E-3 in ²]; typical values of 1.15 to 1.3 μm for Coating Durability Category 3. Note: Less than 1 μm may be used for Coating Durability Categories 1 and 2, AABUS.		
XRF Standards	Appendix 4		Use foils over Mylar. Standards must be calibrated yearly.		
Porosity	N/A		N/A		
Physical:					
Adhesion/Tape Test	IPC-TM-650, Method 2.4.1	3.4	No evidence of plating removal. No evidence of mask removal (<i>not all masks will meet this requirement</i>).		
Solderability	J-STD-003	3.5	Meets solderability requirements of Category 3 durability (greater than six months shelf life). The storage conditions are critical if the deposit is to meet this performance level. Other durability levels acceptable AABUS.		
Chemical:					
Coulometric Stripping	Appendix 5	3.2	Qualification and AABUS frequency.		
Auger / XPS	Appendix 5	3.2	Qualification and AABUS frequency.		
Chemical Resistance	N/A	3.7	AABUS		
Electrical:					
High Frequency Signal Loss	N/A	3.8	N/A		
Contact Resistance	N/A	1.4.2	N/A		
Environmental:					
Whiskers	N/A	3.9	ISn may experience whisker growth under certain use conditions. The end user is responsible to determine likelihood of whisker growth and their potential impact on module's long term reliability.		
Cleanliness	IPC-TM-650, Method 2.3.25	3.6	Maximum 1.56 μg/cm ²		
SIR	IPC-TM-650, Method 2.6.3.5	3.6	1.0E+02 Megohms		
Electrochemical Migration	IPC-TM-650, Method 2.6.14.1		One decade loss.		

of dendritic growth between adjacent conductors or pads. The use of IPC-TM-650, Method 2.6.14.1 “Electrochemical Migration Resistance Test” is recommended for high reliability applications or designs of high density. The resistance values **shall not** drop more than one decade after the test has been completed.

3.7 Chemical Resistance Chemical resistance testing of the ISn finish may be detailed AABUS. This is typically used for harsh end use environments where the possibility of chemical/environmental attack of nonsoldered pads/vias may occur.

3.8 High Frequency Signal Loss The performance of ISn in high frequency applications can be acceptable, but depends on a variety of factors, including interconnect structure (i.e., strip line vs micro strip, interconnect geometry, trace length) and dielectric materials. **Note:** The committee seeks further information on high frequency applications.

3.9 Whisker Issues Immersion tin has been shown to be susceptible to whisker growth under certain conditions. However ISn has NOT been shown to produce whiskers when exposed to the classic acceleration methods used for electrolytic tin. The industry continues to work on a test-method designed to quickly indicate the susceptibility of a deposit to whisker growth. The deposit will be used with the understanding that the responsibility to verify the impact of potential whisker growth on a module’s long term reliability is the end users’. See the excerpt from the joint JEDEC/IPC JP002 guideline document and an example of an OEM’s requirements in Appendix 6.

Table 3-2 is provided as a rating scheme for the severity of whisker growth in a via/plated-through hole or on a SMT pad of a PWB. It does not imply pass/fail or accept/reject criteria. The end user **shall** determine the impact of the severity of the whiskers as per this rating on the end use application of the module/assembly. Examination of the board **shall** be at 100X magnification (see Figures 3-5 through 3-8).

Table 3-2 ISn Whisker Rating Scheme Using 100 X Magnification

Rating	Whisker Size	Number of Whiskers Observed
0	0	0
1	≤10 microns	≤5
2	≤10 microns	≤10
3	≤10 microns	>10
4	≤50 microns	≤5
5	≤50 microns	≤10
6	≤50 microns	>10
7	>50 microns	≤5
8	>50 microns	≤10
9	>50 microns	>10



Figure 3-5 Rating of 1 As Measured at 100 X

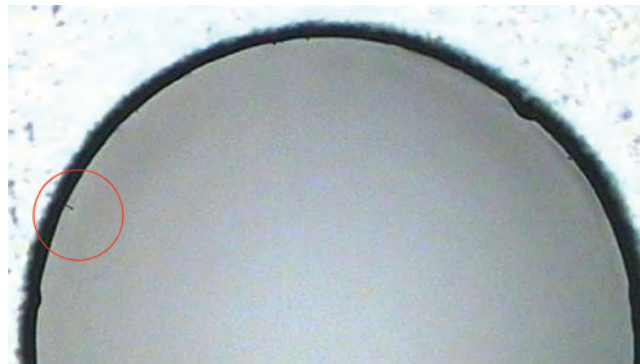


Figure 3-6 Rating of 4 As Measured at 100X

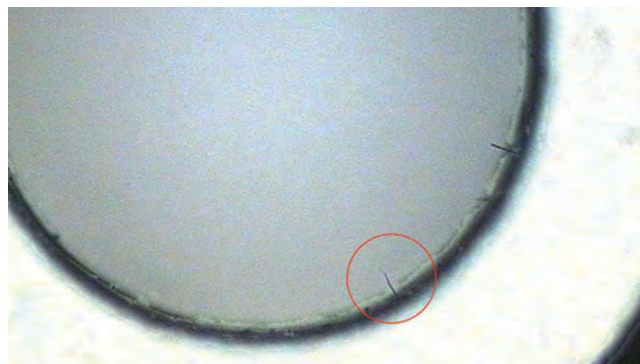


Figure 3-7 Rating of 7 As Measured at 100X

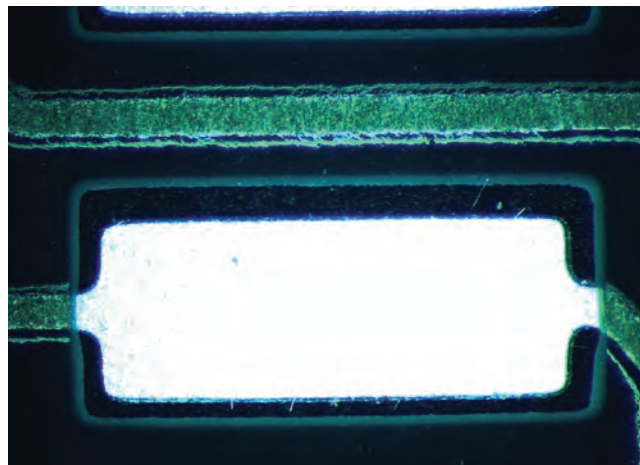


Figure 3-8 Rating of 5 As Measured at 100X

4 QUALITY ASSURANCE PROVISIONS

General Quality Assurance Provisions are specified in IPC-6011 and each sectional specification. Additional requirements for PCB with immersion tin (ISn) plating are specified herein for qualification, acceptance and quality conformance.

4.1 Qualification Qualification of a PCB product is agreed upon by the user and supplier (see IPC-6011). The process capability of a supplier of PCB with ISn finish **shall** be evaluated. ISn is a unique deposit whose shelf life is consumed by the naturally occurring growth of copper-tin IMCs. Thickness of the deposit, as measured by XRF, will not change significantly as a function of shelf life and storage conditions, whereas the useable tin (non-IMCs) does change with shelf life and storage conditions. It is imperative that, during qualification, the distinction between “useable tin” supplied versus “total tin” remaining be made. This will require the use of analytical equipment that may not be found in every PCB fabrication facility and will require the PCB supplier to send samples to an independent source for useable tin verification. Testing for useable tin **shall** be made over the life of the ISn bath. This will insure that, throughout the bath life, a minimum amount of useable tin, to meet the thermal requirements of assembly and/or over the product’s shelf life, is always supplied.

Further, it is strongly recommended that the PCB supplier determine their process capability and the useable tin deposit thickness over the life of a bath during their installation of the specific ISn chemistry bath in their own facility. Having the data set of useable tin versus total deposit thickness, over the full anticipated bath life, may greatly reduce the qualification process imposed on the PCB supplier by the end user.

It should be noted that suppliers of lower deposit thicknesses may produce an ISn deposit that is, in the majority, free of IMCs and will meet the toughest assembly requirements with no difficulties. It should also be noted that supplying 1 micron [40 microinches] of total thickness does not guarantee defect-free assembly with extensive shelf life.

Since the primary function of the ISn deposit is solderability, it is further recommended that soldering perfor-

mance testing be included in the user’s qualification process of the PCB supplier. Meeting the thickness specification but not being able to solder to the PCB product **shall** always be considered cause for rejection.

Note: The following caveat is critical for the user: Know your supplier, know their process and verify that they are following the recommendations of their ISn chemistry supplier.

Appendix 3 describes recommended qualification aspects of the ISn process by a PCB supplier.

4.1.1 Sample Test Coupons Test specimens used for the qualification of a PCB with ISn finish, **shall** be as specified in IPC-6011 and each sectional specification. The specimens/test coupons for an additional testing requirement for multiple types are listed in Table 4-1.

Table 4-1 Qualification Test Coupons

Test	Type 1	Types 2,3,5	Types 4,6	Board
Physical Requirements				
Plating Thickness	M2, M5	M2, M5	M2, M5	X

Acceptance Tests

The sampling plan and frequency of acceptance testing, except the solderability and plating thickness inspections, **shall** be in accordance with IPC-6011 and each sectional specification. The sampling plan of the solderability and thickness of ISn finish **shall** be AABUS.

4.2 Quality Conformance Testing Quality conformance testing **shall** consist of inspections as specified in IPC-6011 and each sectional specification, with the addition of regular thickness inspections. The frequency of thickness inspection **shall** be one inspection (5 XRF measurements) per lot for Classes 1 and 2, and AABUS for Class 3 products.

Any rejection of an ISn-finished lot because of it failing to meet incoming solderability testing requirements and/or it resulting in manufacturing line defects that are proven to be associated with insufficient useable tin, will likely require (AABUS) the supplier on subsequent lots, to provide verification (data) that the ‘useable tin’-to-‘total tin’ relationship developed during qualification still exists.

APPENDIX 1

Chemical Process Definitions

Electroless Process This chemical process promotes continuous deposition of a metal onto the PCB surface through an oxidation-reduction chemical reaction, without the use of an external electrical potential. A reducing agent, such as sodium hypophosphite, donates electrons to the positively charged metal ions in solution, thereby reducing the metal and promoting its deposition onto the catalyzed metal surfaces of the PCB. This reaction is considered auto-catalytic because it will continue to plate in the presence of source metal ions and a reducing agent until the board is removed from the plating bath. The thickness of plated deposits varies according to temperature, chemical parameters and the amount of time spent in the plating bath.

Immersion Process The tin deposit is formed by a chemical displacement reaction with the copper surface of

the PWB. The copper substrate dissolves, donating electrons that reduce the tin ions present in solution to metallic tin.

Additives in the solution modify the electrochemical potential difference between copper and tin, allowing copper to displace tin from solution. The effect of the additives is to reverse the normal positions of copper and tin in the Electromotive Series (which indicates the relative tendency of metals to be oxidized or reduced).

Immersion films will continue to grow while dissolution of the substrate is possible. As the thickness of immersion deposits increase, they become less and less porous and the rate of deposition falls. When the deposit porosity falls to very low values, the deposition rate falls to essentially zero and a constant thickness of deposit is reached. This behavior is described as self-limiting.

APPENDIX 2

Typical Process Sequence

1 Cleaner The purpose of this step is to clean the copper surface in preparation for processing. The cleaner removes oxides, and light surface contaminants and ensures that the copper surface will be in a condition to be uniformly micro-etched. Vendor specifications of temperature, dwell time, agitation and bath chemical control should be followed.

2 Microetch The purpose of this step is to micro-etch the copper and to produce a surface that may be uniformly activated and plated with good deposit adhesion. A variety of different etchant types may be used (for example: sodium persulfate, peroxide/sulfuric). Vendor specifications of temperature, dwell time, agitation and bath chemical control should be followed.

3 Pre Dip Similar materials to tin bath, moderating initial deposition of the tin, providing more controlled uniform deposit.

4 Immersion Tin

5 Post Dip / Cleaner – (optional) pH controlled rinse bath, saponifier / complexer to remove tin salts.

6 Rinsing The purpose of this step is to remove residual process chemicals from the PCB surface after each chemical processing step. This may be achieved in a single or multiple rinse steps. In some instances pre-dip and/or post-dip process steps may also be required for optimum process performance. Vendor specifications of temperature, dwell time, agitation and turn over rate should be followed.

7 Drying The purpose of this step is to ensure the boards are completely dry. This may be achieved by on-line vertical or off-line horizontal drying. Off-line horizontal drying should be preceded by a horizontal rinsing step and should be dedicated to the ISn process. The time and temperature have to be optimized to suit the type of product.

APPENDIX 3

Qualification of ISn Process by the Board Supplier

During process qualification, the following aspects **shall** be required:

Solderability Solderability **shall** meet the requirements of J-STD-003, Category 3 throughout the life of the tin bath. Qualification to lesser durability category ratings, such as 1 or 2, **shall** be AABUS. Due to the affinity of tin for copper, special attention should be paid to copper loading and its effect on the solderability performance

Thickness Distribution Characterize thickness distribution from panel to panel and within the different features of the panel. Establish acceptance criteria. Determine “useable tin” versus “total tin” deposit thickness over the life of the bath by use of either coulometric stripping or Auger analysis.

Compatibility Due to the chemically aggressive nature of the ISn process, verification of material compatibility is very important. Verify that the process is compatible with

pre- and with post-process steps and material. Solder mask and legend ink are good examples of process or material compatibility concerns.

Processability Follow vendor instructions for process control to include: temperature & dwell time, frequency of analysis, dump and remake schedules, controllers, etc. The use of automatic dialysis systems to maintain both a constant and maximum copper loading is an option for high volume production facilities.

SEC / SIR / Electrolytic Corrosion Testing ISn chemical processes may have high ionic content that will produce corrosion failures in very short use time periods unless great detail is paid to the cleanliness of the final product. Multiple tests for SEC, SIR and Electrolytic corrosion are recommended over the useable bath life of a particular chemistry being qualified. Periodic conformance testing should also be requested.

APPENDIX 4

XRF Measurement Techniques

Frank Ferrandino, Matrix Metrologies Inc.

Background and Measurement Considerations Measurement of the thickness of immersion silver (IAg) or immersion tin (ISn) plating on PCBs is an important operation in the manufacture of printed circuit boards. The thickness of the finish has a direct impact on the solderability and the shelf life of the product. Thickness measurement by X-Ray Fluorescence (XRF) is a suitable choice as it is nondestructive, relatively fast, and lends itself well to production environments. However, measurement of thin ISn and IAg deposits present some unique challenges to XRF instrumentation. If not properly configured and/or calibrated, XRF measurements can be both inaccurate and imprecise.

XRF tools all provide a source of x-rays (beam generation column) and some method of x-ray detection of the resultant fluorescence from the sample being measured. Measurement precision depends largely on the intensity of the sample fluorescence (signal), the signal-to-background ratio and the change in signal intensity with respect to change in thickness. Measurement accuracy depends on the accuracy of the calibration standards, and the effectiveness of the calibration model used, as well as any spectrum processing algorithms, which may be used to extract net intensity data from the acquired sample spectrum.

In the case of typical, lower cost XRF tools used to measure plating thickness in production environments, X-Ray sources using tubes with W or Mo anodes are coupled with proportional counter detectors. In most cases, this is a good solution for most plating thickness measurement.

However, with respect to measurement of ISn and IAg on PCBs there are two primary issues, which emerge when using this typical XRF configuration, namely signal level and background noise.

First, measurement precision is often poor because the signal levels (i.e., fluorescence intensities) are low. In addition, because such instruments typically detect the Ag and Sn “K” series x-ray lines, the change in signal per change in thickness is often small. The result is a thickness measurement which is not precise, and which is not sensitive to small changes in plating thickness. Gauge R&R studies typically exceed 50% or more.

The second issue relates to the high energy x-ray scatter originating from the epoxy board material. This scatter will provide excessive background noise in the IAg and ISn spectral regions, which further degrades measurement precision. This background noise also varies with respect to the laminate copper thickness. Since the plating fluores-

cence signal intensity from IAg and ISn is on the same order of magnitude as this background scatter, such variations in background due to changes in Cu thickness can result in 10% to 50% error in thickness measurement.

Recommended XRF Configuration By employing background compensation software which attempts to model the background noise on a sample by sample basis, and by using extra long measuring times (example 120 - 180 seconds), measurement of IAg and ISn is possible using the typical low cost XRF instrument configuration.

In addition, with the use of a modified X-ray beam generation column, one can excite the more efficient L- series x-ray lines for IAg and ISn. Such cost effective modifications are offered by some suppliers for standard XRF tools used by the PCB industry to measure plating thickness.

The use of the L-series x-ray lines provides three benefits, which improve accuracy and measurement precision:

1. The **fluorescence intensities** for the L series x-ray lines can be made to be higher than the K lines for the thickness range under consideration. Higher intensity automatically provides for better measurement precision.
2. Because the x-ray L line series are much lower in energy than corresponding K lines for IAg and ISn, the maximum measurement range is drastically reduced (typically 60 microinches for Ag and 100 microinches for Sn). By virtue of this reduced scale, **the change in L line fluorescence intensity with respect to change in plating thickness** is significantly increased relative to the K line series.
3. Since the L-series are in the low energy part of the x-ray spectrum, low energy scatter from the epoxy board material cannot penetrate the Cu layer to affect the detector. Therefore, background noise levels in this region of the spectrum are much lower than the higher energy portion of the spectrum. The significantly **improved signal-to-noise ratios** result again in better precision. Measurement accuracy is also improved, as there is no background noise variation due to Cu thickness variation from sample to sample.

By making a simple configuration change, measurement accuracies can be improved to $\pm 5\%$ or ± 0.25 microinches, regardless of copper laminate thickness. Gauge R&R results are typically in the range of 10 to 20%, depending on measurement time used and process tolerances. This solution provides adequate measurement of ISn and IAg coatings on larger pad areas (15 mil or larger) and traces which are at least 6 mils wide.