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IPC-4761

Design Guide for Protection of Printed Board Via Structures

IPC-4761

July 2006

A standard developed by IPC

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Developed by the Via Protection Task Group (D-33d)
of the Rigid Printed Board Committee (D-30) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

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Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Via Protection Task Group (D-33d) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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Design Guide for Protection of Printed Board Via Structures

1 SCOPE

The protection of through vias within Printed Wiring Boards (PWB) has evolved from limited use to common practice. Technology has evolved where via fabrication techniques and protection methodologies need to be defined to allow current designs to be manufacturable at an acceptable yield and cost. Numerous techniques and objectives exist, and will be discussed in this document. This document is the product of the IPC D-33d Via Protection Task Group and has been developed to provide guidance for the designer and fabricator on how via protection should be approached as well as guidance on how via protection should be specified in procurement documentation.

1.1 Purpose This guideline provides PWB designers, fabricators and/or users with information on existing methods for the protection of vias on printed boards. In addition to detailing some of the advantages of via protection, production and material issues are given to aid the user in evaluating the benefits and concerns for each type of protection.

1.2 Terms and Definitions The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined below.

Bumped Via Protection – Via protection where the hole plugging or fill material protrudes above the surface of the hole interface producing a convex shape. See Figure 1-1.

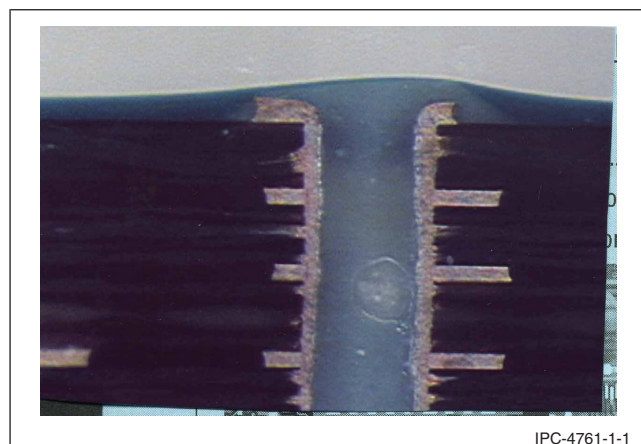


Figure 1-1 Bumped Via Protection Material

Dimpled Via Protection – Via protection where the hole plugging or fill material recedes below the hole interface producing a concave shape. See Figure 1-2.

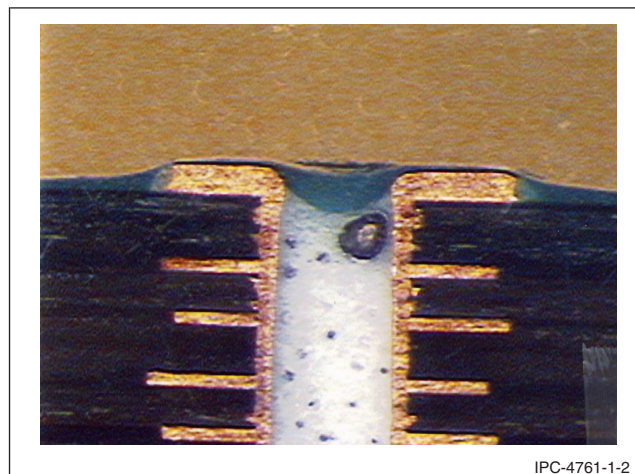


Figure 1-2 Dimpled Via Protection Material

Planarized Via Protection – Via protection where the excess hole plugging or fill material protruding above the hole interface has been removed by a process to produce a coplanar surface. See Figure 1-3.

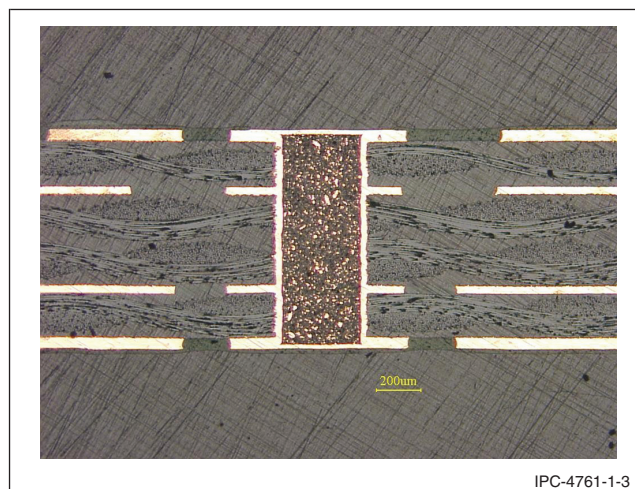


Figure 1-3 Planarized and Capped Via Protection Material

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-A-600 Acceptability of Printed Boards

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

¹www.ipc.org

IPC-2221 Generic Standard on Printed Board Design**IPC-6012** Qualification and Performance Specification for Rigid Printed Boards**3 PWB FABRICATION AND ASSEMBLY GUIDELINES**

Interconnect vias are utilized in routing high-density surface mount components. They provide continuity between the lands on the PWB surface and internal circuitry connections. They are located in close proximity to the lands and the component in order to minimize signal length and to avoid interference with other circuitry on the outer layer. Because they are close to both the component body and the solder joint, care must be taken in the design to avoid harm to either.

There are a number of advantages with providing protection for interconnect vias; however, there are just as many production issues within the PWB fabrication and assembly processes that users must consider.

3.1 Advantages of Via Protection Some of the advantages of protecting vias include the following, though not every advantage is applicable for every via protection type described in 5.1 through 5.7:

- Prevent corrosion caused by PWB fabrication processes such as plating or flux residue, from either fabrication or assembly, from passing through or becoming trapped in plated-through holes (PTHs).
- Improve vacuum handling, placement of surface mount technology (SMT) parts by sealing the surface and to prevent air leakage during In Circuit Test (ICT). Unfilled through hole via holes may contribute to intermittent test probe contact as a result of probe contamination when air is pulled through the unfilled via.
- Prevent solder ball blowout during assembly processes, i.e., wave or reflow, that utilize solder paste
- Prevent solder mask creep into holes
- Reduces solder paste loss
- Isolate via holes of conventional PWB products within the assembly soldering process to prevent migration, shorts, and contamination entrapment under components
- Fill/Flush Vias within build-up cores to ensure planarity for subsequent dielectric layer formation and dielectric separation, or to assure adequate resin fill in the subsequent bonding process
- Prevent migration of adhesives and encapsulants used during assembly under rigid area array integrated circuit (IC) packaging substrates.
- Prevent flux from flowing through vias which can inhibit the curing of bonding adhesives.

For specific advantages of each protection type, see Table 5-1.

3.2 PWB Fabrication Issues There are a number of issues in the PWB fabrication process that need to be taken into consideration when evaluating a protection methodology, including the following:

- Partial plugging can result in solder from the Hot Air Solder Level (HASL) operation being trapped within the vias. During subsequent reflow soldering the solder can be expelled by trapped gasses forming large solder balls on the surface.
- Application of final finishes following single-sided techniques can result in circumferential voids within the surface finish in vias being tented or plugged and may result in reliability issues such as corrosion of exposed copper.
- Adhesion of tent or plug material to final finishes.
- Plugging of vias from both sides of the hole results in manufacturability and reliability issues.
- Process methods and/or manufacturing complexity may vary depending upon the requirements of the end-customer application.
- Hole fill or plug with either solder mask or epoxy fill compound can be difficult to perform depending upon the process used. Voids within high modulus fill or plug materials can be a significant concern, particularly when those voids are in direct contact with the PTH wall, causing a long-term reliability stress riser. Check with specific fill material manufacturer to determine if modulus data is available. Voids located near the surface SMT contact pad are also cause for concern. For these reasons, voids should be kept to a minimum.
- The Coefficient Thermal Expansion (CTE) mismatch characteristic is known to sometimes cause barrel cracks within the hole wall.
- Use of partial via plugging should only be done after application of inert final surface finishes to avoid potential chemical attack to the via hole wall. Partial plugging or tenting from one side can result in bare copper in the via. See 3.4 for additional information on chemical entrapment in plugged vias.
- Application of HASL final finish prior to partial via plugging requires a unique plug operation. HASL imparts a melting metal coating to the copper via wall which is very different from non-melting metal applications; there is consequently no adhesion of the plug material to the barrel of the via, so the plug must be anchored to the laminate and/or solder mask surface surrounding the via for it to stay in place during soldering.
- Utilization of a final finish that does not contain inert metals, such as organic solderability preservative (OSP) coatings, can be a concern for protecting hole wall copper from corrosion. When using OSP finishes it is recommended to use a complete fill operation (see 5.5) or a two-sided tent and cover application (see 5.6).

- Liquid Photo-Imageable (LPI) solder mask is often used to plug vias. However, any solvent containing ink which is forced into a via hole will have difficulty drying the plug of ink in the hole and residual solvents can "pop" later during soldering operations. Also, LPI inks rely on UV and/or thermal energy for their cure, making it difficult to get sufficient UV light down through the plug to get good cure. There are however LPI fill materials on the market that have been specifically optimized for UV cure and, in such cases, high aspect ratio vias are a non-issue for curing.
- Electroless nickel immersion gold (ENIG) plating offers variation in plugged via structures. The plugging operation can be performed before or after metallization. One instance utilizes an LPI dot pattern to open the vias, followed by ENIG metallization and then plugging from one side (see 5.3). Another instance utilizes metallization first followed by a plug operation with a subsequent LPI covering (see 5.4). The resulting difference in appearance among the two techniques is the opening in the LPI that is required to allow the plating into the hole.

3.2.1 Fill or Plug Separation from Plated Hole Wall

There exists the potential for separation of the fill or plug material from the knee of the plated hole which may entrap chemistry as shown in Figure 3-1. When establishing a protection methodology it is recommended that a maximum allowable depth be established for both hole fill separation and dimples, as shown in Figure 3-1 and 3-2.

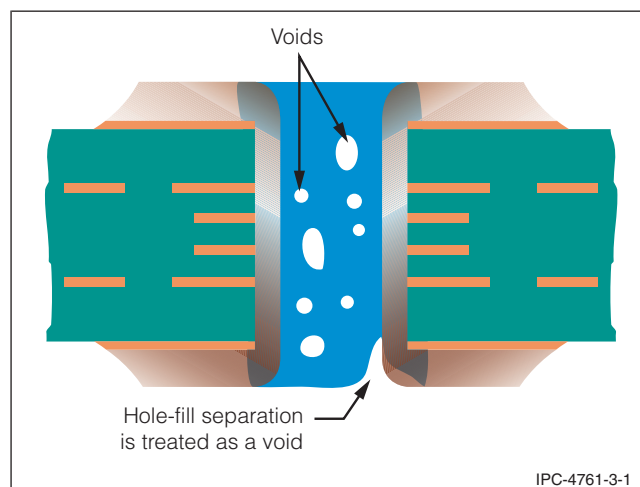


Figure 3-1 Example of Hole Fill/Plug Separation from Plated Hole Wall

3.2.2 Voids Voids can be a concern where material is used to provide a partial plug or complete fill of a via. See Figure 3-3 and Figure 3-4 for examples of voids in via fill material.

3.3 Assembly Process Issues There are several issues in the assembly process that are unique:

- The use of a solder paste stencil requires contact with a flat surface topography to provide a gasketing effect around the solder pad openings.

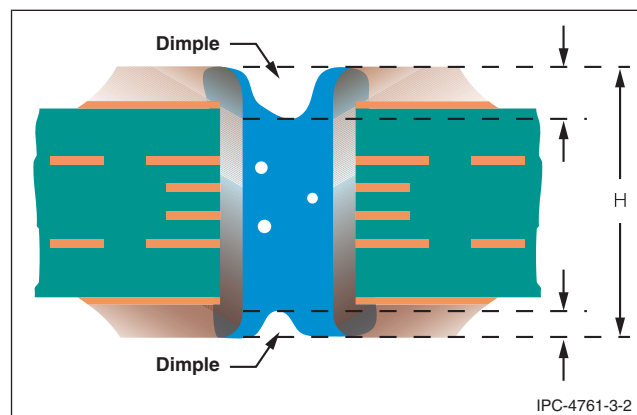


Figure 3-2 Example of Dimples Within Fill/Plug Material



Figure 3-3 Voids in Via Fill Material

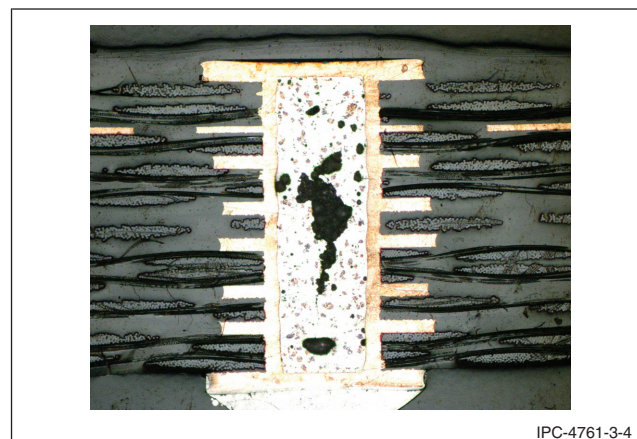


Figure 3-4 Large Voids in Via Fill Material

- Bump height, which is defined as the difference between the height of the mask over the via and the height of the adjacent solderable land, can affect or interrupt the solder stencil paste application. It has been commonly noted in industry that a bump height of 0.076 mm [0.003 in] or greater can cause a non-contact effect on the application of solder paste.
- Vias can serve as a reservoir to entrap flux or other contaminants that become difficult or impossible to clean. This is all especially true when they lie under the component outline.