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IPC-6012F

Qualification and Performance Specification for Rigid Printed Boards

Developed by the Rigid Printed Board Performance Specifications Task Group (D-33a) of the Rigid Printed Board Committee (D-30) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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Qualification and Performance Specification for Rigid Printed Boards

1 SCOPE

1.1 Statement of Scope This specification establishes and defines the qualification and performance requirements for the fabrication of rigid printed boards.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of rigid printed boards based on the following constructions and/or technologies. These requirements apply to the finished product unless otherwise specified:

- Single-sided, double-sided printed boards with or without plated-through holes (PTHs).
- Multilayer printed boards with PTHs with or without buried/blind vias/microvias.
- Active/passive embedded circuitry printed boards with distributive capacitive planes and/or capacitive or resistive components.
- Metal core printed boards with or without an external metal heat frame, which may be active or non-active.

1.2.1 Supporting Documentation

1.2.1 Supporting Documentation IPC-A-600, which contains figures, illustrations and photographs that can aid in the visualization of externally and internally observable acceptable/nonconforming conditions, may be used in conjunction with this specification for a more complete understanding of the recommendations and requirements.

1.3 Performance Classification and Type

1.3.1 Classification This specification establishes acceptance criteria for the performance classification of rigid printed boards based on customer and/or end-use requirements. Printed boards are classified by one of three general Performance Classes as defined in IPC-6011.

1.3.1.1 Requirement Deviations Requirements deviating from these heritage classifications **shall** be as agreed between user and supplier (AABUS).

1.3.1.2 Space Requirement Deviations Space performance classification deviations are provided in the IPC-6012XS Addendum (where “X” is applicable revision published at time of procurement) and is applicable when the addendum is specified within the procurement documentation. Any amendments to the base IPC-6012 published after an Addendum do not extend to that Addendum.

1.3.1.3 Medical Requirement Deviations Medical performance classification deviations are provided in the IPC-6012XM Addendum (where “X” is applicable revision published at time of procurement) and is applicable when the addendum is specified within the procurement documentation. Any amendments to the base IPC-6012 published after an Addendum do not extend to that Addendum.

1.3.1.4 Automotive Requirement Deviations Automotive performance classification deviations are provided in the IPC-6012XA Addendum (where “X” is applicable revision published at time of procurement) and is applicable when the addendum is specified within the procurement documentation. Any amendments to the base IPC-6012 published after an Addendum do not extend to that Addendum.

1.3.2 Printed Board Type Printed boards without PTHs (Type 1) and with PTHs (Types 2-6) are classified as follows and may include technology adders as described in Table 1-1.

Type 1—Single-Sided Printed Board

Type 2—Double-Sided Printed Board

Type 3—Multilayer Printed Board without blind or buried vias

Type 4—Multilayer Printed Board with blind and/or buried vias (may include microvias)

Type 5—Multilayer metal core Printed Board without blind or buried vias

Type 6—Multilayer metal core Printed Board with blind and/or buried vias (may include microvias)

Table 1-1 Technology Adders

Technology Code	Technology
HDI	HDI build-up features (stacked and/or staggered microvias)
VP	Via Protection
WBP	Wire Bondable Pads
MB	Metal Base
AMC	Active Metal Core
NAMC	Non-active Metal Core
HF	External Heat Frame
EP	Embedded Passives per IPC-6017
VIP-C	Via-in-Pad, Conductive Fill
VIP-N	Via-in-Pad, Nonconductive Fill

Example: IPC-6011/6012/3/1/S/-/3/HDI/EP

1.3.3 Selection for Procurement Performance Class **shall** be specified in the procurement documentation.

The procurement documentation **shall** provide sufficient information to fabricate the printed board and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

The procurement documentation **shall** specify the thermal stress test method to be used to meet the requirement of 3.6.1. Selection **shall** be from those depicted in 3.6.1.1, 3.6.1.2 and 3.6.1.3. If not specified (see 5.1), the default **shall** be per Table 1-2.

During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

- Wave solder, selective solder, hand solder assembly processes (see 3.6.1.1)
- Conventional (eutectic SnPb) reflow processes (see 3.6.1.2)
- Pb-free reflow processes (see 3.6.1.3)

1.3.3.1 Selection (Default) The procurement documentation **shall** specify those requirements that are a result of the selection process within this specification. This includes all references to “AABUS”. If the requirement selection is not made in accordance with 1.3.3.2, the procurement documentation, Ordering Data (see 5.1), Customer Drawing and/or supplier control plan (SCP), then the default requirement in Table 1-2 **shall** apply.

Table 1-2 Default Requirements

Category	Default Selection
Performance Class	Class 2
Material	Epoxy-Glass Laminate per 3.2.1
Surface Finish	X ¹ per Table 3-3
Surface Finish	ENIG ² per Table 3-3
Minimum Starting Foil Weight	1/2 oz. for all internal and external layers except Type 1 which shall start with 1 oz. For plated HDI layers – 1/4 oz. for all layers (internal or external)
Copper Foil Type	Electrodeposited per 3.2.4
Hole Diameter Tolerance Plated, components Plated, via only Non-plated	(±) 100 µm [3,937 µin] (+) 80 µm [3,150 µin], (-) no requirement, (may be totally or partially plugged) (±) 80 µm [3,150 µin]

Category	Default Selection
Conductor Width tolerance	Class 2 requirements per 3.5.1
Conductor Spacing tolerance	Class 2 requirements per 3.5.2
Dielectric Separation	65 µm [2,560 µin] minimum per 3.6.2.18
Marking Ink	Contrasting color, nonconductive per 3.3.5
Solder Mask	Not applied, if not specified per 1.3.4.3
Solder Mask, specified	Class T of IPC-SM-840 if class not specified per 3.7
SnPb Solder Coating	Sn63/Pb37 per 3.2.7.3.1
Pb-free Solder Coating	3.2.7.3.2
Solderability Test	Per 3.3.6, Category 2 for SnPb and Category A for Pb-free of J-STD-003.
Thermal Stress Test	IPC-TM-650, Method 2.6.8, Condition A per 3.6.1.1
Test Voltage, Isolation Resistance, Continuity Resistance	Per IPC-9252
Qualification not specified	See IPC-6011

Note 1. Initial Release of designs (drawings) on or prior to October 01 2023.

Note 2. Initial Release of designs (drawings) on or after October 01 2023.

1.3.3.2 Selection System (Optional) The following product selection identifier system is provided for clarification of the build type.

Quality Specification, the generic quality specification.

Specification, the base performance specification.

Type, the printed board type per 1.3.2.

Plating Process, the plating process per 1.3.4.2.

Surface Finish, the surface finish code per 1.3.4.3.

Selective Finish, the selective finish code adder per 1.3.4.3, enter “-” when no selective finish is required.

Classification, the classification per 1.3.1 or performance specification sheet.

Technology Adder, the technology adder as specified in Table 1-1. Add multiple codes as required.

1.3.4 Material, Plating Process and Surface Finish

1.3.4.1 Laminate Material Laminate material is identified by numbers and/or letters, classes and types as specified by the appropriate specification listed in the procurement documentation.

1.3.4.2 Plating Process The copper plating process, which is used to provide conductivity in the holes, is identified by a single number as follows:

1. Acid copper electroplating only
2. Pyrophosphate copper electroplating only
3. Acid and/or pyrophosphate copper electroplating
4. Additive/electroless copper
5. Electrodeposited Nickel underplate with acid and/or pyrophosphate copper electroplating

1.3.4.3 Surface Finish and Coatings The surface finish/coating can be one of the finishes/coatings specified below or a combination of several platings and is dependent on assembly processes and end-use. If required, the thickness **shall** be specified in the procurement documentation. If not specified, the thickness **shall** be as listed in Table 3-3. Coating thickness may be exempted in Table 3-3 (i.e., tin-lead plate or solder coating). Designators for surface finish are as follows:

S	Solder Coating	(Table 3-3)
T	Electrodeposited Tin-Lead, (fused)	(Table 3-3)
X	Either Type S or T	(Table 3-3)
TLU	Electrodeposited Tin-Lead (unfused)	(Table 3-3)
b1	Pb-free Solder Coating	(Table 3-3)
G	Gold Electroplate for Edge Printed Board Connectors	(Table 3-3)
GS	Gold Electroplate for Areas to be Soldered	(Table 3-3)
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic)	(Table 3-3)
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic)	(Table 3-3)
N	Nickel for Edge Printed Board Connectors	(Table 3-3)
NB	Nickel as a Barrier to Copper-Tin Diffusion	(Table 3-3)
OSP	Organic Solderability Preservative	(Table 3-3)
HT OSP	High Temperature OSP	(Table 3-3)
ENIG	Electroless Nickel Immersion Gold	(Table 3-3)
ENEPIG	Electroless Nickel/Electroless Palladium/Immersion Gold	(Table 3-3)
DIG	Direct Immersion Gold	(Table 3-3)
NBEG	Nickel Barrier/Electroless Gold	AABUS
IAG	Immersion Silver	(Table 3-3)
ISn	Immersion Tin	(Table 3-3)
C	Bare Copper	(Table 3-3)
SMOBC	Solder Mask over Bare Copper	(3.2.8)
SM	Solder Mask over Non-Melting Metal	(3.2.8)
SM-LPI	Liquid Photoimageable Solder Mask over Non-Melting Metal	(3.2.8)
SM-DF	Dry Film Solder Mask over Non-Melting Metal	(3.2.8)
SM-TM	Thermal Mask Solder Mask over Non-Melting Metal	(3.2.8)
Y	Other	(3.2.7.11)

1.4 Terms and Definitions The definition of all terms used herein **shall** be in accordance with IPC-T-50 and as follows.

1.4.1 Back-Drilling A method of reducing the overall length of any plated hole by drilling out a portion of the plated hole from either side to a predetermined depth, for purposes of signal integrity or circuit isolation (See Figure 1-1).

Figure 1-2 provides an example of a “shallow back-drill” where the external layer is pierced and approximately 0.05 – 0.127 mm [0.002 – 0.005 in] of the barrel is drilled out in order to prevent shorting of the plated via to any component/chassis placed directly above or below the back-drill side.

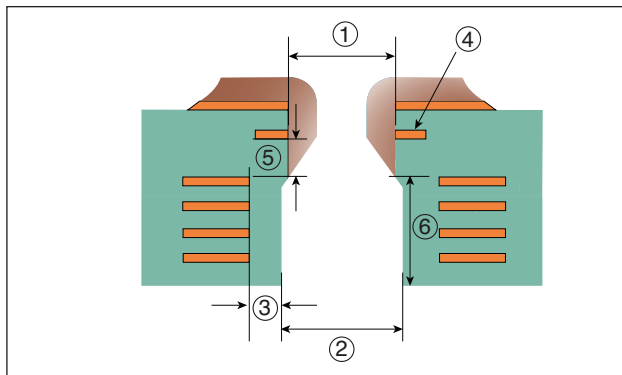


Figure 1-1 Example of a Back-drilled Hole (Not to Scale)

Note 1. Primary drilled hole diameter.

Note 2. Back-drill hole diameter.

Note 3. Distance between nearest conductive feature and back-drill hole.

Note 4. Target Layer (e.g., Must Not Cut Layer).

Note 5. Stub length (excluding target layer copper thickness).

Note 6. Back-drill depth.

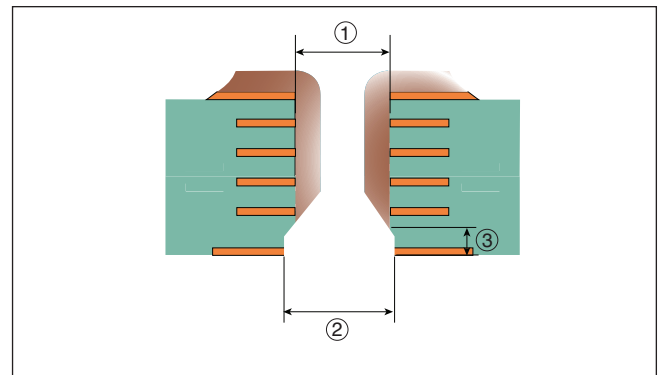


Figure 1-2 Example of a Shallow Back-drill (Not to Scale)

Note 1. Primary drilled hole diameter.

Note 2. Back-drill hole diameter.

Note 3. Back-drill depth.

1.4.2 Stub (Plated Hole) Maximum remaining length of the hole wall plating from target layer to back-drill termination.

1.4.3 Back-drill Depth The distance from the printed board dielectric surface on the back drill penetration side to the nearest remaining copper stub.

1.4.4 Microvia A blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 1-3, terminating on or penetrating a target land, with a total depth (X) of no more than 0.25 mm [0.00984 in] measured from the structure's capture land foil to the target land.

1.4.5 Design Data Data which is communicated to a printed board fabricator and may include mechanical information, electrical design information and requirements concerning end item performance, item end-use environment, item configuration, materials, components, and processes.

1.5 Interpretation “**Shall**” the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a “**shall**” requirement may be considered if sufficient data is supplied to justify the exception. To assist the reader, the word “**shall**” is presented in bold characters.

The words “**should**” and “**may**” are used whenever it is necessary to express non-mandatory provisions. “**Will**” is used to express a declaration of purpose.

The examples shown in the photographs and/or illustrations in this specification are sometimes exaggerated to make the referenced imperfection more apparent. The relationship between the text and the examples is not always parallel; it would be difficult to find many cases so specific that they would always match the acceptance criteria. When photographs or illustrations contained in this standard are not consistent with discussion in the written text, the written text takes precedence and **shall** be followed.

1.6 Presentation All dimensions and tolerances in this specification are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this specification are expected to use metric dimensions. All dimensions greater than or equal to 1.0 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions less than 1.0 mm [0.0394 in] will be expressed in micrometers and microinches.

1.7 Design Data Protection Design data is property owned by an organization or business entity. When design data is known to or in the custody of the printed board fabricator or their agents, it **shall** be protected as specified by the procurement documentation.

If not specified in procurement documentation, the printed board fabricator **shall** nonetheless have internal policies and procedures for protection of the design data.

An optional protocol is defined in 3.10.14.

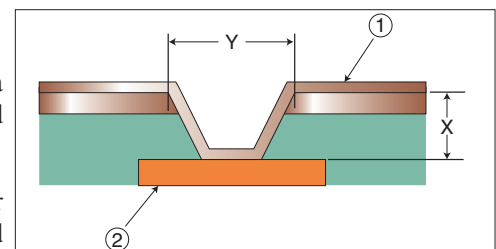


Figure 1-3 Microvia Definition

Note 1. Capture Land.

Note 2. Target Land.

Note 3: X/Y = Microvia Plating Aspect Ratio, with $X \leq 0.25$ mm [0.00984 in] and aspect ratio $\leq 1:1$.

2 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein. If a conflict of requirements exists between this specification and the listed applicable documents, this specification **shall** take precedence.

2.1 IPC¹

IPC-WP-019 An Overview on Global Change in Ionic Cleanliness Requirements

IPC/PERM-WP-022 Mitigation of Pure Tin Risk by Tin-Lead SMT Reflow – Results of an Industry Round-Robin – Final Report

IPC-WP-023 IPC Technology Solutions White Paper on Performance-Based Printed Board OEM Acceptance: Via Chain Continuity Reflow Test: The Hidden Reliability Threat

IPC-A-47 Composite Test Pattern Ten Layer Phototool

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650 Test Methods Manual²

- 2.1.1 Microsectioning, Manual and Semi or Automatic Method
- 2.3.15 Purity, Copper Foil or Plating
- 2.3.25 Detection and Measurement of Ionizable Surface Contaminants
- 2.4.1 Adhesion, Tape Testing
- 2.4.15 Surface Finish, Metal Foil
- 2.4.18.1 Tensile Strength and Elongation, In-House Plating
- 2.4.21 Land Bond Strength, Unsupported Component Hole
- 2.4.22 Bow and Twist
- 2.4.28.1 Adhesion, Solder Resist (Mask), Tape Test Method
- 2.4.36 Rework Simulation, Plated-Through Holes for Leaded Components
- 2.4.41.2 Coefficient of Thermal Expansion, Strain Gage Method
- 2.5.5.7 Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR
- 2.5.7 Dielectric Withstand Voltage, PWB
- 2.6.1 Fungus Resistance, Printed Wiring Materials
- 2.6.3 Moisture and Insulation Resistance, Rigid Boards
- 2.6.3.7 Surface Insulation Resistance
- 2.6.4 Outgassing, Printed Boards
- 2.6.5 Physical Shock, Multilayer Printed Wiring
- 2.6.7.2 Thermal Shock, Continuity and Microsection, Printed Boards
- 2.6.8 Thermal Stress, Plated-Through Holes
- 2.6.9 Vibration, Rigid Printed Wiring
- 2.6.25 Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Test)
- 2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

¹ www.ipc.org

² IPC Test Methods are available on the IPC Web site (<https://www.ipc.org/test-methods>)

IPC-SM-840	Qualification and Performance Specification of Permanent Solder Mask
IPC-1602	Standard for Printed Board Handling and Storage
IPC-1791	Trusted Electronic Designer, Manufacturer and Assembler Requirements
IPC-2221	Generic Standard on Printed Board Design
IPC-2228	Sectional Design Standard for High Frequency (RF/Microwave) Printed Boards
IPC-2251	Design Guide for the Packaging of High Speed Electronic Circuits
IPC-2611	Generic Requirements for Electronic Product Documentation
IPC-2614	Sectional Requirements for Board Fabrication Documentation
IPC-4101	Specification for Base Materials for Rigid and Multilayer Printed Boards
IPC-4103	Specification for Base Materials for High Speed/High Frequency Applications
IPC-4202	Flexible Base Dielectrics for use in Flexible Printed Circuitry
IPC-4203	Adhesive Coated Dielectric Films for Use as Cover Sheets for Flexible Printed Circuitry and Flexible Adhesive Bonding Films
IPC-4552	Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards
IPC-4553	Specification for Immersion Silver Plating for Printed Circuit Boards
IPC-4554	Specification for Immersion Tin Plating for Printed Circuit Boards
IPC-4555	Performance Specification for High Temperature Organic Solderability Preservatives (OS) for Printed Boards
IPC-4556	Specification for Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards
IPC-4562	Metal Foil for Printed Wiring Applications
IPC-4563	Resin Coated Copper Foil for Printed Boards Guideline
IPC-4761	Design Guide for Protection of Printed Board Via Structures
IPC-4781	Qualification and Performance Specification of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks
IPC-4811	Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards
IPC-4821	Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards
IPC-5703	Cleanliness Guidelines for Printed Board Fabricators
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6012XA	Automotive Applications Addendum to IPC-6012 Qualification and Performance Specification for Rigid Printed Boards (where “X” is applicable revision published at time of procurement)
IPC-6012XM	Medical Applications Addendum to IPC-6012 Qualification and Performance Specification for Rigid Printed Boards (where “X” is applicable revision published at time of procurement)
IPC-6012XS	Space and Military Avionic Applications Addendum to IPC-6012 Qualification and Performance Specification for Rigid Printed Boards (where “X” is applicable revision published at time of procurement)
IPC-6017	Qualification and Performance Specification for Printed Boards Containing Embedded Active and Passive Circuitry
IPC-7711/7721	Rework, Modification and Repair of Electronic Assemblies
IPC-9252	Requirements for Electrical Testing of Unpopulated Printed Boards
IPC-9691	User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Test)

2.2 Joint Industry Standards¹

J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
J-STD-003	Solderability Tests for Printed Boards
J-STD-006	Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
IPC/JEDEC-J-STD-609	Marking and Labeling of Components, PCBs and PCBAs to Identify Lead (Pb), Pb-Free and Other Attributes
JEDEC/IPC-JP002	Current Tin Whiskers Theory and Mitigation Practices Guideline

2.3 FEDERAL³

QQ-S-635	Military Standard Steel Plate, Carbon
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2.4 Other Publications

2.4.1 ASTM International⁴

ASTM B-152	Standard Specification for Copper Sheet, Strip, Plate, and Rolled Bar
ASTM B-488	Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses
ASTM B-579	Standard Specification for Electrodeposited Coating of Tin-Lead Alloy (Solder Plate)
ASTM-E-345	Standard Test Methods of Tension Testing of Metallic Foil

2.4.2 Underwriters Lab⁵

UL 94	Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
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2.4.3 National Electrical Manufacturers Association⁶

NEMA LI-1	Industrial Laminated Thermosetting Product Standard
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2.4.4 American Society for Quality⁷

H1331	Zero Acceptance Number Sampling Plans
Z1.4	Sampling Procedures and Tables for Inspection by Attributes

2.4.5 AMS³

SAE-AMS-QQ-A-250	General Specification for Aluminum and Aluminum Alloy, Plate and Sheet
SAE-AMS-2451	Plating, Brush General Requirements

2.4.6 American Society of Mechanical Engineers⁸

ASME B46.1	Surface Texture (Surface Roughness, Waviness and Lay)
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2.4.7 SAE³

GEIA-STD-0005-2	Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems
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3 REQUIREMENTS

3.1 General Printed boards furnished under this specification **shall** meet or exceed the requirements of IPC-6011 and the specific performance class as required by the procurement documentation. Descriptions and purposes of test coupons are documented in IPC-2221, IPC-2221 Appendix A and the legacy IPC-2221 Appendix B.

³ www.sae.org

⁴ www.astm.org

⁵ www.ul.com

⁶ www.nema.org

⁷ www.asq.org

⁸ www.asme.org

IPC-2221 Appendix A and Appendix B conformance coupons are considered interchangeable to the extent referenced herein. However, for all designs that require a “D” coupon, Appendix A “D” coupons **shall** be used unless otherwise specified.

Additionally, for designs with propagated (interconnected) via structures, it is recommended that the fabricator transition to the use of Appendix A “AB/R”, “Propagated B” and “D” coupons for the following reasons:

- Several improved coupon designs for via structures and features that make them more representative of the printed board are available in the Appendix A coupon set.
- Appendix A coupons are significantly denser, and thus require less panel space and are significantly more efficient to test.

Regarding microvias and reliability:

For Class 3 products with microvias, the caution statement within 3.6 recommends the use of the optional requirement 3.10.15. In this case, the Appendix A “D” coupons are required for IPC-TM-650 method 2.6.27, which has been determined to be more reliable in detecting weak microvia structures compared to legacy cross-section evaluations.

Regarding interconnected (complex) via structures:

HDI designs increasingly utilize interconnected via structures. Appendix A Propagated “B” and “D” coupons support interconnected via structures. Appendix B coupons “A”, “B” and “A/B” do not support interconnected via structures.

If the design includes interconnected via structures, it is preferred that they be tested as a complete structure in accordance with 3.6. As such, when the fabricator elects to use Appendix B microsection coupons, the user needs to understand that only the dimensional and quality features related to individual plated holes will be inspected. The structural integrity evaluation of individual B coupons does not test the interconnected effects of propagated via structures, and thus the Appendix A Propagated “B” coupon evaluation is preferred.

Note that revisions to IPC-2221 Appendix A occur independently of revisions to the parent IPC-2221 standard and can be obtained from the online IPC Store.

3.2 MATERIALS

3.2.1 Laminates and Bonding Material Metal clad laminates, unclad laminates and bonding material (prepreg) **shall** be selected from IPC-4101, IPC-4202, IPC-4203, or NEMA LI-1. Polytetrafluoroethylene (PTFE) material types **shall** be selected from IPC-4103. Embedded device materials **shall** be selected from IPC-4811 or IPC-4821. The procurement documentation should specify dielectric, conductive, resistive and insulating characteristics as applicable. The specification sheet number, metal cladding type and metal clad thickness (e.g., weight) **shall** be as specified in the procurement documentation. When specific requirements such as the flammability requirements shown in UL 94 for laminate and bonding materials are required, it is necessary to specify those requirements in material procurement documents.

3.2.2 External Bonding Materials The material used to adhere external heat sinks or stiffeners or used as an insulator layer to the printed board **shall** be selected from IPC-4101, IPC-4203 or as specified in the procurement documentation.

3.2.3 Other Dielectric Materials Photoimageable dielectrics should be specified in the procurement documentation. Other dielectric materials may be specified in the procurement documentation.

3.2.4 Metal Foils Copper foil **shall** be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment and foil profile should be specified on the procurement documentation if critical to the function of the printed board. Resin coated copper foil **shall** be in accordance with IPC-4563.

3.2.4.1 Resistive Metal Foil Resistive metal foil **shall** be as specified on the procurement documentation.

3.2.5 Metal Planes/Cores Internal or external metal planes and/or metal core substrates **shall** be specified on the procurement documentation as shown in Table 3-1.

Table 3-1 Metal Planes/Cores

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As Specified
Steel	QQ-S-635	As Specified
Copper	ASTM-B-152 or IPC-4562	As Specified
Copper-Invar-Copper	IPC-CF-152	As Specified
Copper-Moly-Copper	IPC-CF-152	As Specified
Other	As Specified	As Specified

3.2.6 Base Metallic Plating Depositions and Conductive Coatings The thickness of the plating and/or surface finish coatings **shall** be in accordance with Table 3-3. The copper plating thickness for the surface, PTHs, via holes, blind vias, buried vias and microvias **shall** be as specified in Table 3-10, Table 3-11 and Table 3-12. The greater wrap plating thickness is only applicable to legacy designs per the effectivity dates listed. The thickness for specific use platings **shall** be as specified in Table 3-3. The plating thickness for surface finishes or combinations thereof selected from those listed in 1.3.4.3 **shall** be as specified in Table 3-3. When measurements are required, microsection or suitable electronic measuring equipment examination **shall** be used. Fused tin-lead plating or solder coating only requires visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges. Conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.5.4.7.

Revisions to legacy designs, including those made following the effectivity date after January 01, 2018, **shall** be held at the greater wrap plating thickness unless specifically noted by the User.

Note: Changes to acceptance criteria for copper wrap plating measurements occurred within Amendment 1 to Revision D of IPC-6012. A dual criterion for Class 3 copper wrap plating was established based on design effectivity before and after 01 January 2018. This precludes imposing onto legacy designs any additional qualification activity associated with adopting newer wrap acceptance requirements.

3.2.6.1 Electroless Copper Depositions and Conductive Coatings Electroless depositions and conductive coatings **shall** be sufficient for subsequent plating processes and may be either electroless metal, vacuum deposited metal, or conductive coatings (metallic or non-metallic).

3.2.6.2 Electrodeposited Copper Electrodeposited copper plating **shall** meet the following criteria. Frequency of testing **shall** be in accordance with Table 4-4.

- When tested in accordance with IPC-TM-650, Method 2.3.15, the purity of copper **shall** be no less than 99.50%.
- When tested in accordance with IPC-TM-650, Method 2.4.18.1, using 50 - 100 μm [1,969 - 3,937 μin] thick samples, the tensile strength **shall** be no less than 248 MPa [36,000 PSI] and the elongation **shall** be no less than 12%.

3.2.6.3 Fully Additive Electroless Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification. Deviations **shall** be AABUS.

3.2.7 Surface Finish Depositions and Coatings - Metallic and Non-Metallic

3.2.7.1 Electrodeposited Tin The allowance of and the requirements for use of electrodeposited tin **shall** be AABUS. It is recommended that the user refer to JEDEC/IPC-JP002, IPC/PERM-WP-022 and SAE GEIA-STD-0005-2 for guidance on potential mitigation practices that may delay the onset of, or prevent, tin whisker formation.

3.2.7.2 Electrodeposited Tin-Lead Tin-lead plating **shall** meet the composition (50-70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected wherein the thickness specified in Table 3-3 (Code TLU) applies.

3.2.7.3 Hot Air Solder Leveling (HASL)/Solder Coating The solder coating **shall** be as specified in the procurement documentation and the procured solder used for coating **shall** meet the requirements of J-STD-006. HASL is the process for solder coating that involves dipping a printed board into solder and using hot air to level the resultant solder surface.

The tin content of the SnPb solder **shall** be maintained within +1.0% / -2.5% by weight of the nominal alloy being used, and tin content of Pb-free solder **shall** be maintained within $\pm 1.0\%$ by weight of the nominal alloy being used. Tin content **shall** be tested at the same frequency as testing for copper/gold contamination. The balance of the bath **shall** be lead and/or the items listed above. The total of copper, gold, cadmium, zinc, and aluminum contaminants **shall not** exceed 0.4%.

The frequency of analysis for the HASL solder pot to the limits of Table 3-2 **shall** be determined on the basis of Statistical Process Control (SPC) data or monthly analyses. Records containing the results of all analyses and solder bath usage (e.g., total time in use, amount of replacement solder or area throughput) **shall** be maintained for a minimum of one year for each process/system. The percentage of each element in an alloy **shall** be determined by a standard analytical procedure with sufficient resolution. The analytical method **shall** consider the homogeneity of the sample by using optical emission spectrometry or an equivalent elemental analysis instrument. The above stated tolerance and impurity levels of the alloy **shall** conform to limits of Table 3-2. If contamination exceeds the limits, intervals between the analyses, replacement or replenishment **shall** be shortened.

Table 3-2 Maximum Limits of Solder Bath Contaminant

Contaminant	Maximum Contaminant Weight Percentage Limit SnPb Alloys	Maximum Contaminant Weight Percentage Limit Sn-Cu-Ni (SN100) Pb-free Alloy
Copper (Cu)	0.3	1.1 ¹
Gold (Au)	0.2	0.2
Aluminum (Al)	0.006	0.006
Nickel (Ni)	0.050	0.100
Lead (Pb)	N/A	0.1
Total of Copper (Cu), Gold (Au), Aluminum (Al) Contaminants	0.4	N/A

Note 1. A maximum copper limit of 1.0% may be specified AABUS. Printed boards that are characterized as thick and thermally demanding may have potential PTH fill and/or solder joint defects due to the impact of copper on solder flow characteristics.

3.2.7.3.1 Eutectic Tin-Lead Solder Coating The solder used for conventional, Pb-bearing coatings **shall** be in accordance with the requirements of 3.2.7.3. SnPb solder **shall** conform to the contaminant level specified in Table 3-2.

3.2.7.3.2 Pb-Free Solder Coating The solder used for Pb-free solder coating **shall** be in accordance with the requirements of 3.2.7.3. The Pb-free solder bath **shall** conform to the contaminant level specified in Table 3-2. Use of other Pb-free solder alloy contamination limits **shall** be AABUS.

3.2.7.4 Electrodeposited Nickel Nickel plating thickness **shall** be as specified in Table 3-3 (Code N). When used as an undercoat or barrier layer for gold or other metals, the thicknesses **shall** be as specified in Table 3-3 (Code NB).

3.2.7.5 Electrodeposited Gold Electrodeposited gold plating **shall** be in accordance with ASTM-B-488. Purity and hardness **shall** be specified in the procurement documentation. The thickness **shall** be as specified in Table 3-3 (Code G, GS, GWB-1 and GWB-2).

For Reference Only: Industry investigations have shown that a gold-tin intermetallic phase forms under normal soldering process parameters. Prevention of detrimental gold embrittlement of solder joints is possible, provided there is enough solder volume present to allow dissolution of the gold so that the overall weight percentage of gold in the solder joint is below the 3-4% range.

3.2.7.6 Electroless Nickel Immersion Gold (ENIG) ENIG plating deposit **shall** be in accordance with IPC-4552. Deposit thickness, XRF measurement methodology and frequency of sample thickness measurements per panel **shall** be In Accordance With (IAW) IPC-4552 on appropriately sized pads (See the IPC-2221 Appendix A “W” coupon). The number of panels per lot to be measured **shall** be in accordance with Table 4-3 for plating/coating thickness.

3.2.7.7 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) ENEPIG plating deposit **shall** be in accordance with IPC-4556. Deposit thickness, XRF measurement methodology and frequency of sample thickness measurements per panel **shall** be IAW IPC-4556 on appropriately sized pads (See the IPC-2221 Appendix A “W” coupon). The number of panels per lot to be measured **shall** be in accordance with Table 4-3 for plating/coating thickness.

3.2.7.8 Immersion Silver (IAG) Immersion silver plating deposit **shall** be in accordance with IPC-4553. Deposit thickness and XRF measurement methodology per panel **shall** be IAW IPC-4553 on appropriately sized pads (See the IPC-2221 Appendix A “W” coupon). The number of panels per lot to be measured **shall** be IAW Table 4-3 for plating/coating thickness. Frequency of sample thickness measurements per panel **shall** be sufficient to render a statistically valid standard deviation for the lot.

3.2.7.9 Immersion Tin (ISn) Immersion tin plating deposit **shall** be in accordance with IPC-4554. Deposit thickness and XRF measurement methodology per panel **shall** be IAW IPC-4554 on appropriately sized pads (See the IPC-2221 Appendix A “W” coupon). The number of panels per lot to be measured **shall** be in accordance with Table 4-3 for plating/coating thickness. Frequency of sample thickness measurements per panel **shall** be sufficient to render a statistically valid standard deviation for the lot.

3.2.7.10 Organic Solderability Preservative (OSP) OSP deposit **shall** be in accordance with IPC-4555. OSPs are anti-tarnish and solderability protectors applied to copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating storage, pre-assembly baking and sequential soldering processes impact solderability. Coating requirements for standard (Code OSP) and high-temperature (Code HT OSP) OSP formulations are in Table 3-3.

3.2.7.11 Other Metals and Coatings The allowance of and the requirements for use of other depositions as a surface finish per 1.3.4.3 such as bare copper, palladium and rhodium **shall** be AABUS.

Table 3-3 Final Finish, Plating and Coating Requirements

Code	Final Finish/Plating/Coating	Thickness	Applicable Acceptability Specification	Marking Code ¹
S	Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-003	b0
b1	Pb-Free Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-003	b1
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable ²	J-STD-003	b0
X	Either Type S or T	b0		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	ASTM B-579	b0
G	Gold for edge printed board connectors and areas not to be soldered - minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	ASTM-B-488	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered –maximum ³	0.45 µm [17.72 µin]	ASTM-B-488 J-STD-003	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) – minimum	0.05 µm [1.97 µin]	ASTM-B-488	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3.0 µm [118 µin]	None	b4
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	Class 1 and Class 2 0.3 µm [11.8 µin]	ASTM-B-488	b4
		Class 3 0.8 µm [31.5 µin]		
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3.0 µm [118 µin]	None	b4
N	Nickel - Electroplate for edge printed board connectors - minimum	Class 1 2.0 µm [78.7 µin]	None	N/A
		Class 2 and Class 3 2.5 µm [98.4 µin]		
NB	Nickel-Electroplate as a barrier ⁴ - minimum	1.3 µm [51.2 µin]	None	N/A
OSP	Organic Solderability Preservative	Solderable ⁶	J-STD-003	b6
HT OSP	High Temperature Organic Solderability Preservative	Solderable ⁶	IPC-4555 J-STD-003	b6
ENIG ⁵	Electroless Nickel	IPC-4552 J-STD-003		b4
	Immersion Gold			b4