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Qualification and Performance Specification for Flexible/Rigid-Flexible Printed Boards

*Supersedes IPC-6013D Amendment 1
April 2018*

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IPC-6013E

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Developed by the Flexible Circuits Specifications Subcommittee
(D-12) of the Flexible Circuits Committee (D-10) of IPC

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Users of this publication are encouraged to participate in the
development of future revisions.

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Qualification and Performance Specification for Flexible/Rigid-Flexible Printed Boards

1 SCOPE

1.1 Statement of Scope This specification covers qualification and performance requirements of flexible printed boards. The flexible printed board may be single-sided, double-sided, multilayer, or rigid-flex multilayer. All of these constructions may or may not include stiffeners, plated-through holes (PTHs), and blind/buried vias.

The flexible or rigid-flex printed board may contain build up High Density Interconnect (HDI) layers. The printed board may contain embedded active or passive circuitry with distributive capacitive planes, capacitive or resistive components conforming to IPC-6017.

The rigid section of the printed board may contain a metal core or external metal heat frame, which may be active or nonactive. Revision level changes are described in 1.7.

1.2 Purpose The purpose of this specification is to provide requirements for qualification and performance of flexible printed boards designed to IPC-2221 and IPC-2223.

1.3 Performance Classification, Board Type, and Installation Usage

1.3.1 Classification This specification recognizes that flexible printed boards will be subject to variations in performance requirements based on end-use. These performance classes (Class 1, Class 2, and Class 3) are defined in IPC-6011.

1.3.2 Printed Board Type Performance requirements are established for the different types of flexible printed boards, classified as follows:

Type 1 - Single-sided flexible printed boards containing one conductive layer, with or without stiffeners.

Type 2 - Double-sided flexible printed boards containing two conductive layers with PTHs, with or without stiffeners.

Type 3 - Multilayer flexible printed boards containing three or more conductive layers with PTHs, with or without stiffeners.

Type 4 - Multilayer rigid and flexible material combinations containing three or more conductive layers with PTHs.

Type 5 - Flexible or rigid-flex printed boards containing two or more conductive layers without PTHs.

1.3.3 Installation Uses

Use A - Capable of withstanding flex during installation.

Use B - Capable of withstanding continuous flexing for the number of cycles as specified on the procurement documentation.

Use C - High temperature environment (over 105 °C [221 °F]).

Use D - UL Recognition. See UL 94 and UL 796F.

1.3.4 Selection for Procurement For procurement purposes, performance class and installation usage **shall** be specified in the procurement documentation.

The documentation **shall** provide sufficient information to the supplier so that the supplier can fabricate the flexible printed boards and ensure that the user receives the desired product. Information that should be included in the procurement documentation is to be in accordance with IPC-2611 and IPC-2614.

Note: If the drawing specifies the requirement in words, designators are not required.

The procurement documentation **shall** specify the thermal stress test method and the number of cycles (in relation to reflow profiles in IPC-TM-650, Method 2.6.27) to be used to meet the requirement of 3.6.1. Selection **shall** be from those depicted in 3.6.1.1, 3.6.1.2, 3.6.1.3 and 3.6.1.4. If not specified (see 5.1), the default **shall** be per Table 1-1.

During the selection process, the user should take into consideration the following when determining the appropriate thermal stress test method:

- Wave solder, selective solder, hand solder assembly processes (see 3.6.1.1)
- Conventional SnPb reflow processes (see 3.6.1.2)
- Lead-free reflow processes (see 3.6.1.3 and 3.6.1.4)

IPC-6016, a sectional performance specification for HDI printed boards, was canceled by the IPC. Relevant HDI conformance and acceptance criteria has been transferred to this revision of this specification.

The addition of IPC-2221 Appendix A conformance coupons (beginning with Revision B of the design standard) by the printed board manufacturer to the manufacturing panel **shall** be AABUS.

1.3.4.1 Selection (Default) The procurement documentation **shall** specify those requirements that are a result of the selection process within this specification. This includes all references to “AABUS”. If the requirement selection is not made in accordance with the procurement documentation, Ordering Data (see 5.1), Customer Drawing and/or supplier control plan (SCP), then the default requirements in Table 1-1 **shall** apply.

Table 1-1 Default Requirements

Category	Default Selection
Performance Class	Class 2
Installation Usage	Use A
Material	Fabricator defined
Final Finish	Finish X (Electrodeposited tin lead, fused or solder coated) or alternate Finish ENIG allowed on designs (drawings) with Initial Release on or after January 01, 2021.
Minimum Starting Foil	1/2 oz. for all internal and external layers. For plated HDI layers – ¼ oz. for all layers (internal or external)
Copper Foil Type	Fabricator defined
Plated Component Hole Diameter Tolerance	(±) 100 µm [3,937 µin]
Plated Via Hole Diameter Tolerance	(+) 80 µm [3,150 µin], (-) no requirement, (may be totally or partially plugged)
Non-plated Hole Diameter Tolerance	(±) 80 µm [3,150 µin]
Conductor Width tolerance	Class 2 requirements per para. 3.5.1
Conductor Spacing tolerance	Class 2 requirements per para. 3.5.2
Dielectric Separation	Minimum rigid dielectric spacing shall be 90 µm [3,543 µin]. Minimum flexible dielectric spacing shall be within 20% of the selected thickness
Lateral Conductor Spacing	100 µm [3,937 µin] minimum
Marking Ink	Contrasting color, nonconductive
Solder Mask	Not applied, if not specified
Solder Mask, specified	Class T of IPC-SM-840 if class not specified
Solderability Test	Per 3.3.6, Category 2 for SnPb and Category A for Pb-free of J-STD-003
Test Voltage, Isolation Resistance	Per IPC-9252
Qualification not specified	See IPC-6011
Profile tolerance	0.5 mm [0.0197 in] for all external edges
Thermal Stress Test	IPC-TM-650, Method 2.6.8, Condition A or, if utilizing polyester flexible material, Condition C per 3.6.1

1.3.5 Material, Plating Process and Final Finish

1.3.5.1 Laminate Material Laminate material is identified by numbers and/or letters, classes and types as specified by the appropriate specification listed in the procurement documentation.

1.3.5.2 Plating Process The copper plating process used to provide the main conductor in the holes is identified by a single number as follows:

- 1) Acid copper electroplating only
- 2) Pyrophosphate copper electroplating only
- 3) Acid and/or pyrophosphate copper electroplating

- 4) Additive/electroless copper
- 5) Electrodeposited Nickel underplate with copper electroplating

Note: Pyrophosphate copper electroplating is no longer in use.

1.3.5.3 Final Finish and Coatings The final finish/coating can be one of the finishes/coatings specified below or a combination of several platings and is dependent on assembly processes and end-use. If required, the thickness **shall** be specified in the procurement documentation. If not specified, the thickness **shall** be as listed in Table 3-2. Coating thickness may be exempted in Table 3-2 (i.e., tin-lead plate or solder coating). Designators for final finish are as follows:

S	Solder Coating	(Table 3-2)
T	Electrodeposited Tin-Lead, (fused)	(Table 3-2)
X	Either Type S or T	(Table 3-2)
TLU	Electrodeposited Tin-Lead (unfused)	(Table 3-2)
b1	Lead-free Solder Coating	(Table 3-2)
G	Gold Electroplate for Edge Printed Board Connectors	(Table 3-2)
GS	Gold Electroplate for Areas to be Soldered	(Table 3-2)
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic)	(Table 3-2)
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic)	(Table 3-2)
N	Nickel for Edge Printed Board Connectors	(Table 3-2)
NB	Nickel as a Barrier to Copper-Tin Diffusion	(Table 3-2)
OSP	Organic Solderability Preservative	(Table 3-2)
HT OSP	High Temperature OSP	(Table 3-2)
ENIG	Electroless Nickel Immersion Gold	(Table 3-2)
ENEPIG	Electroless Nickel/Electroless Palladium/Immersion Gold	(Table 3-2)
DIG	Direct Immersion Gold	(Table 3-2)
NBEG	Nickel Barrier/Electroless Gold	(Table 3-2)
IAg	Immersion Silver	(Table 3-2)
ISn	Immersion Tin	(Table 3-2)
C	Bare Copper	(Table 3-2)
SMOBC	Solder Mask over Bare Copper	(3.2.8)
SM	Solder Mask over Non-Melting Metal	(3.2.8)
SM-LPI	Liquid Photoimageable Solder Mask over Non-Melting Metal	(3.2.8)
SM-DF	Dry Film Solder Mask over Non-Melting Metal	(3.2.8)
SM-TM	Thermal Mask Solder Mask over Non-Melting Metal	(3.2.8)
Y	Other	(3.2.7.11)

1.4 Terms and Definitions The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined in 1.4.1 through 1.4.8.

1.4.1 As Agreed Upon Between User and Supplier (AABUS) Indicates additional or alternate requirements to be decided between the user and the supplier in the procurement documentation. Examples include contractual requirements, modifications to purchase documentation and information on the drawing. Agreements can be used to define test methods, conditions, frequencies, categories or acceptance criteria within a test, if not already established.

1.4.2 Button Plating A selective plating technique in which copper is plated only in the hole barrel and a portion of the outer layer pads. This method is utilized to avoid or minimize additional plating on the outer layer of flex circuitry to control thickness and/or increase flexibility.

1.4.3 Cover Material A thin dielectric material used to encapsulate circuitry, most commonly for flexible circuit applications.

1.4.3.1 Covercoat Material deposited as a liquid onto the circuitry that subsequently becomes a permanent dielectric coating.

Note: Covercoats may have reduced performance in tight bend radius applications.

1.4.3.2 Coverfilm Film made from

- i) a homogeneous, single component
- ii) separate layers of generically similar chemistries; or
- iii) as a composite blend

1.4.3.3 Coverlay Film and adhesive made from separate layers of generically different chemistries.

1.4.4 Target Land (Via Bottom Land) The internal land portion during formation of a blind or buried microvia.

1.4.5 Capture Land (Via Top Land) The external land portion during formation of a blind or buried microvia.

1.4.6 Microvia A blind structure (as plated) with a maximum aspect ratio of 1:1 when measured in accordance with Figure 1-1, terminating on or penetrating a target land, with a total length of no more than 0.25 mm [0.0098 in] measured from the structure's capture land foil to the target land.

1.4.7 Core A single-sided, double-sided or multilayer board or flex circuit that is used as a carrier for HDI layers and meets the requirements of one of the following performance specifications: IPC-6012, IPC-6013, IPC-6015 or IPC-6018.

1.4.8 Design Data Data which is communicated to a printed circuit board fabricator and may include mechanical information, electrical design information and requirements concerning end item performance, item end-use environment, item configuration, materials, components, and processes.

1.5 Interpretation “**Shall**,” the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a “**shall**” requirement may be considered if sufficient data is supplied to justify the exception.

The words “should” and “may” are used whenever it is necessary to express nonmandatory provisions.

“Will” is used to express a declaration of purpose. To assist the reader, the word “**shall**” is presented in bold characters.

The examples shown in the photographs and/or illustrations in this specification are sometimes exaggerated to make the referenced imperfection more apparent. The relationship between the text and the examples is not always parallel; it would be difficult to find many cases so specific that they would always match the acceptance criteria. When photographs or illustrations contained in this standard are not consistent with discussion in the written text, the written text takes precedence and **shall** be followed.

1.6 Presentation All dimensions and tolerances in this specification are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this specification are expected to use metric dimensions. All dimensions greater than or equal to 1.0 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions less than 1.0 mm [0.0394 in] will be expressed in micrometers and microinches.

1.7 Design Data Protection Design data is property owned by an organization or business entity. When design data is known to or in the custody of the printed board fabricator or their agents, it **shall** be protected as-specified by the procurement documentation.

If not specified in procurement documentation, the printed board fabricator **shall** nonetheless have internal policies and procedures for protection of the design data.

An optional protocol is defined in 3.10.17.

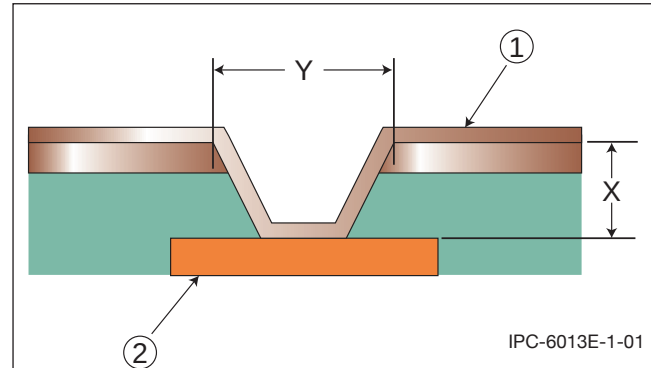


Figure 1-1 Microvia Definition

Note 1. Capture Land.

Note 2. Target Land.

Note 3: X/Y = Microvia Plating Aspect Ratio, with $X < 0.25$ mm [0.0098 in] and aspect ratio $< 1:1$.

1.8 Revision Level Changes Changes made to this revision of the IPC-6013 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the Figure or Table header.

2 APPLICABLE DOCUMENTS

The following specifications form a part of this specification to the extent specified herein. If a conflict of requirements exists between IPC-6013 and the listed applicable documents, IPC-6013, with the exception of IPC-6011, **shall** take precedence.

2.1 IPC¹

IPC-WP-023 IPC Technology Solutions White Paper on Performance-Based Printed Board OEM Acceptance: Via Chain Continuity Reflow Test: The Hidden Reliability Threat

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-CF-152 Composite Metallic Materials Specification for Printed Wiring Boards

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650 Test Methods Manual²

2.1.1 Microsectioning, Manual and Semi or Automatic

2.3.15 Purity, Copper Foil or Plating

2.4.1 Adhesion, Tape Testing

2.4.2.1 Flexural Fatigue and Ductility, Foil

2.4.3 Flexural Fatigue, Flexible Printed Wiring Materials

2.4.18.1 Tensile Strength and Elongation, In-House Plating

2.4.21 Land Bond Strength, Unsupported Component Hole

2.4.22 Bow and Twist

2.4.28.1 Adhesion, Solder Resist (Mask) Tape Test Method

2.4.36 Rework Simulation, Plated-Through Holes for Leaded Components

2.4.41.2 Coefficient of Thermal Expansion - Strain Gage Method

2.5.7 Dielectric Withstand Voltage, PWB

2.5.5.7 Characteristic Impedance and Time Delay of Lines on Printed Boards by TDR

2.6.1 Fungus Resistance Printed Wiring Materials

2.6.3 Moisture and Insulation Resistance, Printed Boards

2.6.4 Outgassing, Printed Boards

2.6.7.2 Thermal Shock and Continuity, Printed Boards

2.6.8 Thermal Stress, Plated-Through Holes

2.6.25 Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Test)

2.6.27 Thermal Stress, Convection Reflow Assembly Simulation

IPC-QL-653 Qualification of Facilities that Inspect/Test Printed Boards, Components and Materials

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-1791 Trusted Electronic Designer, Manufacturer and Assembler Requirements

IPC-2221 Generic Standard on Printed Boards Design

IPC-2223 Sectional Design Standard for Flexible Printed Boards

IPC-2251 Design Guide for the Packaging of High Speed Electronic Circuits

IPC-2611 Generic Requirements for Electronic Product Documentation

IPC-2614 Sectional Requirements for Board Fabrication Documentation

1. www.ipc.org

2. Current and revised IPC Test Methods are available through the IPC Web site (www.ipc.org/test-methods).

- IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards
- IPC-4103** Specification for Base Materials for High Speed/High Frequency Applications
- IPC-4202** Flexible Bare Dielectrics for use in Flexible Printed Wiring
- IPC-4203** Adhesive Coated Dielectric Films for Use in Fabrication of Flexible Printed Wiring
- IPC-4204** Metal-Clad Flexible Dielectrics for Use in Fabrication of Flexible Printed Wiring
- IPC-4552** Electroless Nickel/Immersion Gold Plating for Electronic Interconnections
- IPC-4553** Specification for Immersion Silver Plating for Printed Circuit Boards
- IPC-4554** Specification for Immersion Tin Plating for Printed Circuit Boards
- IPC-4556** Specification for Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards
- IPC-4562** Copper Foil for Printed Wiring Applications
- IPC-4563** Resin Coated Copper Foil for Printed Boards Guideline
- IPC-4761** Design Guide for Protection of Printed Board Via Structures
- IPC-4781** Qualification and Performance Specification of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks
- IPC-4811** Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards
- IPC-4821** Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards
- IPC-6011** Generic Performance Specification for Printed Boards
- IPC-6017** Qualification and Performance Specification for Printed Boards Containing Embedded Passive Devices
- IPC-7711/21** Rework, Modification and Repair of Electronic Assemblies
- IPC-9241** Guidelines for Microsection Preparation
- IPC-9252** Requirements for Electrical Testing of Unpopulated Printed Boards
- IPC-9691** User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing)

2.2 Joint Industry Standards³

- J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies
- J-STD-003** Solderability Tests for Printed Boards
- J-STD-006** Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications
- J-STD-609** Marking and Labeling of Components, PCBs and PCBA's to Identify Lead (Pb), Pb-Free and Other Attributes
- JP002** Current Tin Whiskers Theory and Mitigation Practices Guideline

2.3 Other Publications

2.3.1 American Society for Testing and Materials⁴

- ASTM B 488** Standard Specification for Electrodeposited Coatings of Gold for Engineering Uses
- ASTM B 579** Standard Specification for Electrodeposited Coatings of Tin-Lead Alloy

2.3.2 Underwriters Lab⁵

- UL 94** Tests for Flammability of Plastic Materials for Parts in Devices and Appliances
- UL 796F** Flexible Materials Interconnect Constructions

2.3.3 National Electrical Manufacturers Association⁶

- NEMA LI-1** Industrial Laminate Thermosetting Product

3. www.ipc.org

4. www.astm.org

5. www.ul.com

6. www.nema.org

2.3.4 American Society for Quality ⁷

H1331 Zero Acceptance Number Sampling Plans

Z1.4 Sampling Procedures and Tables for Inspection by Attributes

2.3.5 AMS ⁸

SAE-AMS-QQ-A-250 Aluminum Alloy, Plate and Sheet

SAE-AMS-2451 Plating, Brush General Requirements

2.3.6 American Society of Mechanical Engineers ⁹

ASME B46.1 Surface Texture (Surface Roughness, Waviness and Lay)

2.3.7 Federal ¹⁰

QQ-S-635 Steel

3 REQUIREMENTS

3.1 General Flexible printed boards furnished under this specification **shall** meet or exceed the requirements of IPC-6011 and the specific performance class as required by the procurement documentation. Descriptions and purposes of test coupons are documented in IPC-2221 and its related appendices. Although conformance to the detailed requirements may be determined by examination of specific quality control coupons, these requirements apply to all coupons or sample flexible printed boards and to deliverable flexible printed boards. These requirements are also based on the assumption that the flexible printed board was designed to the appropriate IPC design standard.

3.2 Materials Used in this Specification All materials used in construction of the flexible printed board **shall** comply with applicable specifications and the procurement documentation. The user has the responsibility to specify on the procurement documentation materials capable of meeting the requirements of this specification and end item use.

Note: When possible, material call-out information should be reviewed with the supplier so as to obtain concurrence that the part will meet the requirements of this specification and, if necessary, to update the procurement documentation accordingly.

3.2.1 Laminates and Bonding Materials Metal-clad laminates, unclad laminates, and bonding material (prepreg) should be selected using IPC-4101, IPC-4103, IPC-4202, IPC-4203, IPC-4204, or NEMA LI 1-1989. Embedded device materials **shall** be selected from IPC-4811 or IPC-4821 and should be as specified in the procurement documentation including dielectric, conductive, resistive and insulating characteristics as applicable. The specification sheet number, metal cladding type and metal clad thickness (weight) should be as specified in the procurement documentation. When there are specific requirements, it is necessary to specify those requirements on the material procurement documentation.

3.2.1.1 Flexible Material Options At the supplier's option, flexible metal-clad dielectrics and adhesive coated dielectric films may be manufactured using individual components per IPC-4562, IPC-4202, and IPC-4203. In addition, materials per IPC-4204 may be substituted where individual components are specified.

3.2.2 External Bonding Materials The material used to adhere external heat sinks or stiffeners to the flexible printed board should be selected from IPC-4101, IPC-4202, IPC-4203, IPC-4204, or as specified on the procurement documentation.

3.2.3 Other Dielectric Materials Photoimageable dielectrics should be specified in the procurement documentation. Other dielectric materials may be specified on the procurement documentation.

3.2.4 Metal Foils Copper foil should be in accordance with IPC-4562. Foil type, foil grade, foil thickness, bond enhancement treatment, and foil profile should be specified on the master drawing if critical to the function of the flexible printed board. Resin coated copper foil **shall** be in accordance with IPC-4563.

7. www.asq.org

8. www.sae.org

9. www.asme.org

10. SAE.org

3.2.4.1 Resistive Metal Foil Resistive metal foil **shall** be specified in the procurement documentation.

3.2.5 Metal Planes/Cores Metal planes and/or metal core substrates **shall** be specified on the master drawing as shown in Table 3-1.

Table 3-1 Internal or External Metal Planes

Material	Specification	Alloy
Aluminum	SAE-AMS-QQ-A-250	As Specified
Steel	QQ-S-635	As Specified
Copper	ASTM-B-152 or IPC-4562	As Specified
Copper-Invar-Copper	IPC-CF-152	As Specified
Copper-Moly-Copper	IPC-CF-152	As Specified
Other	As Specified	As Specified

3.2.6 Base Metallic Plating Depositions and Conductive Coatings The thickness of the plating/final finish coatings **shall** be in accordance with Table 3-2. The copper plating thickness for the surface, PTHs, via holes, blind and buried vias **shall** be as specified in Table 3-3, Table 3-4, Table 3-5 and Table 3-6. The thickness for specific use platings **shall** be as specified in Table 3-2. The plating thickness for final finishes or combinations thereof selected from those listed in 1.3.4.3 **shall** be as specified in Table 3-2. Fused tin-lead plating or solder coating only requires visual coverage and acceptable solderability testing per J-STD-003. Coverage of platings and metallic coatings does not apply to vertical conductor edges. Conductor surfaces may have exposed copper in areas not to be soldered within the limits of 3.5.4.7.

3.2.6.1 Electroless Copper Depositions and Conductive Coatings Electroless depositions and conductive coatings **shall** be sufficient for subsequent plating processes and may be either electroless metal, vacuum deposited metal, or metallic or non-metallic conductive coatings.

3.2.6.2 Electrodeposited Copper Electrodeposited copper plating **shall** meet the following criteria. Frequency of testing **shall** be in accordance with Table 4-4.

- When tested in accordance with IPC-TM-650, Method 2.3.15, the purity of copper **shall** be no less than 99.50%.
- When tested in accordance with IPC-TM-650, Method 2.4.18.1, using 50 - 100 μm [1,969 - 3,937 μin] thick samples, the tensile strength **shall** be no less than 248 MPa [36,000 PSI] and the elongation **shall** be no less than 18%.

3.2.6.3 Fully Additive Electroless Copper Depositions Additive/electroless copper platings applied as the main conductor metal **shall** meet the requirements of this specification. Deviations **shall** be AABUS.

3.2.7 Final Finish Depositions and Coatings - Metallic and Non-Metallic

3.2.7.1 Electrodeposited Tin The allowance of and the requirements for use of electrodeposited tin **shall** be AABUS. It is recommended that the user refer to JEDEC/IPC JP002 for guidance on potential mitigation practices that may delay the onset of, or prevent, tin whisker formation.

3.2.7.2 Electrodeposited Tin-Lead Tin-lead plating **shall** meet the composition (50-70% tin) requirements of ASTM B-579. Fusing is required unless the unfused option is selected wherein the thickness specified in Table 3-2 (Code TLU) applies.

3.2.7.3 Hot Air Solder Leveling (HASL)/Solder Coating The solder coating **shall** be as specified on the master drawing and the procured solder used for coating **shall** meet the requirements of J-STD-006. HASL is the process for solder coating that involves dipping a printed board into solder and using hot air to level the resultant solder surface.

3.2.7.3.1 Eutectic Tin-Lead Solder Coating The solder used for conventional, lead-bearing coatings **shall** be in accordance with the requirements of 3.2.7.3, except the thickness **shall** be in accordance with Table 3-2 (Code S).

3.2.7.3.2 Lead-Free Solder Coating The solder used for lead-free solder coating **shall** be in accordance with the requirements of 3.2.7.3, except the thickness **shall** be in accordance with Table 3-2 (Code b1).

3.2.7.3.3 Deviations to these requirements **shall** be AABUS.

3.2.7.4 Electrodeposited Nickel Nickel plating thickness **shall** be as specified in Table 3-2 (Code N). When used as an undercoat or barrier layer for gold or other metals, the thicknesses **shall** be as specified in Table 3-2 (Code NB).

3.2.7.5 Electrodeposited Gold Electrodeposited gold plating **shall** be in accordance with ASTM-B-488. Purity and hardness **shall** be specified in the procurement documentation. The thickness **shall** be as specified in Table 3-2 (Code G, GS, GWB-1 and GWB-2).

For Reference Only: Industry investigations have shown that a gold-tin intermetallic phase forms under normal soldering process parameters. Prevention of detrimental gold embrittlement of solder joints is possible, provided there is enough solder volume present to allow dissolution of the gold so that the overall weight percentage of gold in the solder joint is below the 3-4% range.

3.2.7.6 Electroless Nickel Immersion Gold (ENIG) ENIG plating deposit **shall** be in accordance with IPC-4552. Deposit thickness **shall** be in accordance with IPC-4552 and as specified in Table 3-2 (Code ENIG). Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

The number of thickness measurements **shall** be in accordance with IPC-4552 or a minimum of 1 reading per side, per panel sampled, whichever is higher.

3.2.7.7 Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) ENEPIG plating deposit **shall** be in accordance with IPC-4556. Deposit thickness **shall** be in accordance with IPC-4556 and as specified in Table 3-2 (Code ENEPIG). Allowable thickness cited in Table 3-2 could skew to the lower or higher part of the range for optimum connector or solderable surface metallurgy. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

The number of thickness measurements **shall** be in accordance with IPC-4556 or a minimum of 1 reading per side, per panel sampled, whichever is higher.

3.2.7.8 Immersion Silver Immersion silver plating **shall** be in accordance with IPC-4553 (see Table 3-2 (code IAg)). Pad size for thickness measurements **shall** be in accordance with IPC-4553. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

The number of thickness measurements **shall** be in accordance with IPC-4553 or a minimum of 1 reading per side, per panel sampled, whichever is higher.

3.2.7.9 Immersion Tin Immersion tin plating deposit **shall** be in accordance with IPC-4554 (see Table 3-2 (code ISn)). Deposit thickness range **shall** be in accordance with IPC-4554. Frequency of sample thickness measurement for Class 1, Class 2 and Class 3 **shall** be in accordance with Table 4-3 for plating/coating thickness.

The number of thickness measurements **shall** be in accordance with IPC-4554 or a minimum of 1 reading per side, per panel sampled, whichever is higher.

3.2.7.10 Organic Solderability Preservative (OSP) OSPs are anti-tarnish and solderability protectors applied to copper to withstand storage and assembly processes in order to maintain solderability of surfaces. The coating storage, pre-assembly baking and sequential soldering processes impact solderability. Specific solderability shelf-life and soldering cycle requirements, if applicable, **shall** be specified in the procurement documentation. This applies to both standard and high-temperature OSP formulations. Coating requirements for standard (Code OSP) and high-temperature (Code HT OSP) OSP formulations are in Table 3-2.

3.2.7.11 Other Metals and Coatings The allowance of and the requirements for use of other depositions as a final finish per 1.3.5.3 such as bare copper, palladium and rhodium **shall** be AABUS.

Table 3-2 Final Finish, Plating and Coating Requirements

Code	Final Finish/Plating/Coating	Thickness	Applicable Acceptability Specification	Marking Code ¹
S	Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-003	b0
b1	Lead-Free Solder Coating over Bare Copper	Coverage & Solderable ²	J-STD-003	b1
T	Electrodeposited Tin-Lead (fused) - minimum	Coverage & Solderable ²	J-STD-003	b3
X	Either Type S or T	b0		
TLU	Electrodeposited Tin-Lead Unfused - minimum	8.0 µm [315 µin]	J-STD-003	b3
G	Gold for edge printed board connectors and areas not to be soldered - minimum	Class 1 and Class 2 0.8 µm [31.5 µin]	ASTM-B-488	b4
		Class 3 1.25 µm [49.21 µin]		
GS	Gold Electroplate on areas to be soldered –maximum ³	0.45 µm [17.72 µin]	ASTM-B-488 J-STD-003	b4
GWB-1	Gold Electroplate for areas to be wire bonded (ultrasonic) – minimum	0.05 µm [1.97 µin]	ASTM-B-488	b4
	Electrolytic nickel under gold for areas to be wire bonded (ultrasonic) - minimum	3.0 µm [118 µin]	None	b4
GWB-2	Gold Electroplate for areas to be wire bonded (thermosonic) - minimum	Class 1 and Class 2 0.3 µm [11.8 µin]	ASTM-B-488	b4
		Class 3 0.8 µm [31.5 µin]		
	Electrolytic nickel under gold for areas to be wire bonded (thermosonic) - minimum	3.0 µm [118 µin]	None	b4
N	Nickel - Electroplate for edge printed board connectors - minimum	Class 1 2.0 µm [78.7 µin]	None	N/A
		Class 2 and Class 3 2.5 µm [98.4 µin]		
NB	Nickel-Electroplate as a barrier ⁴ - minimum	1.3 µm [51.2 µin]	None	N/A
OSP	Organic Solderability Preservative	Solderable ⁶	J-STD-003	b6
HT OSP	High Temperature OSP	Solderable ⁶	J-STD-003	b6
ENIG ⁵	Electroless Nickel	IPC-4552 J-STD-003		b4
	Immersion Gold			b4
ENEPIG ⁵	Electroless Nickel	IPC-4556 J-STD-003		b4
	Electroless Palladium			N/A
	Immersion Gold			b4
DIG	Direct Immersion Gold (Solderable Surface)	Solderable ⁶	J-STD-003	b4
IAg	Immersion Silver	IPC-4553 J-STD-003		b2
ISn	Immersion Tin	IPC-4554 J-STD-003		b3
C	Bare Copper	AABUS	AABUS	N/A

Note 1. These marking and labeling codes represent the codes for surface finish categories established in IPC/JEDEC-J-STD-609.

Note 2. Hot Air Leveling (HAL) or Hot Air Solder Leveling (HASL) processes are considered to have a degree of difficulty in their control. This, coupled with pad sizes and geometries placing additional challenges on such processes, places the creation of a practical minimum thickness outside the scope of this specification. See also 3.3.6.

Note 3. See notation in 3.2.7.5.

Note 4. Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.

Note 5. For process control and qualification, surface measurements are evaluated to the applicable IPC-455X standard for coating thickness as measured on a nominal pad size of 1.5 x 1.5 mm [0.060 x 0.060 in] or equivalent area.

Note 6. See 3.3.6.

Table 3-3 Surface⁷ and Hole Copper Plating Minimum Requirements for Through-Holes^{1,2,3}

Copper – average		Class 1	Class 2	Class 3
	Type 2	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
	Type 3 and Type 4 except as noted below	25 µm [984 µin]	25 µm [984 µin]	25 µm [984 µin]
	Type 3 and Type 4 greater than 1.5 mm [0.059 in] thickness and has low T _g materials less than 110 °C in the areas of the board spanned by PTHs	35 µm [1378 µin]	35 µm [1378 µin]	35 µm [1378 µin]
Copper (Min. Thin Areas)				
	Type 2	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
	Type 3 and Type 4 except as noted below	20 µm [787 µin]	20 µm [787 µin]	20 µm [787 µin]
	Type 3 and Type 4 greater than 1.5 mm [0.059 in] thickness and has low T _g materials less than 110 °C in the areas of the board spanned by PTHs	30 µm [1181 µin]	30 µm [1181 µin]	30 µm [1181 µin]
	Minimum Wrap ⁴	AABUS	5 µm [197 µin]	12 µm [472 µin] ⁵
	Minimum Wrap ⁴	AABUS	5 µm [197 µin]	5 µm [197 µin] ⁶

Note 1. Does not apply to microvias (see 1.4.6).

Note 2. Copper plating (1.3.5.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces, except where selective (button) plating is allowed, the requirements of 3.6.2.16 apply. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. See 3.6.2.12.

Note 4. Wrap copper plating for filled PTHs and vias **shall** be in accordance with 3.6.2.12.1.

Note 5. Initial Release of designs (drawings) prior to June 30, 2018.

Note 6. Initial Release of designs (drawings) on or after July 01, 2018.

Note 7. The minimum average values specified here are used to calculate the minimum finished conductor thickness in Table 3-20.

Table 3-4 Hole Copper Plating Minimum Requirements for Buried Vias > 2 Layers, and Blind Vias¹

Copper – average ^{2,4}		Class 1	Class 2	Class 3
	Type 3 and Type 4 except as noted below	20 µm [787 µin]	20 µm [787 µin]	25 µm [984 µin]
	Type 3 and Type 4 greater than 1.5 mm [0.059 in] thickness and has low T _g materials less than 110 °C in the areas of the board spanned by PTHs	30 µm [1181 µin]	30 µm [1181 µin]	35 µm [1378 µin]
Thin areas ⁴				
	Type 3 and Type 4 except as noted below	18 µm [709 µin]	18 µm [709 µin]	20 µm [787 µin]
	Type 3 and Type 4 greater than 1.5 mm [0.059 in] thickness and has low T _g materials less than 110 °C in the areas of the board spanned by PTHs	28 µm [1102 µin]	28 µm [1102 µin]	30 µm [1181 µin]
Wrap ³		AABUS	5 µm [197 µin]	12 µm [472 µin] ⁵
Wrap ³		AABUS	5 µm [197 µin]	5 µm [197 µin] ⁶

Note 1. Does not apply to microvias (see 1.4.6).

Note 2. Copper plating (1.3.5.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for filled PTHs and vias **shall** be in accordance with 3.6.2.12.1. Alternatives to wrap plating **shall** be AABUS.

Note 4. See 3.6.2.12.

Note 5. Initial Release of designs (drawings) prior to June 30, 2018.

Note 6. Initial Release of designs (drawings) on or after July 01, 2018.

Table 3-5 Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)¹

	Class 1	Class 2	Class 3
Copper – average ^{2,4}	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas ⁴	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap ³	AABUS	5 µm [197 µin]	6 µm [236 µin] ⁵
Wrap ³	AABUS	5 µm [197 µin]	5 µm [197 µin] ⁶

Note 1. See 1.4.6 for definition of microvia.

Note 2. Copper plating (1.3.5.2) thickness **shall** be continuous and wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for filled microvias **shall** be in accordance with 3.6.2.12.1 or 3.6.2.12.3. Alternatives to wrap plating **shall** be AABUS.

Note 4. See 3.6.2.12.

Note 5. Initial Release of designs (drawings) prior to June 30, 2018.

Note 6. Initial Release of designs (drawings) on or after July 01, 2018.

Table 3-6 Hole Copper Plating Minimum Requirements for Buried via cores (2 layers)¹

	Class 1	Class 2	Class 3
Copper – average ^{2,4}	12 µm [472 µin]	12 µm [472 µin]	12 µm [472 µin]
Thin areas ⁴	10 µm [394 µin]	10 µm [394 µin]	10 µm [394 µin]
Wrap ³	AABUS	5 µm [197 µin]	7 µm [276 µin] ⁵
Wrap ³	AABUS	5 µm [197 µin]	5 µm [197 µin] ⁶

Note 1. For through vias in the buried core.

Note 2. Copper plating (1.3.5.2) thickness **shall** be continuous and extend or wrap from hole walls onto outer surfaces. Refer to IPC-A-600 for discussion on copper plating thickness for hole walls.

Note 3. Wrap copper plating for buried via cores **shall** be in accordance with 3.6.2.12.1 or 3.6.2.12.3. Alternatives to wrap plating **shall** be AABUS.

Note 4. See 3.6.2.12.

Note 5. Initial Release of designs (drawings) prior to June 30, 2018.

Note 6. Initial Release of designs (drawings) on or after July 01, 2018.

3.2.8 Polymer Coating (Solder Mask) When permanent solder mask coating is specified, it **shall** be a polymer coating conforming to IPC-SM-840.

3.2.9 Fusing Fluids and Fluxes The composition of the fusing fluids and fluxes used in solder coating applications **shall** be capable of cleaning and fusing the electrodeposited tin-lead plating and bare copper to allow for a smooth adherent coating. The fusing fluid **shall** act as a heat transfer and distribution medium to prevent damage to the bare laminate of the flexible printed board. The type and composition of the fusing fluid **shall** be optional to the flexible printed board manufacturer.

Note: Fusing fluid compatibility should be confirmed with end users' cleanliness requirements due to the diverse interactions experienced at assembly soldering.

3.2.10 Marking Inks Marking inks **shall** be permanent and should conform to IPC-4781 or be as specified in the procurement documentation. Marking inks **shall** be applied to either the flexible printed board or to a label applied to the flexible printed board. Marking inks and labels **shall** be capable of withstanding fluxes, cleaning solvents, soldering, and cleaning and coating processes encountered in later manufacturing processes.

3.2.11 Hole Fill Insulation Material Material used for hole fill for flexible printed boards **shall** be as specified on the procurement documentation.

3.2.12 Heatsink Planes, External Thickness and materials for construction of heatsink planes and insulation material **shall** be as specified in the procurement documentation.

3.2.13 Via Protection Materials used for a via protection method **shall** be as specified. Via protection types are described in IPC-4761.

3.2.14 Embedded Passive Materials Embedded passive materials are defined as materials and processes which add capacitive, resistive and/or inductive functionality within the printed board, and which may be used with conventional core materials for the manufacture of flexible printed boards. These include laminate materials, resistive metal foils, plated resistors, conductive pastes, protectant materials, etc. Embedded passive materials **shall** be selected from IPC-4811 or IPC-4821 or as specified in the procurement documentation.

3.3 Visual Examination Finished flexible printed boards **shall** be examined in accordance with the following procedure. They **shall** be of uniform quality and **shall** conform to 3.3.1 through 3.3.9.

Visual examination of microvia structures for applicable dimensional or workmanship attributes **shall** be conducted at 30X minimum.

Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx. 1.75X). For feature sizes less than or equal to 0.254 mm [0.010 in] in size, visual examination **shall** be conducted at 4 – 10X. If the acceptable condition of a suspected defect is not apparent, it should be verified at progressively higher magnifications (up to 40X) to confirm that it is a defect. Dimensional requirements such as spacing or conductor width measurements may require other magnifications and devices with reticles or scales in the instrument, which allow accurate measurements of the specified dimensions. Contract or specification may require other magnifications.

3.3.1 Profile Edges **shall** be clean cut and without metallic burrs. Nonmetallic burrs are acceptable as long as they are not loose and/or do not affect fit and function. Panels that are scored or routed with a breakaway tab **shall** meet the depanelization requirements of the assembled flexible printed board.

When edge spacing is designed in accordance with IPC-2223, the distance between the haloing penetration, any edge delamination or blister and the nearest conductive feature **shall** not be less than the minimum lateral conductor spacing, or 100 μm [3,937 μin] if not specified.

When edge spacing is not designed in accordance with IPC-2223, evaluations for nicks, crazing, delamination and haloing **shall** be AABUS.

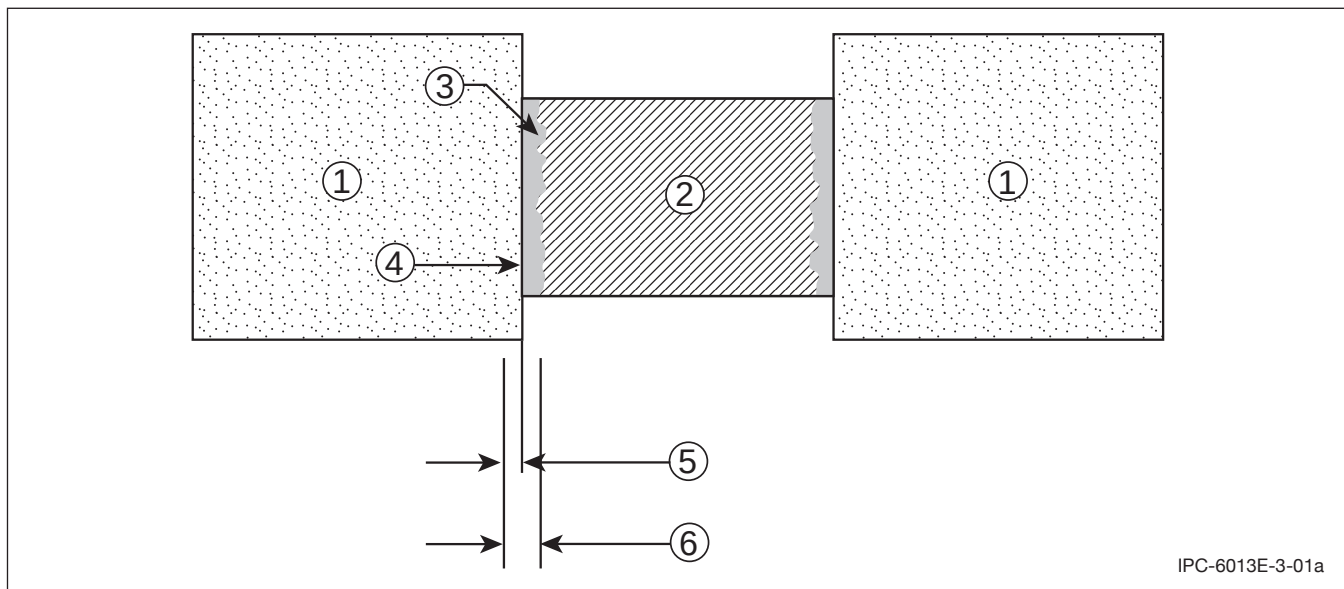
3.3.1.1 Edges, Rigid Section When edge spacing is designed in accordance with IPC-2223, nicks or crazing along the edge of the printed board, edge of cutouts and edges of non-plated holes are acceptable provided the penetration does not exceed 50% of the distance from the edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less.

3.3.1.2 Edges, Flexible Section (Excluding Stiffened Areas) Tears, cuts or nicks **shall** not be allowed within the flexible sections. When nicks and tears occur as a result of tie-in tabs to facilitate circuit removal, the extent of these imperfections **shall** be AABUS. Minimum edge to conductor spacing **shall** be as specified in the procurement documentation.

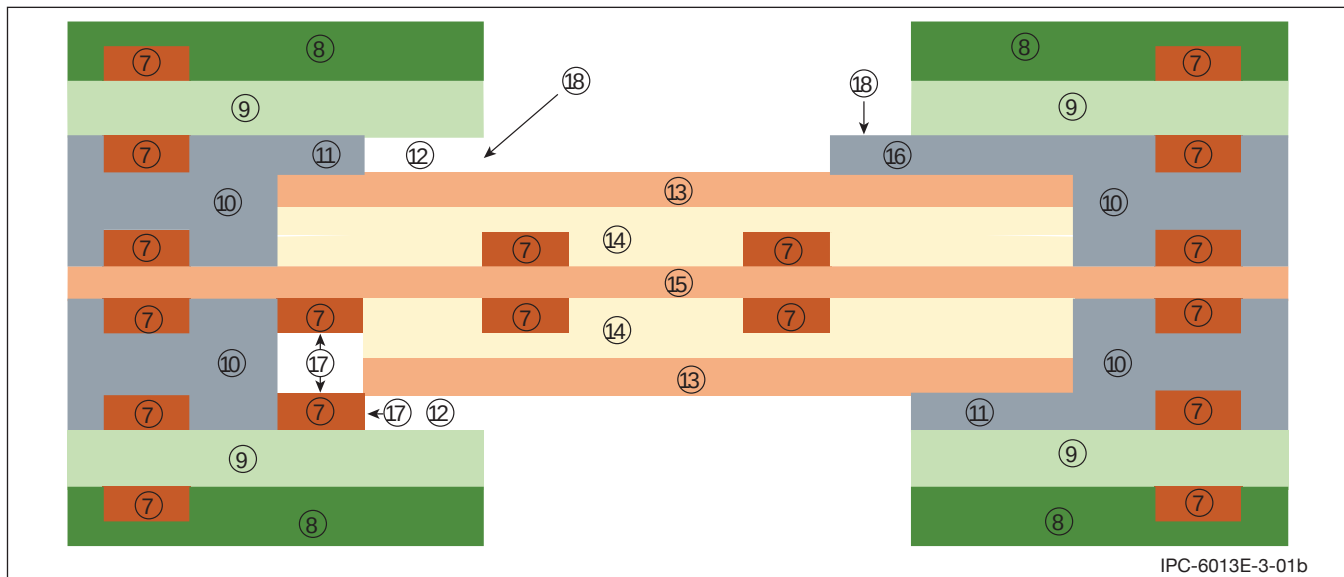
3.3.1.3 Transition Zone, Rigid Area to Flexible Area The transition zone is the area centered on the edge of the rigid portion from which the flex portion extends. The inspection range is limited to 3.0 mm [0.118 in], centered on the transition, which is the edge of the rigid portion (see Figure 3-1A). Visual imperfections inherent to the fabrication technique (i.e., adhesive squeeze-out, localized deformation of dielectric and conductors, protruding dielectric materials, crazing, or haloing) **shall** not be cause for rejection. A non-laminated gap due to material misalignment, prepreg cutback, etc. within the transition zone, which is not delamination, may recede into the rigid section up to 50% of the distance from the edge to the nearest conductor to a maximum of 1.5 mm [0.059 in], whichever is less. See Figure 3-1B for examples. Imperfections in excess of that allowed **shall** be AABUS, or as so stated on the procurement documentation.

Coverlay, bond ply or sheet adhesive penetration into the rigid zone is preferred to be at least 0.635 [0.025 in] but **shall** be sufficient to provide coverage of exposed conductors and **shall** not extend to the nearest via hole. Destructive Physical Analysis (DPA) requirements to validate observations **shall** be AABUS; evidence of coverlayer and prepreg overlap **shall** be present during a DPA evaluation.

3.3.1.4 Pouch materials In some board designs, manufacturers may need to use pouch material to protect internal layers in flex regions. Prior approval **shall** be obtained from the procuring activity for initial release of designs (drawings) on or after July 01, 2021. Pouch material may be evident in the transition zone. It is acceptable provided the overall thickness requirements of the rigid sections are not violated and does not extend beyond the flexible area of the transition zone requirements of 3.3.1.3.



IPC-6013E-3-01a

Figure 3-1A Transition Zone

IPC-6013E-3-01b

Figure 3-1B Transition Zone**Note 1.** Rigid Printed Board**Note 2.** Flex Circuit**Note 3.** Adhesive or Prepreg Flow**Note 4.** Potential Haloing of Rigid Printed Board along Edge is permitted in Transition Zone**Note 5.** 1.5 mm [0.059 in]**Note 6.** Limit of Inspection Range (3.0 mm [0.118 in]), centered on the Transition Zone.**Note 7.** Conductor.**Note 8.** Solder Mask.**Note 9.** Rigid Cap.**Note 10.** Prepreg.**Note 11.** Overlap.**Note 12.** Gap.**Note 13.** Polyimide Cover.**Note 14.** Cover Adhesive.**Note 15.** Polyimide Core.**Note 16.** Overlap with Squeeze-Out.**Note 17.** Nonconforming Exposed Conductor Due to Lack of Dielectric Insulation.**Note 18.** Acceptable Conditions of Gap/Squeeze-out within Inspection Range described in Note 6.

3.3.2 Construction Imperfections Imperfections include those characteristics that are both internal and external within the printed board but are visible from the surface.

3.3.2.1 Measling Measling is acceptable for Class 1, Class 2 and Class 3 end product. Measled areas in laminate substrates exceeding 50% of the spacing between non-common conductors are a process indicator for Class 3 end product, indicating a variation in material, equipment operation, workmanship or process that is not a defect. Although process indicators should be monitored as part of the process control system, disposition of individual process indicators is not required and affected product should be used as is.

Note: Measling is an internal condition which does not propagate under thermal stress and has not been conclusively shown to be a catalyst for CAF growth. Delamination is an internal condition which may propagate under thermal stress and may be a catalyst for CAF growth. The IPC-9691 uses guide for CAF resistance testing and IPC-TM-650, Method 2.6.25, provide additional information for determining laminate performance regarding CAF growth. Users who wish to incorporate additional criteria for measles conditions may consider incorporating the provisions of IPC-6012ES Space and Military Avionics Addendum which does not allow measles.

3.3.2.2 Cracking Cracking is acceptable for all classes of end product provided the imperfection does not reduce the conductor spacing below the minimum and there is no propagation of the imperfection as a result of thermal testing that replicates the manufacturing process. For Class 2 and Class 3, the distance of cracking **shall** not span more than 50% of the distance between adjacent conductors.

3.3.2.3 Delamination/Blister Delamination and blistering is acceptable for all classes of end product provided the area affected by imperfections does not exceed 1% of the printed board area on each side and does not reduce the spacing between conductive patterns below the minimum conductor spacing. There **shall** be no propagation of imperfections as a result of thermal testing that replicates the manufacturing process. For Class 2 and Class 3, the blister or delamination **shall** not span more than 25% of the distance between adjacent conductive patterns. Refer to IPC-A-600 for more information.

3.3.2.4 Entrapped Particles The following sections address particles entrapped on the external surface of the printed board or within the printed board.

3.3.2.4.1 Foreign Inclusions Translucent particles **shall** be acceptable. Other particles trapped within the printed board **shall** be acceptable, provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in 3.5.2.

3.3.2.4.2 Foreign Inclusions Between Flexible Printed Board and Stiffener Opaque foreign material determined to be located between the flexible printed board and stiffener **shall** be acceptable provided the bulge or height of opaque foreign material is no larger than 100 μm [3,940 μin]. It **shall** not be larger than 5% of the bonding area of the stiffener. There **shall** be no contact with a component hole or printed board outline. No threadlike foreign material may protrude from the outline edge greater than 1.0 mm [0.040 in]. Opaque foreign material **shall** not reduce the spacing between adjacent access openings below the minimum spacing specified in 3.5.2.

3.3.2.4.3 External Prepreg Resin Deposit Prepreg resin in Type 4 printed boards that comes loose from the uncured laminate sheet and bonds to the external coverlay material **shall** be acceptable.

3.3.2.5 Weave Exposure There **shall** be no weave exposure on the printed board for Class 3. Weave exposure or exposed/disrupted fibers are acceptable for Class 2 and Class 1 provided the imperfection does not reduce the remaining conductor spacing (excluding the area(s) with weave exposure) below the minimum. Refer to IPC-A-600 for more information.

3.3.2.6 Mechanically Induced Disrupted Fibers Exposure of disrupted fibers due to mechanical damage are acceptable for all Classes provided the imperfection does not bridge conductors and does not reduce the remaining lateral conductor spacing below the minimum.

3.3.2.7 Scratches, Dents, and Tool Marks Scratches, dents, and tool marks are acceptable, provided they do not expose conductors or disrupt fibers greater than allowed in 3.3.2.4 and 3.3.2.5 and do not reduce the dielectric spacing below the minimum specified. Dents or tool marks that cause delamination, changes in physical size of the conductor, or reduces conductor width or spacing **shall** be rejectable.

3.3.2.8 Surface Microvoids Surface voids are acceptable provided they do not exceed 0.8 mm [0.031 in] in the longest dimension; bridge conductors; nor can the voids exceed 5% of the total flexible printed board area per side.

3.3.2.9 Color Variations in Bond Enhancement Treatment Mottled appearance or color variation in bond enhancement treatment is acceptable. Random missing areas of treatment **shall** not exceed 10% of the total conductor surface area of the affected layer.

3.3.2.10 Pink Ring There is no existing evidence that pink ring affects functionality. The presence of pink ring may be considered an indicator of process or design variation but is not a cause for rejection. The focus of concern should be the quality of the lamination bond.

3.3.2.11 Deformation Anomalies Coverlay and coverfilm **shall** be continuous with no cracks in the film. Anomalies such as wrinkles and creases **shall** be evaluated for separation and **shall** meet the requirements of 3.6, provided such imperfections do not violate conductor spacing of 3.5.2 nor any of the following subsections. Each separation **shall** be no larger than 0.64 square mm [0.001 square in] and **shall** maintain the coverfilm seal with 0.127 mm [0.005 in] to the board edge or the coverfilm opening. Total separations in aggregate **shall** not exceed 1% of the printed board area on each side. Soda strawing **shall** be evaluated in accordance with 3.3.2.11.4.

DPA may be required to validate observations and methods **shall** be AABUS.

3.3.2.11.1 Wrinkles A ridge or ripple in the coverlay or coverfilm, having a ratio of height to width less than or equal to 1:1, that is formed during or after the material has adhered to the substrate. The presence of wrinkles may be considered an indicator of process or design variation but is not a cause for rejection if there is no evidence of separation or delamination in excess of the delamination requirements in 3.3.2.3.

3.3.2.11.2 Coverlay and Coverfilm Creases A permanent deformation only in the coverlay or coverfilm, having a ratio of height to width greater than 1:1, that is caused by a fold produced under pressure. The presence of creases may be considered an indicator of process or design variation but is not a cause for rejection if there is no evidence of separation or delamination in excess of the delamination requirements in 3.3.2.3.

3.3.2.11.3 Circuit Creases A permanent deformation in the conductors that may or may not include the cover material. Visually discernible cracks in the conductor **shall** be cause for rejection. Other deformations **shall** be evaluated AABUS.

3.3.2.11.4 Soda Strawing A long tubular-like void along the edges of conductive patterns where the coverlay or coverfilm is not bonded to the base material surface or the edge of the conductor. The presence of soda strawing may be considered an indicator of process or design limitations but is not a cause for rejection if there is no evidence of separation in excess of the delamination requirements in 3.3.2.3.

3.3.2.12 Cover Material Requirements

3.3.2.12.1 Cover Material Coverage Cover material **shall** be continuous with no cracks. Cover material coverage manufacturing variations resulting in skips, voids, and misregistration are subject to the following restrictions:

- Metal conductors shall not be exposed or bridged by blisters in areas where cover material is required. Touch up, if required to cover these areas with cover material, shall be of a material that is compatible and of equal resistance to soldering and cleaning as the originally applied cover material.
- In areas containing parallel conductors, cover material variations shall not expose adjacent conductors unless the area between the conductors is purposely left blank as for a test point or for some surface mount devices.
- Cover material need not be flush with the surface of the land. Misregistration of a cover material-defined feature **shall** not expose adjacent isolated lands or conductors (see Figure 3-2).
- Cover material is allowed on lands for PTHs to which solder connections are to be made, provided the external annular ring requirements for that class of products are not violated. Cover material **shall** not encroach upon the barrel of this type of PTH. Other surfaces, such as edge flexible printed board connector fingers and surface mount lands, **shall** be free of cover material, except as specified. Cover material is allowed in PTHs and vias into which no component lead is soldered, unless the procurement documentation requires that the holes be completely solder filled. Cover material may tent or plug via holes as specified by the procurement documentation. Lack of adhesive fill in tented vias **shall**

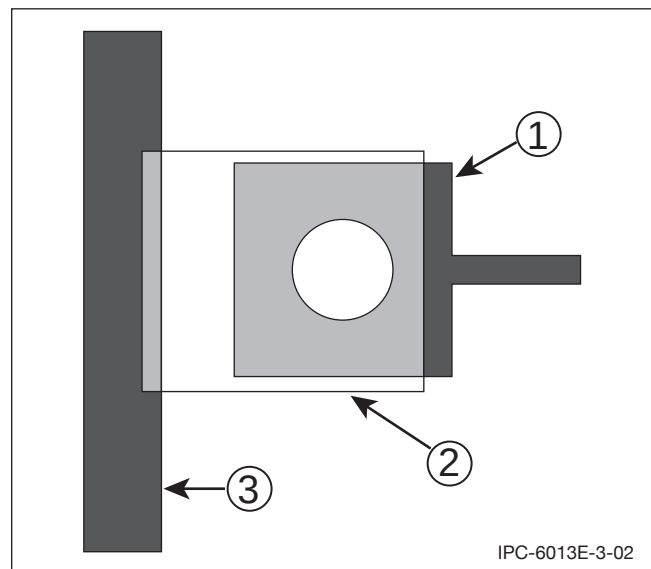


Figure 3-2 Unacceptable Cover Material Coverage

Note 1. Terminal Pad

Note 2. Cover Material Opening

Note 3. Conductor