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Design and Assembly Process Implementation of 3D Components

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of the Packaged Electronic Components Committee (B-10) of IPC

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Design and Assembly Process Implementation of 3D Components

1 SCOPE

This document describes the design and assembly challenges and ways to address those challenges for implementing 3D component technology. Recognizing the effects of combining multiple uncased semiconductor die elements in a single-package format can impact individual component characteristics and can dictate suitable assembly methodology. The information contained in this standard focuses on achieving optimum functionality, process assessment, end-product reliability and repair issues associated with 3D semiconductor package assembly and processing.

1.1 Purpose Performance-driven electronic systems continue to challenge companies in search of more innovative semiconductor package methodologies. The key market driver for semiconductor package technology is to provide greater functionality and improved performance without increasing package size. The package interposer is the key enabler. Although glass-reinforced epoxy-based materials and high-density Cu interconnect capability will continue to have a primary role for array-configured packaging, there is a trend toward alternative dielectric platforms as well as toward combining multiple functions within the same die element. To address this movement, an increasing number of semiconductor die developed for advanced applications now require higher I/O with contact pitch variations that are significantly smaller than the mainstream semiconductor products previously in the market. For these applications, companies are developing interposer technologies that can provide interconnect densities far superior to organic-based counterparts.

1.1.1 Target Audience The target audiences for this standard are managers, design/process engineers and operators who deal with:

- Implementing 3D semiconductor packaging
- Interposer, substrate and printed board design
- Board-level assembly, inspection and repair processes

1.1.2 Intent This standard intends to provide useful and practical information to those who are designing, developing or using 3D-packaged semiconductor components or those who are considering 3D package implementation. The 3D semiconductor package may include multiple die elements—some homogeneous and some heterogeneous. The package may also include several discrete passive SMT devices, some of which are surface mounted and some of which are integrated (embedded) within the components' substrate structure.

1.2 Classification IPC standards recognize that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in manufacturability, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between classes.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

1.3 Measurement Units All dimensions and tolerances in this specification are expressed in hard SI (metric) units and bracketed soft imperial [inch] units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions < 1 mm [0.0394 in] will be expressed in micrometers and microinches.

1.4 Use of "Lead" For readability and translation, this document uses the noun lead only to describe leads of a component. The metallic element lead is always written as Pb.

1.5 Abbreviations and Acronyms Periodic table elements are abbreviated in the standard. See Appendix A for full spellings of abbreviations (including elements) and acronyms used in this standard.

1.6 Terms and Definitions Other than those terms listed below, the definitions of terms used in this standard are in accordance with IPC-T-50.

1.6.1 Die* Separated piece(s) of a semiconductor wafer that constitutes a discrete semiconductor or integrated circuit (IC). They are normally uncased and leadless forms of an electronic component.

*singular or plural

1.6.2 Electronic Element A bare die/wafer or discrete component (resistor, capacitor, inductor, transistor, diode, fuse, etc.) with metallized terminals or terminations ready for mounting. The element can be an IC or a discrete electrical, optical or microelectronic mechanical system (MEMS) element. Individual elements cannot be further reduced without destroying their stated function.

1.6.3 Interposer A material placed between two surfaces to provide electrical insulation, redistribution of electrical connections, mechanical strength and/or controlled mechanical and thermal separation between the two surfaces.

1.6.4 Substrate The insulating material upon which a conductive pattern may be formed. (The base material may be rigid or flexible. It may be a dielectric or insulated metal sheet.) For this document, the term substrate refers to an interconnect platform fabricated from organic dielectric materials (rigid, flexible or a combination of rigid and flexible materials). Sometimes referred to as package substrate.

1.6.5 Electronic Package An individual electronic element or elements in a container that protect the contents to ensure integrity and provide terminals to interconnect the container to an outer circuit. Package outline is generally standardized or meets guideline documents. A package may function as electronic, optoelectronic or MEMS, and it may include bioelectronic elements (e.g., sensors).

1.6.6 Electronic Module A functional block that contains individual electronic elements and/or electronic packages to be used in a next-level assembly. An individual module may include an application-specific function or multiple electronic functions (e.g., optoelectronic, mechanical). The module typically provides protection of its elements and packages to ensure the required level of reliability.

1.6.7 Three-Dimensional (3D) Packaging Three-dimensional (3D) integration of heterogeneous elements, using traditional interconnection processes, to achieve vertically configured interconnections.

1.7 Implementation Challenges The next generation of 3D assembly has many implementation challenges, since the technology is complex and requires process expertise that may require foundries, outsourced semiconductor assembly and test (OSAT) providers and original design manufacturers (ODMs). There is no clear direction where 3D packages will be built, tested and assembled. The type of process to be used and the order of assembly and stacking is not defined and depends on the assembler's expertise.

Figure 1-1 illustrates the technological complexity of 3D assembly.

As mobile electronics markets continue to see significant growth, there will be an increasing demand for product miniaturization and higher product performance expectation. Developers of personal communication and computing products, for example, have already adopted multicore processors. Furthermore, these high-performance processors will require greater memory bandwidth. To meet these market trends, manufacturers are predicting faster process capability and anticipate reduced power requirements to extend battery life. Next-generation semiconductor package solutions also are projected to be physically robust. While materials for organic-substrate-based applications will meet most commercial applications, more severe operating environments may require a more robust (nonorganic) base substrate material.

Industry may continue to rely on organic-based platforms for a majority of semiconductor packaging applications. When

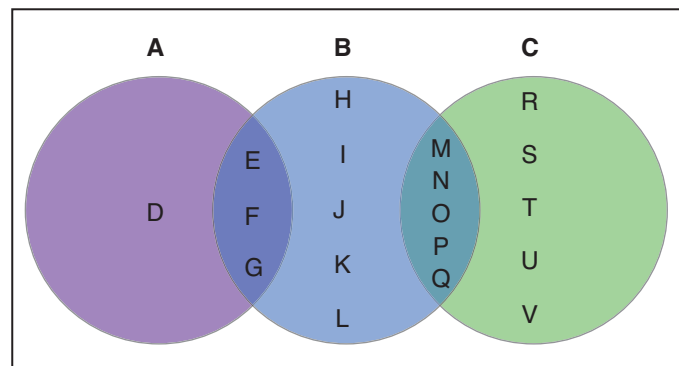


Figure 1-1 3D Technology Complexity

- A – Foundry
- B – Outsourced semiconductor assembly and test (OSAT)
- C – Original design manufacturer (ODM)
- D – Wafer process
- E – Wafer test known good die (KGD)
- F – Through-silicon via (TSV) interposer
- G – Micro bumping
- H – Package assembly
- I – Wire bond
- J – Wafer-level packaging (WLP)
- K – Package mold
- L – Wafer bumping
- M – Package bumping
- N – Die attach
- O – 2.5D assembly
- P – Underfill
- Q – Prestacked
- R – Printed board assembly
- S – Package-on-package (PoP) assembly
- T – Rework
- U – Corner glue
- V – System test

addressing miniaturization of excessively high I/O and through-silicon via (TSV) die stacking applications, 2.5D silicon- and glass-based platforms will likely prevail. In addition, technology developers with proven intellectual property (IP) may choose to license core IP as a shared resource across multiple users, amortizing development costs.

The ability to extend core IP through reuse, or by leveraging IP across multiple platforms, offsets the full nonrecurring engineering (NRE) costs that companies would normally incur when introducing a new IP usage model. Amkor Technologies, for example, has indicated advanced 2.5D system in package (SiP) architectures can support leading-edge system performance requirements while reducing time-to-market and lowering total cost of ownership (when compared to packaged system on chip (SoC) platforms). It is generally understood 2.5D TSV architecture represents a viable approach to single-package system design and allows benefits such as:

- Power and performance improvements, enabling new applications
- Smaller form factor
- Silicon layer count reduction for reduced cost and cycle time
- Employment of die utilizing the best technology node at the best price and performance (keeping foundry capital expenditures low)
- Die partitioning and optimization for memory, analog, performance, power management, etc.
- Higher effective die yields obtained through die recovery
- Integration of memory technologies with clear downstream benefits for bandwidth and power (serving as replacements to eDRAM/eFlash)
- Accelerated time to market
- Risk reduction in the manufacturing schedule

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-SM-817 General Requirements for Dielectric Surface Mounting Adhesives

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-2221 Generic Standard on Printed Board Design

IPC-2226 Sectional Design. Standard for High Density Interconnect (HDI) Printed Boards

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-3406 Guidelines for Electrically Conductive Surface Mount Adhesives

IPC-3408 General Requirements for Anisotropically Conductive Adhesive Films

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4202 Flexible Base Dielectrics for Use in Flexible Printed Circuitry

IPC-4562 Metal Foil for Printed Board Applications

IPC-7092 Design and Assembly Process Implementation for Embedding Passive and Active Components

IPC-7094 Design and Assembly. Process Implementation for Flip Chip and Die Size Components

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525 Stencil Design Guidelines

IPC-7711/21 Rework, Modification and Repair of Electronic Assemblies

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

IPC-9702 Monotonic Bend Characterization of Board-Level Interconnects

IPC-9703 IPC/JEDEC Mechanical Shock Test Guidelines for Solder Joint Reliability

IPC-9704 Printed Circuit Assembly Strain Gage Test Guideline

¹ www.ipc.org

2.2 Joint Industry Standards²

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

JP002 JEDEC/IPC Current Tin Whiskers Theory and Mitigation Practices Guideline

IPC J-STD-005 Requirements for Solder Paste

IPC J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

J-STD-020 Moisture/Reflow Sensitivity Classification for Nonhermetic Surface Mount Devices

J-STD-030 Selection and Application of Board Level Underfill Materials

J-STD-033 Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

J-STD-035 Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Components

2.3 JEDEC³

JESD 30 Descriptive Designation System for Semiconductor-Device Packages

JC 63 Multiple Chip Packages

JEP 95 Design Guide 4.14

JESD22-A100 Cycled Temperature Humidity Bias Life Test

JESD22-A102 Accelerated Moisture Resistance – Unbiased Autoclave

JESD22-A104 Temperature Cycling

JESD22-A106 Thermal Shock

JESD22-A108 Temperature, Bias, And Operating Life

JESD22-A110 Highly Accelerated Temperature And Humidity Stress Test (Hast)

JESD22-A113 Preconditioning Of Nonhermetic Surface Mount Devices Prior To Reliability Testing

JES22-B103 Vibration, Variable Frequency

JESD22-B104 Mechanical Shock

JESD22-B110 Mechanical Shock – Component And Subassembly

JEP-122 Failure Mechanisms And Models For Semiconductor Devices

JEP-131 Potential Failure Mode And Effects Analysis (Fmea)

JEP-143 Solid State Reliability Assessment Qualification Methodologies

JEP-158 3D Chip Stack With Through-Silicon Vias (TSVs): Identifying, Evaluating and Understanding Reliability Interactions

2.4 Government Electronics and Information Technology Association (GEIA)⁴

GEIA-STD-0005-1 Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead Free Solder

GEIA-STD-0005-2 Standard for Mitigating the Effects of Tin Whiskers in Aerospace and Electronic Systems

3 GENERAL DESCRIPTION

3.1 Technology Overview Electronic packaging is changing from the traditional package of substrate and die to three-dimensional (3D) packaging technology. The electronics industry has experienced a semiconductor package technology renaissance. This is due to the growing number of innovative 3D package assembly methodologies and approaches which enable continually maximizing product functionality and density without increasing product size. Multiple-die packaging commonly utilizes a substrate and/or interposer as a base. By integrating multiple-die elements within a single-package outline, overall product functionality can be increased while the package size becomes smaller than its predecessors, improving performance and capability. Some of the 3D packaging technology solutions are:

- Multiple-die stacking
- System-in-package (SiP)
- System-in-chip (SiC)

² www.ipc.org
³ www.jedec.org
⁴ www.geia.org

- Package-on-package (PoP)
- Package stacking with interposer
- Embedded package
- Wafer/wafer, die/die bonding
- Optoelectronics package

Assembly of semiconductor die onto an organic substrate or glass/silicon interposer is essentially the same as assembly for standard IC packaging formerly using lead frames, but substrate- or interposer-based IC packaging for 3D applications can adopt a wider range of materials and alternative assembly processes.

3.1.1 Die Stack Package When vertically stacking two or more semiconductors for wire-bond assembly, the die elements will ideally have a progressively smaller outline. This tiered configuration allows all die to be sequentially attached on top of one another in a single operation, leaving the edge of the die elements accessible for the subsequent wire-bond operation, typical of that shown in Figure 3-1.

This tiered die format will generally furnish the lowest overall multiple-die package profile. There is also a potential for improving package performance due in part to the very short coupling between vertically configured semiconductor die. Because they generally utilize a common substrate or interposer, the package typically exhibits lower resistance, lower inductance and lower overall power consumption.

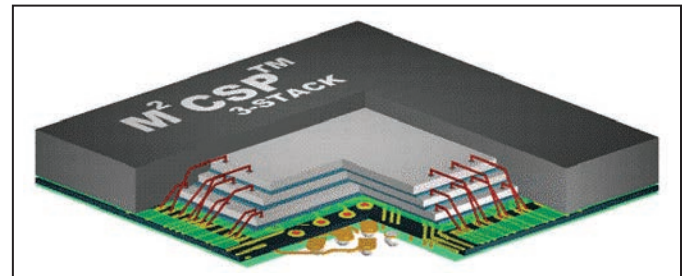


Figure 3-1 Die Stack Package Assembly

Figure source: STATS ChipPACK

3.1.2 Package Stack A package stack refers to vertically mounting one or more prepackaged and tested die elements. Memory semiconductor companies adopted this process to provide a simple solution for furnishing significantly higher-density configurations to keep pace with more advanced processors.

3.1.3 Package-on-Package (PoP) Package-on-package (PoP) technology consists of at least two microelectronic packages which are assembled in a vertical stack and utilizes a fine-pitch ball grid array (FBGA) to join the package sections. The lower package of the stack includes a pattern of metallized lands on its top surface, through which mechanical and electrical attachments are made with the upper package (illustrated in Figure 3-2). The ball pattern of the upper package is designed to facilitate the connection between the packages.

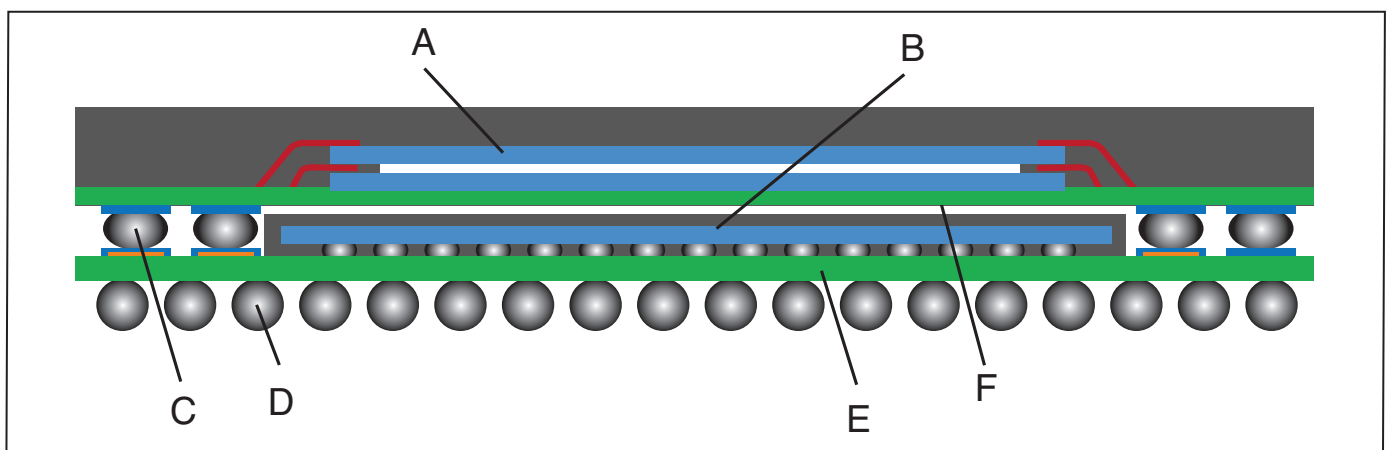


Figure 3-2 Mixed-Function Package-on-Package (PoP) Example

- A – Stacked memory package on upper level
- B – Flip-chip-mounted logic on lower level
- C – Contact pitch on upper section (0.05 mm - 0.65 mm [0.020 in to 0.03 in])
- D – Contact pitch on lower section (0.50 mm - 0.65 mm [0.020 in - 0.026 in - 0.031 in])
- E – High- T_g organic multilayer interposer
- F – Two-layer high- T_g organic interposer

3.1.4 Interposer Silicon and glass are the ideal interposer materials for flip-chip and SiP applications in terms of coefficient of thermal expansion (CTE) to match the physical properties of the silicon-based semiconductors mounted on the interposer surface. Organic materials such as polyimides may be acceptable depending on user requirements.

3.1.5 Through-Silicon Via (TSV) TSV technology is the key to successful implementation of silicon as an interposer base. The processes developed for etching or drilling and then plating very small vias in this extremely brittle medium have enabled the dramatic expansion of I/O density and increased product performance.

3.1.6 Through-Glass Via (TGV) Through-glass via (TGV) technology has enabled developers to take advantage of significantly lower base material cost (compared to silicon). TGV drilling and plating processes are very different from the TSV process; however, glass interposers are said to furnish far lower transmission loss than silicon-based interposers.

3.1.7 System on Chip (SoC) SoC technology is a package in which there are multiple functions implemented into one silicon die. It may include one or more processors, memory and related peripheral functions on a single silicon platform. The heterogeneous SoC may include logic, analog and passive elements mounted onto a ceramic, silicon or glass material as a base platform in a planar (two-dimensional, 2D) format.

Figure 3-3 is an example of SoC consisting of a single large die containing multiple functions.

One advantage of SoC is high electrical performance with low power consumption since all functions are on one silicon die. The disadvantage is that it creates multiple functions on one die, which is very complicated, costly and time consuming.

3.1.8 System in Package (SiP) SiP, also known as multichip module (MCM), is multiple die or chip scale packages (CSPs) mounted on a single package substrate. Developing a SiP with related but dissimilar functions within a single package outline enables greater printed board surface utilization and potentially can provide enhanced electrical performance.

A typical system application would combine logic, memory and analog functions in a vertically configured 3D package utilizing an organic base substrate for interconnection. One advantage of SiP is each die could use a different process technology, as appropriate, for the functionality needed. One package can also consist of old and new technologies. Converse to its flexibility is the challenge to develop an SMT attachment and compatible process that can integrate these devices onto the package substrate.

Figure 3-4 shows a SiP package with four unique die connected in one package substrate.

3.1.9 Wafer-Level Packaging (WLP) Wafer-level packaging (WLP) has evolved to further reduce the packaged die footprint. In this approach, the wafer coming out of the semiconductor fab is the starting point for package processing. Multiple methods have been developed to package the die by performing much of the processing on the wafer before it is singulated.

A common method begins by adding a redistribution layer (RDL) to the active side of the wafer to bring the I/O pads to a uniform array format. Next, a dielectric layer is deposited and pads are opened at the desired contact points. Solder paste or preformed solder balls are then deposited on the pads and then the wafer is reflowed. The back of the wafer can then be marked with a part number and/or logo. Finally, the wafer is singulated by sawing.

The resulting package is not only small, but it has minimal electrical parasitics and, potentially, low cost in high volume, especially after the nonrecurring expenditure specific to each wafer has been absorbed (Figure 3-5).

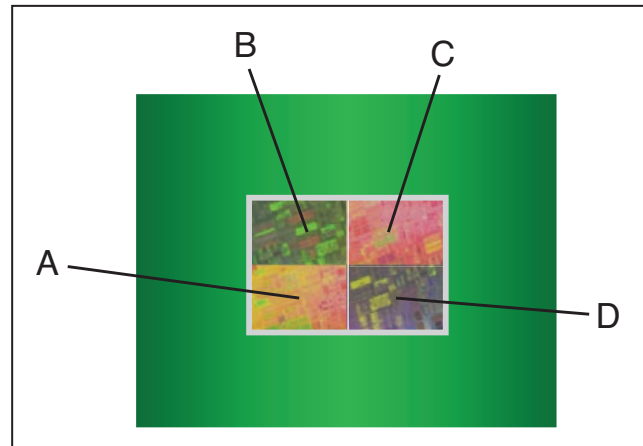


Figure 3-3 System on Chip (SoC) Example

- A – Analog/radio frequency (RF) portion
- B – Logic portion (high performance)
- C – Logic portion (low performance)
- D – Memory portion

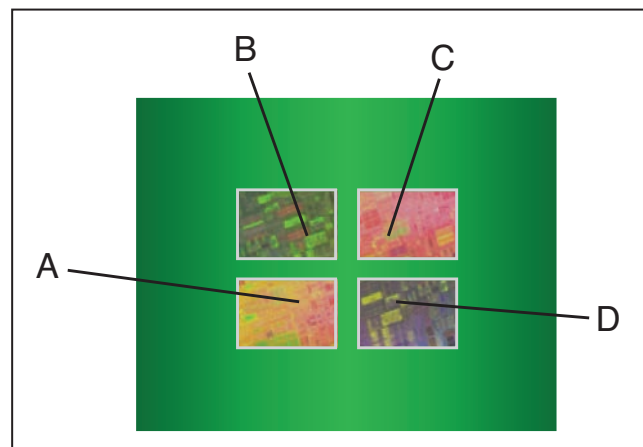


Figure 3-4 System in Package (SiP) Example

- A – Analog/radio frequency (RF) die
- B – Logic die (high performance)
- C – Logic die (low performance)
- D – Memory die

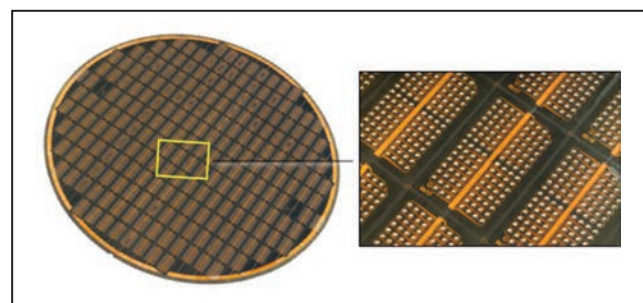


Figure 3-5 Wafer-Level Packaging (WLP) for High-Performance Memory

Figure source: Tessera

3.1.10 Fan-Out Wafer-Level Packaging (FOWLP) Fan-out WLP technology is used to redistribute the very fine-pitch I/O of a die element to a more process compatible contact pitch without increasing the die size. The basic die element is prepared with contact features suitable for flip-chip attachment to an interposer substrate base, where the substrate interposer performs the function of “fanning out” the I/O of the die element to a uniform array format more efficient for board or substrate mounting. In fan out WLP technology the wafer is diced into chips, and then the dies are placed in a carrier with space for fan out around the die. Molding and a redistribution layer (RDL) are added to the dies followed by attaching interconnect solder balls. The FOWLP could be a molded package or have an exposed die molding where the thinnest mold cup can be achieved (see Figure 3-6).

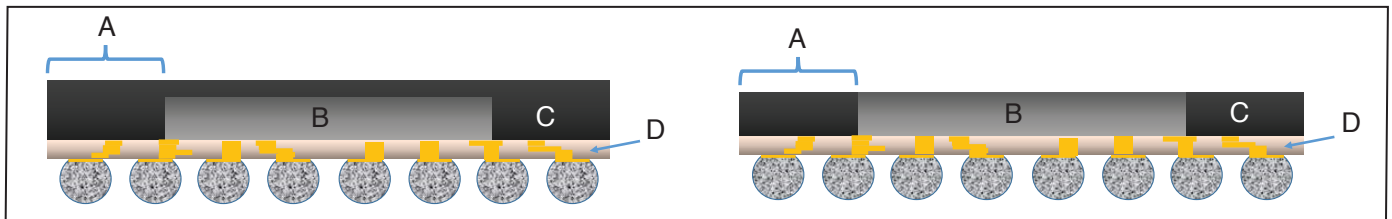


Figure 3-6 Fanout Wafer Level Package Examples

Figure note: FOWLP on left, exposed molding FOWLP on right

A – Fan-out area
B – Die
C – Mold
D – RDL

3.1.11 Substrate The material selected for component substrates can be either of the following:

- Ceramic
- Organic, glass-reinforced resin system
- Nonreinforced film

Bismaleimide-triazine (BT) laminate is one of the preferred substrate materials for array-configured semiconductor package applications. Polyimide is also used for component substrates. The material is composed of high-strength and high-temperature polymers, which are suitable for any electronic package application requiring high performance or which will operate in harsh environments.

3.2 Package Geometric Space As semiconductor die elements shrink in size, companies work to increase package density and enhance functional performance. To support this effort several semiconductor package assembly providers are expanding the role of the interposer to interconnect both heterogeneous logic functions and homogeneous memory within a single package outline.

3.2.1 Two-Dimensional (2D) Package A 2D package consists of one or more die mounted in a single plane. A 2D package could be any of the following:

- Standard BGA package with one die
- SoC with one die and multiple-function silicon
- SiP with a lot of silicon die

The die could use flip-chip, wire bonding or any other die-attached technology. Figure 3-7 shows an example of a 2D SiP with two flip-chip die.

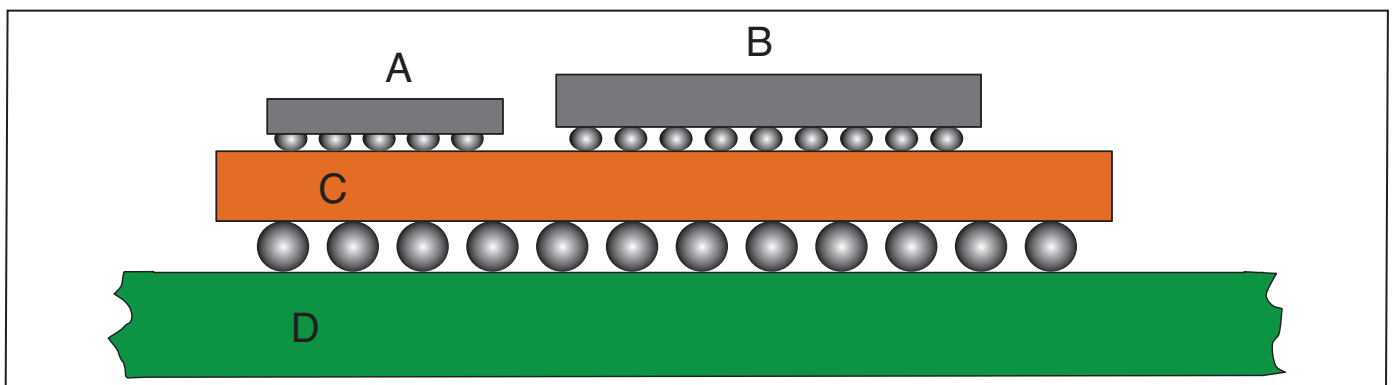


Figure 3-7 Example of a 2D System in Package

A – Die #2
B – Die #1
C – Package substrate
D – Printed board

3.2.2 Two-and-a-Half-Dimensional (2.5D) Package A two-and-a-half-dimensional (2.5D) package consists of one or more die mounted on an intermediate interposer and then mounted onto the package substrate. The interposer could be silicon, glass, ceramic or organic furnished with through vias for connecting the die metallization layer to the package substrate metallization layer. Figure 3-8 shows a 2.5D SiP package in which an interposer with TSVs is placed between the SiP substrate and the two flip-chip die elements.

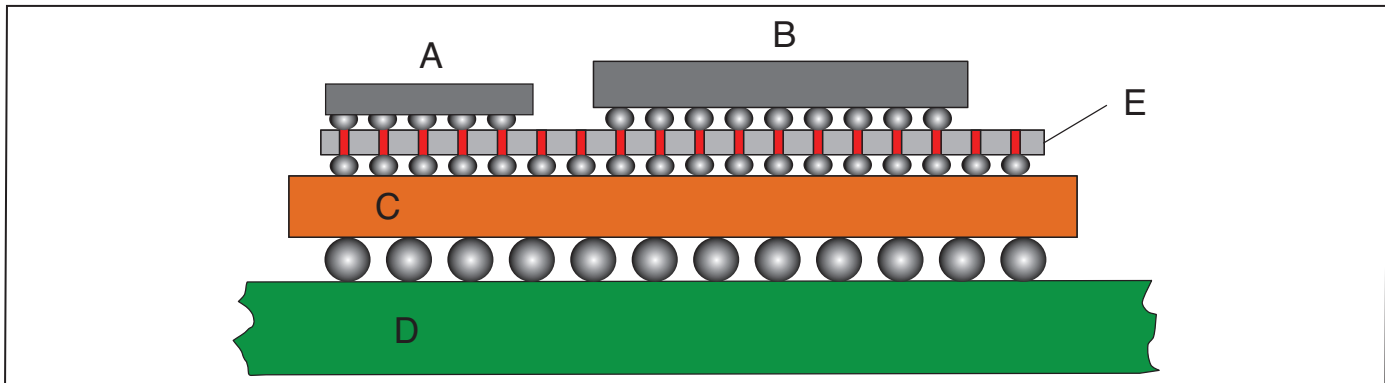


Figure 3-8 Example of a 2.5D System in Package (SiP)

A – Die #2
B – Die #1
C – Package substrate
D – Printed board
E – Interposer

A 2.5D interposer serves as a high-density interconnect platform to accommodate multiple heterogeneous and/or homogeneous semiconductor packaging applications. The base material for the interposer is a silicon wafer commonly used in manufacturing semiconductor elements. Prior to metallization for circuit interconnect, small via holes are ablated through the silicon material. The advantage of using 2.5D technology is the ability to stack different silicon technologies on a single substrate. This simplifies the assembly process until 3D challenges can be resolved. Two-and-a-half-dimensional packaging also has time-to-market advantages since it requires less integration design time and less manufacturing time.

3.2.3 Three-Dimensional (3D) Package There are many approaches for 3D packaging, such as:

- Package-on-package
- Stacked die with wire bond
- Stacked die with wire bond and flip chip
- Stacked die with TSV
- Stacked die utilizing intermediate interposers

There are many challenges involved in 3D packaging that relate to manufacturing process complexities and high cost. The printed board example shown in Figure 3-9 has a PoP device on the left and a distinct 3D multiple-die package assembly on the right. The 3D package assembly represents a SiP having two intermediate interposer structures. The larger interposer accommodates four vertically stacked through-mold-via (TMV) packaged die as well as an assembly with two flip-chip die mounted onto a smaller intermediate interposer.

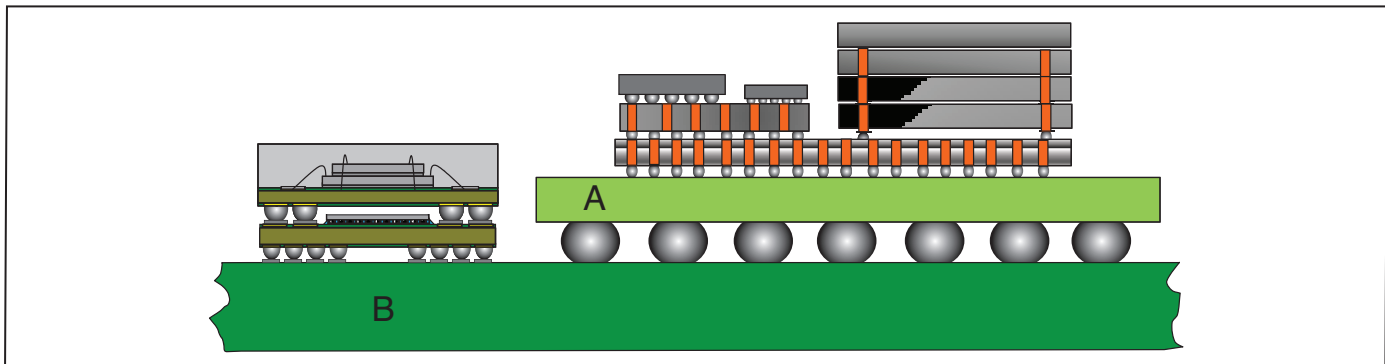


Figure 3-9 3D Package-on-Package (PoP) and System in Package (SiP) on a Printed Board

A – Package substrate
B – Printed board

3.3 Embedded Circuitry Technology Embedded circuitry can be formed using formed sheets of passive materials, discrete passives or by placing thin, small outline discrete passive components and semiconductor die elements within the layering structure of a printed circuit board.

Implementing embedded circuitry will continue to be a viable solution for a broad segment of the electronics packaging industry, especially handheld and consumer sectors, for which very small size and low power consumption are key marketing factors.

Figure 3-10 shows an example of embedded uncased active and passive component elements.

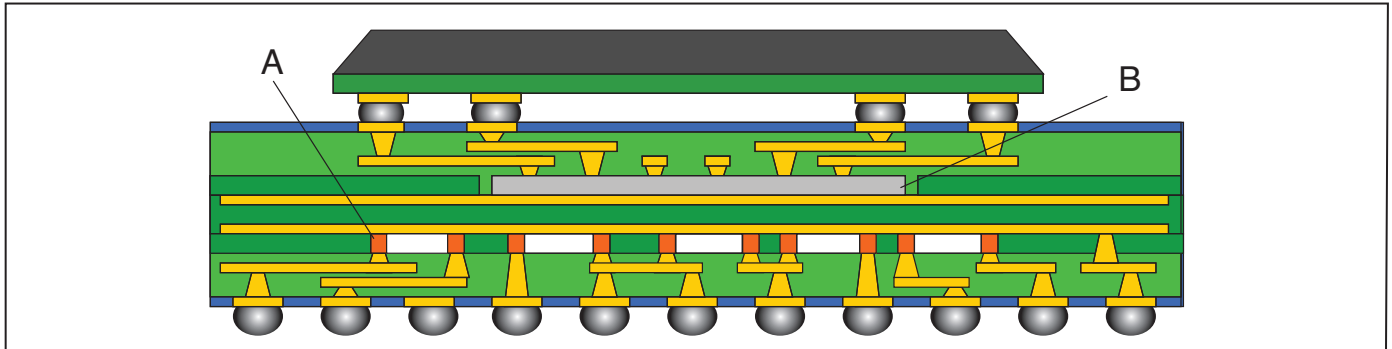


Figure 3-10 Ball Grid Array (BGA) Substrate with Embedded Active and Passive Elements

A – Embedded passive components
B – Embedded active die element

High-performance applications can benefit also when related components are positioned near one another. Close coupling of related components contributes to minimizing signal delay and cross-talk problems. Refer to IPC-6017 and IPC-7092 for additional information on embedded circuitry. Selection of components to be embedded within the package substrate, however, needs to be made early in the design process (see 8.4).

3.4 Advanced Packages The industry is shifting away from complex, integrated circuits (ICs) to advanced packaging such as 2.5D, 3D-IC, fan-out and system-in-package (SiP). Using a heterogenous integration approach, the SoC disaggregated to chiplets and integrated into one package. The integration can consist of SiP, 3D, 2D and 2.5D interconnect and WLP (fan-in or fan-out). The goals are to reduce costs, enable customization and improve yields. This is accomplished by vertically stacking modular components and instead of merging dies together, separating them into several chiplets that are designed for specific tasks using a specific process. The chiplets also can be even made by different manufactures. Each piece of silicon chiplet is optimized and will deliver the best performance and power characteristics. Companies can mix-and-match the chiplets and connect them using a die-to-die interconnect scheme.

Figure 3-11 shows the package trend from monolithic die to MCM module to SiP and then advanced package with chiplets. The figure shows an advanced package with four 3D stacked memory (HBM) and a main die with four chiplets.

Some of the technologies described in Section 4 are found in implementation of various advanced packages with multiple dies.

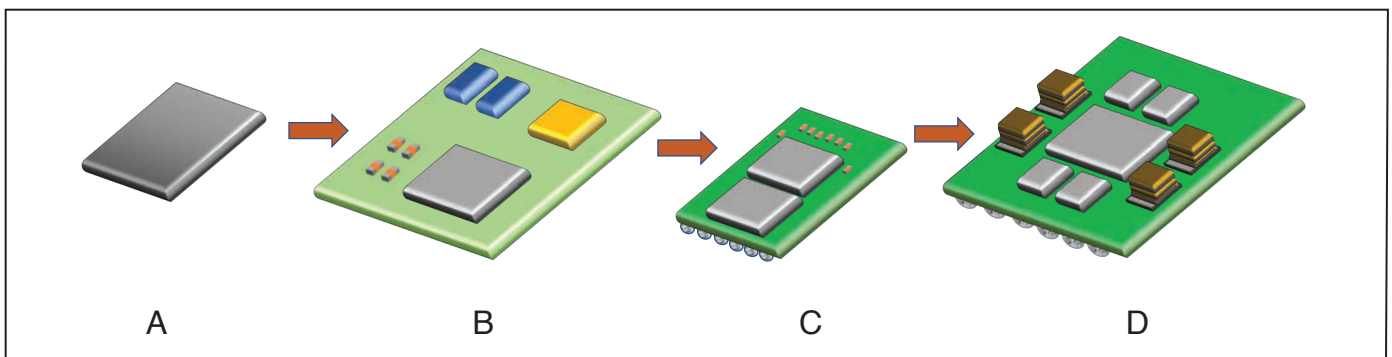


Figure 3-11 Advanced Package Trends

A – Monolithic die
B – MCM
C – SiP
D – Advanced package

4 DEVICE CONSIDERATIONS

3D IC packaging technologies is a key for future system enablement. It is being used in a wide variety of applications to create heterogeneous package approach that can mix and match different process technology chips with different memory devices. It is especially used where those applications require high computing power and memory capacity. It is already being used widely for memory enhancement and continues to spread to logic graphics and RF applications. There are many types of 3D IC packages technologies to accommodate the different applications and use options. Different package suppliers are using different 3D package technology and unique 3D solutions some of which will be discussed in the following section.

Passive and active components both may be incorporated into a package substrate. Most commercial passive elements are furnished with a terminal compatible for solder processing, while semiconductors require further preparation. Semiconductor elements have traditionally been configured for Au wire-bond termination. Cu wire-bond termination, however, has evolved into the mainstream for both single- and stacked-die package applications (see 4.7).

Converting to Cu wire requires additional plating operations (explained further in 5.7). Flip-chip mounting will require similar plating processes as well as surface redistribution of the wire-bond terminal sites to a more uniform array contact pattern (see 4.6.1).

Many have found that by reducing the component population on the substrate surface, package-level assembly is less complex and smaller, often resulting in lower fabrication cost. Although size and cost reductions are significant attributes, the close coupling of key elements can also contribute to improving functional performance. See 4.3 for more detail on passive component variations for embedding.

4.1 Package Assembly Variations Assembling semiconductor die onto a substrate or interposer is essentially the same process as standard I/C packaging in lead frames; however, substrate-based IC packaging for 3D applications can adopt a wider range of materials and several alternative processes may be used in their assembly.

4.1.1 Die Stack (Wire Bond) In an effort to improve component density, companies have experienced success in stacking multiple die elements directly onto a single substrate interposer using wire-bond processes. While most die elements are furnished with wire-bond sites at the edge of the die, synchronous dynamic random-access memory (SDRAM) die elements have center-positioned wire-bond pad sites. This factor has complicated the die stacking process. Because of the excessively long and unbalanced wire-bond interface, signal speed is significantly degraded. There are three array-type package configurations in wide use for stacking high-performance SDRAM:

- Opposing-face, top face-up, bottom face-down
- Staggered stack RDL modified for edge bond
- Face-up, RDL modified for edge bond (two- and four-die stack)

Stacking two- and four-memory die with perimeter-located bond pads has been fairly successful; however, a surface RDL needs to be added onto the wafer to reposition the wire-bond pads to the outer edge of the die. Additionally, these die elements will typically have the same physical outline.

When stacking die directly on top of one another, it will be necessary to add spacers between each die element to clear the wire-bond loop height. Examples of opposing-face and face-up memory package variations are compared in Figure 4-1.

The overall package height can be a critical roadblock for many applications. Even though the die elements can be made very thin, the accumulated stack-up height generated by the added spacer and wire-bond loop profile on the top die may not be acceptable.

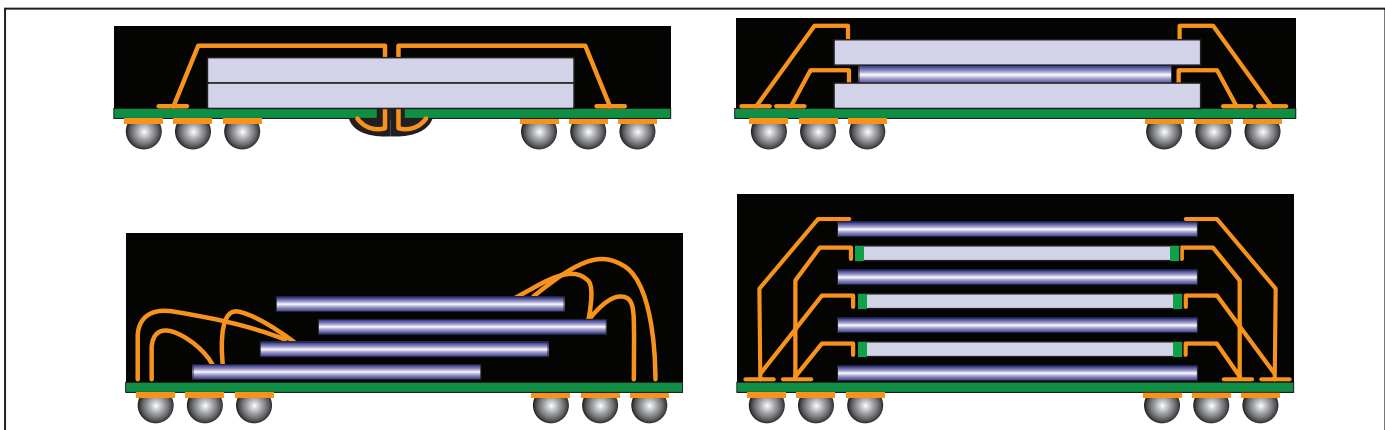


Figure 4-1 Comparing Current Two-Die and Quad-Die Package Solutions

Figure source: Invensas

4.1.2 Package-on-Package (PoP) Technologies Package stacking typically begins with the processor die element packaged onto the base substrate. It will likely have significantly more I/O than any other closely related semiconductor functions. The processor die may be mounted face-up for wire-bond assembly or (after wafer-level redistribution and bumping) mounted face-down for direct solder attachment. The second-level package layer commonly furnishes memory functions (see Figure 4-2).

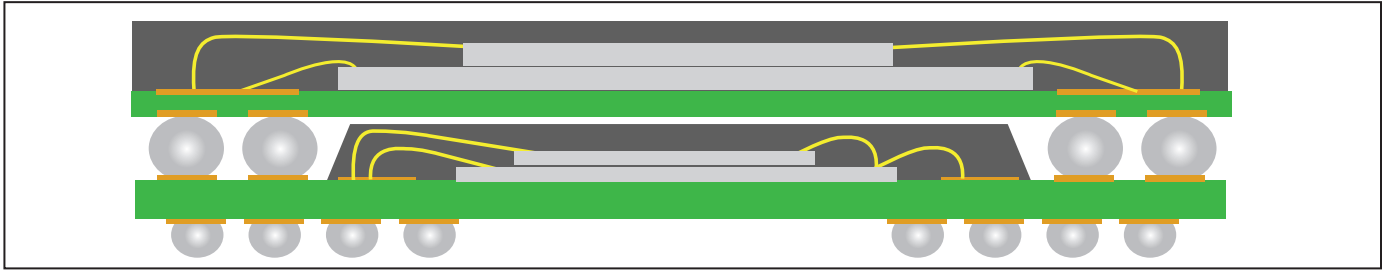


Figure 4-2 Standard Package-on-Package (PoP) Example with Stacked Die

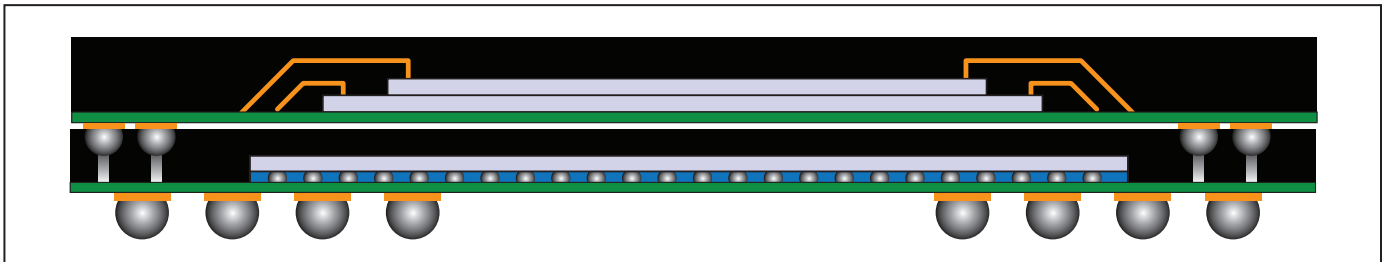


Figure 4-3 Through-Mold Via (TMV) Package-on-Package (PoP)

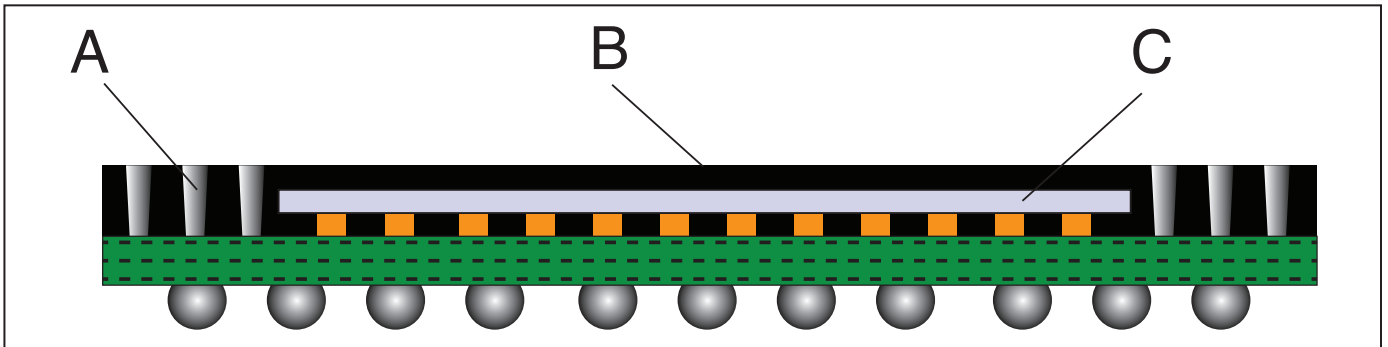


Figure 4-4 Lower Package-on-Package (PoP) Section with Through-Mold Vias (TMVs)

- A – Solder-filled through-mold via (TMV)
- B – Mold compound
- C – Flip chip die element

Although the classic PoP is in wide use throughout the packaging industry, users have found that the joined package sections tend to warp during printed board-level assembly. Warping is attributed to significant solder defects (e.g., bridging, opens, dewetting).

The requirement for a larger solder ball contact and rather wide contact pitch on the upper package section is another issue. The larger solder ball is necessary to clear the mold cap on the lower package section.

To overcome the effects of warping during board-level assembly, the mold compound has been extended to the edge of the substrate. Vias in the mold are provided for access to the lower printed board contact features (see Figure 4-3). The vias, prefilled with solder, enable the use of much smaller solder balls on the upper package section and allow reduction of the spacing between contact sites. This technology is known as through-mold via (TMV) (see 4.1.3).

4.1.3 Through Mold Via (TMV) Adopting through-hole-via technology on the lower section of the PoP section enables significantly closer spacing of the package interface contacts (Figure 4-4). Via sites can be formed as part of the mold process or selectively ablated after molding. It is vital that the Cu surfaces on the lands be free of any mold residue before filling with solder.

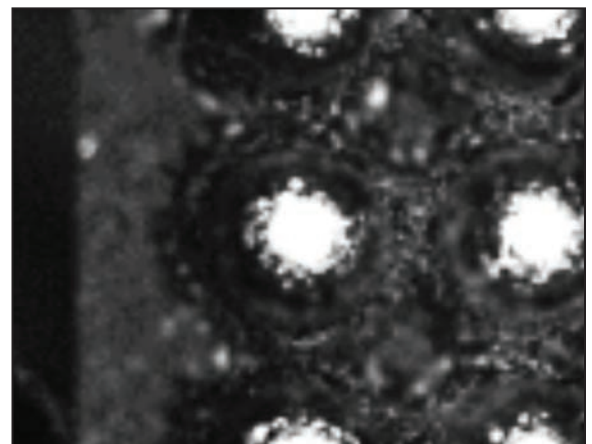


Figure 4-5 Through-Mold Via (TMV) Solder Balls

The most common devices today have solder balls on the bottom package inside the molded via (see Figure 4-5). The memory ball is placed on the bottom package ball inside the molded via to create the connection.

Analysts predict that although the PoP configuration has a very secure near-term position in the industry, newer generations of silicon products will be far more complex and require:

- Significantly higher pin counts
- Solutions for thermal management
- Accommodation for much finer contact pitch variations

Via holes are slightly tapered to provide a larger diameter on the top surface of the mold. Table 4-1 illustrates the typical differences between the bottom of the taper and the top.

Table 4-1 Through-Mold Via (TMV) Examples

Via Position	Average (μm)	Minimum (μm)	Maximum (μm)	Standard Deviation (μm)
Top	449	440	462	5.909
Bottom	313	309	321	3.465

Table source: Amkor Technologies

Depositing solder to fill the via sites includes solder jetting, printing or depositing several tiny solder spheres in each via, followed by mass reflow processing to provide a solid solder fill.

4.1.4 Through-Mold Interconnect (TMI) The TMI process utilizes Cu bond-wire on the lower section of the PoP package. The wire interconnect is arranged in a perimeter-array pattern and encased in the mold compound, encapsulating the semiconductor die mounted onto the organic substrate (Figure 4-6).

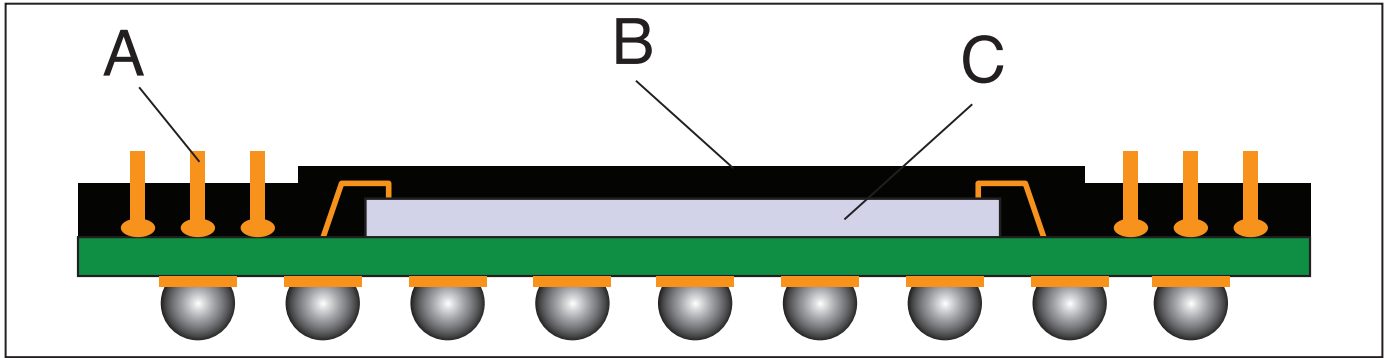


Figure 4-6 Lower Package-on-Package (PoP) Section with Through Mold Interconnect (TMI)

Figure source: Invensas

- A – Cu wire interconnect
- B – Mold compound
- C – Semiconductor die element

The TMI process can furnish an array-configured contact pitch at or below 200 μm. For example, a 14 mm x 14 mm [0.55 in x 0.55 in] package outline can be configured with more than 400 interconnects between the lower and upper package sections. This interconnect solution is very economical and lends itself to a wide variety of 3D PoP packaging applications. Because package assembly technologies utilize the existing semiconductor package infrastructure, they do not require large capital investment and can be quickly implemented to provide increased PoP package I/O and performance.

4.1.5 High-Density Package-on-Package (PoP) Current PoP interconnect technologies have attempted to improve package interface density with smaller solder balls and finer contact pitch. This is done by using laser-drilled and solder-filled vias in the mold cap or by adopting higher density printed board interposers.

The challenge is how to address the complexity of the next-generation multiple-die package assembly. To overcome the limiting aspects of the current method for PoP assembly, alternative very fine-pitch substrate interconnect solutions have evolved.

4.1.5.1 Cu Pillar Interconnect (CuPI) The developer of this Cu pillar interconnect (CuPI) packaging technology states that when compared to solder ball-joined PoP, CuPI PoP provides a more stable package-to-package interface, produces a very reliable product and furnishes excellent electrical performance. Furthermore, the Cu pillar interface is not prone to fatigue by electromigration because the current is distributed uniformly. The Cu pillar contacts are formed on the bottom surface of the upper package substrate using an additive plating process. The developer claims the Cu pillar contacts can be furnished with < 0.20-mm [0.008 in] pitch (see Figure 4-7).

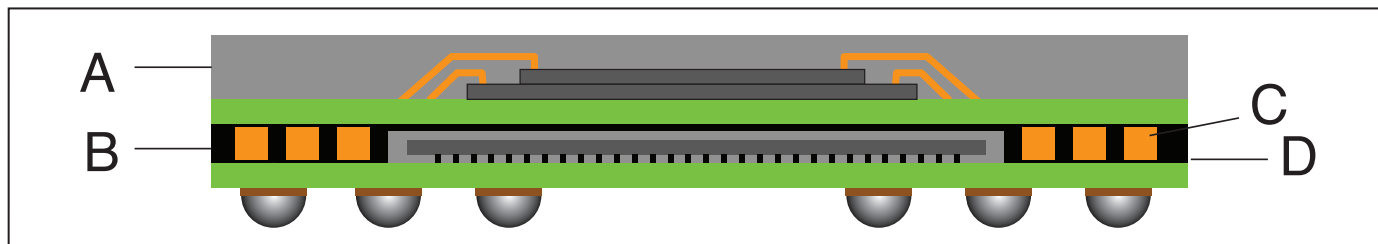


Figure 4-7 Cu Pillar Interconnect (CuPI) Package-on-Package (PoP)

A – Pretested memory section

B – Pretested logic section

C – ≤ 0.3 -mm-pitch [0.012 in] Cu micropillar on upper package section

D – Thermocompression Cu-Sn-Cu bond

The joining of the Cu pillars on the upper package section to the adjacent Cu land features on the lower package section of the package employs a thermocompression reflow (TCR) technology. During the TCR process, underfill is first dispensed onto the top surface of the lower package substrate. The upper package section is placed and is then thermocompression bonded to the lower substrate.

4.1.5.2 Micro-Pillar (μ PILR) The micro-pillar (μ PILR) PoP device has the advantage of an extended solder-wetting plane provided by the Cu pillar contacts, making it less susceptible to solder defects caused by minor substrate warping. One of the benefits of this high-density package substrate structure is the ability to reduce interconnect solder volume and tailor the solder shape to allow closer spacing of interconnects between package and printed board (see Figure 4-8).

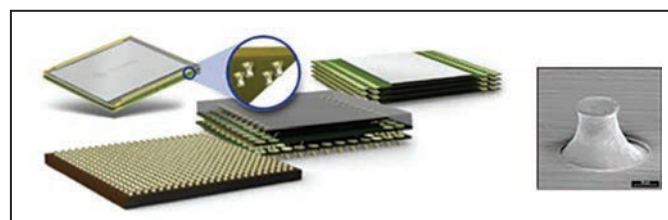


Figure 4-8 High-Density Micro-Pillar (μ PILR) Array Packaging

Figure source: Invensas

When comparing the μ PILR contact profile to the more common solder ball connections, the contact geometry is significantly smaller in diameter and height, enabling a much lower finished package profile. The slightly tapered profile of the solid Cu core contact is coated with an electroless Ni/immersion Au (ENIG) alloy which is compatible with either eutectic or Pb-free soldering processes.

4.1.5.3 Bond Via Array (BVA) Bond via array (BVA) package technology employs a unique solid-Cu wire-bond-based package stacking and interface technology that enables a substantial reduction in interface contact pitch between lower and upper PoP sections. The wire contacts are encased and physically reinforced within the mold compound that encapsulates the lower package semiconductor. The mold is designed so the wire contacts can extend from the top surface of the lower substrate to align with matching solder bump contact locations on the bottom surface of the upper package (see Figure 4-9).

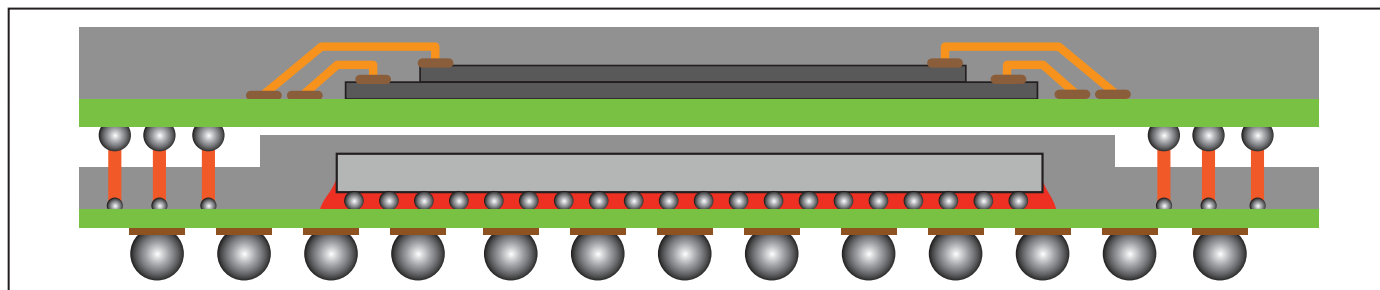


Figure 4-9 Bond Via Array (BVA) With Fine-Pitch Cu Wire Interconnect

Figure source: Invensas

The BVA wire bonding process utilizes conventional wire-bond equipment, which enables a contact pitch as small as $50\ \mu\text{m}$. The Cu wire can extend to any length required for PoP interface.

4.1.5.4 Direct-Bond Interconnect (DBI) Direct-bond interconnect (DBI) is a heterogeneous Cu/silicon-to-Cu/silicon joining process furnishing an in-situ electrical interface. The process can be utilized for joining silicon-based wafers, stacking individual die or mounting singulated or stacked-die elements to a silicon-based interposer structure. DBI is already proven for high-volume manufacturing of complementary metal-oxide semiconductor (CMOS) image sensors and provides a scalable, low-cost solution for very high-density and high-I/O interconnect applications (see Figure 4-10).

The DBI shown in Figure 4-10 is scalable to finer pitch and higher density submicron pitch semiconductors. The bond strength of the Cu/silicon-to-Cu/silicon interface is $1\ \text{J/m}^2$ at room temperature and will provide $> 3\ \text{J/m}^2$ after the 150°C annealing process.

This is a solderless joining process. Because there is no air gap between surfaces, there is no requirement for underfill.

4.1.6 Folded Stack Packaging Flexible substrate materials enable folding of die elements into a very thin single fine-pitch BGA (FBGA) package outline that is only slightly greater than the largest die of the set (see Figure 4-11). Two-, three- and four-die assemblies have been developed, primarily for packaging memory elements; however, more complex mixed-component product variations have evolved for medical applications (e.g., hearing devices, implants).

4.1.7 Package-on-Package Interposer (PoPi) Package-on-package interposer (PoPi) is a technology for maintaining an adequate gap, with small pitch, in 3D packages. This technology uses an ultra-thin picture frame interposer which is prestacked on the memory pads of the bottom package. The interposer elevates the memory pads to ensure sufficient clearance is maintained between the bottom surface of the top memory package and the die of the bottom logic package during placement and reflow. The memory package is placed on top of the interposer and then reflowed with the bottom package. Figure 4-12 shows an example of a PoPi device.

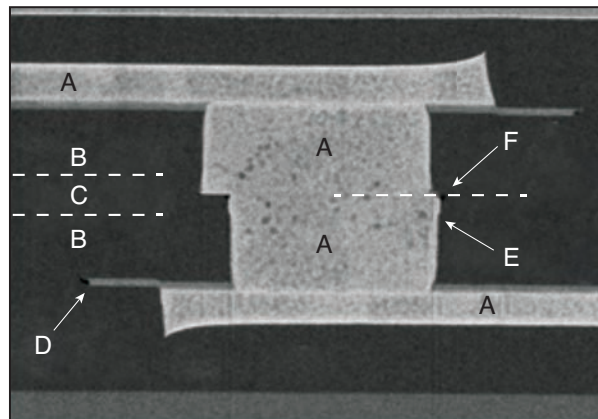


Figure 4-10 Direct Bond Interface (DBI)

A – Cu	D – Sn barrier / adhesion layer
B – Silicon oxide	E – Sn-tungsten barrier
C – Silicon-Ni barrier	F – Bond interface

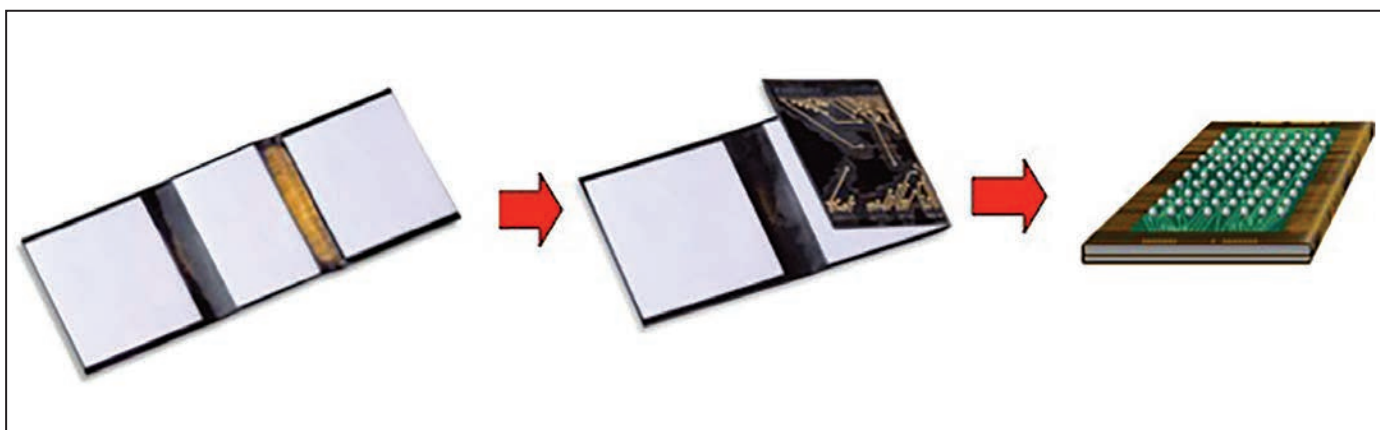


Figure 4-11 Three-Memory Die on Flexible Circuit Substrate

Figure source: Intel

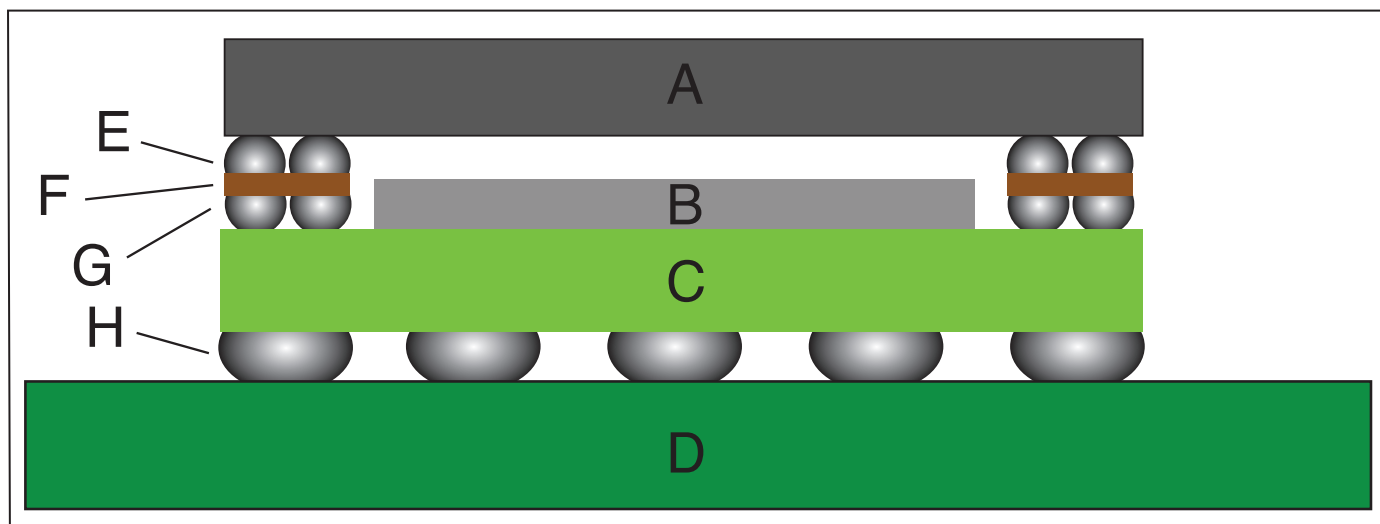


Figure 4-12 Package-on-Package Interposer (PoPi)

A – Top package (memory)	E – Top package solder joints
B – Die	F – Interposer
C – Bottom package (logic)	G – Interposer solder joints
D – Printed board	H – Bottom package solder joints

4.1.8 Thin Small Outline Package (TSOP) Stacking Leaded packages can also be stacked. The advantage of stacking thin small outline packages (TSOPs) is the use of low-cost components and quick integration time, using the industry mainstream DRAM packages.

Figure 4-13 shows two 0.5-mm-pitch memory TSOPs stacked with an organic interposer. A plated-through hole (PTH) connects the memory packages.



Figure 4-13 Stacked Thin Small Outline Package (TSOP) Devices

4.1.9 High Band Memory (HBM) Through-silicon-via for stacking memory has emerged as an efficient joining technology enabling both capacity expansion and the extension needed for higher bandwidth.

High-bandwidth memory (HBM) is a dynamic random-access memory (DRAM) technology that uses through-silicon vias (TSVs) to interconnect stacked DRAM die. Joining these vertically stacked TSV-configured memory die elements requires a relatively high-temperature Sn alloy-based solder composition that is plated or deposited onto the Cu terminal surfaces.

Flux is applied to opposing surfaces, and then die elements are aligned and sequentially stacked onto each other. Mass reflow solder processing completes the joining process followed by flux residue removal and possibly including polymer underfill. See Figure 4-14.

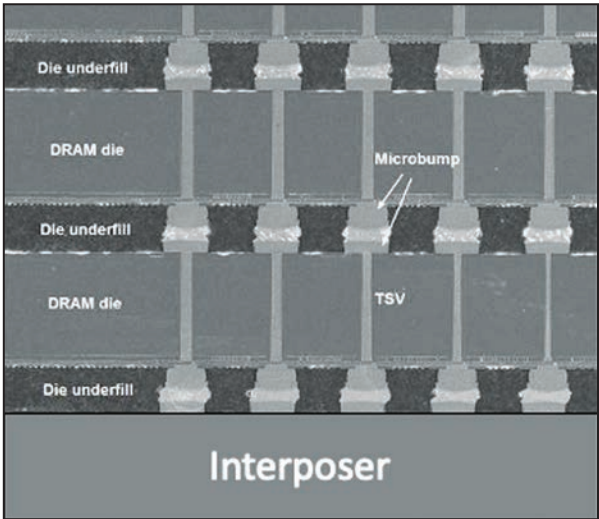


Figure 4-14 High-Band Memory (HBM)
Image source: TechInsights

4.1.9.1 Silicon Bridge Interposer A silicon bridge interposer is a method to connect multiple dies. In this approach, a passive silicon interposer with conventional metal layers and TSVs connects the micro bumps of the different dies. Figure 4-15 shows a package with silicon bridge interposer with a die and HBM stacked.

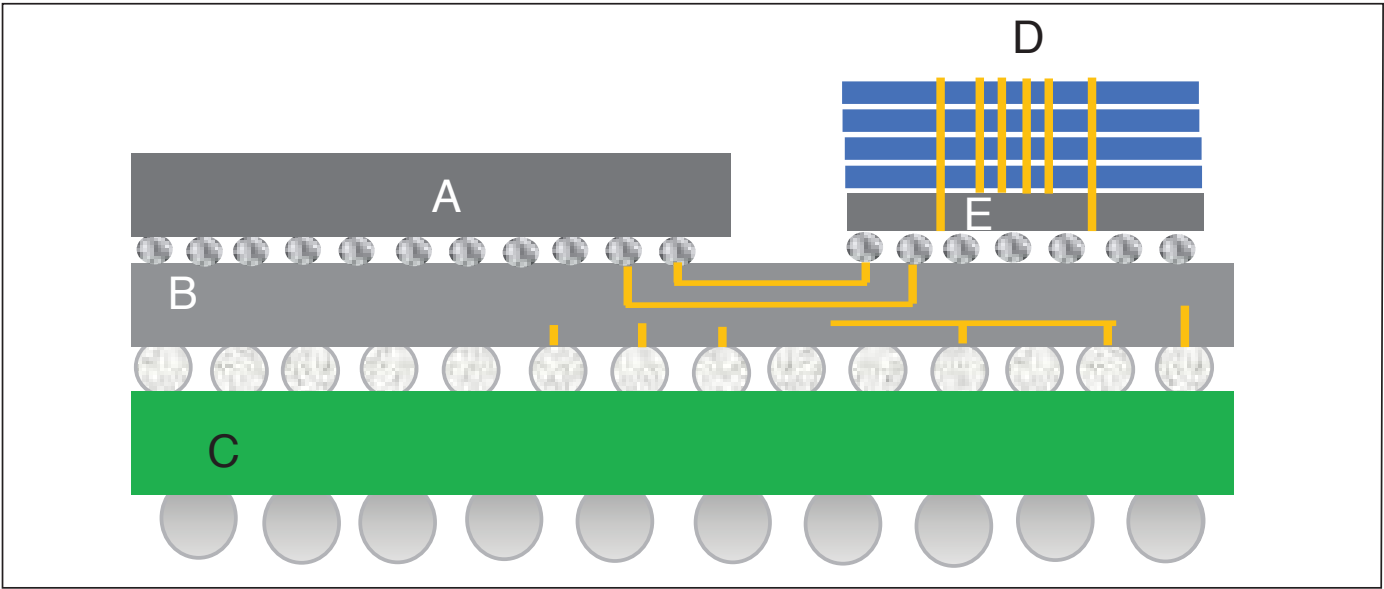


Figure 4-15 Silicon Bridge Interposer with Stacked Die and HBM

- A – Die 1
- B – Silicon interposer
- C – Package substrate
- D – HBM stacked dies
- E – Die 2

4.1.9.2 Embedded Multi-Die Interconnect Bridge (EMIB) Another method to connect multiple die is through an embedded multi-die interconnect bridge (EMIB). This approach does not use TSVs. Rather, it uses a silicon bridge embedded into the package substrate. This is a simple design of 2.5D package without the cost of TSVs and a full interposer. See Figure 4-16.

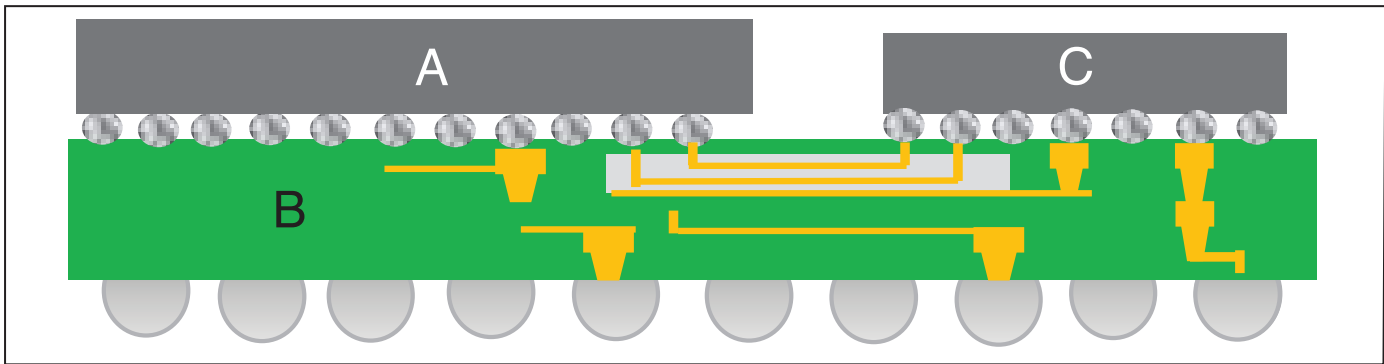


Figure 4-16 Embedded Multi-Die Interconnect Bridge (EMIB)

A – Die 1
B – Package substrate
C – Die 2

4.1.10 Die/Wafer Stack Cu-to-Cu Through-Silicon Via (TSV) There are three primary wafer-to-wafer bonding methodologies for 3D TSV interconnects:

- Fusion (or molecular) bonding
- Metal-to-metal thermocompression bonding
- Adhesion bonding

Each of these methods has its advantages and disadvantages, but there is no standard process for TSV wafer preparation and joining.

There are also process control concerns associated with each method:

- Wafer-to-wafer alignment required for the fusion metal process ± 150 nm
- Metal oxide (if allowed to form) can prevent adequate bond formation
- Excessive heat and bonding force can result in nonuniform bond strength between wafer layers.

For either Cu-to-Cu process variation, surface roughness control and oxidation are important to allow the opposing metal surfaces to come into intimate contact.

Figure 4-17 shows an illustration of a TSV.

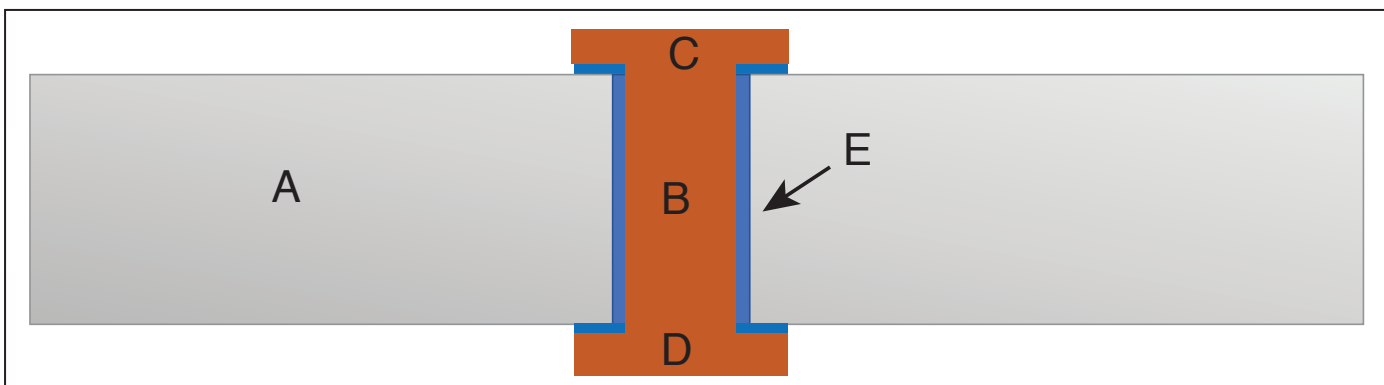


Figure 4-17 Through-Silicon Via (TSV)

A – Silicon
B – Cu-filled via
C – Bond pad
D – Landing pad
E – Passivation layer

4.1.10.1 Cu-Sn-Cu Fusion Bond Joining die elements in a 3D vertical format has been proven to alleviate a great deal of power dissipation concerns. This is because it enables significantly shorter interconnect between individual die elements.

Memory semiconductors are ideal for direct vertical joining because many of the I/O (pins) can be connected in parallel. Although several techniques have evolved for TSV and wafer-to-wafer joining, the solid-Cu-plated via methodology enables a Cu-Sn-Cu fusion bond process to complete wafer interconnect.

The wafer joining process is considered low temperature because it requires no more than 400 °C to complete the Cu-tin-Cu fusion. This joining process, illustrated in Figure 4-18, is a two-stage procedure that begins with the initial precise alignment and room-temperature prebonding of the wafers. Following prebonding, the wafer is exposed to an annealing process that includes high temperature and pressure. This joining process is significantly enhanced with the deposition of a thin layer of Sn-alloy onto the exposed Cu TSV features.

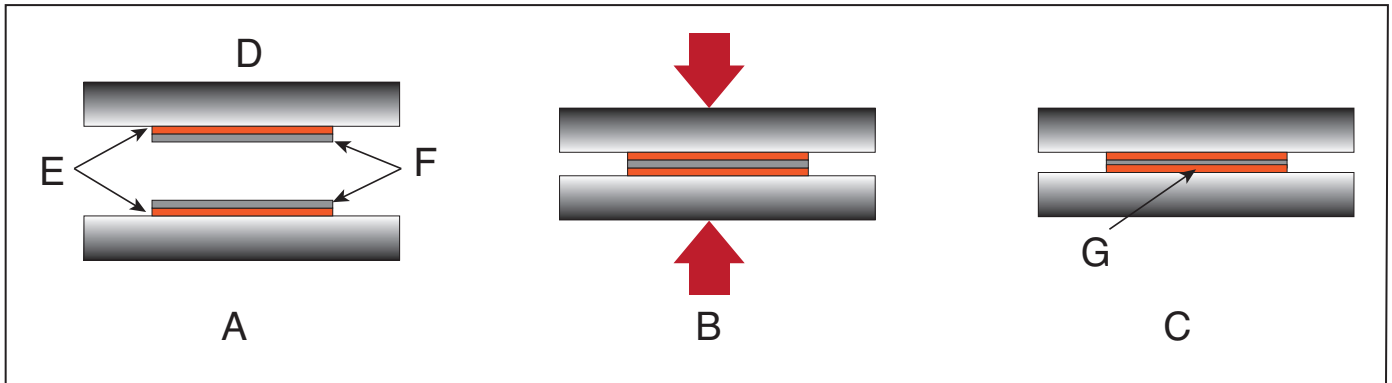


Figure 4-18 Fusion Bond Process

A – Align wafers
B – Apply heat and pressure
C – Bonding complete
D – Silicon wafers

E – Cu
F – Sn
G – Cu₃Sn interface

Fusion wafer bonding is considered by some to be the most efficient method for metal-to-metal via joining. This joining process is a two-stage procedure that begins with the initial precise alignment and prebonding (die-to-interposer or die-to-wafer level platform). The system selected for performing this task needs to be able to maintain precise alignment accuracy. When the stacked wafers are heated to ~ 400 °C, the Sn alloy will completely diffuse into the opposing Cu TSV features to form a stable Cu-tin-Cu (Cu₃Sn) intermetallic at the TSV interface (see Figure 4-19).

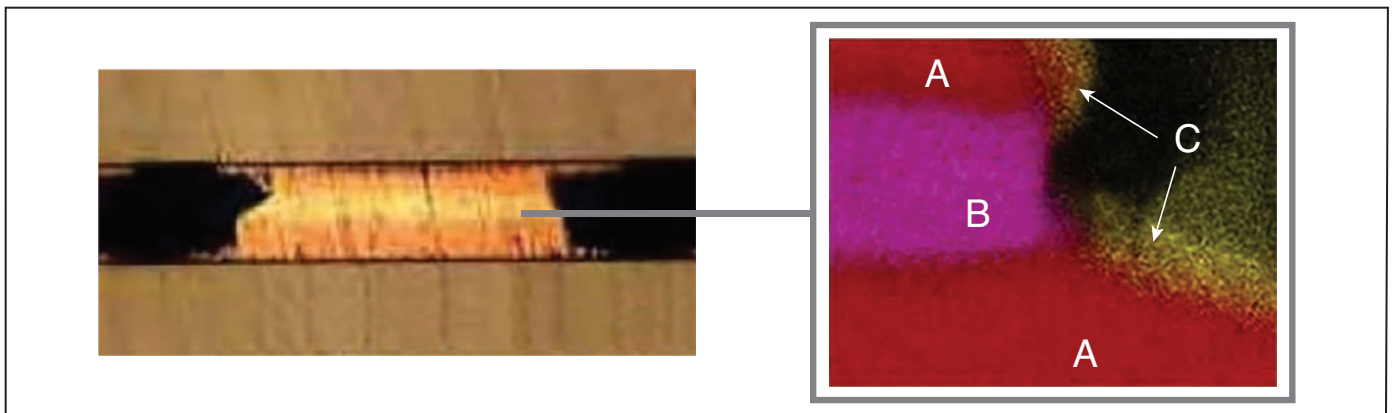


Figure 4-19 Intermetallic Bonds (Cu/Cu₃Sn/Cu)

Left – Cross-section image of the bond between wafer pairs
A – Cu
B – Cu₃Sn
C – Yellow

Due to the process complexities and semiconductor yield concerns associated with wafer-to-wafer joining, many companies opt to stack individual die elements. Although the TSV process is performed at the wafer level, the singulated die elements are easier to test.

4.1.10.2 Thermocompression Bonding Direct Cu to Cu is widely used for TSV bonding because the material has a high diffusion rate and has relatively soft ductile properties (see Figure 4-20). Joining two Cu planes requires thermal presses with a temperature range between 380 °C and 450 °C. The press needs to be able to apply a uniform force between 20 kN and 80 kN for 20 to 60 minutes to complete joining of the Cu surfaces. The primary disadvantage of the direct Cu-to-Cu bonding process is the aggressive cleaning required to remove oxidization that rapidly forms on the unprotected Cu surface.

Au can also be used for wafer-to-wafer joining, requiring temperatures (slightly below the Cu-to-Cu joining process) between 260 °C and 400 °C and an applied force above 40 kN for 20 to 45 minutes. The advantage over Cu-to-Cu joining is that Au does

not form an oxide, eliminating the aggressive cleaning procedure needed prior to bonding Cu surfaces. The primary disadvantage is the fluctuating cost of Au alloy.

4.1.10.3 Adhesion Bonding Anisotropic conductive adhesives provide mechanical strength and electrical conductivity at TSV interconnection points. These materials can be spin- or spray-coated onto silicon wafers or applied as a film media and bonded at a moderate 150 °C to 250 °C.

The advantages of adhesion bonding are:

- Reduced space between wafers
- Lower assembly process temperatures
- Potential for reducing cost

The primary disadvantage of conductive adhesives is the need for an additional passivation (dielectric coating) requirement to insulate the backside of the wafer.

IPC-3406 details guidelines for electrically conductive surface mount adhesives. IPC-3408 provides performance requirements of conducting adhesives, considering the chemistry of the adhesive and the material composition of the filler particles. Both standards furnish details for isotropic and anisotropic adhesives used for attaching flip chips prepared with noble alloy contacts. They cover performance requirements of the material when used in the assembly, as well as long-term performance characteristics.

4.1.11 Three-Dimensional (3D) Interposer/Substrate Packaging This is a technology in which a silicon die element or multiple joined die elements are placed onto the silicon interposer with a conventional reflow solder process. The silicon or glass interposer interconnects the die elements on its upper surface and redistributes the conductors to a very fine-pitch contact array pattern on the lower surface. Solder bumps or preformed solder balls are furnished on the lower surface pattern for attachment to the organic-based substrate (see 8.5).

4.2 General Requirements Multiple-die package planning needs to establish interconnection priorities that include the number of data lines, estimated data speed and power dissipation method. The substrate or interposer developed will require optimization to ensure interconnect lengths are minimized. This optimized design will generally improve overall signal speed and enable significant reduction in power dissipation.

4.3 Device Preparation Before opening containers, place the containers on an electrostatic discharge (ESD)-protected workstation. The work surface of the table and the floor area are to be covered by a static dissipative work surface. Moreover, all the static dissipative surfaces and the workstation needs to be connected to a common ground point. In addition, an operator's connection needs to be added and connected to the common ground point. A wrist strap is commonly used to establish the operator's connection to the workstation. Handling individual components should be avoided. However, when necessary for test and/or product verification, direct physical contact needs to be avoided. Human hands contain oil, which can contaminate the contacts and can impact the integrity of the solder interface. Refer to J-STD-033 for detail regarding the handling, packing, shipping and use of moisture/reflow-sensitive surface-mount devices.

4.3.1 Cleaning When devices furnished to the production floor are in the sealed tray carriers from the supplier, there is generally no need to clean parts before use. When kitting personnel or operators in the assembly environment inadvertently handle

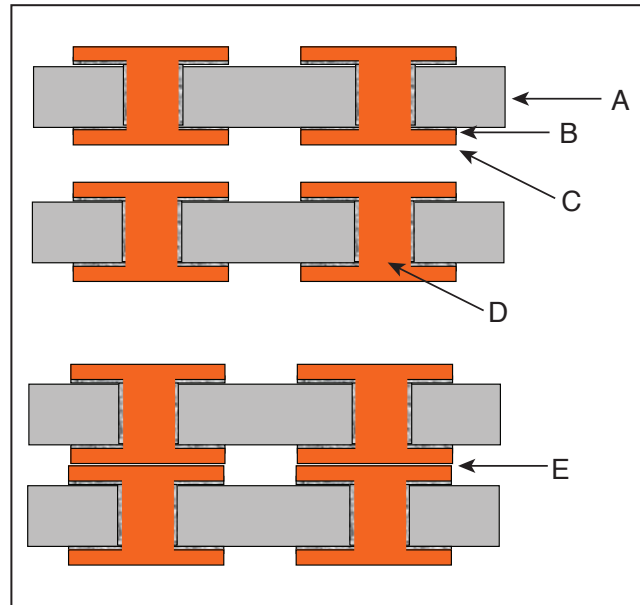


Figure 4-20 Intermetallic Thermo-compression Bonding

- A – Si wafer
- B – Tantalum allow seed layer
- C – Sn-plated Cu alloy land
- D – Cu-filled TSV
- E – Cu-Sn-Cu (Cu₃Sn) intermetallic at the surface



Figure 4-21 Benchtop Small-Batch Ultrasonic Cleaner