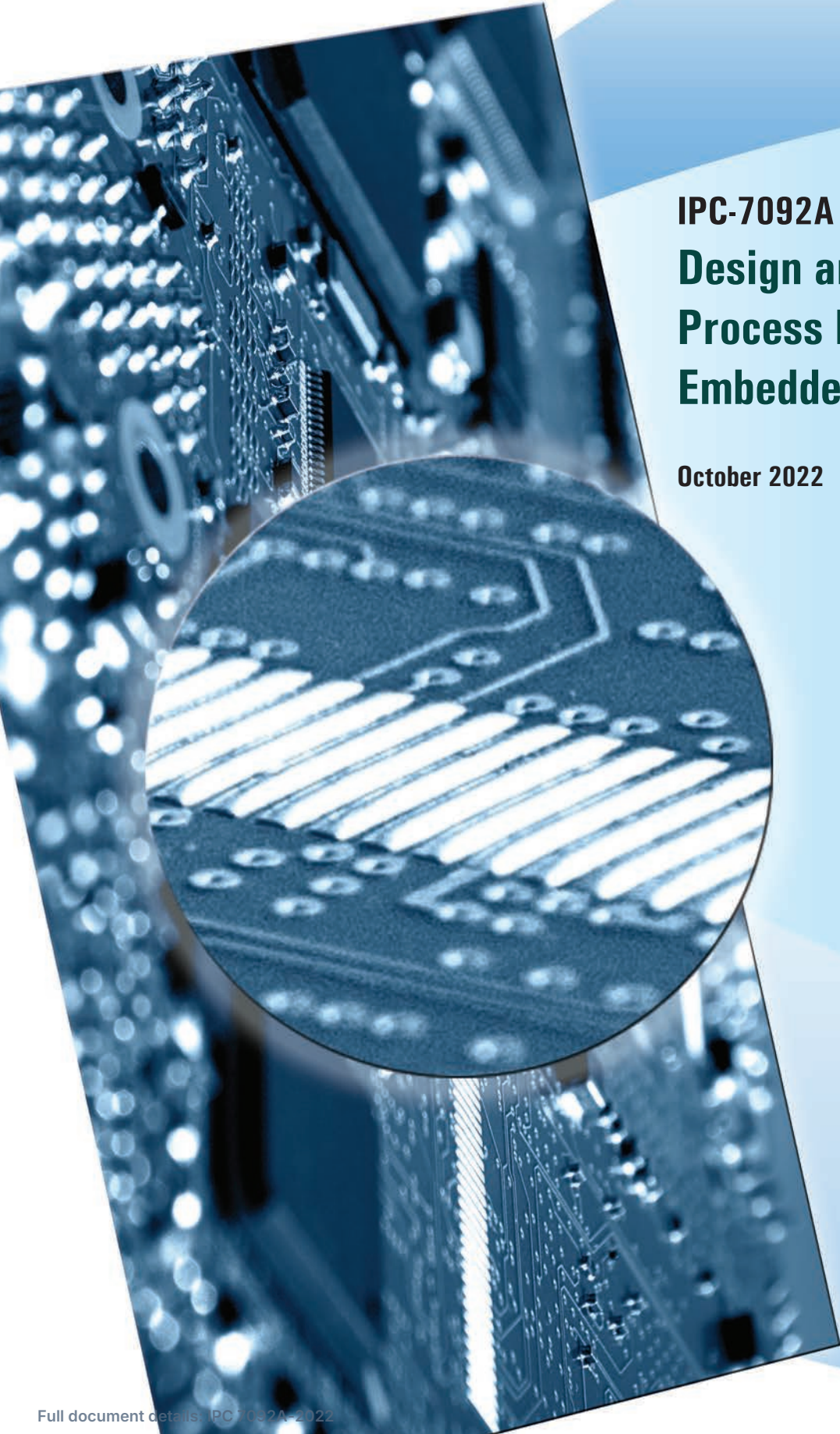




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A large, tilted, blue-tinted microscopic image of a printed circuit board (PCB) occupies the left side of the cover. It shows intricate patterns of copper traces, vias, and solder pads. A circular inset in the center of this image provides a magnified view of a specific area, highlighting the fine details of the board's surface, including a series of parallel gold-colored strips.

IPC-7092A

Design and Assembly Process Implementation for Embedded Circuitry

October 2022



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Users of this publication are encouraged to
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Design and Assembly Process Implementation for Embedded Circuitry

1 SCOPE

This document describes the design, materials and assembly challenges associated with implementing embedded circuitry into a printed board. It covers various aspects of embedded circuitry related with the design, selection, processing and testing to achieve a completed multilayered structure that is ready for surface mount and/or through-hole component attachment.

1.1 Purpose The target audiences for this document are product developers, design/process engineers and technicians who develop electronic assemblies that include embedded circuitry in the printed board as a part of the final product. The purpose is to provide useful and practical information to those who are involved in the decision making of either formed or placed, passive or active components and to help establish selection criteria, inspection techniques, testing processes and reliability test validations.

1.1.1 Intent This document identifies characteristics that influence the successful implementation of a robust embedded circuitry process. In many applications, the variation between forming and placing methods and materials are reviewed with the intent to highlight significant differences that relate to the decision as to when, why or how to establish the quality and reliability of the final product. The information also establishes the robustness that the embedded portion of the product can survive the continued processing in order to complete an embedded circuitry printed board assembly.

1.2 Classification IPC standards recognize that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in manufacturability, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between classes.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

1.3 Measurement Units All dimensions and tolerances in this specification are expressed in hard SI (metric) units and bracketed soft imperial [inch] units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions < 1 mm [0.0394 in] will be expressed in micrometers and microinches.

1.4 Definition of Requirements—The words **shall** or **shall not** are used in the text of this document wherever there is a requirement for materials, preparation, process control or acceptance.

The word **should** reflects recommendations and is used to reflect general industry practices and procedures for guidance only.

The word **will** is used to express a declaration of purpose.

Line drawings and illustrations are depicted herein to assist in the interpretation of the written requirements of this Standard. The text takes precedence over the figures.

1.5 Use of “Lead” For readability and translation, this document uses the noun lead only to describe leads of a component. The metallic element lead is always written as Pb.

1.6 Abbreviations and Acronyms Periodic table elements are abbreviated in the standard. See Appendix A for full spellings of abbreviations (including elements) and acronyms used in this standard.

1.7 Terms and Definitions Other than those terms listed below, the definitions of terms used in this standard are in accordance with IPC-T-50.

1.7.1 Active Device An electronic component that can change a signal or respond to the signal in a way that is dependent upon the nature of the signal and/or other controlling factors. (This includes diodes, transistors, amplifiers, thyristors, gates, ASICs and other integrated circuits that are used for the rectification, amplification, switching, etc., of analog or digital circuits in either monolithic or hybrid form).

1.7.2 Device An electronic component or group of components for the purpose of controlling or modifying the flow of current through it/them (e.g., resistors, capacitors, inductors, diodes and semiconductors/transistors).

1.7.3 Discrete Component A separate part of an embedded circuitry substrate that performs a circuit function (e.g., resistor, capacitor, transistor).

1.7.4 Embedded Circuitry Active or passive circuitry which is placed or formed within a substrate.

1.7.5 Embedded Circuitry (Placed) Functional circuitry that is placed between the layers of the primary interconnect substrate, as opposed to being on the surface.

1.7.6 Embedded Circuitry (Formed) Circuitry created from raw materials, inside the primary interconnect substrate, as opposed to being on the surface.

1.7.7 Embedded Circuitry Base-Core Completely processed base-core configurations containing active and/or passive placed and/or formed embedded circuitry.

1.7.8 Embedded Circuitry Printed Board Assembly A printed board assembly with embedded circuitry.

1.7.9 Embedded Circuitry Printed Board A printed board which contains embedded circuitry.

1.7.10 Embedded Circuitry Substrate The general term for a completely processed substrate material configuration which contains embedded formed or placed components and is intended for additional mounting in order to complete a functional component package.

1.7.11 Embedded Passive (Sheet Formed) A sheet of resistive, capacitive or inductive material which is laminated onto a dielectric and either etched or lased away to define individual resistors, capacitors or inductors.

1.7.12 Embedded Substrate Board A multilayered printed board that provides point-to-point connections and embedded passive and/or active components, which are formed or placed (connected) during the fabrication process.

1.7.13 Mounting Base The general term for the mounting substrate onto which discrete passive or active components are added, intended to become placed after additional layer processing (the mounting-base may be double-sided or multilayer and can be made of organic or nonorganic materials).

1.7.14 Passive Array (Embedded) Composed of multiple passive components of like function, arranged in a uniform manner, then formed or placed in a multilayer substrate. Examples include an array of capacitors or resistors.

1.7.15 Passive Component (Element) A discrete electronic device that behaves in a fixed way in response to a signal of a given characteristic. (This includes components such as resistors, capacitors, inductors and transformers.)

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC-WP-023 IPC Technology Solutions White Paper on Performance-Based Printed Board OEM Acceptance: Via Chain Continuity Reflow Test: The Hidden Reliability Threat

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-TM-650 Test Methods Manual

2.5.7 Dielectric Withstanding Voltage, PWB

2.6.3 Moisture and Insulation Resistance, Printed Boards

2.6.8.1 Thermal Stress, Laminate

2.6.26 DC Current Induced Thermal Cycling Test

¹ www.ipc.org

IPC-SM-784 Guidelines for Chip-on-Board Technology Implementation

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-1782 Standard for Manufacturing and Supply Chain Traceability of Electronic Products

IPC-1791 Trusted Electronic Designer, Fabricator and Assembler Requirements

IPC-2221 Generic Standard on Printed Board Design

IPC-2316 Design Guide for Embedded Passive Device Printed Boards

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-2588 Sectional Requirements for Implementation of Part List Product Data Description

IPC-3406 Guidelines for Electrically Conductive Surface Mount Adhesives

IPC-3408 General Requirements for Anisotropically Conductive Adhesives Films

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-4563 Resin Coated Cu Foil for Printed Boards Guideline

IPC-4811 Specification for Embedded Passive Device Resistor Materials for Rigid and Multilayer Printed Boards

IPC-4821 Specification for Embedded Passive Device Capacitor Materials for Rigid and Multilayer Printed Boards

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6017 Qualification and Performance Specification for Printed Boards Containing Embedded Active and Passive Circuitry

IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-9111 Troubleshooting for Printed Board Assembly Processes

IPC-9151 Printed Board Process, Capability, Quality and Relative Reliability (PCQR2) Benchmark Test Standard and Database

IPC-9252 Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

2.2 The American Society of Mechanical Engineers (ASME)²

ASME Y14.1 Drawing Sheet Size And Format

ASME Y14.1M Metric Drawing Sheet Size And Format

ASME Y14.44 Reference Designations for Electrical and Electronics Parts and Equipment

ASME Y32 Graphic Symbols For Plumbing Fixtures For Diagrams Used In Architecture And Building Construction (Historical Reference Only)

2.3 IEEE³

IEEE/ANSI 315 IEEE Standard for Graphic Symbols for Electrical and Electronics Diagrams (Including Reference Designation Letters)

2.4 SAE International⁴

GEIA-STD-0005-1 Performance Standard for Aerospace and High Performance Electronic Systems Containing Lead Free Solder

GEIA-STD-0005-2 Standard for Mitigating the Effects of Tin Whiskers in Aerospace and Electronic Systems

2.5 UL⁵

UL 746 Polymeric Materials – Use in Electrical Equipment Evaluations

UL 796 UL Standard for Safety Printed Wiring Boards

² www.asme.org

³ www.ieee.org

⁴ www.sae.org

⁵ www.ul.com

3 GENERAL DESCRIPTION

Passive components (e.g., resistors, capacitors, inductors) and active components that have been integrated within the printed board or substrate interposer structure are referred to as embedded circuitry. A wide variety of materials and methods can be used when embedding these circuit functions within the printed board. There are a number of advantages gained when adapting embedded circuitry technology

- More efficient surface area utilization
- Improved electrical performance
- Lower cost

Furthermore, as frequencies rise and circuits become more complex, more passive elements will be required in order to maintain signal integrity.

By reducing the component population on the board surface, board-level assembly is less complex and the board can be made smaller. The smaller substrate, even when more complex, often results in lower cost. Although size and cost reductions are significant attributes, embedding components can contribute to improved functional performance. When signal rise times decrease and frequencies increase, the lead-inductance associated with interconnecting discrete surface mount components begins to degrade overall circuit function. Moving the component from the outer surface of the board into the substrate layers reduces both lead-inductance and parasitic capacitance. In digital circuits, for example, clock rates and signal rise time improves. In analog circuits, both bandwidth and signal rise times improve.

Electronic components may be formed from selected material or may be placed using premanufactured active or passive components intended for that application. The resulting product then may become an embedded circuitry substrate or an embedded circuitry printed board. Although neither is a completed electronic assembly, the embedded circuitry substrate or embedded circuitry printed board should be able to be electrically tested and be durable to withstand the subsequent assembly process operations (see Figure 3-1). When two or more dissimilar active die elements are embedded within the printed circuit substrate layers, the substrate may be classified as a system-in-package (SiP) or the base structure for the SiP having additional components mounted onto its outer surface(s). As the complexity associated with the component types being embedded has increased, the design, quality assurance and reliability requirements have changed.

The current state of the electronics industry as it pertains to embedded circuitry is that the majority of printed board fabricators have introduced formed embedded passive components, particularly thin-film resistors and capacitance planes. Several fabricators have the capability to provide embedded passive components formed from screen printed polymer thick film (PTF) materials. Some fabricators also have the ability to provide placed embedded passive components. To date, only a few fabricators in Asia and Europe are providing embedded active components of the placed variety. From an OEM perspective, the primary adaptors of embedded circuitry technology have been those where size, weight and power (SWaP) are at a premium (e.g., handheld). A notable exception to this is embedded capacitance planes, which have seen pervasive use

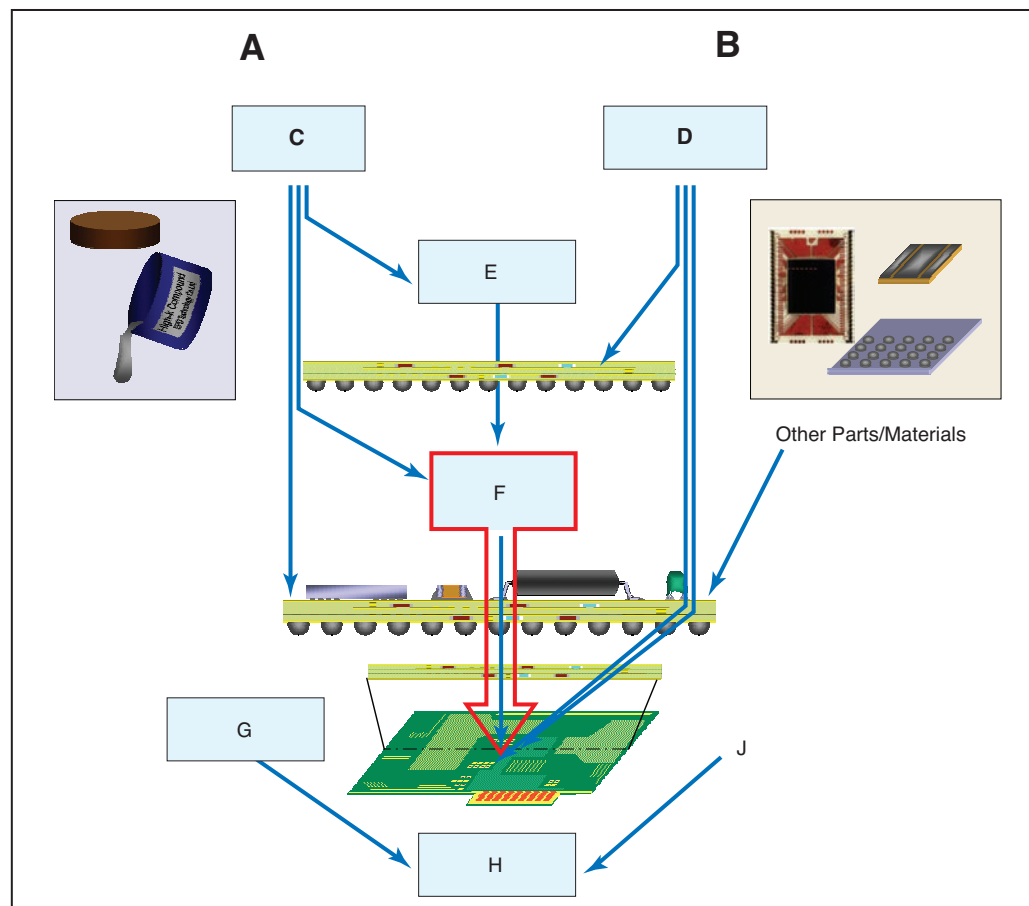


Figure 3-1 Embedded Circuitry Substrate Hierarchy

A – Formed

B – Placed

C – Material

D – Discrete component

E – Substrate (interposer) with

embedded circuitry

F – Module (package) with

embedded circuitry

G – Printed board with embedded

circuitry

H – Printed board

with other parts/materials

in the industry, including handheld, high-performance computing and telecommunications. Embedded placed active components are used predominantly in SWaP-driven and niche applications (e.g., performance), while embedded formed active components are only in a few niche applications. See Figure 3-2.

3.1 Technology Overview The first decision that needs to be made is whether or not to use an embedded circuitry solution. This decision may depend on the application, cost, performance or some other metric which may be a driving force. Several materials properties need to be considered. In addition, when making the decision as to whether or not to embed a particular component in a circuit, one should keep in mind availability of manufactured passive and active components intended for the placement process.

Considerations include:

- Available tolerance of the embedded parts
- Drift limits following thermal shock or humidity exposure
- Aging behavior
- Temperature coefficients of capacitance or resistance (TCC/TCR)
- Power handling capacity (may include geometry of part)
- Breakdown field and leakage currents
- Q – especially important for RF and filter applications
- Parts that need circuit tuning (difficult with embedded circuitry, if the circuit needs to be tuned after complete build)
- Special requirements for some parts (e.g., low-noise metal film resistors)
- Available space for embedded parts, especially large capacitors
- Density of embedded parts (For typical embedded formed passive component implementation, there will be a breakeven cost crossover point at some specific component density.)
- Completed board test, verification complexity and cost
- Temperature coefficients of expansion (mechanical compatibility between substrate and embedded device)
- Embedded device terminations and interconnect with traces

The illustration in Figure 3-3 shows the embedded passive selection process with cost as a driver. The passive component bill of materials (BOM) is first limited by the component values and tolerances versus the available embedded passive technologies. Second, critical components, such as those required for circuit tuning, high Q or low noise, are screened out. Third, space concerns are examined to be sure all of the embedded parts will fit in the required geometry, choosing a combination of parts that fit both physically and logically. Finally, cost needs to be considered, as it is the driver in this example. If the resulting cost analysis is lower for the embedded solution as compared to the surface mount technology (SMT) alternative, then the process continues.

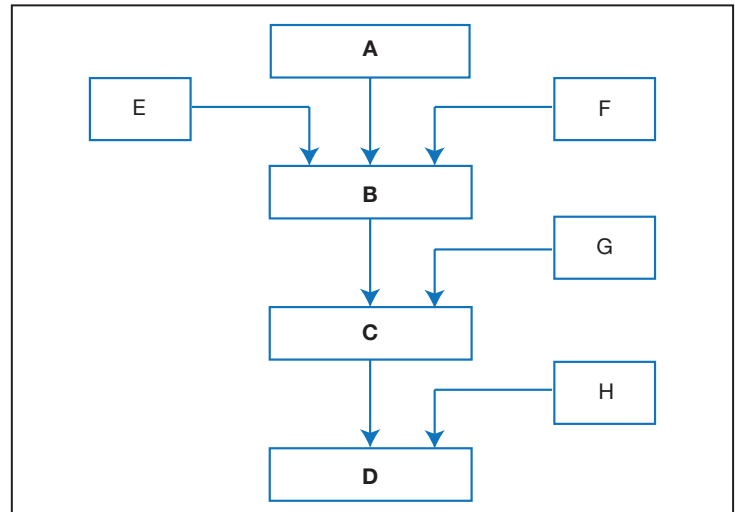


Figure 3-2 Embedded Product Manufacturing Sequence

- | | |
|---|---|
| A – Mounting base | F – Inserted or formed active or passive components |
| B – Embedded component base core | G – Additional layers of copper and dielectric circuits on both sides |
| C – Embedded component printed board | H – Active and/or passive components on top and bottom |
| D – Embedded component printed board assembly | |
| E – Dielectric and copper material | |

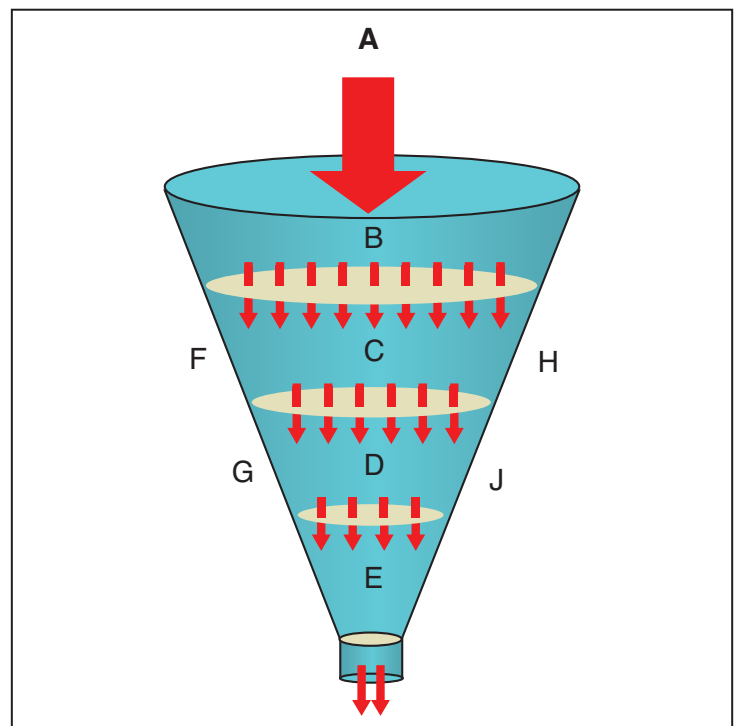


Figure 3-3 Embedded Passive Selection Process with Cost as a Driver

- | | | |
|---|--|--|
| A – BOM and electrical schematic | E – Cost vs SMT | H – Passives required for fine tuning circuit |
| B – Analyze component values and tolerances | F – High Q, power, TCC/TCR requirements | J – Noise, mutual capacitance/ inductance and parasitics due to layout |
| C – Sort out components too critical to embed | G – Inductor radius, capacitor area, resistor geometry and orientation | |
| D – Space and Rf interaction limitations | | |

These arguments only determine whether or not a set of components should be embedded. Perhaps the more difficult questions to answer are which embedding type will be used, whether a formed embedded passive, a manufactured passive device or another type of device? The most common approach is to perform an economic analysis of embedded passive or active components.

This includes:

- 1) Reduce the system cost by the purchase price and conversion costs associated with the replaced discrete passives or actives
- 2) Reduce the board size by the sum of the layout areas associated with the replaced discrete passives and determine the new number of boards on the production panel
- 3) Determine the new board cost based on a higher per-unit-area cost for the embedded passive panel fabrication and the new panel yield computed
- 4) Determine the available manufactured components intended for placement or the materials that might be used in producing formed passive components

Table 3-1 compares and contrasts the various device types by criteria such as cost, size, performance and reliability. The selection of the appropriate embedded circuitry type is at least as critical as the selection of the components to embed.

From Table 3-1, discretes provide the best rating for flexibility, time to market and availability, while embedded passives have only a fair to good rating for the same categories. This particular comparison points directly back to the decision to implement an embedded solution. Some ways to overcome drawbacks of embedded passive solutions include improved design models and circuit simulation.

Table 3-1 Passive Component Selection Criteria

	Discretes	Arrays and Networks	Integrated Passive Devices (IPD)	Embedded Passives
Description	A single passive element (capacitor, resistor or inductor) in a leaded or surface-mount case	Passive arrays combine multiple passive elements of like function (i.e., all capacitors or all resistors) in a single surface-mount case. Networks combine passives of more than one function (e.g., capacitors + resistors) in a single surface-mount case. A network typically contains four to 12 elements.	Multiple passive elements of more than one function and possibly a few active elements (e.g., resistors, capacitors, diodes) in a single surface-mount or chip scale package Typically, contains more than 20 elements May also be referred to as super components	Passive devices that are buried in the substrate material (rather than being mounted on top)
Cost	Good – Benchmark for all other technologies	Better when local densities have four or eight devices close together	Better when high local densities are application specific	Better when average component density is above a specific density Cost = Panel-size dependent
Size	Good – Board area required for each and every device	Better – Up to 50% and greater board area savings over discrete elements	Better – Application-specific IPDs can replace dozens of components.	Best – No surface board area required (devices are buried)
Performance	Good – Self-resonates at low frequencies	Good – Self-resonates at low frequencies	Better – Qualified out to several gigahertz (GHz).	Best – Ideal components; when buried underneath the integrated circuit (IC), they serve, due mainly to decreased lead length and avoidance of the inductance of the connection loops.
Reliability	Good – Heavy use of solder joints	Better – Slightly reduces solder joints	Better – Significantly reduced solder joints	Best – Greatest reduction of solder joints and vias/plated-through holes (PTHs)
Flexibility	Best – Most flexible for both design and manufacturing	Better than IPDs and embedded passives	Better than embedded passives	Good – Requires modeling and simulation
Time to Market	Best – Flexibility allows quick turns	Better – Simple quad and octal arrays can be designed in quickly	Good – IPDs require additional design iterations for wireability	Fair – Most board shops require at least five to seven days to build an embedded passives board.
Availability	Best – Highly available from multiple sources	Better – Standard parts from multiple suppliers	Better – Nonstandard parts from multiple suppliers	Fair – Few suppliers of some specific types of embedded passives
Values	Best – All values available at commodity prices.	Better – Thick-film arrays offer high values.	Good – Thin-films have limited capacitor values.	Good – Currently limited to low values.
Tolerances	Best – Tight tolerances available at commodity prices.	Better – Both offer tight tolerances.	Better – Thin-films offer tight tolerances.	Good – Loose tolerance as formed, better with trimming.

Another similar comparison is that discretes also have a best rating for values and tolerances, while embedded is only a good rating for both. The improved performance of embeddeds may accept the looser tolerances of embedded. For instances, there is enough area available in the embedded solution to allow for larger resistor or capacitor sizes, thus extending the component value range (see Figure 3-4 for an example). Alternatively, for both of these comparisons, perhaps the best solution is to implement embedded circuitry using placed discrete components.

Additionally, an embedded circuitry solution using passive arrays and networks or IPDs could provide an ideal compromise or solution. Note that passive arrays and networks or IPDs would be used when there are multiple resistors, capacitors or inductors serving the same active device—a very common occurrence in electronic systems. This latter consideration is even more critical when the active device is also embedded.

3.1.1 Passive Resistors, Capacitors and Inductors

Resistors – A formed resistor will have two Cu lands with resistance material applied between the lands. The shape of the resistance material can be a simple rectangle or a shape designed to maximize resistor element length while minimizing area (see Figure 3-4). In each case, the resistance material needs to overlap the Cu lands.

Capacitors – Forming a capacitor element within the multilayer circuit structure is a more complex process. There are two primary techniques for fabricating embedded capacitors:

- 1) Dielectric material laminated between opposing Cu circuit layers similar to that shown in Figure 3-5.
- 2) Dielectric material deposited directly onto circuit layers using a thick-film screening process, sandwiched between Cu and/or thick-film conductor electrodes. See Table 3-2 for examples of common thick- and thin-film ceramic technologies.



Figure 3-4 Serpentine Resistor Element

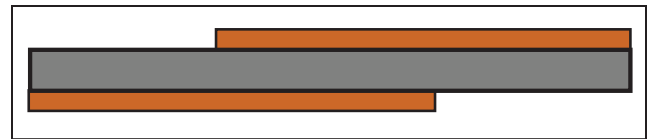


Figure 3-5 In-laminate Dielectric Capacitor Elements

Table 3-2 Common Thick- and Thin-Film Ceramic Technologies

Approach	Product	Deposition Process	Dielectric Material	Dk	Thickness (μm) [in]	Capacitance Density (nF/cm²)
Thick film	Paste	Screen printing	BT*/glass	3,000	10 to 20 [0.0003 to 0.0007]	130 to 270 per layer
Thin film	Laminate	Solution deposition	BT/BST** PLZT***	200 to 3,000	0.5 to 1.0	200 to 4,400
		Sputter	BST	200 to 1,000	0.5 to 0.8	200 to 1,700
		Modified chemical vapor deposition	Alumina	9	0.1	80
		Anodization	Tantalum pentoxide	50	0.02 to 0.1	440 to 2,200

Table notes:

* Barium titanate

** Barium strontium titanate

*** Pb zirconate titanate

Inductors – Discrete inductor elements can be integrated directly into the Cu circuit layers. Unlike formed resistors or capacitors, they require no special materials or special fabrication processes. The Cu pattern will be designed using thin circuit traces configured in spiral like geometry. A combination of line width, number of turns, shape and conductor length define the inductance. Figure 3-6 shows a spiral inductor commonly designed into a circuit structure. The spacing between turns will determine the resonant frequency of the inductor. A wider spacing, for example, will typically reduce capacitance and raise the inductance frequency. Although no special materials are required to form inductors, introduction of a ferromagnetic material can increase inductance values.

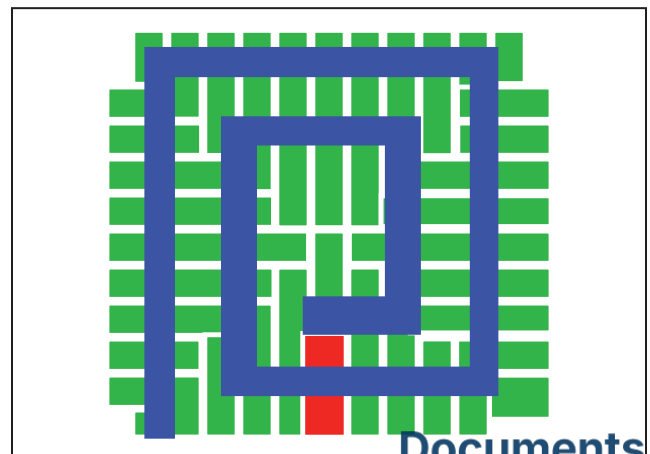


Figure 3-6 Inductor Detailed Cu Pattern

3.1.2 Active Transistors, Memory and Logic

Transistors – Discrete elements can be integrated into the circuit structure using thin films of organic or inorganic compounds. One printable inorganic semiconductor adapts an amorphous combination of InGaZnO (amorphous indium gallium zinc oxide, a-IGZO) that can be cured at low temperature. Electrodes in these transistors are typically metal, but they may consist of conductive organic compounds.

Memory – Based on the use of functional polymer material and flexible films, memory functions have been developed to provide data storage within the circuit structure. These unique materials are ideally suited for consumer products such as personalized toys and online-enabled game cards, authenticity identification, smart packaging, displays, organic LEDs, organic solar cells and all-printed radio-frequency identification (RFID) applications. Widespread use of organic semiconductor materials is predominantly in a surface printing application, as opposed to being embedded within a printed board.

Logic – Printing inks used to create semiconductor functionality consist of conductive and semiconductive conjugated polymers and/or other nano materials that are formulated into solvents. Printing is done one layer at a time (semiconductor, conductor, insulator, resistor and dielectric). Each layer is deposited using advanced printing systems enabling feature sizes as small as 10 μm [0.0003 in] and the layers need to align precisely for the device to function properly.

3.2 Embedded (Placed) Technology Preformed discrete components can be integrated within layers of the printed board. The highest level of interest is primarily focused on miniature passive capacitors and resistors (typical of that shown in Figure 3-7) since they represent the majority of components used on a printed board. See also 6.4.3.

A number of companies, however, are also embedding uncased active semiconductor devices within the circuit layers. The substrate manufacturing process combines printed board fabrication, component packaging and assembly into a single manufacturing operation. The benefit of combining processes can result in simplified logistics, more efficient material use and better equipment utilization.

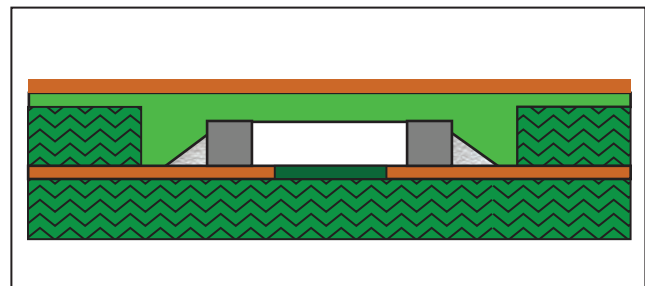


Figure 3-7 Embedded Discrete Passive Device Attached to Printed Board Inner Layer Surface

3.2.1 Passive Resistors, Capacitors and Inductors

Discrete Resistors – A wide value range of miniature resistors are available for embedding within the printed board or substrate structure. Both thick- and thin-film resistors are offered in a 01005 case size (0.40 mm x 0.20 mm x 0.13 mm [0.0157 in x 0.0078 in x 0.0051 in]). Although these devices have a low power rating (0.031 W), the operating temperature range (-55 °C to 125 °C [-67 °F to 257 °F]), resistor values and tolerances specified are the same as the larger resistor body size components.

Discrete Capacitors – The size and value range of general purpose multilayer ceramic capacitors suitable for embedded circuitry applications is not as broad as the resistor family noted in the preceding. The primary factor impacting thickness will be the specific dielectric type and value. Small outline capacitors with the X7R dielectric, for example, are available in a 0201 case size (0.60 mm x 0.30 mm x 0.15 mm [0.0236 in x 0.0118 in x 0.0059 in]). X7R formulations are called temperature stable ceramics and fall into EIA Class II materials. X7R is the most popular of these intermediate dielectric constant materials with an operating range of -55 °C to 125 °C [-67 °F to 257 °F].

Discrete Inductors – Inductors are available in outline formats typical of the resistor and capacitor families. A thin-film multilayer example has a 01005 body size (0.4 mm x 0.2 mm x 0.2 mm in height [0.0157 in x 0.0078 in x 0.0078 in]), with an inductance range between 0.4 nH to 9.1 nH. Multilayer ceramic inductors as small as 0402 (1.0 mm x 0.5 mm x 0.5 mm [0.0393 in x 0.0196 in x 0.0196 in]) are available as well, in values that range between 1.0 nH and 120 nH.

3.2.2 Active Transistors, Memory and Semiconductors

Discrete Semiconductors – Embedded semiconductor technology has been utilized in small-volume production by a few European and Asian manufactures for several years. The first volume application that adopted embedded semiconductor technology was by Murata in Kyoto, Japan. Casio's Tokyo factory manufactured a mobile TV tuner module in which they embedded a processor die within an organic multilayer printed board. A flip-chip configured SDRAM memory component was mounted onto the outer surface using conventional SMT processes (see Figure 3-8).

By embedding the semiconductor on an inner layer directly in line with a related semiconductor package mounted on the outer surface, the conductor interface can be minimized. With the die element mounted within or onto the substrate interposers core layer, resin-coated Cu (RCC) is laminated over the area to enable circuit interface to the layers above. The interface is made through small microvias that are laser ablated and plated directly to the bond-sites of the die element. Additional layers are sequentially built-up on the substrates base to complete the interface to the outer surface layers of the interposer.

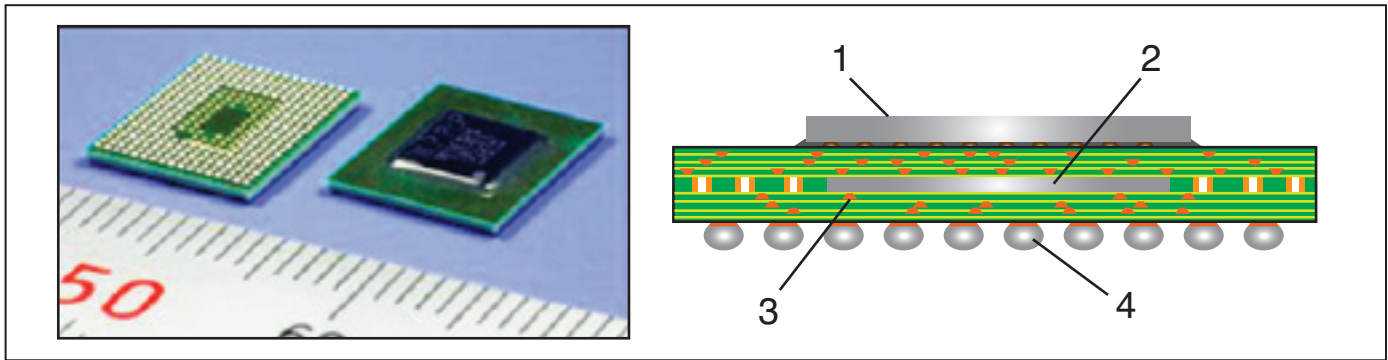


Figure 3-8 Embedded Process Die into Component Package Interposer

Figure source: Casio Micronics

- | | |
|---|--|
| <p>1. 128 Mb SDRAM</p> <p>2. Embedded Processor</p> | <p>3. 3-2-3 substrate interposer</p> <p>4. Solder ball contacts for SMT mounting</p> |
|---|--|

Other methods of embedding semiconductors that are in use besides the face-up microvia interconnect involve face-down bonding. One method of face-down bonding is to interconnect the die bond pads, using solder, conductive adhesive or anisotropic conductive film, directly to mirror image pads on the substrate surface. Another variation of this is Au-Au bonding, when both the die and substrate pads have been Au bumped or plated. When using solder or conductive adhesive attach, the die will typically be underfilled prior to adding circuit layers over and around the die.

Another method of face-down bonding is similar to face-up bonding, except the die is adhesively bonded, active side to the substrate, forming additional layer(s) of dielectric and Cu foil or RCC over and around the die, and then laser drilling and plating microvias from the back side up to the die bond pads. In this case, the initial substrate would be a thin-film dielectric (e.g., polyimide) or a Cu foil. In either case, the thin-film dielectric or Cu foil may be temporarily bonded to a carrier substrate for ease of chip placement. Of the described methods of embedded semiconductors, face-up or face-down bonding with microvia interconnects seem to be the most prevalent methods in use.

Another type of active device that may be placed alongside a large silicon chip or within the board in a manner similar to the passive devices is the diode or diode arrays used as protection devices. Embedding discrete active devices such as analog devices and circuit protection diodes and transient voltage suppression (TVS) devices can save board space and improve performance with parts sized similar to passive devices.

3.3 Material Requirements The base platform for embedding components is typically one of two material sets: alumina (ceramic) or a high-glass transition temperature (T_g) glass-reinforced epoxy laminate. The base structure (interposer) needs to be mechanically stable enough to withstand the process temperatures of the entire assembly and fabrication processes. The material sets selected need to be able to accommodate either formed or placed passive and active component elements.

3.3.1 Mounting Materials

Multilayer Ceramic – Figure 3-9 illustrates the layering of a ceramic-based substrate with a cavity section for embedding a single uncased semiconductor element.

Organic Based Multilayer – Because of the strong infrastructure and fabrication process versatility, organic glass-reinforced resin-based material dominates the embedded circuitry printed board and substrate market. shows a typical organic-based multiple Cu layer substrate structure interconnected with laser-ablated, Cu plated via holes.

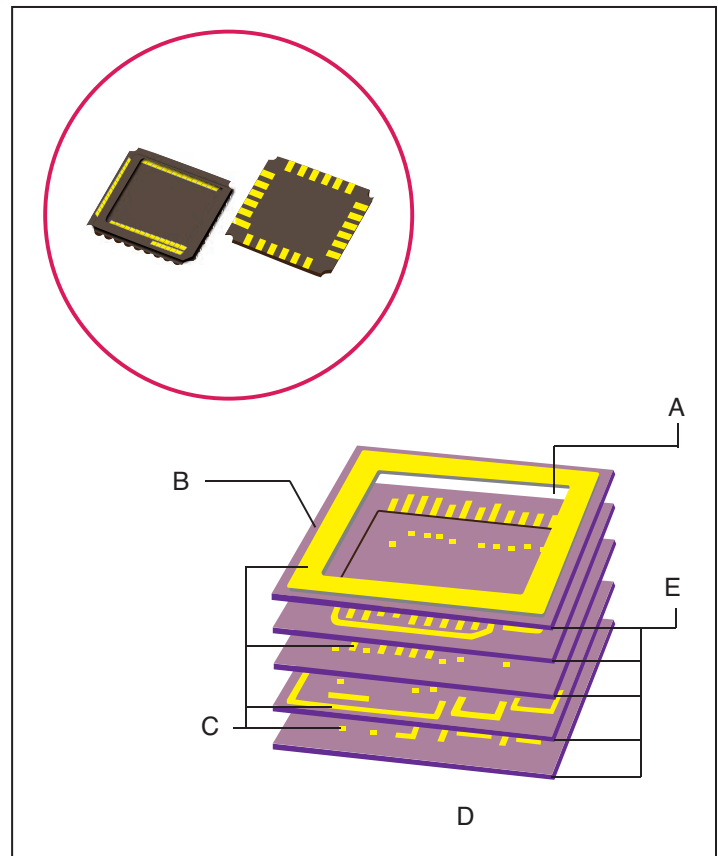


Figure 3-9 Multilayer Ceramic Substrate for Packaging a Single Semiconductor Element

- | | |
|---|---|
| <p>A – Irregular-shape processing technology</p> <p>B – Material technology</p> | <p>C – Metallization technology</p> <p>D – Design technology</p> <p>E – Multilayer ceramic technology</p> |
|---|---|

3.3.2 Component Formation Materials Embedded passive devices and the phrase embedded passives are considered to be equivalent. A number of manufactures have developed materials that can be used for the fabrication of embedded passive resistor and capacitor devices within the finished printed board substrate. There are two documents that furnish detailed information regarding the materials developed for forming passive component elements within the circuit structure. IPC-4811 describes materials that can be used for the forming resistor devices within the finished printed board substrate. It provides information on general classifications and associated characteristics of embedded passive device materials. IPC-4821 provides information on general designations and associated characteristics of formed capacitor materials.

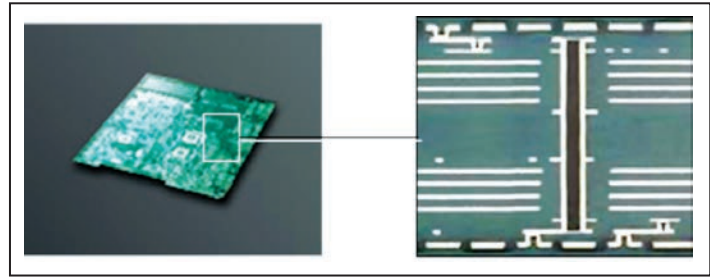


Figure 3-10 Organic Based Multilayer Circuit Structure

Figure source: *Ibiden*

3.3.3 Attachment Materials

Resistors – Laminate-like resistor materials defined in IPC-4811 are thin layers of high-resistance material that are placed between the Cu foil and dielectric material of the inner layer board. They could be on one or both sides of the double-sided laminate. The Cu foil and deposited resistor material are typically etched into different patterns using two different etch steps. The resistor material is commonly supplied as a coating on one side of Cu foil. This Cu-based layer is commonly used to form an additional circuit layer on a build-up multilayer printed board (embedded within the layers or on the outer-layer(s) of a multilayer board when easy access is needed for post-fabrication laser trim of the resistor element).

Capacitors – IPC-4821 defines two methodologies used to form capacitor elements within the printed board structure:

- Laminate (Cu-dielectric-Cu)
- Nonlaminar using deposited materials

Laminate-like capacitor materials take the form of a thin dielectric layer with or without Cu foil or other metal cladding on one or both sides. The dielectric may be reinforced with glass cloth like conventional FR-4 or nonwoven aramid fibers. The dielectric may be polymer only, polymer filled with ceramic powder, a thin layer of metal oxide or a thin layer of ceramic.

Nonlaminar-like capacitors use dielectric and sometimes conductor materials that are supplied in the form of paste, liquid, powder or vapor-deposited material. The capacitor dielectric is terminated between two conductor features. The two conductor features may be Cu foil or some other electrically conductive material that is applied by screen printing, plating or sputtering. As with the laminate-like materials, the embedded passive capacitor device is applied by the printed board fabricator during inner layer fabrication processes.

3.3.4 Encapsulation Materials Encapsulation materials are generally an organic-based dielectric composite applied over already formed discrete embedded resistors and capacitors. The material acts as a passivation to protect the discrete elements from exposure to the subsequent printed board chemistries and processes. For instance, an encapsulation material may be placed over a formed resistor to prevent interfacial attack between the conductor and resistor materials that could occur during prelamination bond enhancement processing or simply to planarize the structure to minimize damage that could occur from the high pressure of the lamination process. Encapsulant materials can also be used to prevent mechanical damage such as abrasion, scratches or flexing of the thin core materials. The primary intent is to ensure correct resistor and capacitance values are maintained after completing fabrication of the board.

3.4 Cost Analysis Economics encompass an assessment of the total life cycle cost of a design decision where the lifecycle includes the circuit and fabrication process, design, manufacturing, testing, reliability, marketing, sustainability and end-of-life of the product. The decision to convert a design using discrete components to a design using embedded circuitry has more ramifications than reducing the cost of part procurement and paying more for the board. In addition, there are hosts of other cost and benefit issues to be considered that will translate into lifecycle costs at some level.

While the cost advantages for use of embedded circuitry may hinge on various factors, they will reduce assembly costs, shrink the required board size and eliminate purchasing and handling costs associated with traditional assembly using surface mount component technology. Note that in the case of embedded placed components, some of these costs will not be eliminated, but rather transferred from the printed board assembler to the printed board fabricator. In addition, there are some significant performance benefits in locating passive components closer to their associated signal pins or with embedding the die element into the substrate.

These economic advantages or performance improvements need to be traded off against the higher cost (per unit area) of boards fabricated with embedded circuitry and possible decreases in throughput and yield of the board fabrication process.

In considering only passive components, the application-specific costs depend on many effects when embedded passives are present in a printed board. Table 3-3 shows the positive and negative factors that influence the decisions to embed either formed or placed passives into the multilayer structure.

Table 3-3 Factors That Impact the Decision Process for Embedding Components

Positive Factors	
Increases	Decreases
Number of printed boards fabricated on a panel due to decreased board size	Smaller printed board area due to a reduction in the number of SMT passive components
SMT component density resulting in better signal quality	Printed board design simplified due to the integration of resistors and bypass capacitors within the substrate
Potential for higher second-level assembly process yields	Reduced layer count, overall assembly costs, solder process defects and rework
Negative Factors	
Increases	Decreases
Printed board cost per unit area due to process complexity	Printed board fabrication throughput impacted by process variables
Wiring density requirements due to the reduced printed board area	Overall printed board fabrication yield due to process related defects

Several other recurring system costs may also be affected by the use of embedded passives. For example, the need to electromagnetically shield the board may be reduced or eliminated when certain passives are embedded (saving on expensive materials and their assembly), and the costs associated with thermal management of the board may also be affected. Another significant factor to note is that a defective embedded circuitry cannot be reworked or repaired like a typical SMT or through-hole assembly, but rather the entire unit may need to be scrapped.

Due to the conflicting nature of many of the effects listed in Table 3-3, the overall economic impact of replacing discrete passives with embedded passives is not trivial to determine and, in general, yields application-specific guidelines instead of general rules of thumb. The very nature of tradeoff analysis is one in which the greater the detail necessary to accurately model a system, the less general and more application-specific the result. The more exotic the application, the more the analysis needs to consider cost performance conditions and sometimes time-to-market opportunities, especially when embedded active circuitry is being considered.

3.4.1 Fabrication and Manufacturing Cost Modeling The results of the initial analysis in embedding passive components can determine the basic system cost. A representative modeling process can also provide additional information that demonstrates the effects that need to be considered in the model. Some of these are:

- 1) Accumulate the area of the component size including land patterns of discrete passives to be embedded
- 2) Reduce printed board area by the accumulated discrete passive area from step 1
This step is optional (i.e., the printed board area may be fixed.)).

- 3) Formed and placed resistors

Determine the area occupied by each embedded resistor on wiring layers. Perform routing analysis, removing nets and vias associated with resistors that are embedded and accounting for area blocked by embedded resistors on wiring layers. Routing is assumed to be unaffected by discrete resistors embedded using subtractive thin-film materials or similar dedicated layer addition approaches. All nets and vias associated with embedded bypass capacitors are removed from the routing problem, and it is expected that embedded singulated capacitors do not affect routing analysis. Using these assumptions, determine the relative change in routing resources due to embedding selected passives.

- 4) Compute the number of required layer pairs for the embedded passive implementation

Do this using the layer requirements, the relative routing requirements for the embedded substrate and either a fixed measure of the routing efficiency associated with the conventional board or a range of possible efficiencies. Determine these efficiencies under the assumption that the conventional version of the board did not include any more layer pairs than it needed to route the interconnects.

- 5) Compute the number of printed boards per panel (number-up)

Gather this information using the board size and the effective panel fabrication costs (layer and material requirements, yields and resistor trimming costs).

6) Determine the relative printed board fabrication cost variation using layer pair throughput modeling

A layer pair variation model can be based on throughput between a standard layer pair versus one that is being prepared for embedding passive components. Note that fabrication cost and throughput are not always synonymous (i.e., a long bake process can significantly impact throughput, while having minimal impact on cost).

7) Accumulate passive formed component costs or passive placed assembly cost, test, rework and printed board fabrication costs (lamination, relamination blind/buried via etc.) to obtain total relative cost

8) Determine the yield of layer pairs that include embedded passives

9) Determine the trimming cost for embedded formed resistors

The necessity of trimming is determined by the resistor's tolerance. The application-specific cost per trim is determined by modeling the throughput of a laser trimming process. Since laser trimming can only increase resistance value, it may be necessary to consider 100% laser trimming. This will be dependent on end-use specifications and as-formed resistor tolerance.

The analysis in Figure 3-11 focuses on differences in system cost between embedded passive and discrete passive solutions. Therefore, all cost elements that are approximately equivalent for the embedded and conventional system are effectively ignored (i.e., all functional testing of the system and procurement and assembly costs associated with nonembeddable parts).

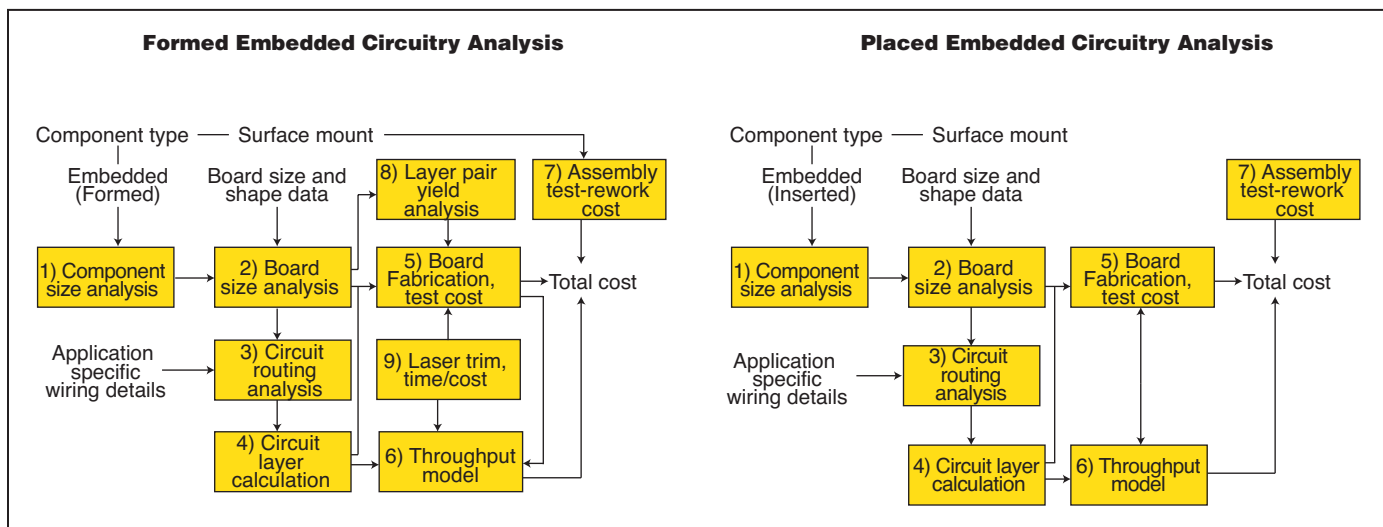


Figure 3-11 Comparing Cost Models for Embedding Passive Components

3.4.2 Lifecycle Costs Affected by Embedded Circuitry

Lifecycle activities that will be affected by embedded passive or active components include:

- **Design costs** – Include costs of engineering and other technical personnel and tools to design, verify and test boards that include embedded circuitry. This includes costs for specialized training and new CAD tools, library models for embedding passive or active components and any other specialized design tools for embedded board design and verification. Also included in the design costs are prototyping costs. Embedding components may also affect the degree to which a design can be reused and upgraded (redesign and retrofit costs).
- **Nonrecurring costs** – Equipment is not the only nonrecurring cost that may be associated with embedding components. There will be additional tooling (artwork) for layer pair production, additional chemistries to be managed during the board fabrication process, and licensing fees and royalties may need to be paid for the use of technology, material and/or processes. Most of these costs will be absorbed in the board procurement.
- **Time-to-market** – If the design, verification and prototyping of the embedded circuitry printed board requires more time than for a conventional printed board, this additional labor cost needs to be considered in determining which technology to use. Delays in time-to-market for a new product of weeks or months may cause significant revenue loss and, in some cases, the opportunity for timely market introduction may be lost.
- **Performance value** – Embedding components may provide size or performance improvements in a system that enables increases in market share for the manufacturer. It may be possible that for some quantifiable increase in system cost, a manufacturer can differentiate itself from its competition by providing a product that is lighter, smaller, faster, more reliable or possesses greater functionality than its competition, and the customer is willing to pay extra for one or more of these improvements. Embedding strategic active components may also protect the intellectual property of the product owner.

- **Qualification and certification** – The introduction of new materials and processes into board fabrication requires material providers and board fabricators to assess and possibly update safety certifications (e.g., UL certification). While the cost of this type of certification is not directly borne by the users of embedded circuitry, it will be reflected in the printed board costs. Conversely, there may be a reduction in costs associated with qualifying discrete component manufacturers.
- **Liability** – Embedding passive and active components or any new technology, material or process may carry with it unforeseen financial liabilities. The manufacturer will be liable for the material(s) impact on user or employee health or the environment. Long-term studies of the effects of the materials and the processes used to incorporate components into boards may be necessary to prove or disprove liability claims.
- **Sustainability** – A collection of many activities, all of which have an economic impact. In general, sustainability is all the activities necessary to:
 - Keep an existing system operational
 - Continue to manufacture and field versions of the system that satisfy the original requirements
 - Manufacture and field new versions of the system that satisfy evolving requirements
 - Adjust to changes in system reliability either as warranty costs (replacement) or as maintenance costs (repair)

Conventional wisdom is that system reliability will improve with embedded circuitry because of the reduction in the number of solder joints; however, this will only be realized if the end-product reliability does not commensurately decrease due to other specific effects.

Sustainability, however, goes further than reliability driven replacement and repair. Sustainability also means that the system should remain manufacturable through the end of its support life (to fulfill additional requirements for new product and spare replenishment). Embedded passives and actives may mitigate some obsolescence problems by replacing discrete parts that would become obsolete. Conversely, if the materials used to manufacture formed embedded passives within the board become obsolete (i.e., replaced by newer materials), the overall obsolescence problem may well become much worse.

- **Environmental and end-of-life** – The fabrication of passive components within boards may affect the volume of waste produced during the board fabrication process. Disposition of board fabrication waste is a significant contributor to the price of boards. If any of the materials selected for embedded passive components contribute to the waste stream and are considered hazardous, then the waste disposition costs could increase. Waste disposition is also a factor at the other end of the lifecycle (i.e., at end-of-life). Depending on the type of product the embedded substrate board is being used within and the location in the world where the product is being sold, the manufacturer may bear some or all of the cost of disposing of the product when the consumer no longer uses it.
- **Financial** – Several costs associated with creating and holding inventory (handling, storage, procurement) associated with discrete passive and active components are potentially avoided, including the money invested in stored components as opposed to being invested elsewhere. Conversely, in the case of embedded placed components, these inventory costs are transferred from board assembler to board fabricator.

3.5 Product Safety Design Considerations Including embedded circuitry in printed boards may initiate the need for testing to determine compliance with the safety concerns listed in the end-product UL Standards. These end-product standards designate compliance with UL Recognized Component Standards for printed board laminate materials: UL 746E, UL 796 and UL 796F. Some low-voltage or low-energy printed boards may only require flammability compliance, but most consumer end products require additional types of compliance.

The fabricator may need to supply samples for UL testing not only for the added embedded circuitry and/or materials, but possibly because the embedded circuitry processing may drive temperature, time and/or concentration limits beyond which the fabricator has already been qualified for. In another example, the fabricator may need to replace a smooth Cu foil with one of higher roughness to achieve better adhesion. This change of Cu foil would also require additional UL testing. Also note that the change in Cu foil type may affect electrical performance of the entire circuit, which would not be evaluated by UL testing, but instead would fall back on the original circuit designer. The UL compliance requirements are for safety, not to verify if the printed board works properly.

3.6 Case Study and Decision Making Embedded circuitry can increase the cost of the raw board, so technical evaluation will need to be done to justify the implementation of embedded circuitry. To justify embedded circuitry, the designer needs to determine the resistors, capacitors, inductors and any active device(s) prior to CAD layout. Evaluation of cost should be based on a cost of poor quality (COPQ) projected estimate in the early stages of design or an actual COPQ after the product has been released to production for the purpose of respin and/or improved design.

Resistors for embedded are determined based on the number of resistors within a 10X range of the same value. Pull-up and pull-down resistors are highly recommended for embedded technology. Pull-up resistors are used in electronic logic circuits to ensure inputs to logic systems settle at expected logic levels if external devices are disconnected or high-impedance is introduced. A pull-down resistor works in the same way but is connected to ground. It holds the logic signal near 0 V when no other active

device is connected. Also, the selection of resistive material and the value of resistive sheet are determined by the value of components. Multiple component values can be used on a single resistive sheet.

Capacitors for embedded are determined based on the total quantity of placement with the same value capacitors to be embedded. Decoupling capacitors are highly recommended for embedded technology.

Inductors for embedded are determined based on the total quantity that can achieve nominal design value when formed within existing circuit layers, with or without the addition of a ferromagnetic material. Q factor capability is also an important consideration for embedding. If multilayer inductors are being considered, the designer needs to also consider the impact of added via interconnects and may choose to reserve these for build-up layers of a high-density interconnect (HDI) printed board. For large inductance values or High Q requirements, the designer may consider embedded placed discrete inductors.

Active components such as application-specific integrated circuits (ASICs), memory, diodes and diode arrays are determined in the early stages of the design. This will determine the layer count, physical location, power dissipation, routing and testing access. Actives such as diodes and circuit protection are often considered late in the design and can delay final release and qualification. Early consideration and inclusion into embedding with similarly sized passive devices can lead to performance improvements and earlier project completion dates.

3.6.1 General Case Study Every design needs to be evaluated for yield, complexity and design for manufacturability (DfM). These evaluation models are highly recommended to determine the availability of real-estate utilization, manufacturing violation and yield production.

- The projected first-pass yield is the measurement of production effectiveness that determines the level of rework and touch up, which captures the impact of complexity and process capability.
- Complexity will determine the level of density and availability of real estate and provide a unique view into the relationship between complexity and cost.
- DfM analysis capture first-order DfM drivers, defines key design and process attributes and quantifies the impact of manufacturing violations.
- These analyses provide the ability to calculate and determine the COPQ. The return on investment needs to be defined and calculated using COPQ to determine the feasibility of the implementation of embedded circuitry technology.

3.6.2 Scenarios for Embedded Circuitry Engineering designed a printed board assembly with fewer than 500 components, with single-sided mixed technology, six layers stack-up and a 6 x 9 area. The board has one BGA (50 mils pitch) and fewer than five active components.

In this scenario, the CCA is a single-sided board, which indicates that the board is not using all the available real estate. The level of layer count is very low; the number of active components is less than five, which indicates light density of I/O and low placement population. Therefore, this board is not a good candidate for embedded circuitry (see Table 3-4).

Table 3-4 Case Study Examples

	Layers	Technology	Sides	ICs Qty	Ball Grid Array (BGA) Qty/pitch (mm) [in]	Total Component Count	CCA Area (mm) [in]	Comments
Case 1	<8	Mixed	1	<5	1 / 1.0 to 1.25 [0.0393 to 0.0492]	< 500	152 x 228 [5.984 x 8.976]	Real estate availability, layer counts, number of ICs and BGAs indicate this design is not a good candidate for embedded devices.
Case 2	8 to 14	Mixed	2	>5	>5 / 0.8 to 1.0 [0.0314 to 0.0393]	> 500 < 2,000	152 x 228 [5.984 x 8.976]	The high number of ICs and BGAs pitch indicate this design is potential for embedded devices.
Case 3	>14	Mixed	2	>10	> 6 / < 0.8 [0.0314]	> 2,000	152 x 228 [5.984 x 8.976]	The high layer count and ICs quantity and BGA pitch indicate this design has high potential for embedded devices and HDI stack-up design.

4 COMPONENT CONSIDERATIONS

The discrete component parts selected for embedding within a multilayer printed board or interposer structure will be subjected to a number of physical stress conditions. The initial placement of the device onto the inner-layer substrate surface is not a significant concern, but the printed board manufacturing process is a complex series of operations. The most stressful operation in the process is lamination. This equipment relies on steam, electric or hot-oil heated beds that can reach temperatures of 150 °C to > 200 °C [302 °F to 392 °F]. Many systems rely on vacuum to provide a uniform pressure and manage outgassing. The pressure on the laminate during the heating cycle can be as high as 40 Kg/cm² [568 psi] for up to two hours. Following the press operation, the panels are transferred from the hot press to a cold press to cool the material to ambient temperatures. This process may be repeated several times for more complex build-up structures. Build-up layers might be done at significantly lower temperatures and pressures than those described here, depending on the build-up dielectric material that is selected.

4.1 General Requirements Components selected for embedding within the circuit structure needs to be able to withstand the multiple thermal and pressure conditions that occur during the build-up lamination process. In addition, the terminal plating on the component parts need to have a metallization that is compatible with the joining process selected (see 6.3.2).

4.1.1 Part Robustness Evaluations To be compatible with the lamination processes involved, the component parts selected for embedding, passive or active, may be as thin 25 µm [0.0009 in]. Passive device outlines selected will typically be no greater than 0.3 mm x 0.6 mm [0.0118 in x 0.0236 in] and are not likely impacted by fabrication stresses. Larger passive device outlines and thin silicon-based semiconductors, however, are brittle and susceptible to cracking. Although all placed components will likely survive the lamination operations, there is always a possibility the substrate will warp during assembly processing. This is of particular concern when the substrate is exposed to the high temperatures related to reflow soldering. It is strongly suggested that the board designer utilize a balanced or symmetric stack-up in order to minimize the possibility or extent of warpage.

4.1.2 Test Method Correlation Accessing embedded circuitry to facilitate testing will require a strategy. The fabricator of the circuit will have greater opportunity to access components for measuring continuity throughout the build-up process, but access to individual components will be limited. To best facilitate bare board testing of embedded passives, features on the outer surfaces need to be identified. It might be beneficial that rather than measuring individual component values at final board test, that the measurement may bundle the accumulated value established for several interconnected components.

4.1.3 Considerations for Discrete Values With placed resistors, there are few concerns for value selection. Placing discrete capacitor and inductor elements, however, is more restrictive. Capacitor value range is severely restricted with the smaller 01005 and 0201 outline devices. The issue is the limited volume of dielectric material and electrode area. More values may be available in the larger outline components, but they will be significantly thicker. The availability of inductor components in smaller form factors is limited. Silicon-based thin-film multilayer inductors are candidates for embedding, but they are brittle and the outline dimensions are relatively large.

4.2 Component Preparation Passive components, diodes and some transient voltage suppression (TVS) devices, even though they are very small, are typically furnished in a format that is compatible with robotic assembly systems. Diodes and small TVS devices are often shipped in tape and reel, just like many passive devices. Larger active components, however, are more likely to be furnished in tray cassettes.

4.2.1 Passive Component Issues Sourcing passive components from multiple suppliers is often necessary; however, when ordering these devices, the user needs to specifically define the terminal plating requirement. For solder attachment the Sn-plated terminal will be satisfactory. For conductive polymer attachment, the terminal plating may need to include a precious-metal surface finish, such as Ag or Au. When interfacing the component terminals with Cu-plated vias, ordering devices with Cu-plated terminals will be most compatible.

4.2.2 Semiconductor Die Issues Silicon-based semiconductors are processed in a wafer format. The silicon wafer size is typically dependent on the complexity of the die element and the required volume to meet market demand. The active element of the semiconductor is commonly interfaced with the next-level package or carrier using wire-bond technology with the contact metallization applied while the die elements remain in the wafer form. For flip chip or face-down bonding, there are numerous die attach techniques that have been developed to join the die-level device to the substrate. These include reflow soldering, ultrasonic, thermocompression bonding and anisotropic conductive and isotropic conductive polymer adhesives. Au-to-Au interface can be considered as well using thermocompression and ultrasonic energy to complete the flip-chip bonding process.

The bond pads or lands on the die are commonly furnished with Al alloy for Au wire bonding. No further preparation is required for embedding the die using wire-bond, ribbon bond or Au-bump interface. Flip chip is another method of attaching a wafer. In this method, solder bumps are added to the wafer prior to embedding, and the wafer is bonded face-up on the substrate. Flip chip requires solder, conductive polymer or a Cu via interface. The bond sites need to be prepared with a Cu or other metallization prior to placing the flip chip. For general information on flip chip applications, see IPC-7094.

4.2.3 Surface Redistribution Redistribution is the rerouting of existing bond pad locations to better accommodate flip-chip applications. I/O redistribution is a sequential process in which additional conductive layers are serially added to the active wafer surface to provide a uniform grid pattern typical of that shown in Figure 4-1.

Redistribution can provide a uniform array and standard contact assignment to better facilitate component-level testing and board- or module-level assembly. Factors affecting ease of this serial approach are die size, die bond pad size, contact pitch and location selected. The following sequence represents the basic process steps for surface redistribution:

- 1) Apply metal adhesion layer over the active side of wafer
- 2) Spin-coat photo resist over the wafer surface
- 3) Image and develop contact pattern
- 4) Electroplate Ni on the exposed contact sites
- 5) Remove photoresist
- 6) Chemically etch remaining adhesion layer metallization
- 7) Spin-coat photoimageable polymer over the wafer surface
- 8) Image and develop polymer to expose Ni-plated contact sites
- 9) Clean Ni-plated contacts/apply electroless alloy

Following the metallization process, individual die elements are separated from the wafer format using precision dicing saws.

Some suppliers offer die-level redistribution processing; however, die-level processing will typically be much more expensive than wafer-level processing. Nonetheless, die-level processing might be a good alternative at early development or prototyping stages of a project.

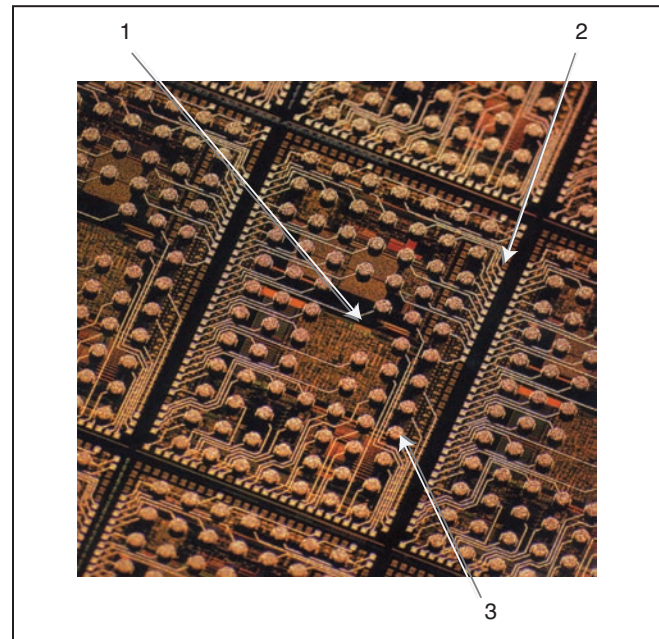


Figure 4-1 Redistribution of Wire-Bond Sites to a Uniform Array Contact Pattern

- 1 – Additive conductor pattern
- 2 – Wire-bond sites
- 3 – Uniform bump contact array

4.3 Post-process Validations Quality and reliability of semiconductor elements on a wafer are ensured through electrical testing and controlled screening methods. Wafer-level probe testing is typically used to perform basic analysis, but it is not widely utilized for performance sorting, reliability screening or massive parallel contacting. The most thorough and reliable electrical testing of the individual die element is when bump or ball contacts are furnished or at the package level when devices can be socketed.

4.4 Known Good Die (KGD) Known good die (KGD) are bare die elements that can be relied upon to exhibit the same quality and reliability as the equivalent single-chip packaged device. In general, single-chip packaged solutions that are targeted for several markets are tested and screened to some common level. This is the most stringent testing that the die supplier can cost effectively perform that satisfies a majority of users. If a particular part number is to be used for critical high-reliability applications requiring lower failure rates (e.g., aerospace, automotive, medical), then a special test and screening procedure can be specified to obtain the higher quality and reliability probabilities, sometimes referred to as up-screening. Consequently, KGD processing requires that die be up-screened during wafer-level probe testing or with a subsequent die-level tests and screens to meet the higher package part quality and reliability targets. The die supplier and user need to agree on the quality and reliability levels that are needed and accept the associated costs for the additional tests and screens.

Quality classification of the die is critical for embedded applications. Although the overall yield on the wafer can be very high and acceptable for conventional single-die packaging, it is strongly recommended that the embedded die candidate be electrically tested before use (see Table 4-1).

Table 4-1 Bare Die Quality Classification

Level	Visual Mechanical Inspection	Electric Characteristics	Early Failures	Long-Term Reliability
Level 1 (KGD)	Sampling specified on product specification	All test items ensured ¹	Ensured ²	Ensured ²
Level 2 (KGD)	Sampling specified on product specification	All test items ensured 1	Not ensured	Not ensured
Level 3 (probed die)	Sampling specified on product specification	Some tests skipped	Not ensured	Not ensured

Note 1. Corresponding to the specified criteria for packaged products

Note 2. The same criteria level as packaged products with burn-in

5 MATERIALS

Each embedded circuit structure will have a unique functional requirement. There are several key factors to consider when selecting materials for an embedded circuitry product:

- Process compatibility
- Physical robustness
- Reliable source of supply
- Use environment
- Cost

This section provides basic criteria for primary material sets commonly used in the fabrication of embedded circuitry substrates.

5.1 Organic Resins The organic platform typically selected for integrating passive and active elements is a high- T_g glass-reinforced epoxy laminate. A growing number of FR-4 laminates detailed in IPC-4101 offer mechanically stable reinforced dielectrics. Several compositions furnished with a relatively high T_g , provide a low dielectric constant (Dk) and exhibit excellent insulation properties.

Organic platforms are typically selected from the materials in Table 5-1. This table comes from IPC-2221 and is provided for reference only. See IPC-2221 for any updates to this table.

Table 5-1 Typical Properties of Common Dielectric Materials

Property	Material						
	Difunctional/ Multifunctional Epoxy (IPC-4101/21)	Epoxy/ Multifunctional Epoxy (IPC-4101/24)	Epoxy/ Multifunctional Epoxy (IPC-4101/26)	Epoxy Triazine (IPC-4101/29)	Bismaleimide Triazine Epoxy (IPC-4101/30)	Polyimide E-glass (IPC-4101/41)	Polyimide Nonwoven Aramid (IPC-4101/53)
Electric Strength (kV/mm)	47	50	53	47	46	51	51
Moisture Absorption (wt%)	0.17	0.15	0.15	0.1	0.15	0.44	0.6
Dissipation Factor (Loss Tangent) @1 MHz	0.022	0.022	0.021	0.008	0.011	0.012	0.015
Thermal Expansion xy-plane (ppm/°C)	12 – 16	12 – 16	11 – 16	10 – 14	10 – 15	12 – 17	6 – 9
Thermal Expansion z-axis below T_g (ppm/°C)	50 – 80	50 – 55	50 – 55	–	55 – 70	40 – 60	80 – 90
T_g (°C) (IPC-4101)	110 – 150	150 – 200	170 – 220	170 – 220	170 – 220	200 – 250	220 minimum
T_g (°C) (DSC)	140	170 – 175	175 – 180	210	185-200	250 – 260	240
Flexural Modulus (Pa)	1.86×10^{10}	1.86×10^{10}	1.93×10^{10}	1.93×10^{10}	2.07×10^{10}	2.69×10^{10}	4.8×10^8
Fill Warp	1.20×10^{10}	2.07×10^{10}	2.20×10^{10}	2.20×10^{10}	2.41×10^{10}	2.89×10^{10}	
Tensile Strength (Pa)	4.13×10^{10}	4.13×10^{10}	4.13×10^{10}	4.13×10^{10}	3.93×10^{10}	4.82×10^{10}	3.14×10^7
	4.82×10^{10}	4.48×10^{10}	5.24×10^{10}	5.24×10^{10}	4.27×10^{10}	5.51×10^{10}	

The term prepreg is an abbreviation for partially cured dielectric resin bonding agent that is embedded within a glass fiber weave to provide mechanical reinforcement or as nonreinforced sheets that are used to bond the reinforced dielectric and Cu circuit layer together. The layer stack is heated and pressed together to the prescribed finished board thickness. Prepreg sheets are available in several thicknesses, depending on the glass weave density, glass fiber size and resin volume (typically 50% to 60% by weight).

5.1.1 Multilayer Printed Board Stack-Up Design The goal of any printed board stack-up design is to select the material and specify the layer ordering such that it adequately delivers the required signal performance and power integrity at the lowest printed board cost. After the appropriate printed board material is selected, consider the following issues to design the layer stack. The total

number of layers required for a given design is dependent on the complexity of the board. These factors include the number of signal nets that need to break out from the ball-grid array (BGA) device, the number of power planes/pours and the component density and type of packages for those components. Typically, large BGA breakouts and individual power or ground plane requirements determine the final board layer count. For complex, field programmable gate array (FPGA) boards, the FPGA device in many cases is usually the largest BGA device on the board and thus determines the board's minimum layer count.

5.1.2 Selecting Relative Dielectric Constant The relative dielectric constant (ϵ_r) is a measure of a material's ability to be polarized by an electric field and store electrostatic energy, as well as its ability to facilitate signal propagation. The relative dielectric constant varies with frequency. Material datasheets often refer to this parameter as Dk. Low ϵ_r or Dk materials make excellent insulators and are good for isolating signals on adjacent layers. From a board designer's perspective, the benefits of a lower dielectric constant include the following:

- Better electrical insulation
- Faster signal propagation through the material
- Higher circuit trace impedance for a given trace geometry
- A reduction in stray circuit trace capacitance

Printed board manufacturers typically characterize ϵ_r at 1 MHz; however, the Dk of a material is generally an inverse function of its frequency. As frequency increases, ϵ_r is reduced. Because of this nonuniformity, a transmission line's impedance can vary from its calculated value at 1 MHz, causing it to differ from what a propagating signal actually sees on the channel. Because digital signals are composed of many frequencies (harmonics), the resulting difference in impedance that is presented to the different harmonics can cause signal loss from both reflections and phase distortion (phase jitter) arising from the different harmonics arriving at the destination at different times. Always choose lower ϵ_r material with a flat frequency response whenever possible for best signal performance and to minimize signal distortion and phase jitter.

5.2 Nonorganic Products The ceramic materials used in manufacturing multilayer substrates for electronics are classified as an inorganic, nonmetallic solid that is defined as a crystalline or partly crystalline structure. Because most common ceramics are crystalline, the definition of ceramic is often restricted to inorganic crystalline materials, as opposed to the noncrystalline glasses. High- and low-temperature co-fired ceramics (HTCC and LTCC) are particularly suited for applications with embedded passive elements and special signal interface requirements. Multilayer ceramic substrates are produced using a combination of metal pastes and ceramic green sheets. These green sheets contain a small percentage of organic content to achieve flexibility and enable punching and green cutting processes.

HTCC substrates are relatively low in cost, but they have limitations. The interconnection metals typically used for the HTCC are tungsten-based or molybdenum-based and, when compared to Au or Ag alloys commonly used for the LTCC process, offer lower electrical conductivity.

5.3 Conductor Characteristics (Cu Foil/Film) The circuit conductor used to interface with components (embedded or surface mounted) is most commonly a thin Cu foil (see Table 5-2). Cu foils are laminated to one or both sides of each dielectric layer, imaged and chemically etched to provide the circuit pattern. See also 8.5.1 for information on specifying Cu foil materials and 8.5.2 for information on determining Cu foil requirements.

Table 5-2 Standard Cu Foil Thickness

Foil Designation	Common Industry Terminology	Metric	
		Area Weight (g/m ²)	Nominal Thickness (μm)
E	5 μm	45.1	5.1
Q	9 μm	75.9	8.5
T	12 μm	106.8	12.0
H	1/2 oz	152.5	17.1
M	3/4 oz	228.8	25.7
1	1 oz	305.0	34.3
2	2 oz	610.0	68.6
3	3 oz	915.0	102.9
4	4 oz	1220.0	137.2
5	5 oz	1525.0	171.5
6	6 oz	1830.0	205.7
7	7 oz	2135.0	240.0
10	10 oz	3050.0	342.9
14	14 oz	4270.0	480.0



5.4 Component Forming Material Materials available for forming embedded circuitry include a broad number of formulations and process variations that are specific to the functional criteria required.

5.4.1 Embedded Passive Component Selection Criteria The first decision that needs to be made is whether or not to use a discrete or embedded solution. Depending on the application, cost, performance or some other metric may be the driving force for the decision. Several materials properties need to be considered when making the decision of whether or not to embed a particular component in a circuit:

- Available tolerance of the embedded parts
- Drift limits following thermal shock or humidity exposure
- Aging behavior
- TCC/TCR
- Power handling capacity (may include geometry of part)
- Breakdown field and leakage currents
- Q – especially important for RF and filter applications

Additional concerns include:

- Available space for embedded parts, especially large capacitor elements.
- Density of embedded parts – cost effectiveness of embedding components may be maximized at some intermediate component density.

There are a growing number of component types that can be considered for embedding (passive and active, formed and placed). The following will furnish guidance on applying the most common formed component methodologies (resistors, capacitors and inductors).

5.4.2 Formed Resistors A formed resistor will have two Cu lands with resistance material applied between the lands. The shape of the resistance material can be a simple rectangle or a shape designed to maximize resistor element length while minimizing area. In each case, the resistance material needs to overlap onto the Cu lands.

Resistor composition may come in either sheets or be printed from polymer formulations. Ceramic resistor technology should be AABUS.

Variations of some of the available commercial formed resistor material sets are shown in Table 5-3.

Table 5-3 Formed Resistor Material Variations

Application	Material type	Technology
Screen print	Polymer thick film	Formed
Thin-film ceramic ¹	Sheet form	Formed
Thin-film (NiCr) ¹	Sheet form	Planar
Thin-film (NiP) ¹	Sheet form	Planar
Thin-film (Pt) ¹	Sheet form	Planar

Note 1. Requires lithographic imaging and etching process

5.4.2.1 Thick-Film Resistors Thick-film resistor materials are formulated to furnish a wide range of primary values. The resistor formulations are based on phenolic chemistry that enables screen printing the elements directly onto prepatterned terminations on the printed board core followed by curing the product at temperatures in the range of 150 °C. An example of a printed board with screen-printed resistor elements is shown in Figure 5-1. This carbon-filled epoxy chemistry has been successfully used for a broad 0 of commercial applications.

Thick-film resistor technology is generally used when tolerances are less critical. Applications are varied and range from simple discrete potentiometers to pull-up and pull-down resistors. Thick-film resistors also have been used as strain gauges in mechanical diagnostic applications and in high-volume radio frequency (RF)

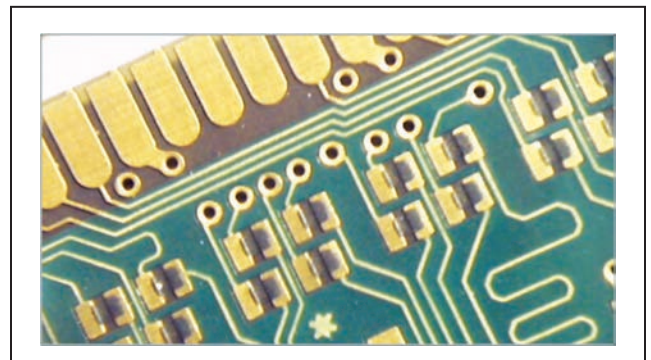


Figure 5-1 Carbon Thick-Film Resistor Example

applications. Figure 5-2 shows a cross-section of a printed resistor element.

5.4.3 Thick-Film Resistor Cost and Performance Material and processing costs related to printing thick-film resistors are typically lower than those related to thin-film metal and metal oxide systems. Moreover, the wide availability of PTF sheet resistivity ranges from 1 Ω/square to 1K ohms/square.

The overall performance of the thick-film resistor materials is related to the optimized circuit design and fabrication process. The materials and process parameters of polymer resistors need to be considered to successfully achieve the performance requirements of circuit designs. For example, the decision on the pad size to aspect ratio to use for a particular resistor element depends on a number of factors. These include target resistance values, electrical considerations, available paste resistivity values, trimming requirements and the distribution of resistances of all the resistors present on the same layer of the board (see Figure 5-3).

The resistance of a linear resistor is written as:

$$R = \pi \times L/A = (\pi/t) \times (L/w) = R_s (L/W)$$

The resistance value can be designed based on the equation of $R = R_s \times N$, where N is the number of squares or aspect ratio 1. Using these standard resistor thick-film equations, along with actual resistor linearity and blend curves, the designer will be able to calculate and design a variety of options for a given desired value. This variety of solutions to the same problem makes designing thick-film resistors embedded into printed boards more complex but more versatile than the selection of surface-mounted passive components. As shown in Figure 5-4, the linearity of the polymer resistors is very good and repeatable. The linearity of these materials will be helpful when designing for particular resistance values.

5.4.3.1 Thick-Film Resistor Design Embedding polymer resistors inside printed boards can be achieved using standard processing equipment. Most printed board fabricators are already equipped with screen printers and curing ovens or furnaces necessary for the

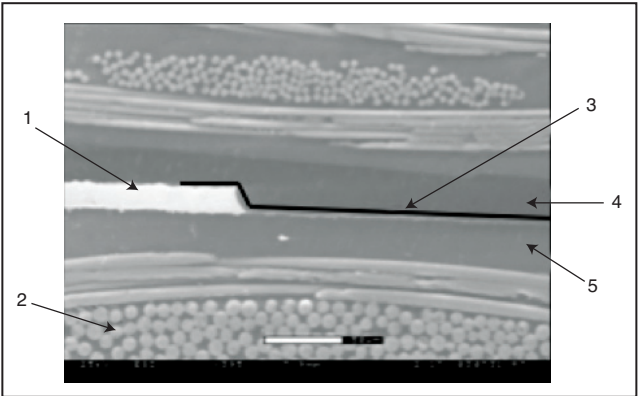


Figure 5-2 Cross-Section of an Embedded (Formed) Resistor Element

1. Etched Cu land on base layer

2. Glass fiber reinforcement

3. Formed resistor element (enhanced)
4. Prepreg on top layer

5. Resin cap on base layer

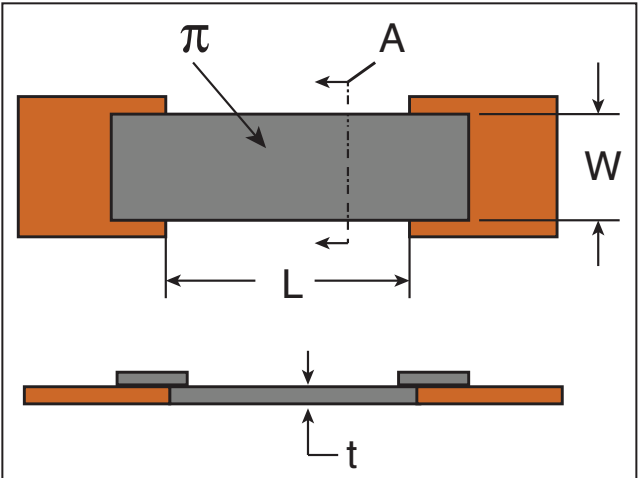


Figure 5-3 Geometry of a Printed Thick-Film Resistor Element

Figure source: DuPont Circuit & Packaging Materials

- π – Resistivity

L – Resistor length

w – Resistor width
- R_s – Sheet resistance in Ω/sq

A – Cross-section area

t – PTF thickness

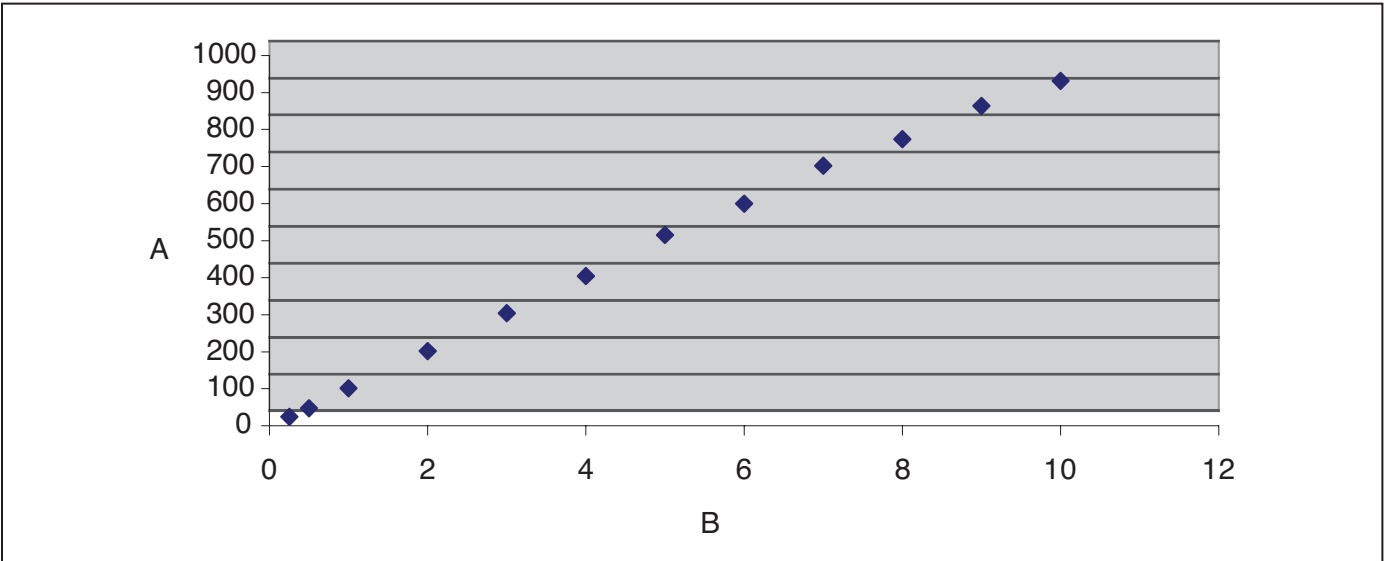


Figure 5-4 Linearity of 100 Ohm Polymer Resistor

- A – Resistivity (Ω)
- B – Number of squares

processing of PTF resistors. To achieve tight tolerances on the order of $< 2\%$ will require a laser trimming system. These polymer resistor inks are screen printed directly on the etched Cu terminations. The example shown in Figure 5-5 defines the primary features controlling the formed resistor element.

Suppliers recommend a Cu foil thickness of $17.5\ \mu\text{m}$ [1/2 oz] to achieve the best print resolution. PTF and ceramic thick-film resistors can be formed directly onto the laminate surface and require only conventional screen printing processing to provide the resistor pattern. The paste-like material is available in resistance values that range between $1\ \Omega$ and $1\ \text{M}\Omega$ per square, while ceramic thick-film material values will range between $10\ \Omega$ and $10\ \text{K}\Omega$ per square.

Examples in Figure 5-6 illustrate how the designer can adjust the geometry of a 1K basic value resistor material to achieve greater values.

The land pattern geometry provided for the printed image should allow for a nominal $0.25\ \text{mm}$ to $50\ \text{mm}$ overlap for the printed PTF material and include allowances for fabrication process variables. The alignment compensation illustrated in Figure 5-7 will ensure that the PTF image printed will maintain the target resistor value even when the resistor element is slightly offset.

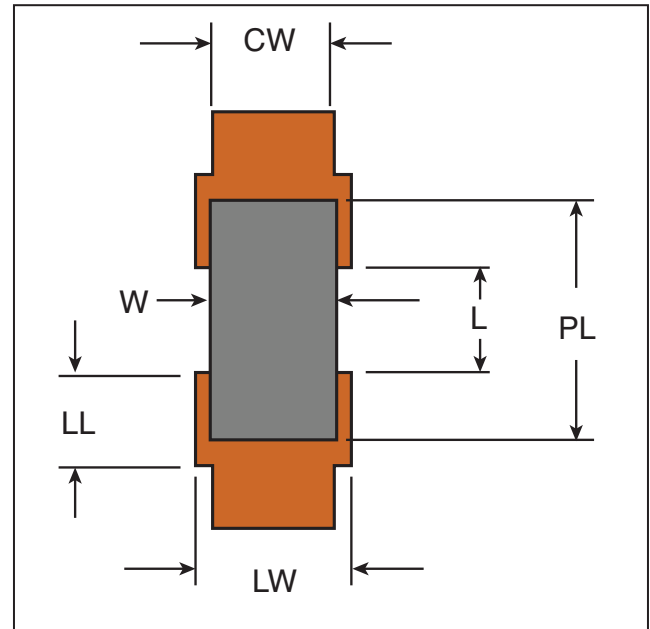


Figure 5-5 Primary Features of the PTF Resistor

L – Resistor length	LL – Land length
W – Resistor width	LW – Land width
PL – Print length	CW – Conductor width

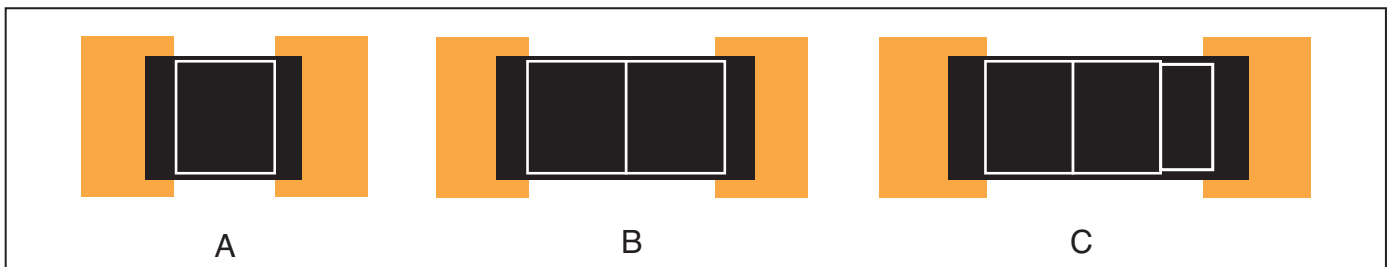


Figure 5-6 Increased Value Adjustment

A – 1 sq = $1\ \text{K}\Omega$
 B – 2 sq = $2\ \text{K}\Omega$
 C – 2.5 sq = $2.5\ \text{K}\Omega$

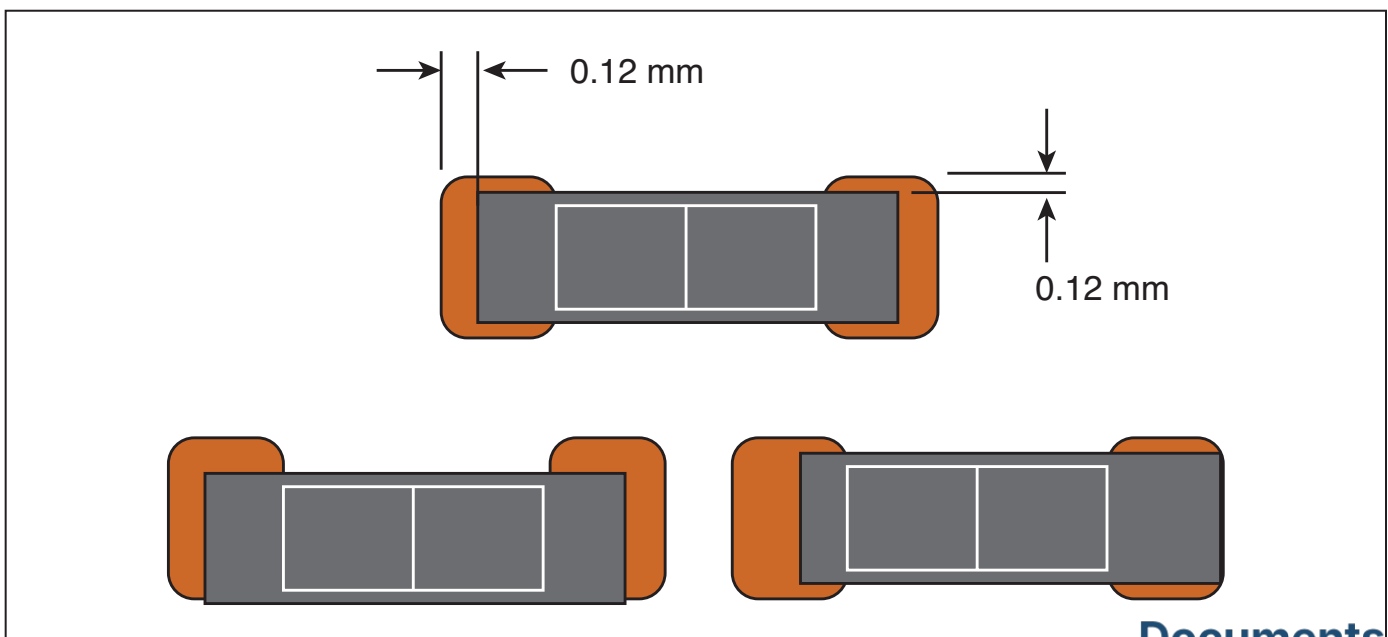


Figure 5-7 Land Pattern Geometry Compensation for PTF Printing

Due to printing and curing complexity and process time, the embedded circuitry printed board fabricator will prefer applying only one resistor value material onto the substrate base layer. To maximize the number of resistor elements on the circuit layer, several techniques can be considered to achieve greater utilization of the process. The examples previously furnished exhibit very basic value geometry requirements. By adjusting the geometry of the resistor element; however, the designer is able to create a relatively wide range of values.

Software packages are available which automatically integrate resistor dimensions into the circuitry. The examples furnished in Figure 5-8 compare in-line and serpentine geometries using the basic value/square ratio. This design method maximizes resistor element value potential while minimizing surface area.

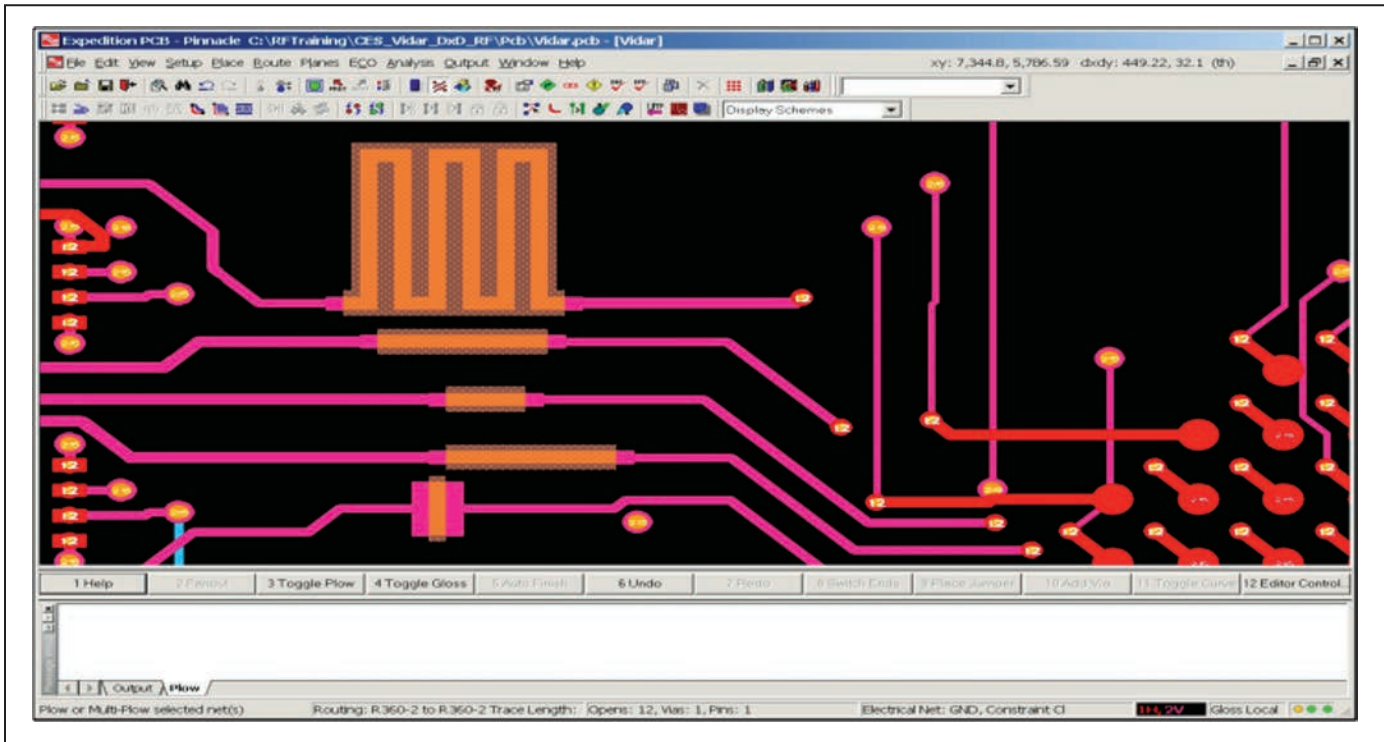


Figure 5-8 Serpentine-Configured Resistor Element

Resistor calculators can also be used to define size based on inputs of ohms, power and tolerance. The serpentine resistor examples shown in Figure 5-9 demonstrate the flexibility in designing resistor elements having more complex values.

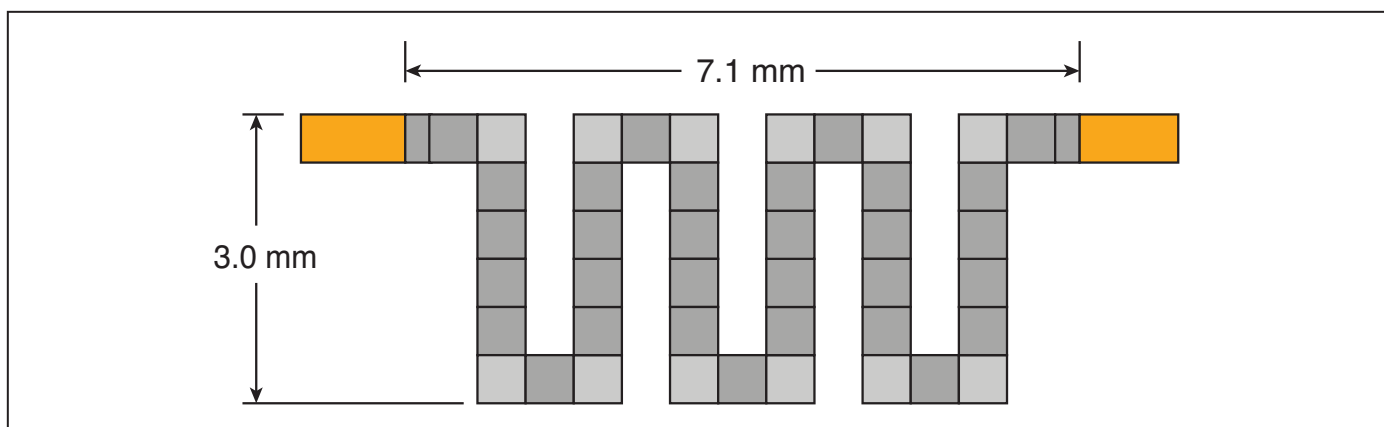


Figure 5-9 Serpentine Resistor Footprint

Figure note: 10 KΩ serpentine resistor footprint 250 Ω/square at 0.5 mm [0.020 in] spacing

5.4.3.2 Thick-Film Process Basics Anything that interferes with the interface of the Cu and printed resistor image may cause resistance value variation. For adhesion purposes, the Cu surface should be free of oils or other surface contaminations and minimal surface oxide. A standard micro-etch process that cleans the Cu surface is sufficient to promote good adhesion and prevent any negative effects on resistance. Because the polymer resistor can maintain good resistance stability, it can be printed directly onto the Cu terminations (immersion Ag treatment on the termination pads is not required).

Once the surface cleaning is complete, screen printing and curing can be performed. Using a standard screen printer with a vision system for registration purposes, the polymer resistor is applied to a cured thickness of 15 μm to 20 μm [0.0005 in to 0.0007 in]. Paste rheology enables good paste transfer, which leaves a resistor print with consistent, straight side walls. This characteristic, along with good thickness control, will provide resistance tolerances in the range of 20%. More precise printing is accomplished using standard stainless steel mesh screens with a backside emulsion buildup (rather than a solid metal stencil).

Curing the printed polymer resistor can be done in a box oven, an infrared furnace or a conventional convection belt furnace. Figure 5-10 shows a typical box oven profile. A two-step temperature profile is recommended for optimum resistor stabilities. The matrix will cross-link at 170 °C, but a heat bump is recommended for optimal performance. Infrared curing furnaces will enable faster cure cycles.

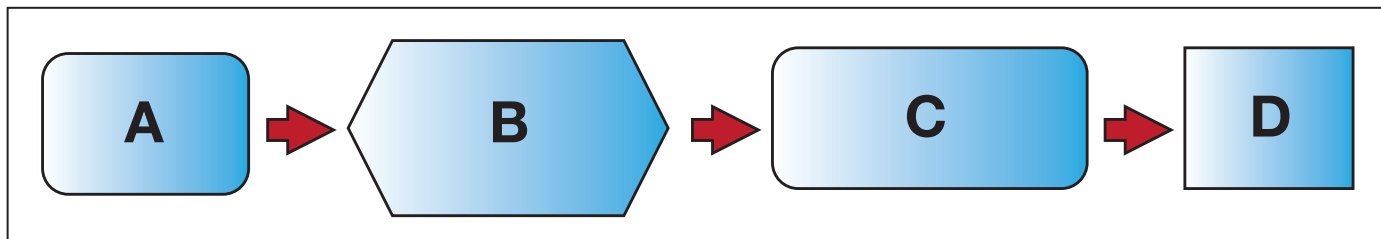


Figure 5-10 Print and Oven Curing Sequence

A – Screen print P1-R

B – Dry at 170 °C for 60 minutes in N_2 environment

C – Heat bump at 250 °C for three minutes in N_2 environment

D – Cooling at room temperature

After the curing process is complete, the panel is ready for further processing.

5.4.3.3 Laser Trim Process Laser trimming can be performed if closer tolerances are required. Laser trimming speeds more associated with ceramic thick-film resistors can be used when hot and cold TCR is within 0 ± 200 ppm. A standard L cut or double and triple plunge cuts are used to trim these resistors to a < 1% tolerance.

The examples shown in Figure 5-11 compare 10 Ω and 1,000 Ω resistors with clean laser-trim kerfs. The power setting, Q rate and byte size need to be adjusted to provide clean cuts without damaging the FR-4 substrate. While different settings may be required for various laser trimming equipment, the parameters are easily obtained with minimal test runs.

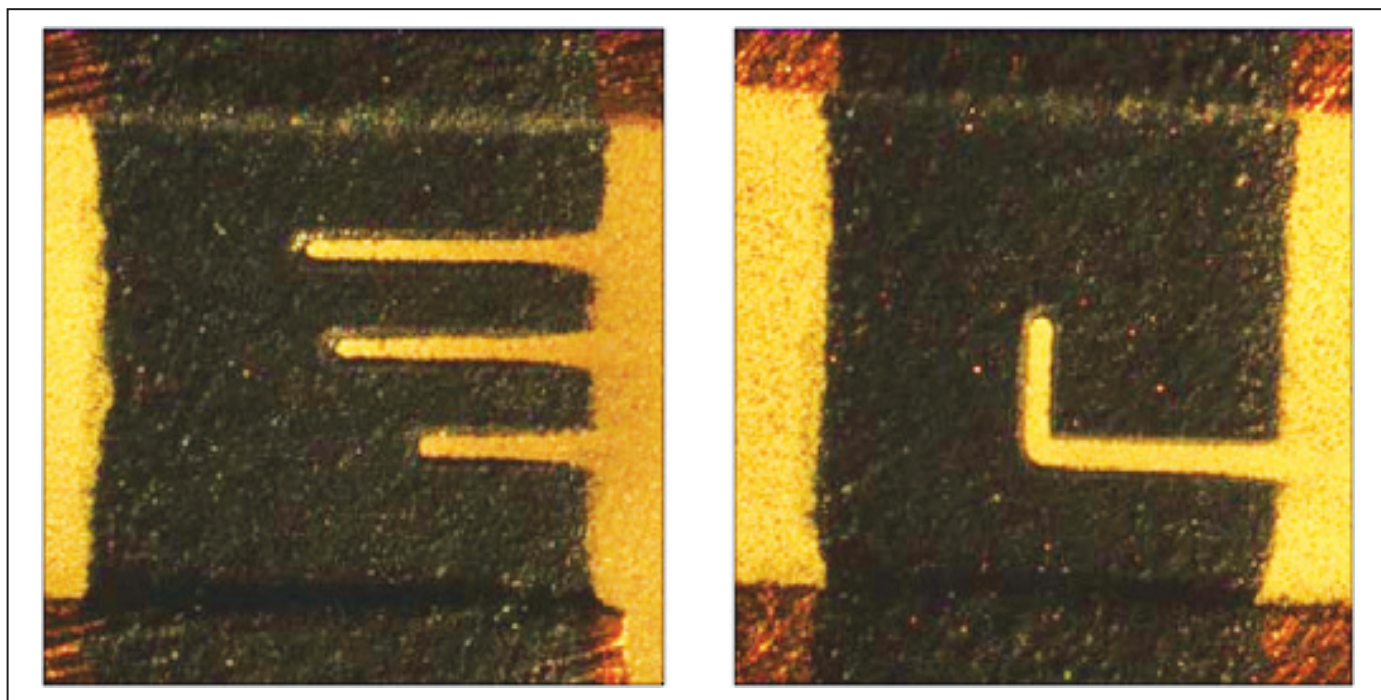


Figure 5-11 Triple Plunge Laser Trim (Left) and Standard L-Cut Trim (Right)

The trimmed resistors are now ready to be embedded into the printed board. Oxide alternatives can be used to promote adhesion without adverse effects to the resistor material.

5.4.3.4 Process for Embedding PTF Resistors If standard black oxide is to be applied, it is recommended that the resistors be encapsulated after trimming but prior to the black oxide treatment. Typical lamination pressures up to 500 psi can be used to laminate the inner layer containing the resistors to the remaining board layers. The panel continues through any other required printed board process steps as normal to create the finished product.

A traditional sequential process for embedding PTF resistors is illustrated in Figure 5-12.

5.4.3.5 Alternative Printed Thick-Film Process For process and performance improvements, a reverse lamination process can be used. Rather than screen printing on an etched inner layer as described earlier, the resistor ink would be printed onto 1 oz. Cu foil. The cured foil is then laminated component side down to single-sided FR-4 using FR-4 prepreg. The standard print, expose, develop, etch and strip process is carried out to create the resistor terminations. Figures 5-13 shows the fabrication sequence for the reverse-lamination process.

There are several benefits to the reverse-lamination process:

- Printing on a flat surface (foil versus etched inner layer) gives better print quality, to achieve tighter coefficient of variation
- More aggressive cure schedules can be used, which promotes better stability after subsequent heat excursions
- Adhesion is improved by printing on treated side of foil, which provides better electrical contact giving better performance and reliability

5.4.3.6 Performance Expectation for PTF Resistors

Once successfully embedded into the printed board, polymer resistors show good reliability performance under various test protocol. As stated previously, embedded resistors need to withstand many environmental and mechanical stresses. Table 5-4 summarizes a few of the environmental tests passed. Good results have been obtained on resistor sizes ranging from 0.25 to 10 squares, 0.5 mm to 2.2 mm [0.0196 in to 0.0866 in] in length and 0.5 mm to 2.0 mm [0.0196 in to 0.0787 in] in width. Printing parameters for smaller resistor geometries need to be developed to optimize printing uniformity.

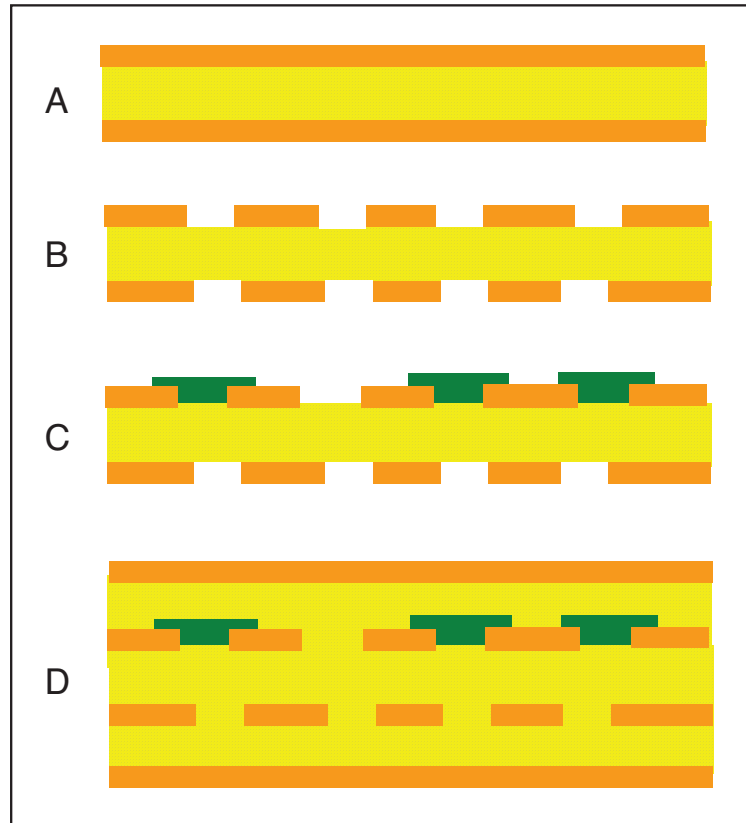


Figure 5-12 Traditional Embedded Circuitry Printed Board Lamination Process Sequence

Figure source: DuPont Circuit & Packaging Materials

- A – Begin with standard inner layer laminate
 B – Mark and etch Cu to prepattern termination pads and circuit traces
 C – Screen print resistor paste overlapping termination pads and cure
 D – Continue to build printed board using standard process

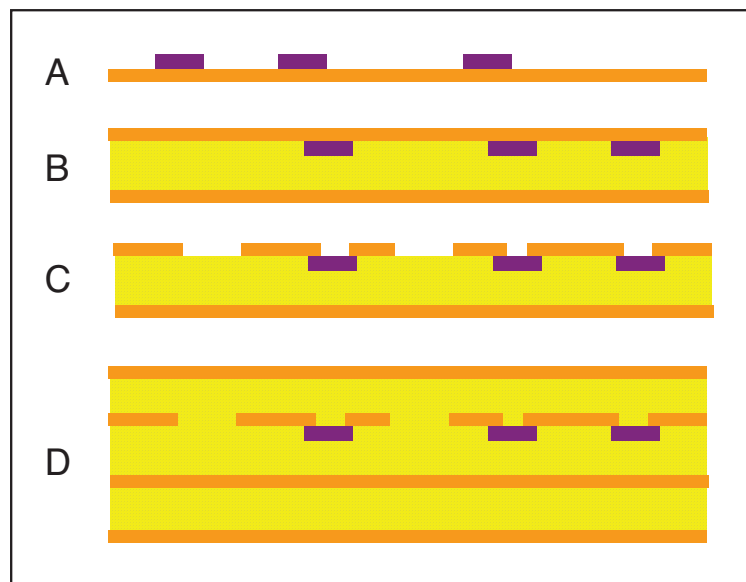


Figure 5-13 Reverse Embedded Circuitry Printed Board Lamination Process Sequence

Figure source: DuPont Circuit & Packaging Materials

- A – Polymer thick-film resistor paste printed and cured on Cu foil
 B – Foil laminated, component-side-down, to single-sided FR-4 core using FR-4 Prepreg
 C – Foil masked and etched to open up resistors and pattern circuit traces
 D – Continue to build printed board using standard process