

IPC-7093A

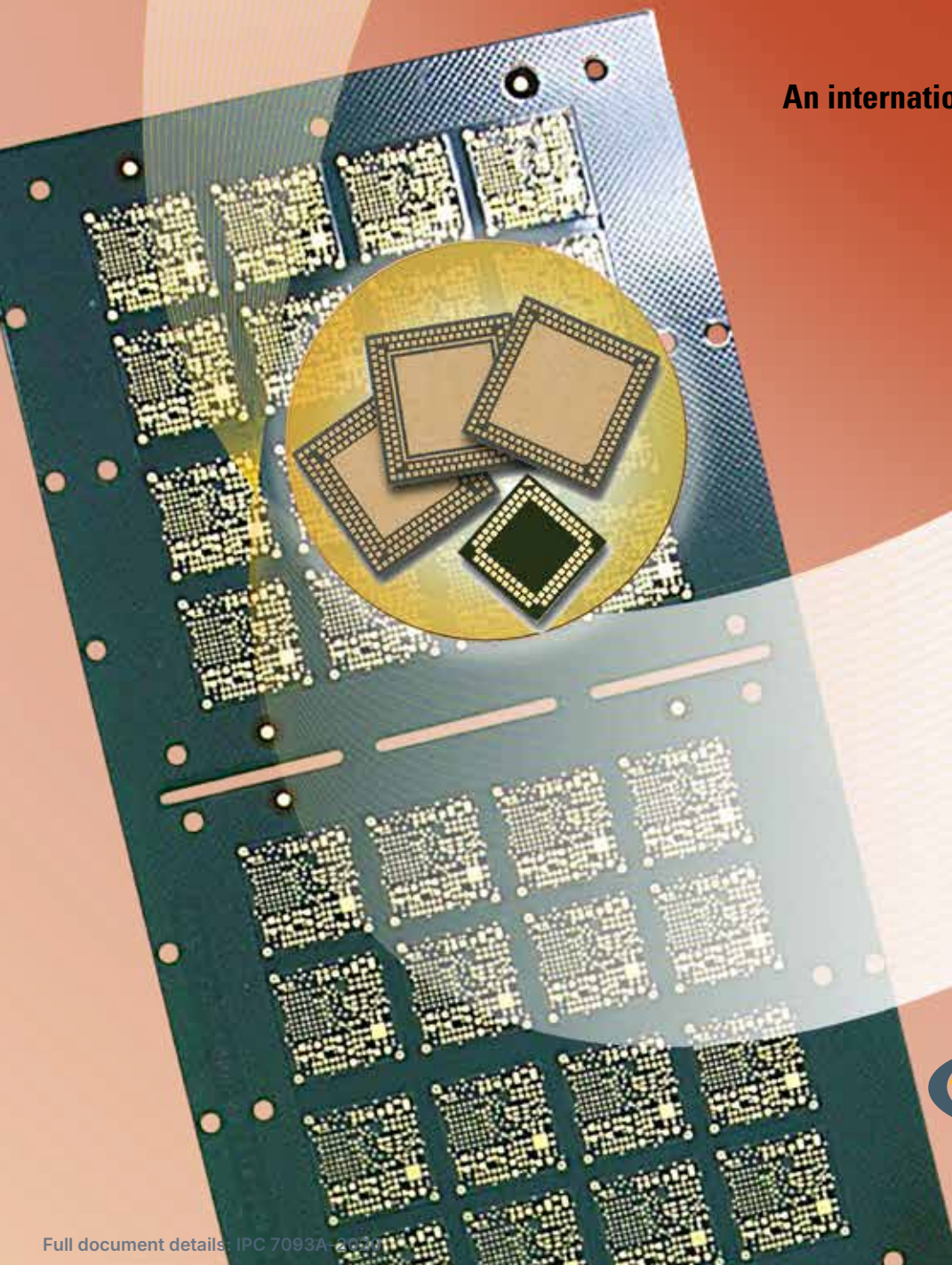
Design and Assembly Process Implementation for Bottom Termination Components (BTCs)

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Design and Assembly Process Implementation for Bottom Termination Components (BTCs)

Developed by the Bottom Termination Components (BTC) Task
Group (5-21h) of the Assembly and Joining Committee (5-20) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

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Design and Assembly Process Implementation for Bottom Termination Components (BTCs)

1 SCOPE

This standard describes design and assembly guidance for implementing bottom termination components (BTCs). The focus of the information contained herein is on critical design, materials, assembly, inspection, repair, quality and reliability issues associated with BTCs.

This standard applies only to BTCs, which are components with planar terminations under the body with or without wettable side terminations or flanks. Examples of BTCs include small-outline no-lead (SON), dual-flat no-lead (DFN), quad-flat no-lead (QFN), land grid array (LGA), etc. (see Section 4).

1.1 Purpose The purpose of this standard is to provide useful and practical information to those who use or are considering using BTCs. The target audiences for this document are physical designers, process engineers, reliability engineers and managers who are responsible for design, assembly, inspection and repair processes of printed boards and printed board assemblies. Information described in this standard enables high-quality and highly reliable BTC assembled devices operating within an electronic system.

This document also describes how to successfully implement robust design and assembly processes for printed board assemblies using BTCs as well as ways to troubleshoot some common anomalies which can occur during BTC assembly. For accept/reject criteria and requirements for BTC assemblies, see J-STD-001 and IPC-A-610.

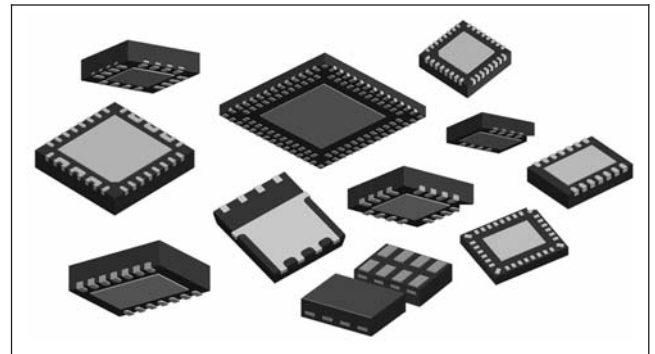


Figure 1-1 Various Forms of BTCs

Figure 1-1 provides an example of various forms of BTCs.

1.2 Classification IPC standards recognize that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in manufacturability, complexity, functional performance requirements and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between classes.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

1.3 Measurement Units All dimensions and tolerances in this specification are expressed in hard SI (metric) units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1.0 mm will be expressed in mm. All dimensions < 1.0 mm will be expressed in μm .

1.4 Definition of Requirements The words **shall** or **shall not** are used in the text of this document wherever there is a requirement for materials, preparation, process control or acceptance. The word “should” reflects recommendations and is used to reflect general industry practices and procedures for guidance only.

Line drawings and illustrations are depicted herein to assist in the interpretation of the written requirements of this standard. The text takes precedence over the figures.

1.5 Process Control Requirements The primary goal of process control is to continually reduce variation in the processes, products or services to provide products or processes meeting or exceeding user requirements. Process control tools such as IPC-9191 or other user-approved system may be used as guidelines for implementing process control.

1.6 Order of Precedence The contract **shall** take precedence over this standard, referenced standards and drawings.

In the event of conflict, the following order of precedence applies:

1. Procurement as agreed and documented between user and supplier.
2. Master drawing, design brief or tech pack reflecting the user's detailed requirements.
3. When invoked by the customer or per contractual agreement, this standard.

When documents other than this standard are cited, the order of precedence **shall** be defined in the procurement documents. The user can specify alternate acceptance criteria.

1.6.1 Clause References When a clause in this document is referenced, its subordinate clauses apply, unless the requirement references specific subordinate clauses.

1.7 Use of "Lead" For readability and translation, this document uses the word lead only to describe leads of a component (sometimes referred to as terminations).

1.8 Abbreviations and Acronyms Periodic table elements are written in their abbreviated form only in this standard. See Appendix A for full spellings of these and other abbreviations and all acronyms used in this standard.

1.9 Terms and Definitions Terms and definitions **shall** be in accordance with IPC-T-50 and 1.9.1 through 1.9.5.

1.9.1 Bottom Termination Component (BTC) Surface mountable electronic component with external connections consisting of planar metallized terminations on the underside that are an integral part of the component body.

1.9.2 Wettable Side Flank A BTC peripheral termination that is partially plated to improve solderability.

1.9.3 Exposed Die Paddle A metallic area on the bottom surface of a component that may or may not require soldering to the printed board and which provides thermal conductivity and improves current carrying capability of the device.

1.9.4 Thermal Pad A Cu feature on a printed board that can be soldered to a BTC exposed die paddle to help conduct heat from the device within the BTC to the printed board.

1.9.5 Thermal Via Conventional Cu-plated through-hole via found within a thermal pad, which is used to dissipate heat and carry current.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-A-610 Acceptability of Electronic Assemblies

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPC-CH-65 Guidelines for Cleaning of Printed Boards and Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-MS-810 Guidelines for High Volume Microsection

1. www.ipc.org

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-TM-650 Test Methods Manual²

2.1.1 Microsectioning Manual and Semi or Automatic Method

2.4.53 Dye and Pull Test Method (Formerly Known as Dye and Pry)

IPC-1401 Corporate Social Responsibility and Sustainability Protocols for Electronic Manufacturing Industry

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-2221 Generic Standard on Printed Board Design

IPC-2226 Sectional Design Standard for High Density Interconnect (HDI) Boards

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-4552 Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Boards

IPC-4553 Specification for Immersion Silver Plating for Printed Boards

IPC-4554 Specification for Immersion Tin Plating for Printed Boards

IPC-4556 Specification for Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG) Plating for Printed Circuit Boards

IPC-4761 Design Guide for Protection of Printed Board Via Structures

IPC-6010 series

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-7094 Design and Assembly Process Implementation for Flip Chip and Die Size Components

IPC-7095 Design and Assembly Process Implementation for Ball Grid Arrays (BGAs)

IPC-7351 Generic Requirements for Surface Mount Design and Land Pattern Standard

IPC-7525 Stencil Design Guidelines

IPC-7526 Stencil and Misprinted Board Cleaning Handbook

IPC-7530 Guidelines for Temperature Profiling for Mass Soldering (Reflow & Wave) Processes

IPC-7711/7721 Rework, Modification and Repair of Electronic Assemblies

IPC-9191 General Guidelines for Implementation of Statistical Process Control (SPC)

IPC-9201 Surface Insulation Resistance Handbook

IPC-9203 Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle

2.2 Joint Standards³

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-004 Requirements for Soldering Fluxes

2. Current and revised test methods are available on the IPC website (www.ipc.org/test-methods.aspx)

3. www.ipc.org

J-STD-005 Requirements for Soldering Pastes

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

J-STD-020 Handling Requirements for Moisture Sensitive Components

J-STD-033 Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

J-STD-075 Classification of Non-IC Electronic Components for Assembly Processes

J-STD-609 Marking and Labeling of Components, Printed Board and Printed Board Assemblies to Identify Lead (Pb), Pb-Free and Other Attributes

2.3 ASME⁴

ASME Y14.5 Dimensioning and Tolerancing

2.4 IEC⁵

IEC 60068-2-58 Environmental Testing – Part 2-58: Tests – Test Td: Test Methods for Solderability, Resistance to Dissolution of Metallization and to Soldering Heat of Surface Mounting Devices (SMD)

2.5 JEDEC⁶

JESD 30 Descriptive Designation System for Electronic-Device Packages

JEP 95 JEDEC Registered and Standard Outlines for Solid State and Related Products

JEP 95, Section 4.8 Plastic Quad and Dual Inline Square and Rectangular No Lead Packages (With Optional Thermal Enhancements) (QFN/SON)

JEP 95, Section 4.19 Quad No-Lead Staggered and Inline Multi-Row Packages (With Optional Thermal Enhancements) (QFN)

JEP 95, Section 4.23 Punch-Singulated Fine Pitch Square Very Thin and Very-Very Thin Profile Leadframe-Based Quad No-Lead Staggered Dual-Row Packages (With Optional Thermal Enhancements) (QFN)

4. www.asme.org

5. www.iec.ch

6. www.jedec.org

3 GENERAL OVERVIEW OF BTCs

This section provides a general overview of BTCs and implementing them into printed board assemblies. The remaining sections of this guideline provide detailed information on the topics covered in this section.

3.1 BTC Types This section describes some of the most commonly known BTC technologies. See Section 4 for detailed descriptions of these and other technologies.

3.1.1 BTCs with Thermal Die Paddle BTCs with a thermal die paddle are BTCs incorporating perimeter input/output (I/O) solder pads which also have an exposed die paddle (under the component body). Soldering of the I/O pads completes signal, power and ground device connections, while the soldered die paddle enables thermal heat sinking from the device within the component to the printed board.

3.1.2 BTCs without Thermal Die Paddle BTCs without a thermal die paddle are physically identical to BTCs with soldered thermal die paddles. However, for BTCs without soldered thermal die paddles, the perimeter I/O pads are soldered only, as there is no die paddle for these device types.

3.1.3 Flip Chip QFN (FC-QFN) Flip chip QFNs (FC-QFNs) have a unique package construction which is generally outside the scope of this standard. I/O pads of FC-QFNs have flip chip bumps that are soldered directly to the printed board. FC-QFNs do not contain a thermal pad. See Figure 3-1 for an example of a FC-QFN.

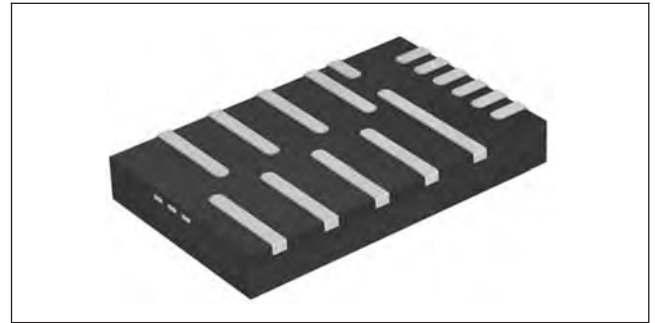


Figure 3-1 Bottom Side of a Flip Chip QFN (FC-QFN) Showing Irregular Solder Terminations

Note: The example shows three different pad sizes and non-symmetrical pad orientation.

See IPC-7094 for more information on FC-QFNs.

3.1.4 Land Grid Array (LGA) LGAs are components with an organic laminate and metallic terminations on their bottom side. These terminations are typically laid out in a regular array. LGAs can be installed in a specially designed LGA socket or soldered to a printed board with lands that align with the terminations on the LGA.

3.1.5 Other BTC Designations This section outlines commonly known BTC designations. At the time of publication, there are an estimated > 150,000 different BTC packages available on the market. For the most current listing of BTC types, refer to JEP 95.

BTCs can be found in many form factors, including those found in Table 3-1. See JESD 30 for surface terminals and additional classifications. All surface terminal devices are considered BTCs. This statement supersedes descriptions and classifications in this section, because this component family is very dynamic and constantly evolving.

Table_3-1 Sample Listing of Some Common BTC Designations

Package Name	Description	JEP 95 Designator
QFN	Quad Flat No-lead	MO-220, MO-241, MO-243, MO-248, MO-250, MO-251, MO-254, MO-262, MO-263, MO-267, MO-288
PQFN	Power Quad Flat No-lead / Plastic Quad Flat No-lead	MO-208, MO-217, MO-239, MO-247, MO-255, MO-296
SON	Small Outline No-lead	MO-196, MO-197, MO-229, MO-232, MO-240, MO-245, MO-287
PSON	Power Small Outline No-lead / Plastic Small Outline No-lead	MO-209, MO-252
DFN	Dual Flat No-lead (two, three, four and six pins)	MO-236, TO-276
SOFL	Small Outline Flat Lead (three, four, five, six and eight pins)	MO-293
SODFL	Small Outline Diode Flat Lead (two pins)	DO-219, DO-220, DO-221, DO-222
SOT89	Small Outline Transistor (three or five pins)	TO-243, EIAJ SC-62
TO-277	Transistor Outline (three pins)	TO-277



Note: A primary reason for the large variety of package types and names is because there was no original standardization for this package type. The guidance provided in this standard attempts to work within the proliferation of these package designations.

3.1.6 BTC Device Manufacturer Acronyms Be aware that BTCs also may be labeled with a wide variety of industry trade names. The following is a sample listing of commonly known device manufacturer acronyms. The list does not include all package instances and is intended for general knowledge only.

Note: Naming conventions are dynamic across the industry.

- AQFN – Advanced quad flat no-lead
- BCC – Bump chip carrier
- BCC+ – BCC with a center pad
- BCC++ – BCC+ with a ground ring
- HVQFN – Thermally enhanced very thin quad flat package
- LCC – Leadless chip carrier
- LLP – Leadless lead frame package
- MIS – Molded interconnect substrate
- MLF – Micro lead frame
- MLFD – Micro lead frame dual
- MLFQ – Micro lead frame quad
- MLP – Micro lead package
- MLPD – Micro lead frame dual
- MLFQ – Micro lead frame quad
- QFM – Quad flat module
- TDQFN – Thin dual quad flat no-lead
- TQFN – Thin quad flat no-lead
- UTQFN – Ultra thin quad flat no-lead
- VFQFN – Very thin fine pitch QFN
- VQFN – Very thin quad flat no-lead
- XSON – Extremely thin small outline no-lead

3.1.7 Description of Different Component Structures As mentioned in 3.1.6, there are many types of BTCs that go by various trade names. Unlike the more traditional lead-frame-packaged semiconductors with protruding leads, BTCs are furnished with flat pads or terminations on the bottom of the package. Those terminations are provided on either two sides or all four sides of the package, in single or multiple rows.

BTCs are leadless, similar to a chip scale package (CSP) in size, with a low profile (≤ 1 mm), excellent thermal dissipation and good electrical performance. Typical BTCs have solderable terminations that are flush with the bottom of the device. These devices can also have smaller solderable termination areas located along the perimeter sides, or flanks, of the package near the bottom of the device.

BTC packages have two types of solderable areas:

- 1) Solderable I/O pads
- 2) Thermal pad(s)

Figure 3-2 shows the top of a BTC (left) and bottom of a BTC (right) without thermal pads.

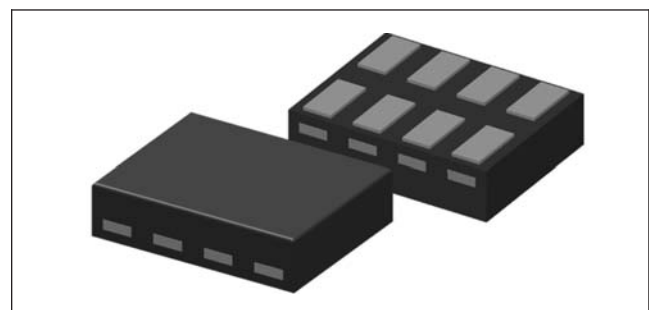


Figure 3-2 BTC Packages without Thermal Pads (Top and Bottom View)

Packages can consist of one or more thermal pad areas (see Figure 3-3 and Figure 3-4). Design considerations for I/O and thermal pad areas are needed. Robust connection for I/O locations is important to ensure adequate functional performance.

of the device. Properly designed thermal pads are required to manage thermal dissipation of the device and current carrying requirements.

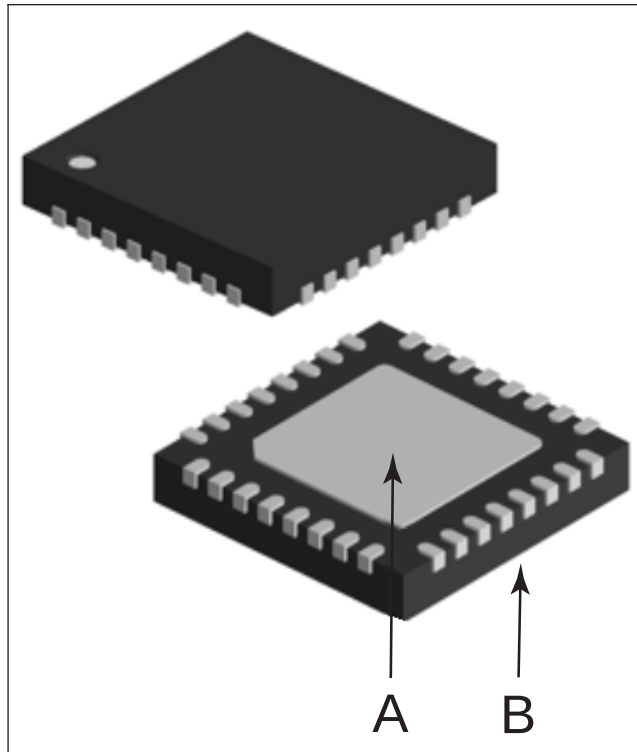


Figure 3-3 Single Thermal Pad QFN Device Example (Top and Bottom View)

A – Die paddle area
B – I/O (signal, power, ground)

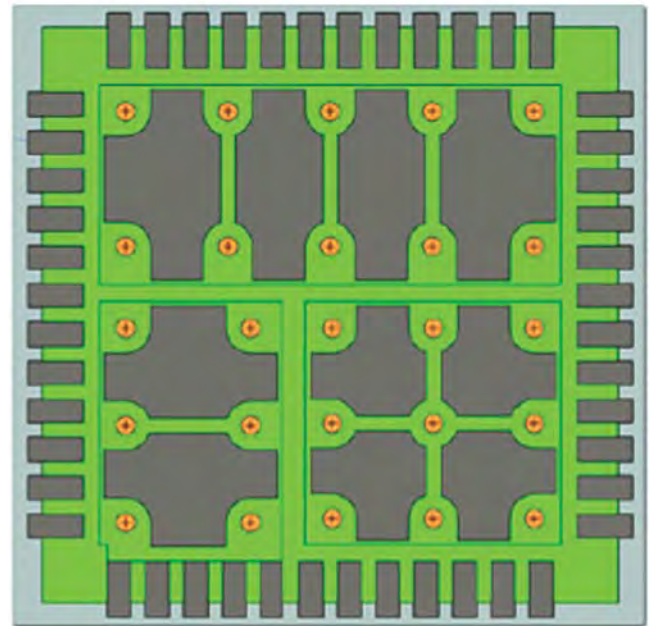


Figure 3-4 Multiple Thermal Pad Design Example

One primary benefit of BTCs is a very low profile. This is a key requirement for newer generations of portable, wireless and handheld electronic products in which weight and package thickness should be minimized. This trend reduces the semiconductor package outlines and profile for portable handheld devices.

The contact pitch for BTC packages is generally ≤ 1 mm, and the packages tend to be smaller. The body outline dimensions can be ≤ 1 mm² or as large as 12 mm². Due to fine-pitch geometries, this package can accommodate a die element that is nearly the same size as the package.

Traditional gull-wing leaded packages have very good, long solder joint reliability life compared to leadless components of the same size. This is because they have very flexible leads. BTCs, however, are not as compliant and may exhibit a relatively shorter solder joint life when subjected to operation in harsh environments. This is because they do not have leads that can take up stresses and strains introduced by differing coefficients of thermal expansion (CTE) between the package and the substrate.

Many BTCs are furnished with a Cu lead frame substrate and offer a thermal enhancement by exposing the die-attach pad on the bottom of the package surface. The die-attach pad provides an efficient heat (and electrical current) path when soldered directly to the printed board. This enhancement also enables stable ground interface by use of down bonds or by electrical connection through a conductive die-attach material. Such thermal pads have the potential for large voids and may even lead to the package floating if the printed solder paste volume on the thermal pad is not tightly controlled.

BTCs come in two formats:

- 1) Punch-singulated
- 2) Saw-singulated

While punch-singulated packages are individually punched from a molded strip during final assembly, saw-singulated packages are assembled in array format and separated into individual components during the final sawing operation (see 4.3.1). Either of these singulation methods can leave the terminal edges without a wettable surface finish.

Saw-singulated packages are divided into two options:

- Full lead package
- Lead pull-back package

While the full lead package has the whole thickness of the lead exposed on the package sides, the lead pull-back package has a bottom-half etch lead frame, resulting in only the top half of the lead thickness exposed to the sides of the package. Figure 3-5 shows the differences in these package configurations.

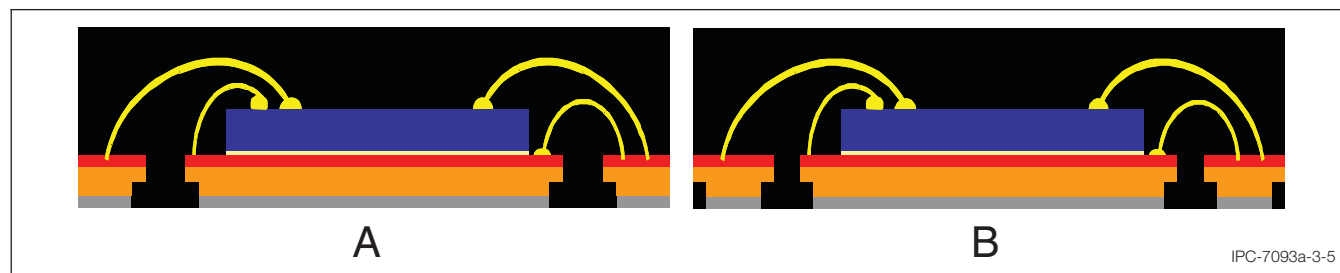


Figure 3-5 Saw-Singulated BTC Packages

A - Saw-singulated, full lead

B - Saw-singulated, lead pull-back

As mentioned, one of the greatest benefits of BTCs is their thinness. BTC packages allow much thinner devices than are possible when using other types of surface mount components. Figure 3-6 shows relative package thicknesses of various component packages.

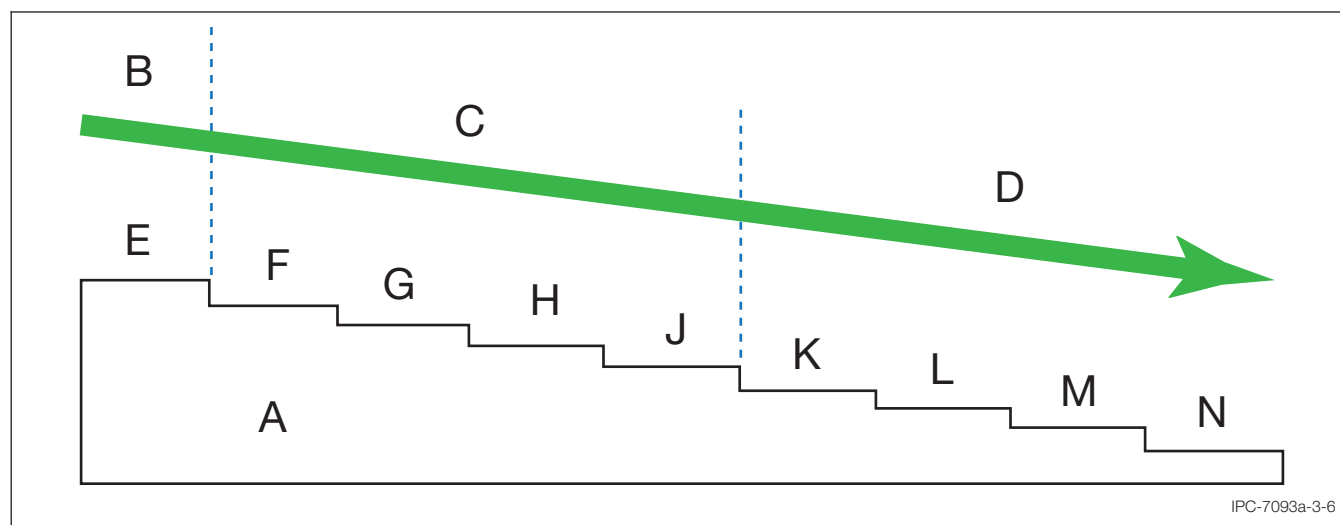


Figure 3-6 Package Thickness Comparison

A - Package height comparison

B - J-lead

C - Gull wing

D - No-lead BTC

E - PLCC (1.27 pitch, 4.57 height)

F - MQFP (0.80 pitch, 4.10 height)

G - LQFP (0.65 pitch, 3.40 height)

H - TQFP (0.50 pitch, 1.60 height)

J - TSQFP (0.40 pitch, 1.20 height)

K - QFN (0.65 pitch, 1.00 height)

L - QFN (0.50 pitch, 0.80 height)

M - QFN (0.40 pitch, 0.60 height)

N - DFN (0.30 pitch, 0.40 height)

While the lack of traditional leads or balls allows reduced package thickness and better electrical and thermal performance, the low stand-off height makes it difficult to remove any trapped flux residues that remain in and around the solder joints. If the flux is active, the potential for corrosion increases. It is necessary for the package and printed board to be very clean.

to achieve good interconnection, or the potential for opens in solder joints will increase. Since the stand-off height is very low, solder joint reliability may be a concern in harsher environments.

3.2 Total Cost of Ownership Low package cost is a key driver for widespread use of BTCs. However, the low package cost may not immediately translate into overall low assembly cost because this package can present challenges in assembly, inspection and rework.

In practice, the total cost of the final assembly is often greatly impacted by decisions made early in the design process. Too often, accounting systems track cost in the door but fail to track cost out the door. Purchasing is measured and rewarded by identifying and procuring at the lowest price, without understanding and fully appreciating the impact on the manufacturing process and long-term reliability of the product and the implied cost of failures. It is incumbent for management to prudently consider and decide on the amount of effort to devote to up-front engineering, including component selection or package design, solder joint design, printed board design and design verification. Management also should understand and appreciate the actual piece part cost, which is comprised of several elements (e.g., cost of components, incoming inspection, assembly, test and final inspection). The decisions made will directly impact product reliability. Table 3-2 lists the key cost contributors and their impacts on total cost of ownership.

If via-in-pad plated-over (VIPPO) structures are included in the printed board design, expect a 15 % to 20 % increase in the cost of the printed board assembly. The added cost is primarily associated with the additional process steps needed for printed board fabrication. Efforts to understand the potential cost increase when using VIPPO via structures is recommended when deciding upon which BTC design approach to use.

Table 3-2 Total Cost of Ownership of BTCs

Cost Contributor	Impact
Incoming inspection	The incoming component inspection level is a function of the confidence the buyer has in the supplier being considered related to the cost of the different potential defects which might be encountered and how they might be resolved. Rework is expensive, but product returns can damage a business.
Component or package design	To meet cost and reliability targets, a reasonable rule to follow is to select or design the lowest-cost package that meets the lead count requirement and power dissipation with the largest pitch tolerable within design constraints. Consideration of the potential change to product specifications to improve product cost and reliability may be desirable under certain circumstances.
Solder joint quality	The solder joint is the most critical factor in product reliability. Solder volume and solder placement are critical to yield and reliability of the BTC assembly. The die-attach pad may be of high importance because some data show reliability is reduced when it is not soldered in place.
Board design	Board materials, via type, layout and land pattern design are all vital and directly affect board cost, assembly yield and reliability.
Assembly method	The assembly process has several steps, including solder paste deposition, component placement, reflow and cleaning. The method chosen can represent a relatively minor percentage of overall cost when done with a well-controlled process, but it can be costly otherwise. In some situations with BTCs, supplementary process equipment may be needed. While this will add some cost, overall cost will be reduced by improving yield.
Test and inspection	While it is impossible to inspect quality into a product, test and inspection are commonly used to ensure process control. Some level of optical, X-ray and electrical test will verify the quality of assemblies. Assembling BTC devices with solderable flanks can promote improved post-reflow inspection capabilities. BTC processing steps do not guarantee solderable flanks. Requiring device suppliers to produce BTCs with solderable flanks may lead to additional processing. Post-reflow inspection that allows bad or marginal solder joint escapes results in lower end-user confidence and higher total cost.
Reliability	Rigorous design control reduces cost by ensuring reliability. Demonstrating the reliability of a design can be an expensive process and represent a major upfront cost. However, a failure (especially a field failure) has arguably even greater cost impact.

3.3 Design and Assembly Process Considerations for QFN Type BTC Packages

3.3.1 Current-Carrying Requirements and Thermal Dissipation The BTC package is often designed to provide excellent thermal performance by incorporating an exposed die paddle on the bottom surface of the package. However, to take full advantage of this, the printed board should have features to effectively conduct heat and current away from the package. This can be achieved by incorporating a thermal pad and thermal vias within the printed board. While a thermal pad provides a solderable surface on the top surface of the printed board (to solder the package die pad to the printed board), thermal vias are needed to achieve a suitable thermal/current path to inner and/or bottom layers of the printed board to remove the heat and to conduct current.

Via count and size of vias placed in the exposed-pad soldering areas should be adapted to device requirements. Whereas a high via count can in principle optimize the electrical and thermal performance of the land, careful balancing of the pros and cons of different design options for the land needs to be conducted. An open-Cu design allows maximized via count at low printed board cost, but it can have certain disadvantages. It can lead to solder in vias and the formation of solder protrusions on the opposite side of the printed board, which may be detrimental in double-sided assemblies or in the formation of short circuits to a conductive housing. Alternative design options may provide a more adequate solution.

3.3.2 Electrical Performance To optimize electrical performance, all circuit traces should be as short as possible. To be most effective, the input and output capacitors should be placed near the BTC device to minimize parasitic trace inductance. Using wide conductors for higher voltage in, higher voltage out and ground will help minimize parasitic electrical effects and enhance thermal transfer between the case and the ambient environment.

BTCs also have superior electromagnetic compatibility (EMC) / electromagnetic interference (EMI) performance over leaded components.

3.3.3 Selection of Solder Paste Type, Stencil Design and Solder Paste Printing BTCs will be assembled with other surface-mount components, including ball grid arrays (BGAs), quad flat packs (QFPs), chip capacitors, resistors, etc. Solder paste type (mesh size) and stencil thickness should typically be based on the component with the lowest pitch and/or smallest case size on the printed board. This component may or may not be a BTC.

It is important to carefully balance the amount of solder paste (solder paste coverage) at the thermal pad land. Solder paste at the thermal pad adjusts the stand-off of the package after reflow, whereby an increased stand-off can have a positive effect on thermal cycling life of the I/O solder joints. Increased stand-off has a positive effect on thermal cycling life of the I/O solder joints, but too much solder paste may result in excessive voiding, depending on the land design (i.e., open Cu with thermal vias) to solder in vias, and lead to the formation of solder protrusions. Moreover, floating of the BTC may result in irregular stand-off, tilting, skew and open solder joints at the I/O terminations. Section 6 provides information on various design options and their pros and cons.

For I/O solder joints, too little paste will create insufficient or, most likely, open solder joints. Excessive paste will generate squeeze balls (solder balls trapped underneath component) and shorts.

3.3.4 Single Thermal Pad Design A single thermal pad design entails one large Cu feature within the printed board land pattern of the BTC. Via holes could also be placed within this single thermal pad to enhance thermal conduction (see Figure 3-7).

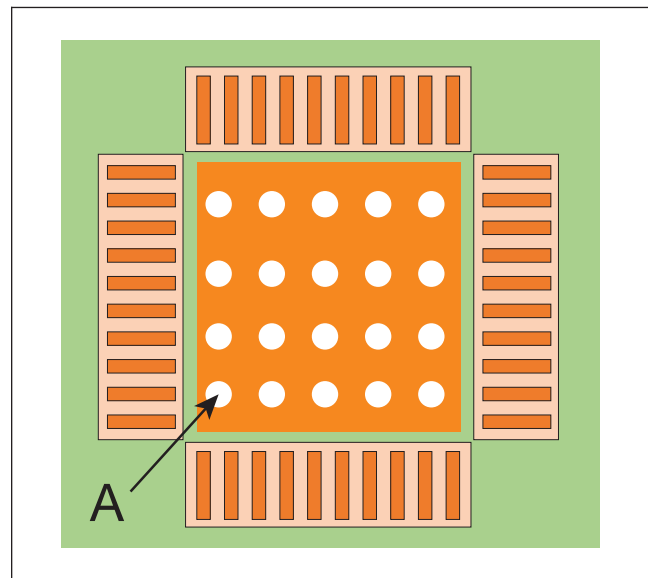


Figure 3-7 Example of a Printed Board Land Pattern with a Single Thermal Pad Containing Vias

A – Via hole

3.3.5 Multiple-Thermal-Pads Design A multiple-thermal-pads design entails distinct Cu features within the printed board pad pattern of the BTC. These Cu patterns are separated by solder mask on the surface of the printed board. Figure 3-8 shows two examples of multiple-thermal-pad patterns.

3.3.6 Wettable Side Flank The lack of a visible solder (toe) fillet on the edge surface of the pins of standard terminations of BTCs (not plated after sawing or punching) has been a major impediment for the use of BTCs in high-reliability applications. This is because such applications have necessitated that a solder fillet be visible at the outer edge of each contact to enable a robust inspection for wetting failures by automatic optical inspection (AOI). To enhance this inspection capability of BTC solder joints, notches are made in the standard termination to enable the terminal edge surface to remain plated after singulation, thereby promoting surface wetting by molten solder during reflow. This termination design is known as a wettable side flank. Figure 3-9 shows a comparison between a standard termination and an exemplary wettable side flank termination.

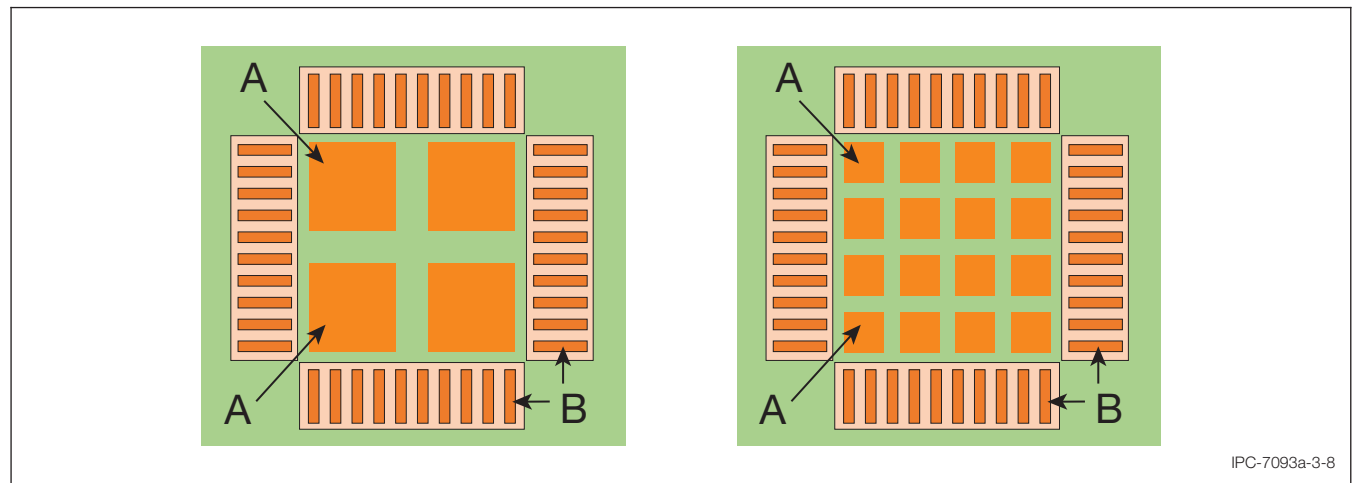


Figure 3-8 Examples of Printed Board Land Patterns with Multiple Thermal Pads

A – Thermal pad
B – I/O pads

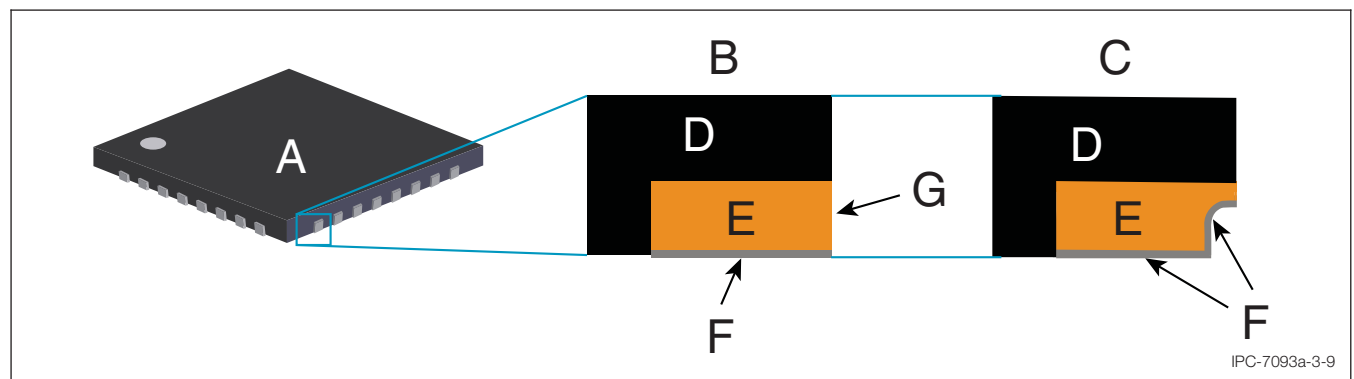


Figure 3-9 Comparison of a Standard BTC Termination and a Wettable Side Flank BTC Termination

A – BTC
B – Cross-section of a standard termination
C – Cross-section of a wettable side-flank termination
D – Mold
E – Termination
F – Solderable surface
G – Unplated Cu surface

3.4 Inspection and Rework

3.4.1 Quad Flat No-Lead (QFN) Solder Joint Inspection In mass production, in particular high-reliability electronic control units, 100 % solder joint inspection is typically implemented (see 7.11). Automated optical inspection (AOI) generally is not capable of detecting all possible failure modes for I/O solder joints of BTCs, but it can detect bridging. However, because the post-package assembly singulation process typically leaves a bare-Cu lead frame at the edge, which is not protected against oxidation and is not easily wetted by molten solder, a solder fillet (toe fillet) does not generally develop. Therefore, no stable inspection for a visible (toe) meniscus and wetting failures of the component can be implemented. A refinement of the lead frame structure, to enable a portion of the terminal edge surface to remain plated after singulation, can overcome this limitation. See 3.5 and 7.11.2.

3.4.2 Automated X-Ray Inspection (AXI) Automated X-ray inspection (AXI) has the same limitations as AOI concerning the inspection for wetting by detecting toe fillets. However, alternative inspection features (i.e., based on the capillary effect) can be devised for AXI (having a much higher sensitivity for the presence/thickness of solder compared to AOI), which enable inspection of proper wetting of the I/O terminations. AXI can also be used to assess voiding in I/O and exposed pad solder joints. Whereas voiding in I/O solder joints is typically very limited (< 25 % of the area of the solder joint), higher voiding levels can occur within the exposed pad solder joints depending on the exposed pad lands design due to their extended size (i.e., the considerable amount of solder paste (and thus flux) deposited). See 7.11.3 for details about AXI and 8.3.1 for details on voiding.

3.4.3 Failure Analysis Microsection analysis is a destructive analysis method enabling cross-sectional visualization of solder joints and assessment of package stand-off heights. It can also be used for assessing relative crack lengths in solder joints after assemblies have been exposed to field loads (e.g., thermal cycling). Relative crack lengths can also be investigated using the dye penetration technique discussed in 8.4.2.2.2. Neither method is intended for production inspection, but they can be used for process development and solder joint life assessment.

3.4.4 Rework Considerations Rework stations for BTC assemblies should be similar to other rework systems and have suitable tools to remove and replace faulty components. Hot-gas and laser systems are used for removing components, redressing the lands and adding the appropriate solder paste or performing and positioning the component before applying heat.

BTCs removed during rework should not be reused within final assemblies. A package that has been removed has been subjected to two reflows. If the assembly is double-sided, the package has been subjected to three reflows. This means the package is at or near the end of the tested and qualified range of known survivability. These removed BTCs should be properly disposed of so they will not be mixed with fresh equivalent BTCs. See 7.12 for more details on rework and repair of BTC assemblies.

3.5 Needs and Expectations Polymer-molded Cu lead-frame-based QFN and SON semiconductor package families are the primary platform for low-cost, low-I/O, small-die applications. When compared with fan-out QFPs and small outline integrated circuit (SOICs), the bottom-terminal lead frame design furnishes a significantly shorter conductive path between the die element and circuit structure. Close coupling of the die to associated components on the board-level assembly facilitates a positive impact on performance and power management. Although these small package outlines furnish a level of economy and enable higher component densities, early generations of the package did not meet the requirements of all users.

A primary detractor of the package has been the lack of a visible solder fillet on the edge surface of the Cu contact features. Although solder joint robustness is not a main concern (number of cycles to failure under thermal cycling typically decreases only marginally, by up to ~20 %, in the absence of an outer, visible fillet), users, primarily those involved in manufacturing products for Class 3 or higher applications, have insisted that a solder fillet be visible at the outer edge of each contact to enable a robust inspection of wetting failures by optical inspection methods (e.g., AOI).

Requests from users to perform a secondary plating or coating process after singulation have been rejected due to cost factors. Package suppliers have, however, responded with refinement to the basic lead frame design that enables a portion of the terminal edge surface to remain plated after singulation.

Some approaches for introducing such pin modifications are explained in the following.

After package assembly, mold and cure processes, a small-step feature can be established at the end on the Cu terminals by application of a partial (with respect to the sawing depth) sawing operation. The final process step before singulation electroplates the exposed Cu terminals with a matte Sn alloy (package assembly sequence illustrated in Figure 3-10).

The step-cut lead frame enables the encroachment of the electroplated matte Sn alloy onto the outer edge of the QFN package outline (see Figure 3-11). The plating facilitates solder wetting during reflow solder attachment.

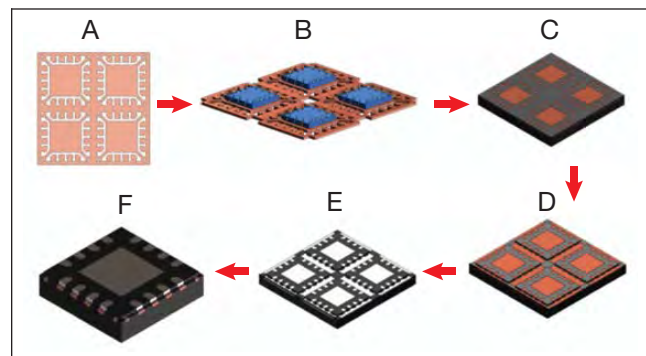


Figure 3-10 Step-Cut Quad Flat No-Lead (QFN) Package Assembly Process

A – Bare L/F strip format top view D – Step cut (additional process)
B – Die attach and wire bond E – Electroplating (matte Sn)
C – Mold encapsulation F – Saw singulation (full cut)

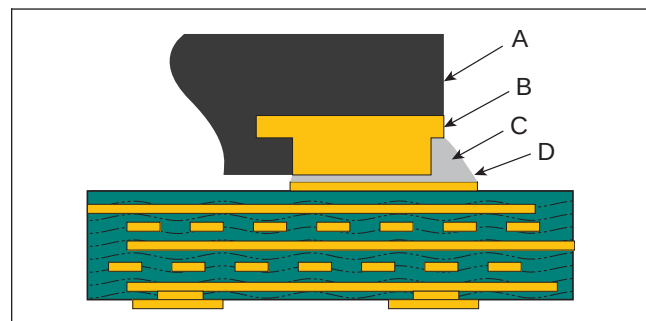


Figure 3-11 Sn-Plated Step-Cut Quad Flat No-Lead (QFN) Lead Frame

A – QFN case profile
B – Bare Cu lead frame end
C – Sn-plated step area
D – Edge visible solder fillet

Another solution can enable a visible toe fillet on the no-lead package. Following the chemical etch or stamp process of the Cu lead frame array, the bottom surface within the contact area is masked to enable a secondary chemical etch process to form a shallow concave depression (dimple) in which the plating remains intact during the final singulation operation. During this singulation operation, the cut is made through the midpoint of the dimple formed in the lead frame array. Figure 3-12 shows the cut lines for such operations.

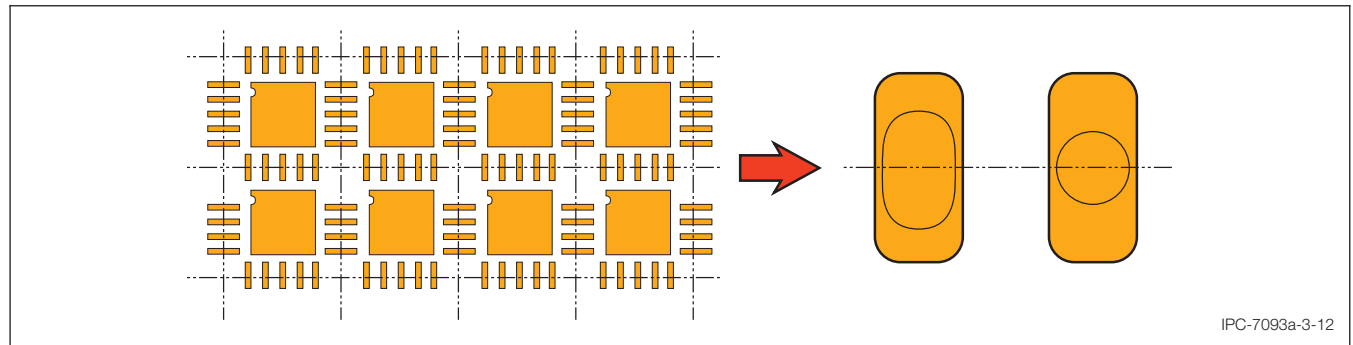


Figure 3-12 Concave Depression Etched into the Bottom Surface of the Contact

Figure 3-13 shows cross-sections of a solder joint resulting from this dimple formation compared with that formed with standard mechanical step-cut process.

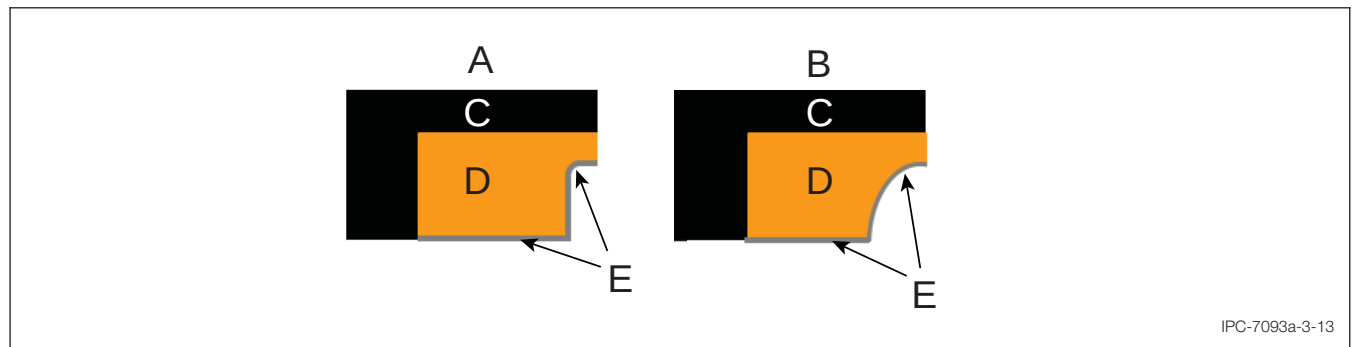


Figure 3-13 Cross-Sectional Representations of Wettable Flank Terminations for Mechanical Precut Process (Left) and Dimple-Formation Chemical Etch Process (Right)

A – Mechanical precut C – Mold E – Solderable surface
B – Chemical etch (dimple) D – Termination

Figure 3-14 shows microscopic images of common pin modifications, enabling the formation of a visible outer solder fillet.

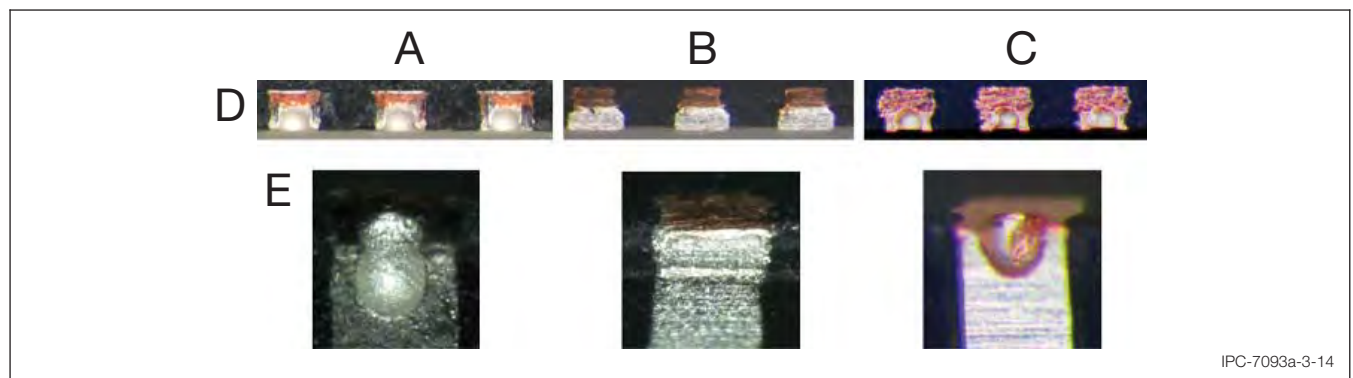


Figure 3-14 Microscopic Images of Common Pin Modifications

A – Dimple and punch C – Dimple and saw E – Bottom/Side view
B – Saw-plate-saw D – Side view

For such pin modifications to be useful in the context of AOI under series production conditions, a certain minimum wetting height should be ensured. This is required to distinguish a wetted pin (good solder joint) from a nonwetted pin (defective solder joint). Using state-of-the-art AOI systems, a minimum wetting height of 100 μm enables a robust optical inspection of solder joints for wetting failures (see 7.11.2).

Recently, BTCs with fully plated terminations, both on the bottom and outer edges, have been made commercially available (see Figure 3-15 and Figure 3-16). This can be achieved for some SON/DFN packages with geometrical restrictions as follows:

- The pads to be plated have to be on two parallel and opposite sides of the package.
- Plating of terminations on all four sides of a package is not possible with this approach.
- The methods require that individual packages are connected by metal features to the lead frame, which are oriented perpendicular to the I/O pads.
- The metal features can be separated at the final singulation step.

A possible future option could be the use of electroless (immersion) Sn to achieve fully wettable flanks for more complex packages. The packages could be fully separated prior to electroless immersion Sn plating. The challenge is the slow growth of the Sn layer, limiting the achievable layer thickness to $< 3 \mu\text{m}$. However, new Sn plating systems are under development, offering good wetting as plated and after storage.

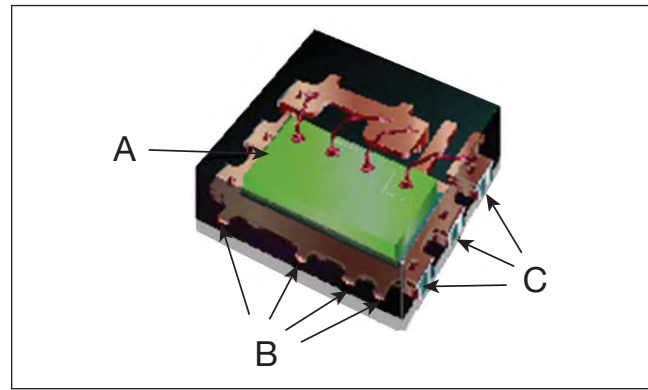


Figure 3-15 Transparent View of a DFN Package

Figure Source: Nexperia

A – Chip
B – Metal connection features
C – Side flanks

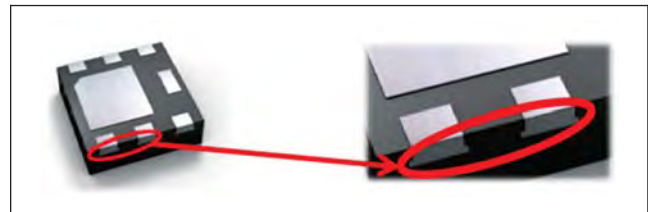


Figure 3-16 Detailed View on Side Wettable Flank Features of a DFN Package

Figure Source: Nexperia

4 COMPONENT CONSIDERATIONS

This section provides details on various BTCs from the point of view of the component manufacturer and describes common fabrication methods using lead frames and substrates and common defects associated with each of these processes. This section also describes the manufacturing process flow for producing different packages as well as geometries, materials and many standard variations.

Although several small outline semiconductor package innovations have been available (e.g., BGA and fine-pitch ball grid array (FBGA)), an effective method to significantly reduce package area and cost was not available until the introduction of SON and QFN package technologies. The most significant feature of these small-outline lead frame package families is their power dissipation capability and minimal electrical parasitics. Improved thermal dissipation performance comes from the exposed lead frame that is used to help pull heat out of the die to a mating thermal pad on the printed board. Electrical parasitics are inherently low due to the small size and short wire bonds.

4.1 General Description of Different BTC Packages There are several options available when specifying BTCs:

- Package configuration
- Pitch (0.4 mm to 1 mm)
- Termination geometry
- Package thickness
- Thermal pad geometry
- Plating

Figure 4-1 shows examples of some BTCs. These parts are available in a variety of configurations. Table 4-1 shows the configurations of QFN and SON (DFN) that are available from one packaging foundry. Other foundries are likely to have many of these, as well as some not described in this standard. JEDEC standards list many other size, lead and thickness combinations that result from a general approach. Most of those listed, however, are not in common use.



Figure 4-1 Various Forms of BTC Parts

Table 4-1 Commercially Available Quad-Flat No-Lead (QFN) and Dual-Flat No-Lead (DFN) Package Configurations

Size (mm)	QFN	DFN	Lead Pitch (mm)	Nominal Thickness (mm)
2 x 2		6, 8	0.50	0.90
3 x 3	8		0.65	0.90
3 x 3	12, 16,	8, 10	0.50	0.90
3 x 3	20		0.40	0.90
4 x 3		12	0.50	0.90
4 x 4	16		0.65	0.90
4 x 4	20, 24		0.50	0.90
5 x 5	20		0.65	0.90
5 x 5	28, 32		0.50	0.90
6 x 6	40		0.50	0.90
7 x 7	48		0.50	0.90
7 x 7	56		0.40	0.90
8 x 8	52, 56		0.50	0.90
9 x 9	64		0.50	0.90
12 x 12	100		0.40	0.90

LGAs are built in comparable sizes to those in the JEDEC standards and Table 4-1. LGA sizes range from 1 mm x 1 mm to 30 mm x 20 mm, while LGAs < 5 mm x 5 mm often have a sensor functionality (e.g., acceleration or pressure sensors) and LGAs > 5 mm x 5 mm often have a connectivity functionality (e.g., Bluetooth) (see Figure 4-2). Many of the larger LGA components include multiple-die elements and several passive devices. These configurations may consist of several different but complementary functions that together create a product that can be classified as a system-in-package (SiP). See 4.6 for more details on LGAs.

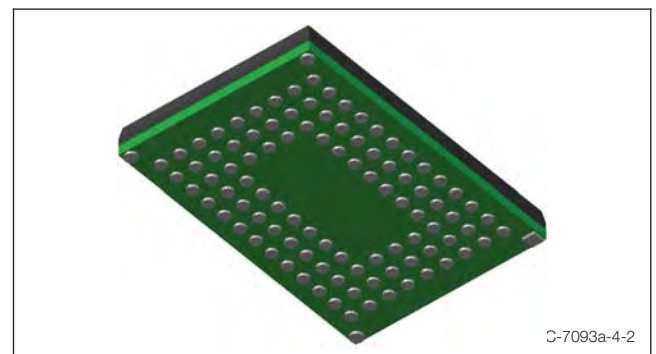


Figure 4-2 Singulated Land Grid Array (LGA) (Bottom of Device)

4.2 Detailed Description and Standards for BTCs

4.2.1 Single-Row Molded Lead-Frame-Based Packaging

The die-attach pad (DAP), when exposed outside the mold compound, serves as a heat spreader. The die element is first bonded to the DAP surface followed by wire-bond termination from the die bond pads to the contact features at its perimeter (see Figure 4-3). The package is completed when the plastic casing is molded around the die and wire-bond area, exposing only the bottom area of terminals for solder attachment.

To control the effects of the large surface area of the die-attach pad feature during reflow, it is necessary to tailor the solder stencil pattern or alter the mating thermal plane on the printed board.

4.2.2 Multiple-Row Molded Lead-Frame-Based Packaging

Plastic quad-configured multiple-row no-lead packages (QFNs) are plastic semiconductor packages with metallized terminals. Terminal contacts are located along the edges of the bottom surface of the package body arranged in one, two or three rows. Typical of the single-row QFN, the multiple-row QFN package is a lead-frame-based product. Multiple-row QFN lead frames require careful design, are fragile and are difficult to process. Instead of a lead frame, a printed board substrate can be used to provide dual-row contacts as described below.

Before wire-bond, the die is bonded to the DAP surface followed by wire-bond termination from the die-bond pads to the contact features at its perimeter (see Figure 4-4).

The package is completed when the plastic casing is molded around the die and wire-bond area, leaving only the bottom area of terminals and heat spreader exposed for solder attachment. The die-attach paddle, when exposed, also serves as a heat spreader.

4.2.3 Plastic-Quad, Dual-Inline, Square and Rectangular No-Lead Packages This section provides some commonly used names for BTCs. See also Table 3-1.

The plastic-quad, dual-inline, square and rectangular, no-lead packages (with optional thermal enhancements) described in this section include JEDEC definitions for SON and QFN packaging.

4.2.3.1 Small-Outline No-Lead (SON) / Dual Flat No-Lead (DFN) Packaging Plastic DFN, which can also be referred to as SON, is a semiconductor package with metallized terminals located on the bottom of the package. The SON has terminals on only two opposite sides of the bottom surface. By design, these terminals are flush with the bottom surface of the plastic package body outline.

4.2.3.2 Quad Flat No-Lead (QFN) Packaging Plastic QFN packages have terminals on all four edges of the bottom surface of the package. The QFN can have a square or rectangular body outline and either symmetric or asymmetric terminal patterns.

Single-row SON and QFN package technology has become a viable low-cost methodology furnishing a package outline only slightly greater than the die. JEDEC defines QFN/SON as a plastic semiconductor package with metallized terminals located on the bottom of the package body along its periphery, as detailed in Figure 4-5.

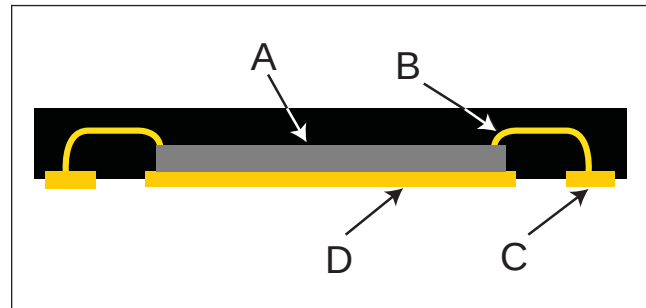


Figure 4-3 Basic Single-Row Lead-Frame-Based Small Outline No-Lead (SON)-Quad Flat No-Lead (QFN) Package Assembly Model

A – Die element attached to DAP feature
B – Wire-bond interface
C – Bottom exposed contact pads
D – Bottom exposed DAP

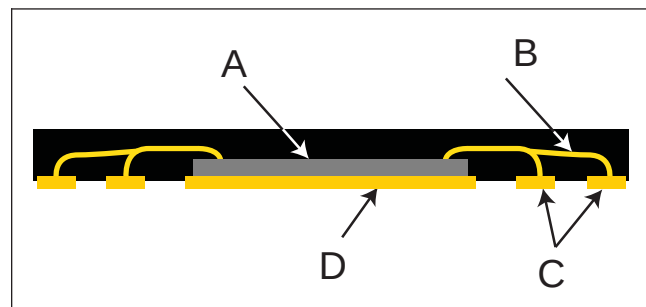


Figure 4-4 Basic Multiple-Row Quad Flat No-Lead (QFN) Package Assembly Model

A – Die element attached to DAP feature
B – Wire-bond interface
C – Bottom exposed contact pads
D – Bottom exposed DAP

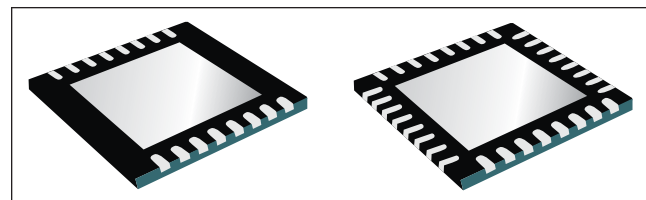


Figure 4-5 Terminal Configuration for Single-Row Small Outline No-Lead (SON) and Quad Flat No-Lead (QFN) Packaging

As noted in earlier sections, because the terminal features are flush with the bottom surface of the plastic body and do not protrude beyond the body outline, these packages are categorized as BTCs or no-lead. In addition, the supplier has the option of producing an exposed heat spreader element on the bottom surface to assist in transferring thermal rise generated by the die element into the host printed board structure using solder or thermally conductive compounds.

The JEDEC design guide defines the symbology, algorithms and recommended dimensions and tolerances for a family of QFN and SON Packages. The guidelines are based on hard metric dimensions and adhere to the geometric dimensioning and tolerancing principles defined in ASME Y14.5.

Regarding the contact numbering method for the SON package positions in Figure 4-6, Terminal #1 (viewed from the top surface) is in the lower left corner. Dimension D should then be measured in the horizontal direction. Similarly, measure dimension E in the vertical direction for both package types. For the QFN, the position of Terminal #1 is perpendicular to the body edge in the upper left corner, as compared in Figure 4-6.

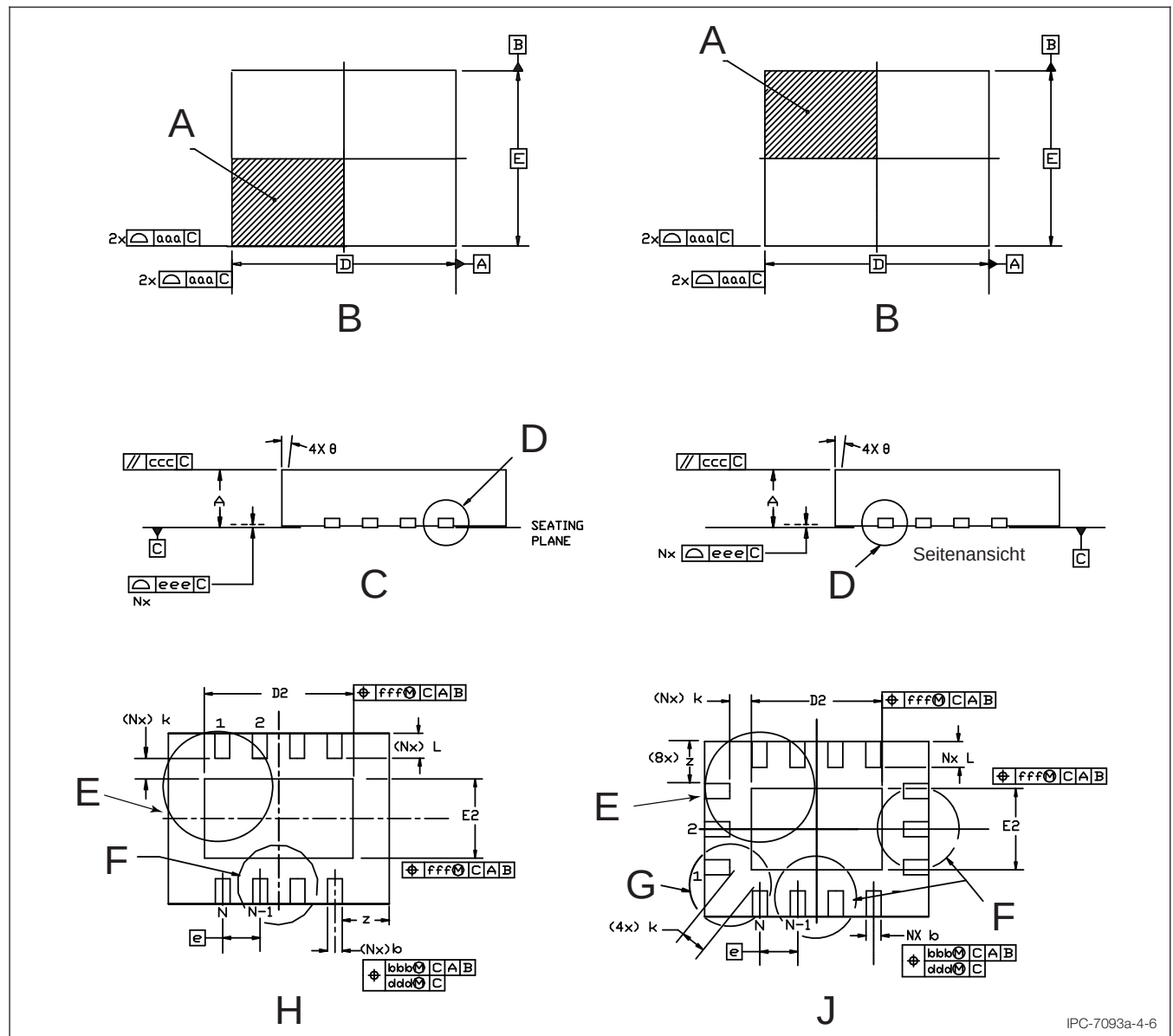


Figure 4-6 JEDEC-Defined Package Outlines for Single-Row Small Outline No-Lead (SON) and Quad-Flat No-Lead (QFN) Packaging

A – Terminal #1 index area

B – Top view

C – Side view

D – See A1 detail

E – See exposed heat feature examples

F – See terminal detail

G – See corner terminal detail

H – Bottom view (both types)

J – Bottom view (all types)



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The Terminal #1 identifier and terminal numbering convention will conform to JEP 95, SPP-002. The Terminal #1 identifier will be located within the zone indicated on the outline drawing. Top-side Terminal #1 indicator may be a molded or marked feature. Optional indicator markings or features may also be furnished on the bottom side.

The basic dimension for D and E suggested in the JEDEC design guide are to be in increments of 0.50 mm, ranging from 1 mm to 12 mm. Outlines with D and E increments < 0.50 mm should be registered as standalone outlines. These outlines should use as many of the algorithms and dimensions stated in this guide as possible to ensure predictability in manufacturing.

The JEDEC guide acknowledges that differing manufacturing processes by supplier companies will require some flexibility in the package configuration. Although the primary controlling dimensions will remain common, the terminal geometry may vary from supplier to supplier.

Figure 4-7 provides an example of two terminal design variations.

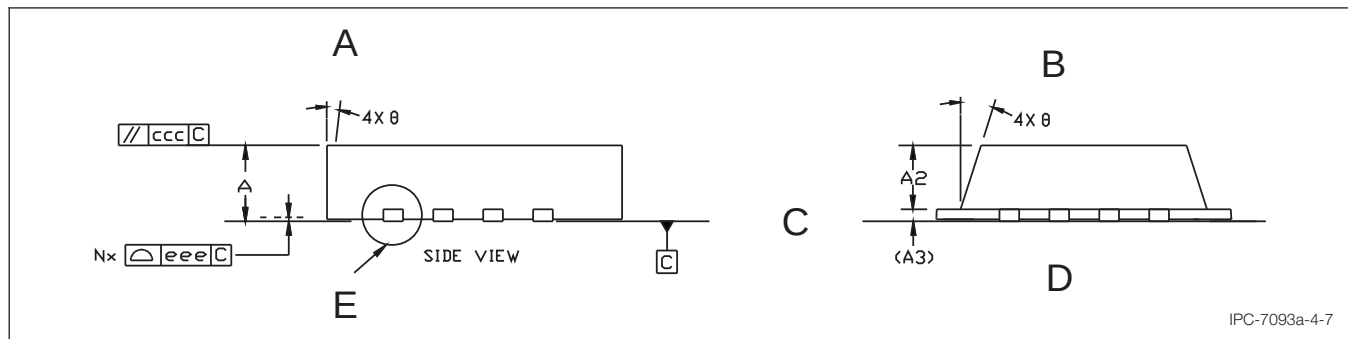


Figure 4-7 Terminal Design Variations for Single-Row Small Outline No-Lead (SON) and Quad Flat No-Lead (QFN) Packaging

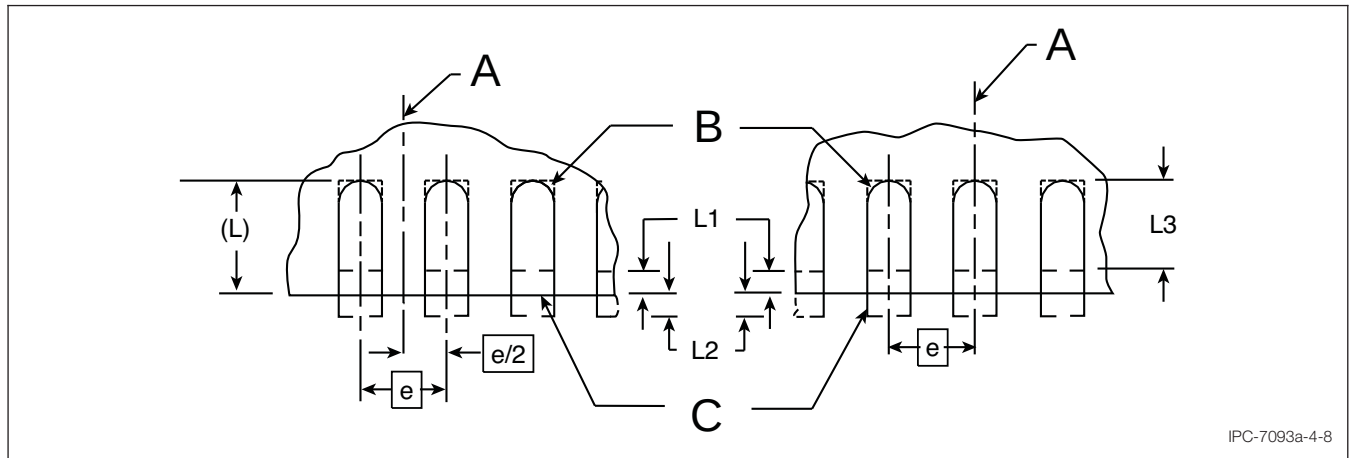
A – Standard (saw cut)
 B – Flange type (molded)
 C – Seating plane
 D – Side view
 E – See A1 detail

There are three terminal variations:

- 1) Pull-back – The terminals are located completely under the package body outline.
- 2) No pull-back – The terminals extend all the way to the edge of the package outline.
- 3) Extended – Terminals extend beyond the body outline (flange type molded version), but the overall measurements do not exceed the D and E dimensions defined in the guideline.

The terminal contacts may be furnished as illustrated in Figure 4-8. The inner edge of corner terminals may be chamfered or rounded to achieve minimum gap k. This feature should not affect the terminal width b, which is measured between 0.15 mm and 0.30 mm from the terminal tip, and it should not include the radiused area (if present).

Suppliers will generally furnish components with a balanced depopulation to reduce unequal surface tension forces that may occur during reflow solder assembly processing. Nonsymmetric package configurations should be separate mechanical outline variations, including depopulation graphics (see Figure 4-9 for three examples). Corner population of terminal features is also an option on the QFN package. SON and QFN, as mentioned, may be furnished with an exposed portion of the die-attach pad on the bottom surface as shown in Figure 4-10. The bottom exposed die-attach pad may be solid or segmented, arranged in a matrix format and may have optional corner radii on each segment.



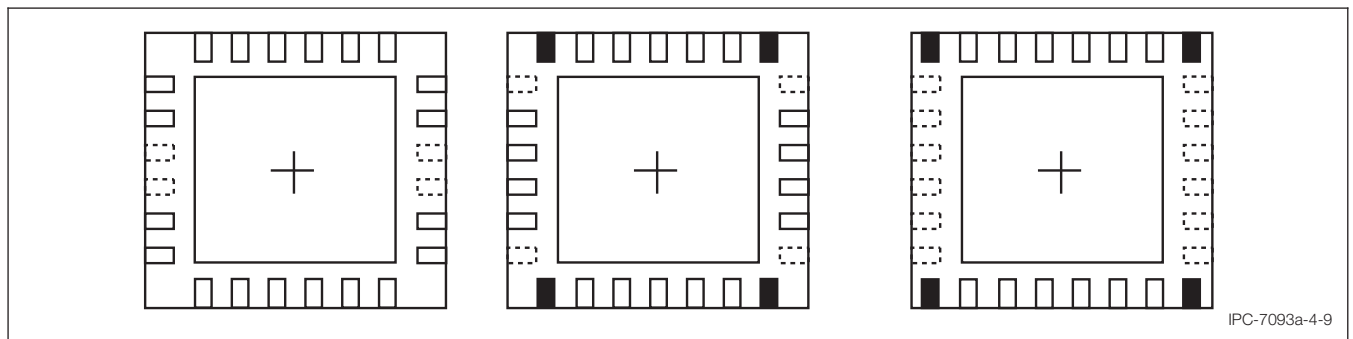
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Figure 4-8 Terminal Contact Layout

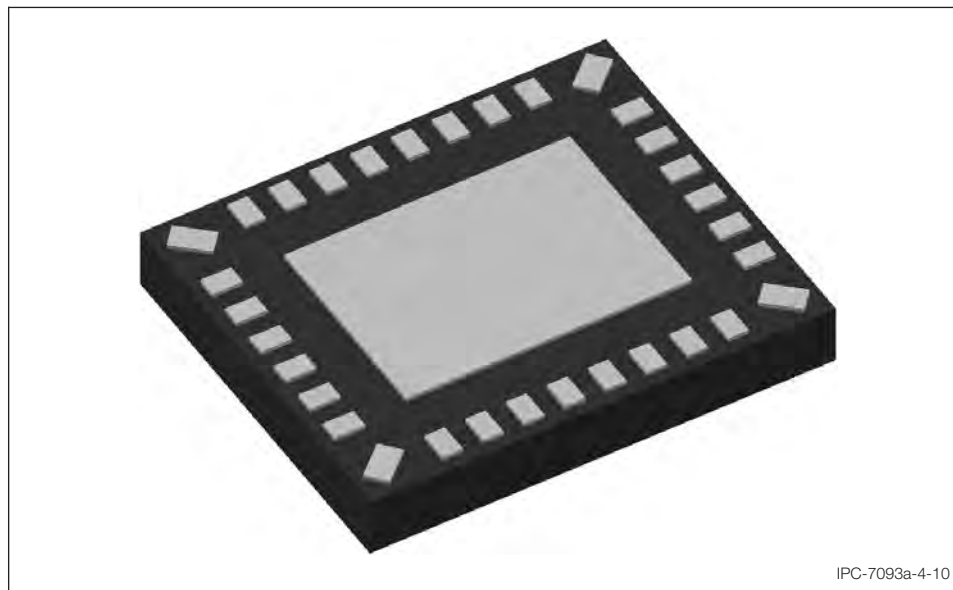
A – Datum A or B

B – Terminal tips (may be rounded)

C – Terminal tip



IPC-7093a-4-9

Figure 4-9 Depopulation Schemes for Single-Row Quad Flat No-Lead (QFN) Packaging

IPC-7093a-4-10

Figure 4-10 Corner Terminals and Exposed Heat Spreader

4.2.3.3 Small Outline No-Lead (SON) / Quad Flat No-Lead (QFN) Terminal Spacing and Dimensions In Figure 4-11, the b dimension represents the width of the metallized terminals (including lead finish) exposed at the bottom surface of the package. The terminal width (b) will vary as the pitch dimension narrows as shown in Table 4-2.

The length (L) of the terminal is measured from the edge of the plastic body. JEP 95, Section 4.8, allows two optional length dimensions defined as short foot and long foot. The terminal is classified as a short-foot variation when L nominal is 0.35 mm to 0.45 mm. If the package terminal dimension L nominal is 0.50 mm to 0.60 mm, it is classified as a long-foot variation.

Regarding contact pitch, although six variations are included in the guideline standard, most products reaching the market have been supplied with either 0.65-mm or 0.50-mm pitch. Devices with 0.40-mm pitch are also offered regularly; however, second-level assembly processing requires very strict control.

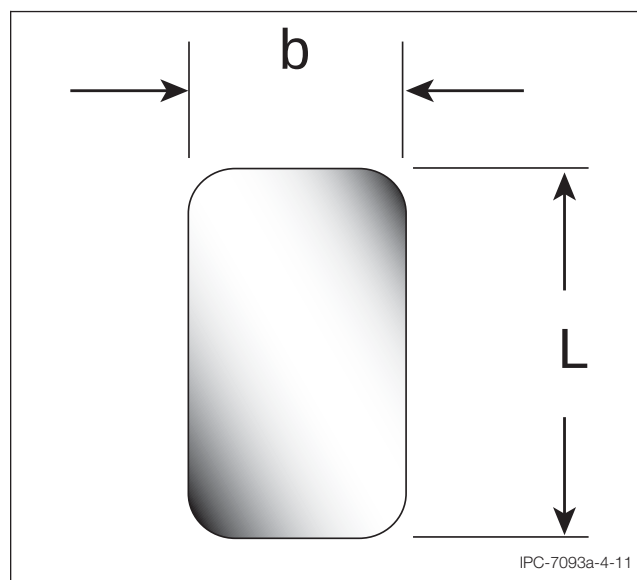


Figure 4-11 Metallized Terminal

b – Terminal width
L – Terminal length

Table 4-2 Terminal Width Variations for Small Outline No-Lead (SON) and Quad Flat No-Lead (QFN) Packages

Contact Pitch (mm)	Terminal Width (b) (mm)		
1.27	0.30	0.40	0.50
1.00	0.30	0.40	0.45
0.80	0.25	0.30	0.35
0.65	0.25	0.30	0.35
0.50	0.18	0.25	0.30
0.40	0.15	0.20	0.25

4.2.4 Punch-Singulated Fine Pitch Square Very Thin and Ultra-Thin Profile Lead-Frame-Based Quad No-Lead Staggered Dual-Row Packages JEP 95, Section 4.23 applies to punch-singulated, fine-pitch, square, very thin and ultra-thin profile lead-frame-based, quad no-lead staggered dual-row packages (with optional thermal enhancements). The examples shown in Figure 4-12 represent dual- and triple-row QFNs with and without optional exposed die-attach pad features.

QFN is described as a plastic semiconductor package with metallized terminals located along the peripheral edges of the bottom surface of the package. As noted, the package terminals are flush with the bottom surface of the plastic package body, so the packages are considered BTC or no-lead. This package has two rows of terminals on all four peripheral edges of the bottom surface of the package (see Figure 4-13).

The dual-row QFN package may have either symmetric or asymmetric terminal patterns. The terminal A1 identifier should be located within the zone indicated on the outline drawing. The top-side terminal A1 indicator may be a molded or marked feature, and an optional indicator on the bottom surface may be furnished as a molded, marked or metallized feature.

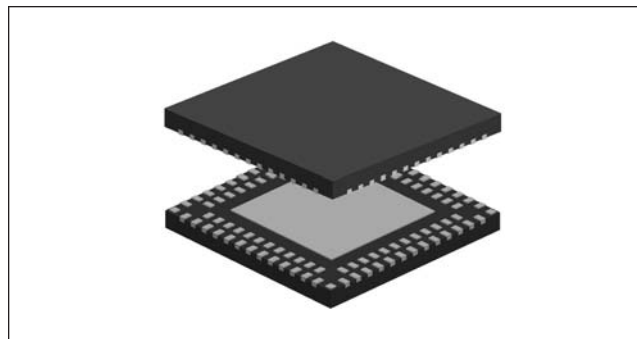
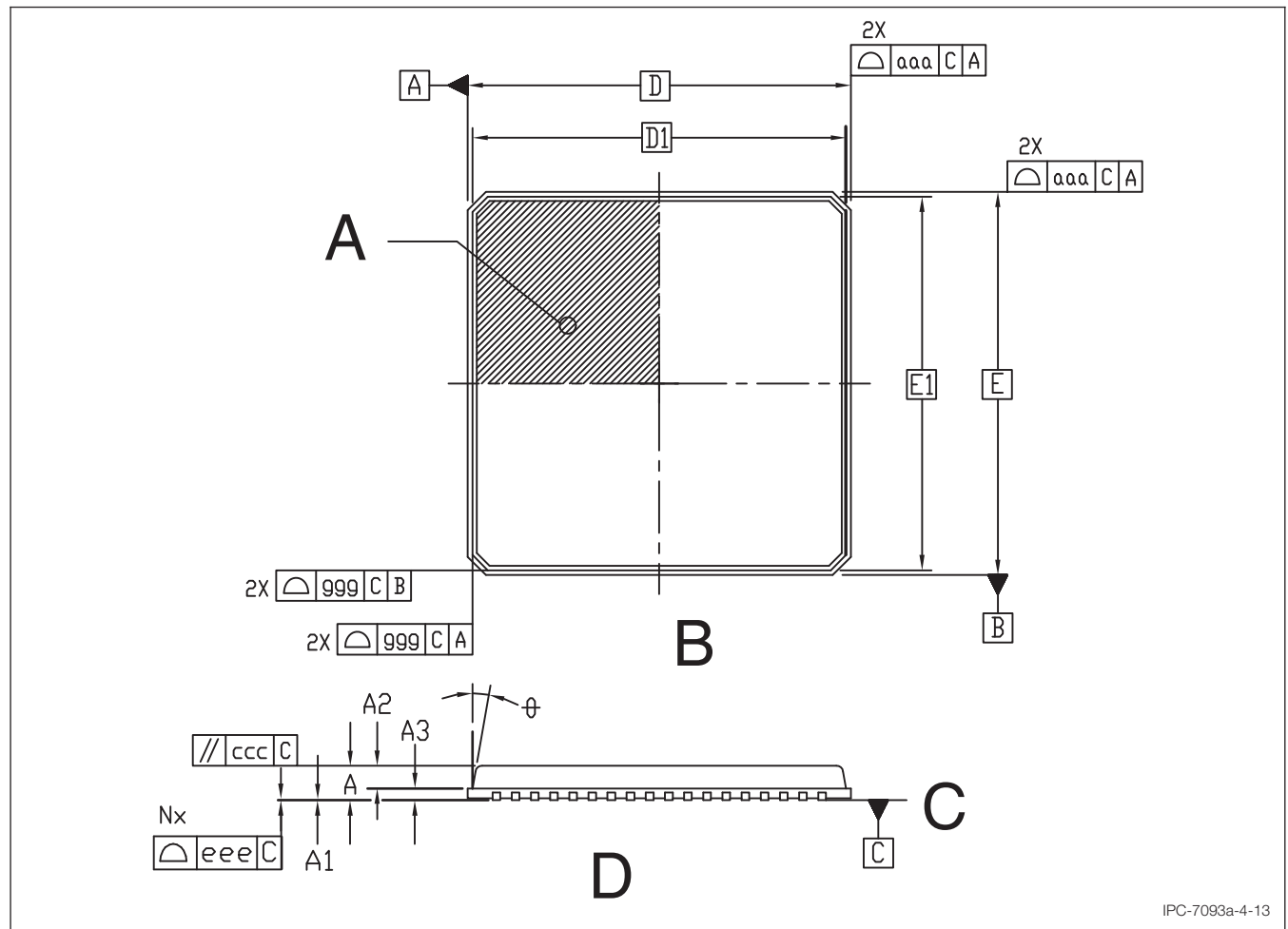


Figure 4-12 Fine-Pitch Two-Row Quad Flat No-Lead (QFN) Packaging



IPC-7093a-4-13

Figure 4-13 Quad Flat No-Lead (QFN) Dual-Row Package (Top and Side Views)

A – Terminal # A1 and B1 index area

B – Top view

C – Seating plane

D – Side view

Regarding the description of the package as very thin and ultra-thin, the overall component height is measured from the seating plane (surface of the host substrate). The very thin (V) version will have a maximum dimension of 1 mm, while the package defined as ultra-thin (W) configuration has a 0.8-mm height limitation. The uniform square body dimensions are established in 1-mm increments from 3 mm to 12 mm and, depending on contact pitch (0.50 mm or 0.65 mm), an established maximum terminal count is possible in the two-row configuration (see Table 4-3).

Table 4-3 Body Outline and Maximum Terminal Count

Body Outline (mm)	Terminal Count by Pitch	
	0.65 mm	0.50 mm
5 x 5	36	52
6 x 6	44	68
7 x 7	60	84
8 x 8	76	100
9 x 9	84	116
10 x 10	100	132
11 x 11	108	148
12 x 12	124	164

Note: Maximum terminal counts are calculated using established formulas.

Outlines with D and E increments < 1 mm will likely be registered as standalone outlines. These outlines should use as many of the algorithms and dimensions stated in this standard as possible to ensure predictability in manufacturing.

Depopulation of terminal features is allowed, but only under the following conditions:

- Depopulation scheme should be consistent in each quadrant of the package.
- Nonsymmetric variations should be broken out as separate mechanical outline variations, including depopulation graphics.

Regarding terminal layout variations, terminals are defined as even- or odd-row spacing, as illustrated in Figure 4-14.

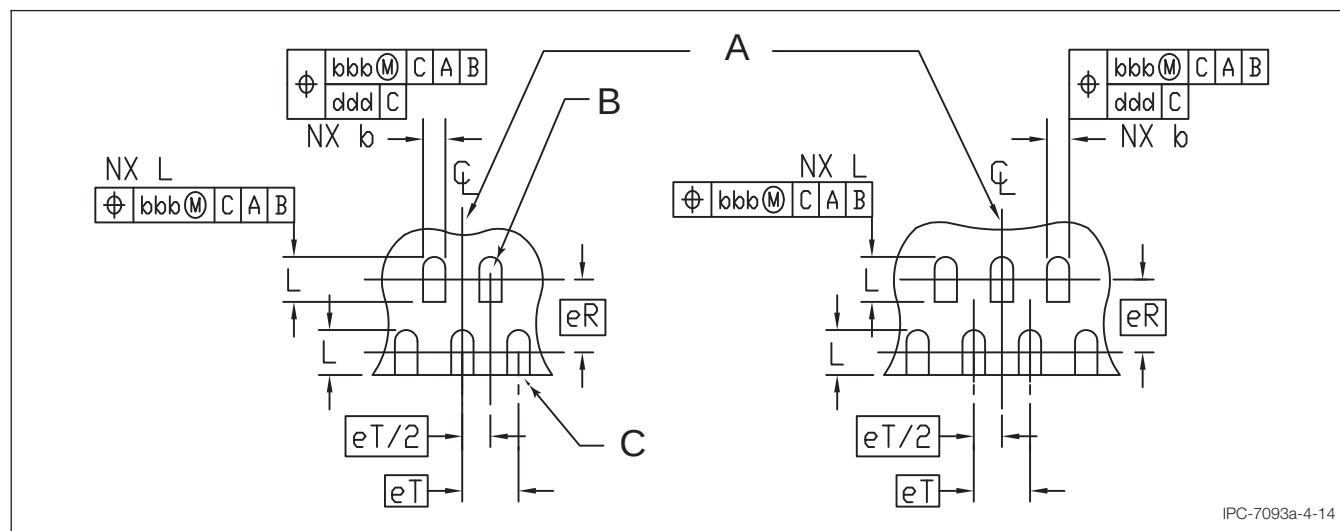


Figure 4-14 Outer and Inner Terminal Layout Variations

A – Datum A or B
B – Inner terminal tip
C – Outer terminal tip

The JEDEC design guide explains that the tolerance that controls the position of the entire terminal pattern (bbb) with respect to datums A and B cannot exceed 0.10 mm. The center of the tolerance zone for each terminal is defined by the basic dimension eT as related to datums A and B.

The bilateral profile tolerance (aaa) that controls the position of the plastic body sides cannot exceed 0.10 mm. The centers of the profile zones are defined by the basic dimensions D and E. Center-line-to-center-line spacing between two adjacent rows of terminals (eR) is 0.65 mm for the 0.50-mm-pitch terminals, and for the 0.65-mm-pitch variation, the spacing is specified at 0.75 mm. The nominal length (L) specified for the metallized terminals (including lead finish) exposed at the bottom surface of the package is 0.40 mm with a minimum/maximum tolerance of 0.10 mm, as illustrated in Figure 4-15 and the dimension included in the figure key. The minimum separation between the inner terminal tip and the heat spreader feature and/or between the terminals at the package corners is 0.20 mm.

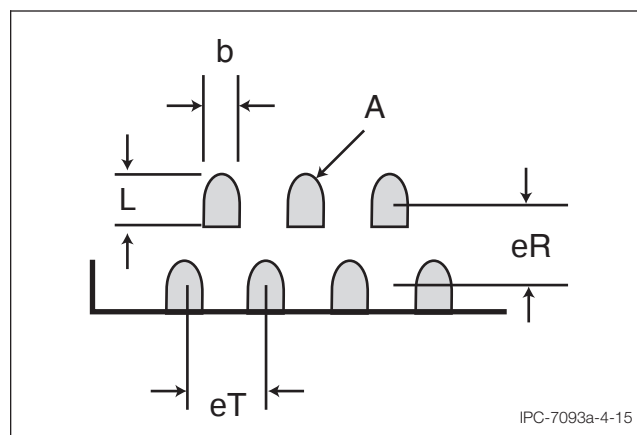


Figure 4-15 Two-Row Terminal Layout

eT – 0.65 mm basic or 0.50 mm basic
eR – 0.75 mm basic or 0.65 mm basic
L – 0.30 mm min. to 0.40 mm max.
b – 0.18 mm min. to 0.30 mm max.
A – Full R (optional)

The tolerance that controls the position of the optional exposed metal heat spreader feature is positioned so the center of the tolerance zone will be the datums defined by the centerlines of the package body. Because the die element is mounted to the inside surface of the heat spreader, thermal transfer of any heat generated by the die can be effectively transferred onto the surface of the host printed board structure. Although the dimple detail on the top surface of the mold compound clearly identifies the orientation of the device, the addition of a small chamfer or notch feature on the exposed die-attach pad (illustrated in Figure 4-16) further assists in confirming the location of the A1 and B1 terminal.

4.2.5 Quad No-Lead Staggered and In-Line Multiple-Row Packages JEP 95, Section 4.19 defines this package family as a plastic quad no-lead (QFN) having staggered or in-line multiple-row terminals. Typical of the preceding package configurations, this QFN family is classified as a plastic semiconductor package with metallized terminals located along the edges of the bottom surface of the package body. The design guide furnishes the primary outline features of the family of packaging, which may be laminate-based or plastic molded lead-frame-based. The primary difference of this variation from the two previous guidelines is that this guideline details the requirements for square or rectangular contact terminal features arranged in two or three rows, typical of those shown in Figure 4-17.

By design, the package terminals are flush with the bottom surface of the plastic package body, so the packages are considered BTC or no-lead and, as noted, the package has two or three rows of terminals on all four edges of the bottom surface of the package.

The package can have a square or a rectangular body as well as symmetric or asymmetric terminal patterns as detailed in Figure 4-18 and Figure 4-19.

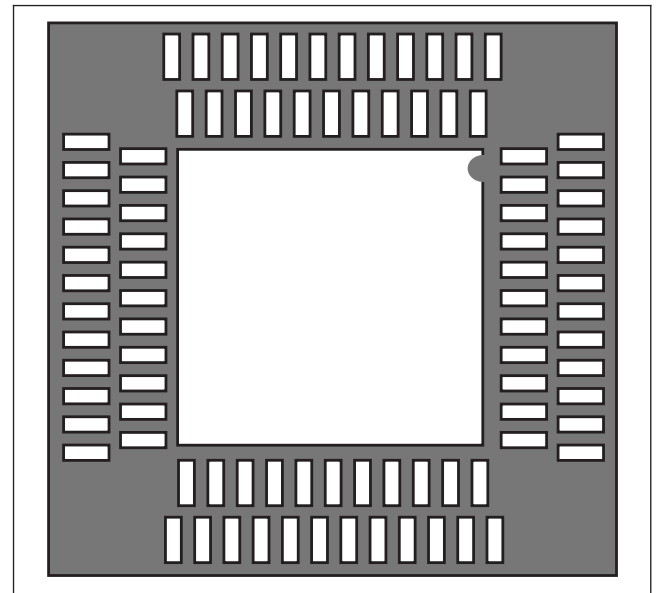


Figure 4-16 Notch Feature on Exposed Die-Attach Pad

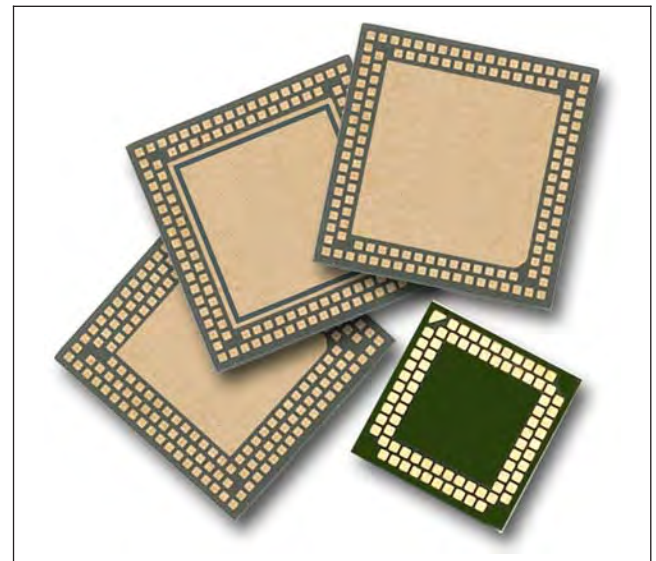


Figure 4-17 Two- and Three-Row Quad Flat No-Lead (QFN) Package Examples

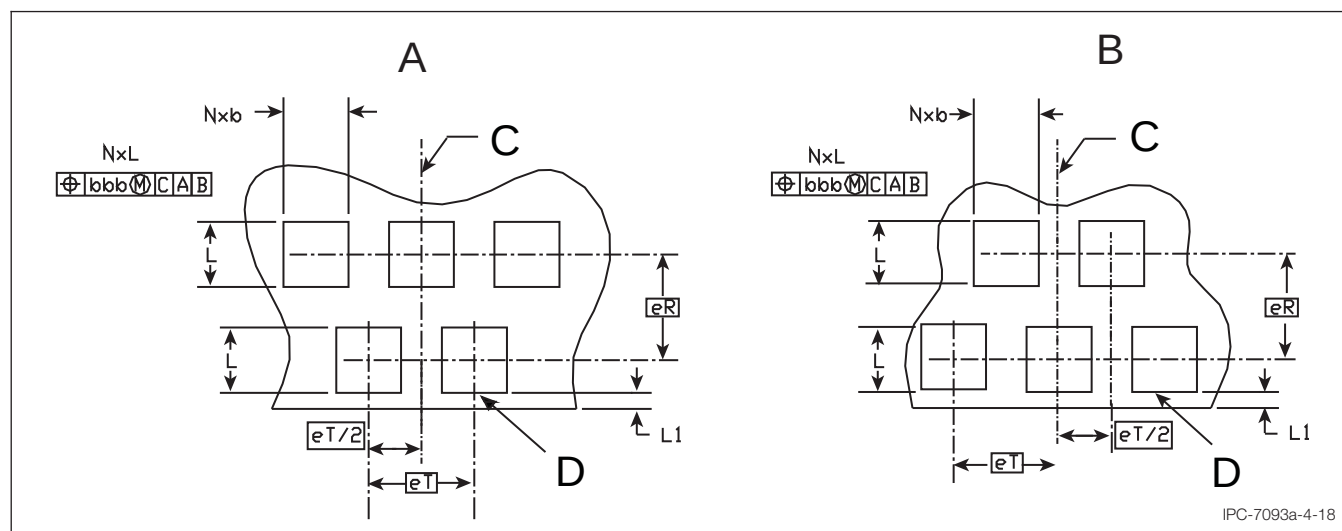


Figure 4-18 Basic Two-Row Terminal Layout Variations

- A - Even terminal format
- B - Odd terminal format
- C - Datum A or B
- D - Terminal tip

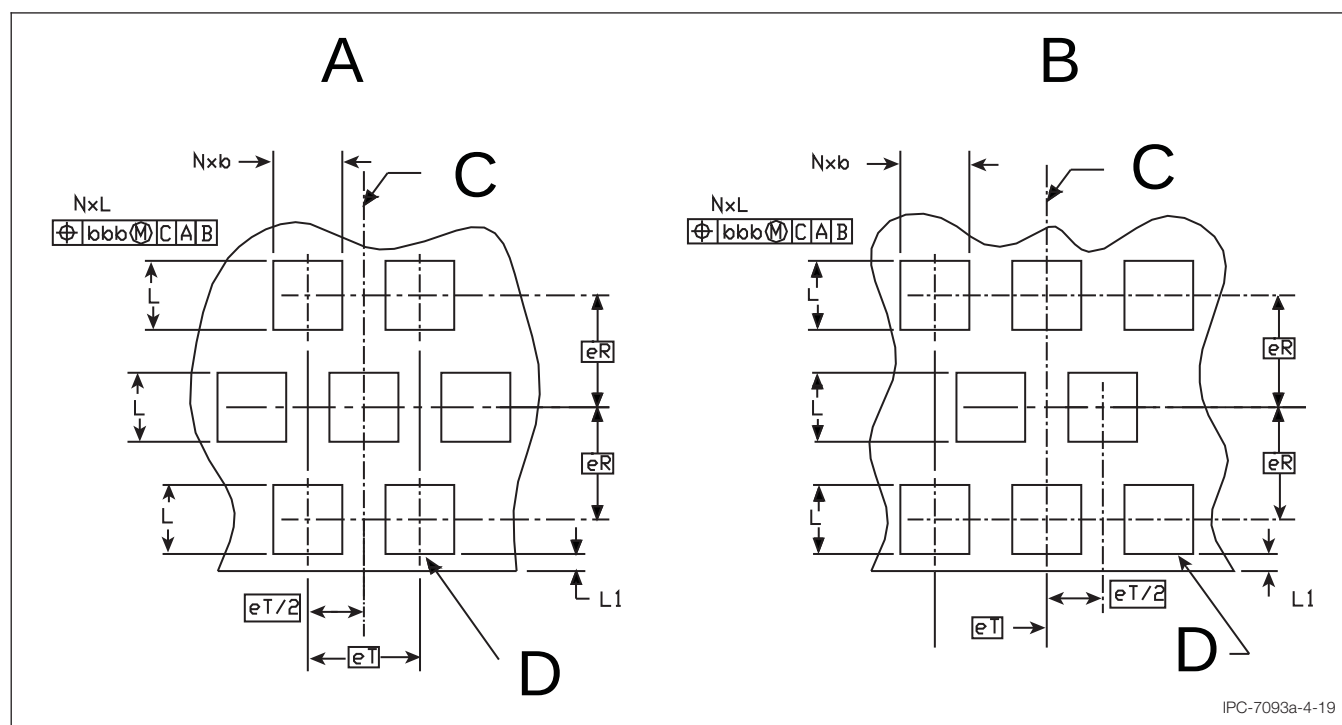


Figure 4-19 Basic Three-Row Terminal Layout Variations

- A - Even terminal format
- B - Odd terminal format
- C - Datum A or B
- D - Terminal tip

Three contact pitch (e) variations are specified: 0.65 mm, 0.50 mm and 0.40 mm. The dimensions defined for the terminals are adjusted to allow clearance at various pitch conditions. The supplier has the option of selecting uniform or nonuniform 'b' and 'L' dimensions to provide a square or rectangular geometry (see Figure 4-20 and Table 4-4).

Table 4-4 Contact Geometries

Contact Pitch (e)	Dimension b (mm)			Dimension L (mm)		
	min	nom	max	min	nom	max
0.65	0.35	0.40	0.45	0.35	0.40	0.45
0.50	0.25	0.30	0.35	0.25	0.30	0.35
0.50*	0.20	0.25	0.30	0.25	0.30	0.35
0.40	0.15	0.20	0.25	0.20	0.25	0.30

*Optional variation to expand the clearance between terminal features.

The tolerance that controls the position of the terminals to each other (e) is nominally defined at 0.05 mm. The tolerance that controls the position of the entire terminal pattern with respect to datums A and B is 0.10 mm for 0.65-mm- and 0.50-mm-pitch packages and is reduced to 0.07 mm for the 0.40-mm-pitch package variation. The center of the tolerance zone for each terminal is defined by the basic dimension e as related to datums A and B.

Overall package outline dimensions are defined as D for package width and E for package length. The current JEDEC guideline specifies that D and E dimensions be in increments of 0.50 mm, ranging from 4 mm to 19 mm. Outlines with D and E increments < 0.50 mm should be registered as stand-alone outlines. These outlines should use as many of the algorithms and dimensions stated in this standard as possible to ensure predictability in manufacturing. The overall package height is not defined, but the JEDEC guideline recommends a profile no higher than 1 mm, where the overall component height is measured from the seating plane (surface of the host substrate). The unilateral tolerance located above the seating plane, wherein the bottom surface of all terminals should be located, is 0.08 mm. This tolerance is commonly known as the coplanarity of the package terminals. The tolerance, which controls the top surface of the package, is nominally 0.1 mm. The basic QFN package outline shown in Figure 4-21 defines the basic outline features referenced in the preceding for D (package width), E (package length) and A (overall package height).

Terminal A1 identifier should be located within the zone indicated on the outline drawing. The top-side terminal A1 indicator may be a molded or marked feature. The optional indicator on the bottom surface may be a molded, marked or metalized feature. See Figure 4-22 for examples of pin 1 indicator.

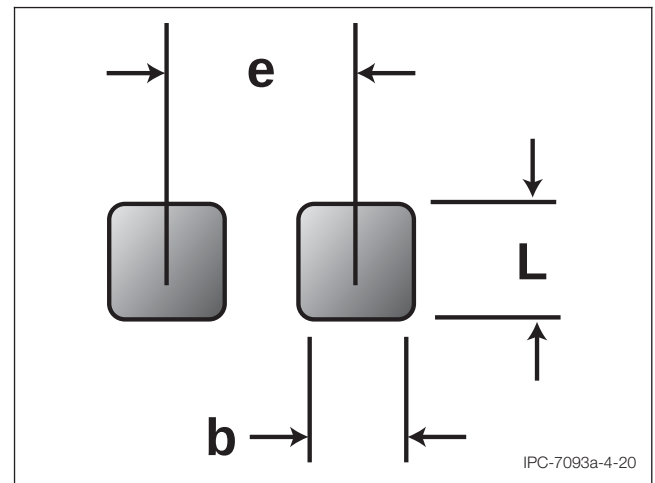


Figure 4-20 Contact Geometry Variations

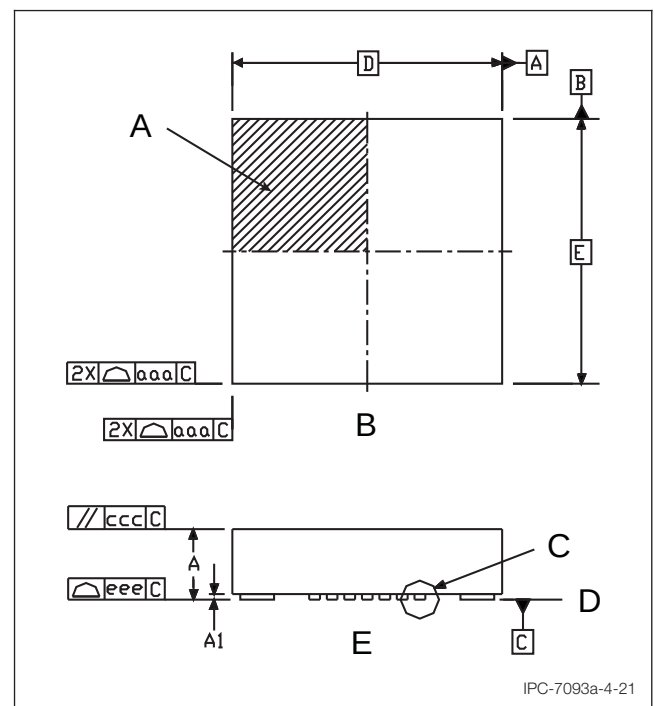


Figure 4-21 Basic Quad Flat No-Lead (QFN) Package Outline Drawing

A – Terminal # A1 index area
B – Top view
C – Detail E
D – Seating plane
E – Side view

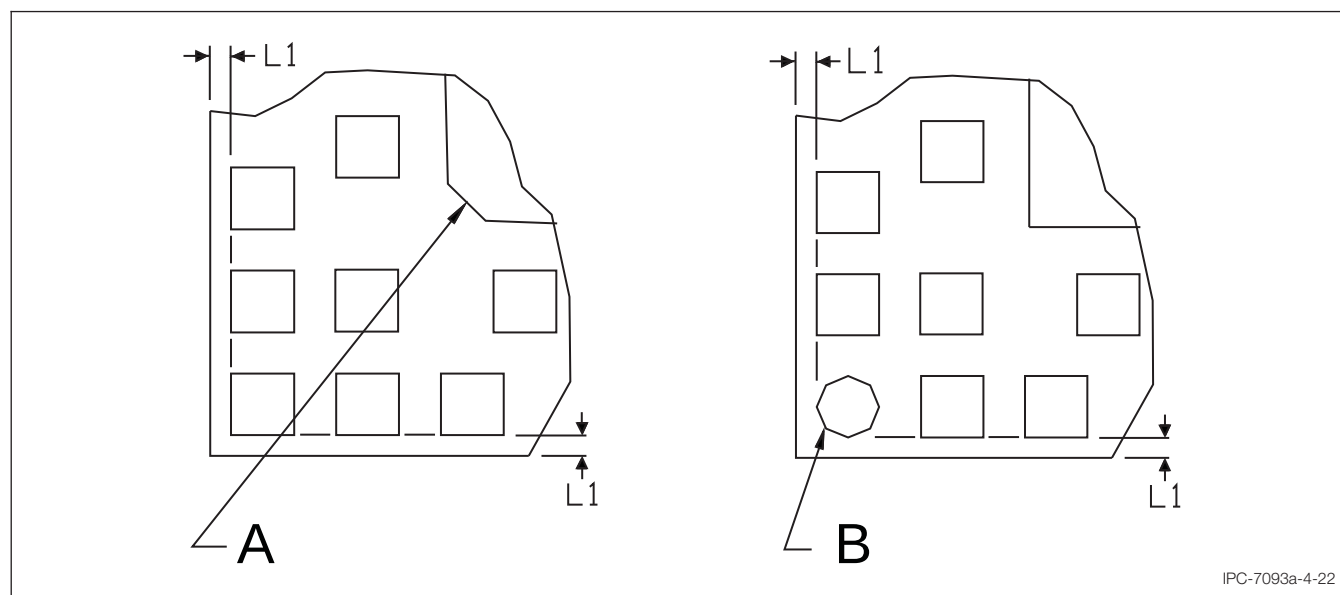


Figure 4-22 Pin 1 Location Option

A – Chamfer corner terminal A1 identifier

B – Circular pad terminal A1 identifier

4.3 Detailed Description of Quad Flat No-Lead (QFN) and Small Outline No-Lead (SON) / Dual Flat No-Lead (DFN) Packages

4.3.1 Manufacturing Methods BTC package configurations are frequently used for individual semiconductor chips and less frequently to package multiple components (see Figure 4-23).

The outline dimensions of the BTC package family range from 1 mm x 1 mm outline having only four terminals to 12 mm x 12 mm outline with as many as 108 terminals. The package height may vary between 0.4 mm to 1.5 mm, but package heights 0.8 mm to 1 mm are more common. There are several terminal spacing (pitch) variations allowed on BTCs, with 0.4 mm, 0.5 mm and 0.65 mm being the most common.

QFNs and SONs (DFNs) are most commonly assembled on an etched or stamped metal lead frame that is 0.150-mm to 0.200-mm thick. Figure 4-24 shows the die-attach side of a multiple-site lead frame panel. Figure 4-25 shows the bottom side of the panel.

The lead frame panel shown in Figure 4-24 and Figure 4-25 measures 75 mm x 300 mm and includes four sections, each having 42 QFN sites (7 mm x 7 mm). The bottom, or terminal side, of the lead frame panel will be covered with a protective film that prevents mold compound from encroaching onto the terminals' surface during the over-mold process.

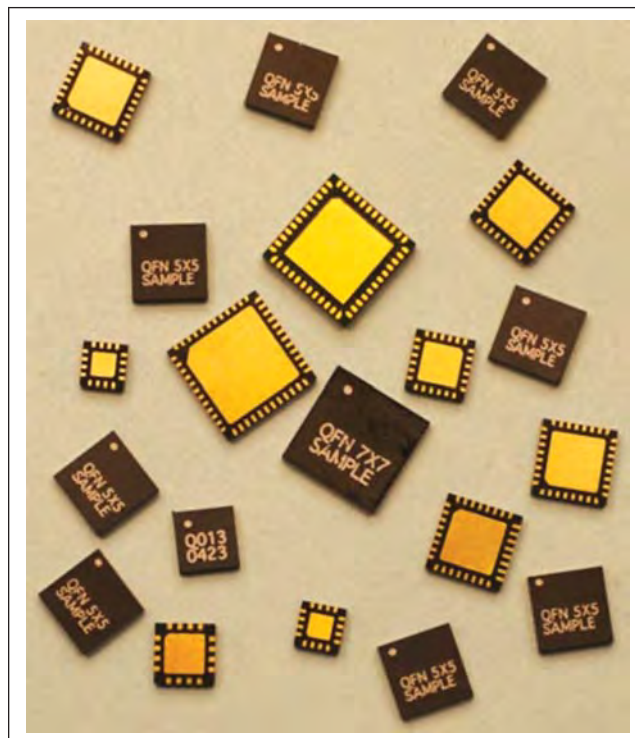


Figure 4-23 Various BTC Packages

Lead frames are usually made from rolled sheet Cu etched from both sides with slightly different patterns. The difference in etch pattern gives the undercut evident in the drawings and sketches in this section. The major purpose for the undercuts is to provide mechanical interlocking of the mold compound, which leads to increased mechanical strength.

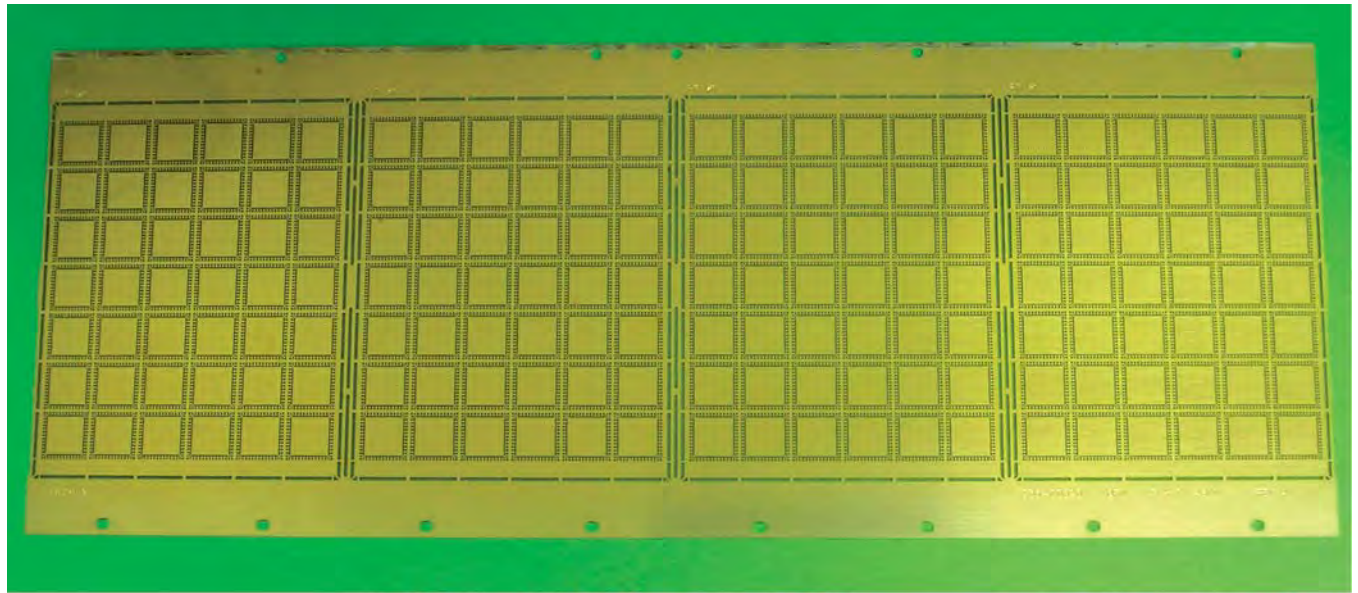


Figure 4-24 Typical Die Attach Side Lead Frame with NiPdAu Finish for QFNs

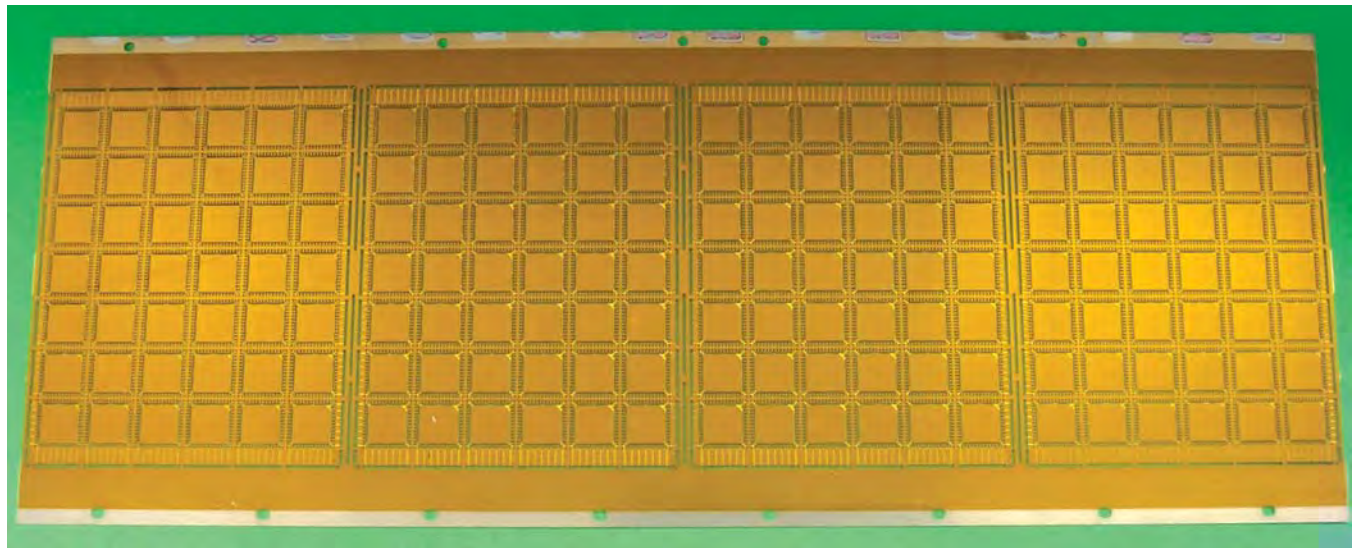


Figure 4-25 Typical Solder Pad Side of a Quad Flat No-Lead (QFN) Panel with Tape Over the Lead Frame

In preparation for package assembly and to accommodate the eventual mounting of the BTC package, the lead frames are electroplated with alloys compatible with wire-bond processing and reflow soldering (NiPdAu alloy composition being most common).

Another option is to spot-plate the wire-bond sites with an Ag alloy, leaving the remaining area of the Cu-based lead frame without plating until after the over-mold process. The remaining exposed contact and thermal pad features on the panel are plated with a Sn alloy finish for solder attachment.

Cu is also used to replace Au wire in high-volume wire bonding applications. In high volume, the cost savings of Cu vs. Au is significant, which is why many wire-bonded packages, including BTCs, are produced using that material.

While Cu saves significant cost in volume, much tighter control over the bonding parameters (e.g., ball size, force, temperature, ultrasonic power, duration) is required for high-quality, robust Cu wire bonding for each specific assembly than for Au. A careful set of experiments (design of experiments (DOE)) is often required to define these Cu bonding parameters for each chip/substrate combination and assembly. The cost of this DOE is significant, so recovering that cost through the lower cost of Cu vs. Au requires the production of many parts.

The BTC package assembly process may vary somewhat from one supplier to another, but the basic sequence of assembly for the product described in the preceding will follow the flow of the diagram detailed in Figure 4-26.

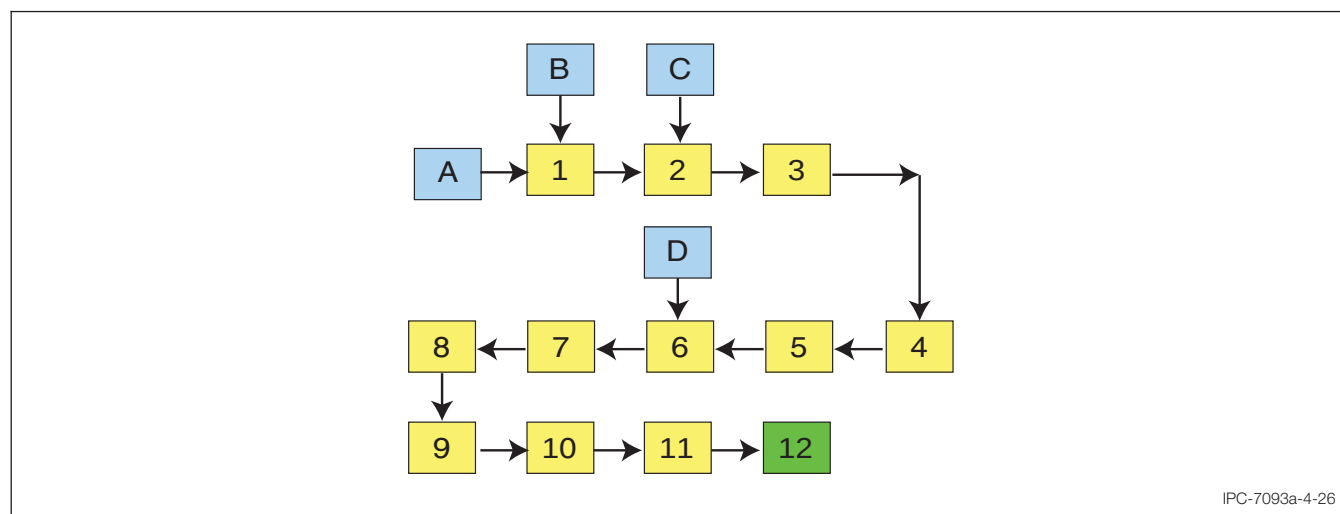


Figure 4-26 Quad Flat No-Lead (QFN) Fabrication with Saw Singulation

Note: Process temperatures used at the various assembly steps are dependent on the materials selected.

Blue – Raw material

Yellow – Assembly process step

Green – Finished part

A – Lead frame

B – Die-attach material

C – Die

D – Mold compound

1 – Dispense die-attach material

2 – Place die

3 – Cure die-attach material (125 °C to 200 °C)

4 – Au/Cu ball bond (150 °C)

5 – Place lead frame in cavity mold

6 – Transfer mold to lead frame (150 °C)

7 – Remove lead frame array from mold

8 – Mark

9 – Saw singulate

10 – Test and bin

11 – Bake (depending on MSL rating)

12 – Package finished part for shipment

Figure 4-27 shows an over-molded version of the lead frame in Figure 4-24. The example is a four-section over-molded array right after it was removed from the mold. The dark areas are the molding compound that form the four arrays, each of which measures approximately 45 mm x 55 mm. The dark areas around the periphery and between the molded arrays are mold compound that fills slots in the lead frame.

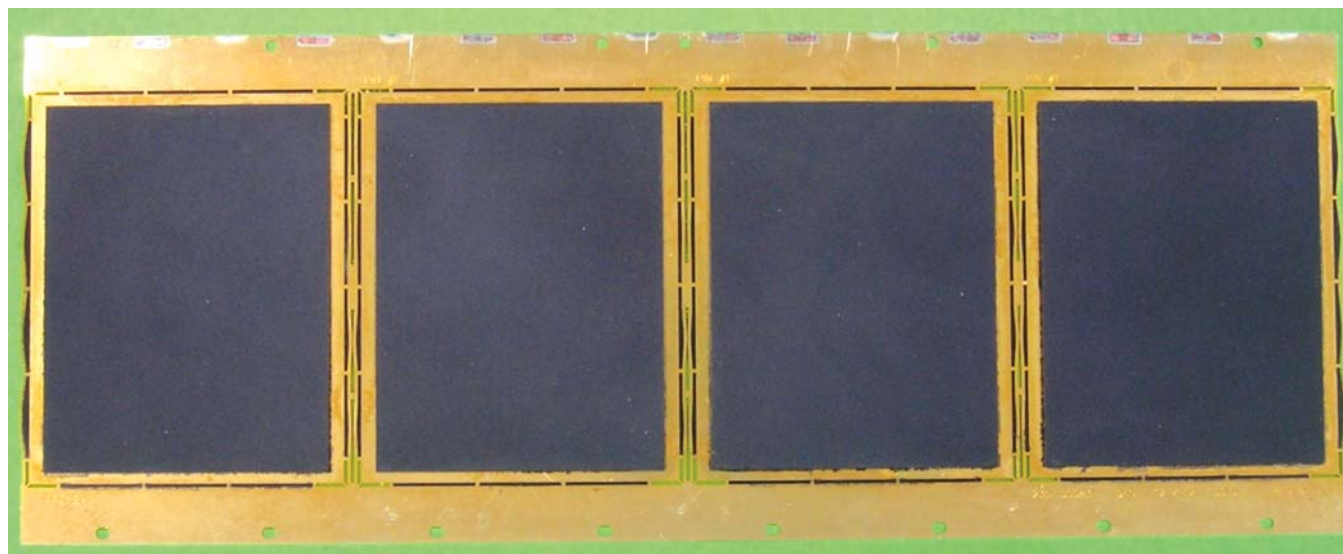


Figure 4-27 Over-Molded Lead Frame Configuration

After the over-mold process, individual devices will be marked and singulated from the panel format. The most common method for singulation of BTCs is using a precision saw. An alternative method uses a punch press operation. For this method, the mold design will be segmented at each device site to provide access for the die punch. Due to the high cost of tooling and additional equipment required for punch singulation, this technique is typically reserved for very-high-volume production.

Figure 4-28 shows the process flow for punch-singulated QFNs.

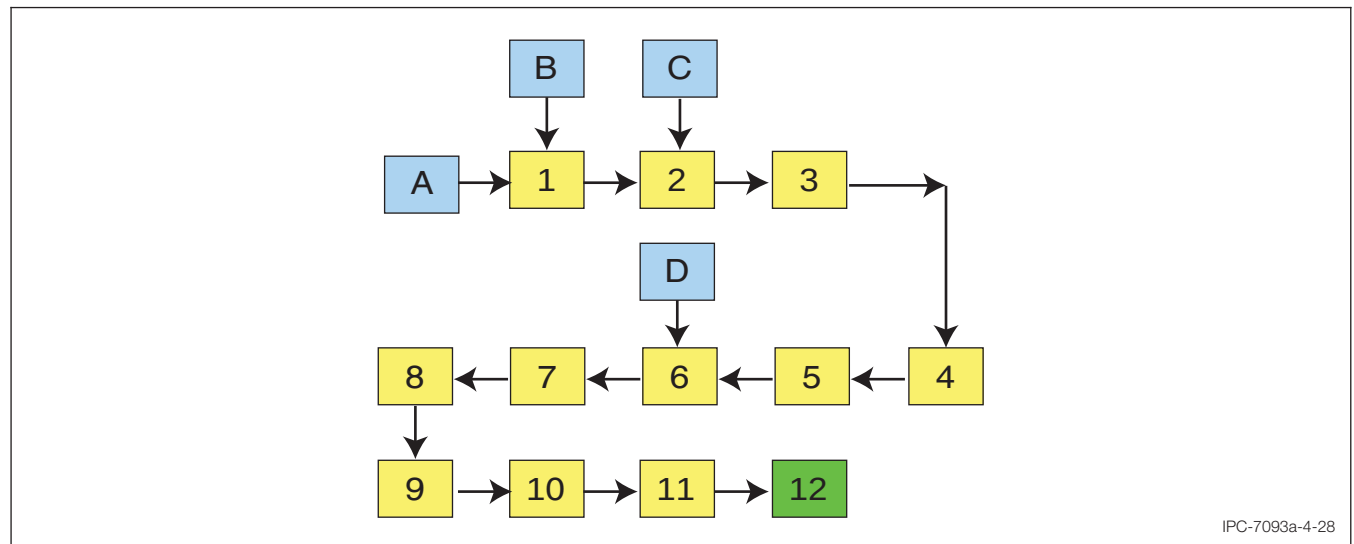


Figure 4-28 Quad Flat No-Lead (QFN) Fabrication with Punch Singulation

Note: Process temperatures used at the various assembly steps are dependent on the materials selected.

Blue – Raw material
 Yellow – Assembly process step
 Green – Finished part
 A – Lead frame
 B – Die-attach material
 C – Die
 D – Mold compound

1 – Dispense die-attach material
 2 – Place die
 3 – Cure die-attach material (125 °C to 200 °C)
 4 – Au/Cu ball bond (150 °C)
 5 – Place lead frame in cavity mold
 6 – Transfer mold to lead frame (150 °C)

7 – Remove lead frame array from mold
 8 – Mark
 9 – Punch singulate
 10 – Test and bin
 11 – Bake (depending on MSL rating)
 12 – Package finished part for shipment

The mold design for the punch singulation method is more complex and expensive than those used for saw singulation. Punch singulation requires a mold with a cavity for each part so the web of the lead frame remains exposed between individual parts. This web is punched out in a single stroke with a die that matches the part.

Saw singulation and punch singulation leave bare Cu edges on the leads where they are cut from the lead frame. These bare edges can serve as a surface for a solder fillet if the solder system will wet the bare Cu. Some users may also require BTC suppliers to take additional measures, after singulation, to preserve flank solderability. These measures are intended to allow users to rely on toe fillets formed along the BTC flanks as an aid to reliable assembly inspection.

The illustrations in Figure 4-29 show the detailed differences that result when using punch singulation and saw singulation. While punch-singulated packages are individually punched from the molded strip during final assembly, the saw-singulated packages are assembled in array format and separated into individual components during the final sawing operation.

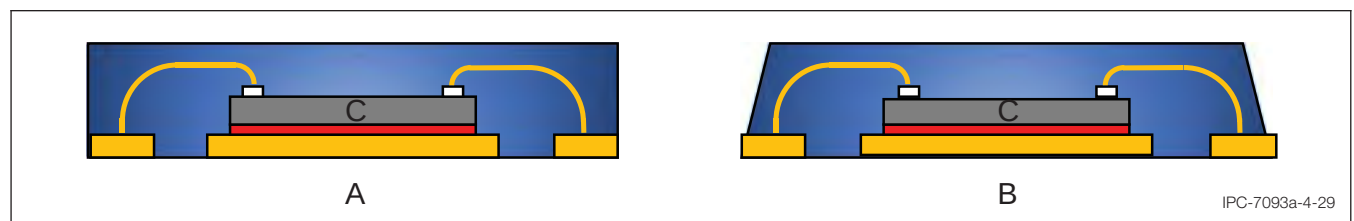


Figure 4-29 Comparing Punch-Singulated and Saw-Singulated Packages with Wire Bond Options

A – Punch-press singulation
 B – Saw-cut singulation
 C – Die

The image on the left in Figure 4-29 is punch-singulated from an array of individually molded sites. The mold cavity walls have some draft shown in the sketch to facilitate removing the molded parts from the cavities.

A second characteristic of punch-singulated devices evident in the image on the left in Figure 4-29 is the small lead frame extension beyond the edge of the molding compound to provide space to prevent the die from cutting the mold compound.

The image on the right in Figure 4-29 shows the saw-singulated cross-section that lacks both draft and the extended lead.