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Design and Assembly Process Implementation for Flip Chip and Die-Size Components

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Association Connecting Electronics Industries



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Developed by the Flip Chip Mounting Task Group (5-21g) of the
Assembly & Joining Processes Committee (5-20) of IPC

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Users of this publication are encouraged to participate in the
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Table of Contents

1 SCOPE	1	4.5.3 Solder Paste Deposition	17
1.1 Target Audience and Intent	1	4.5.4 Solder Electroplating	18
1.2 Definition of Requirements	1	4.5.5 Other Bumping Techniques and Materials	18
1.3 Classification of Product	1	4.6 Ball and Bump Terminal Process for Flip Chip	18
2 APPLICABLE DOCUMENTS	1	4.6.1 Dimensional Control	18
2.1 IPC	1	4.6.2 Metallurgical Integrity	19
2.2 Joint Industry Standards	2	4.6.3 Cleanliness of Bumping Site	19
2.3 JEDEC	3	4.7 Surface Redistribution	19
3 REQUIREMENTS AND TECHNOLOGY OVERVIEW	4	4.8 Cu Post or Pillar Termination	20
3.1 Terms and Definitions	4	5 FLIP CHIP POST-FABRICATION PROCESSING	20
3.1.1 Acronyms and Abbreviations	4	5.1 Test and Reliability Screening	20
3.2 History of Flip Chip Mounting	4	5.1.1 Known Good Die (KGD)	20
3.2.1 Advantages of Flip Chip Mounting	5	5.1.2 Known Quality Die (KQD)	20
3.3 History of Die Size and Chip Scale Array Packaging	5	5.1.3 Wafer Testing and Equipment Challenges/Concerns	20
3.3.1 Film-Based Package Substrate	6	5.1.4 Reliability Screening at the Wafer or Die Level	21
3.3.2 Commercial Package Variations	7	5.2 Wafer Thinning (Grinding and Polishing)	22
3.3.3 Redistribution	7	5.2.1 Thinning and Polishing Process	22
3.3.4 Advantages of Die-Size Package and Chip Scale Package (CSP) Technology	7	5.2.2 Processing Effect on the Quality of the Die	22
4 FLIP CHIP TECHNOLOGY	8	5.3 Singulation	22
4.1 Electrical Design Considerations	8	5.3.1 Sawing	22
4.1.1 Equivalent Circuitry	8	5.3.2 Scribe and Break	23
4.1.2 Final Metal Traces	9	5.4 Laser Sawing	24
4.1.3 Inductance and Capacitance	10	5.4.1 Wafer Dicing With Deep Reactive-Ion Etching (DRIE) Process	24
4.1.4 High-Frequency Performance	10	5.5 Shipping and Handling	24
4.2 Thermal Design	10	6 FLIP CHIP INTERCONNECTING SUBSTRATES	25
4.2.1 Bump Interconnect Thermal Model	11	6.1 Substrate Base Material	25
4.3 Flip Chip Preparation for Mounting	12	6.1.1 Flexible Base Substrates	25
4.3.1 Design Guide Checklist	12	6.1.2 Reinforced-Resin Substrates	26
4.3.2 Final Metal	14	6.1.3 Cu Conductor Base Metals for Flexible and Reinforced Laminates	26
4.3.3 Surface Passivation	14	6.1.4 Ceramic Substrates	26
4.3.4 Footprint Population	15	6.1.5 Si-Based Substrates	27
4.4 Design Output Requirements	16	6.2 Surface Finish Properties	28
4.4.1 Final Metal Reticle Mask	16	6.2.1 Chemical Plating Finishes (Electrolytic and Electroless)	28
4.4.2 Passivation (Terminal Via) Reticle Mask and Plan	16	6.2.2 Thick-Film Metallic Finishes	28
4.4.3 Unit Cell Design	16	6.2.3 Thick-Film Deposition Processes	28
4.5 Land Pattern Design	17		
4.5.1 Land Pattern for Ceramic Substrate Design	17		
4.5.2 Solder Bumping	17		

6.2.4	Sputtered (Thin-Film) Conductive Finishes	28	7.6	Contact Array Redistribution	40
6.2.5	Sputtered Metal Deposition Process	28	7.6.1	Staggered-Array Planning	40
6.3	Alternative Circuit Forming Processes	28	7.6.2	Die Shrink Considerations	41
6.3.1	Laser Direct Image (LDI)	28	7.7	Flip Chip and Chip Scale Package (CSP) Assembly	41
6.3.2	Inkjet Imaging	29	7.7.1	Passivation Material Requirements	41
6.3.3	Silkscreen and Stencil Printing	29	7.7.2	Requirements for Bump and Ball Terminal Alloy	41
6.3.4	Direct Image Conductive Inks Process	29	7.7.3	Flux for Flip Chip and Chip-Size Package Mounting	42
7	PACKAGE-LEVEL STANDARDIZATION	30	7.7.4	Solder Paste for Flip Chip and Chip- Size Package Mounting	42
7.1	Controlling Physical Features	30	7.7.5	Electrically Conductive Adhesives for Flip Chip Attachment	42
7.2	Mechanical Outline Standards for Die-Size Ball Grid Array (DSBGA) Packaging	30	7.7.6	Underfill Material Requirements	42
7.2.1	JEDEC Standard for Die-Size BGA (DSBGA)	31	7.7.7	Encapsulation Material Requirements	43
7.2.2	Ball Terminal Measurement	32	7.8	Flip Chip and Chip Scale Assembly Performance Requirements	43
7.2.3	Die-Size Ball Grid Array (DSBGA) Outline Consideration	32	7.8.1	Thermal Cycle Stress Testing of Soldered Assemblies	43
7.3	Electrical Performance Planning	32	7.9	Trays for Flip Chip and Chip-Size Packages (Shipping and Delivery)	43
7.3.1	Modeling and Simulation	33	8	SYSTEM-LEVEL ISSUES	44
7.3.2	Electromagnetic Radiation	33	8.1	Design for Assembly	44
7.3.3	Electrical Bias Created by Nonelectrical Phenomena	33	8.1.1	Flip Chip, Die-Size Ball Grid Array (DSBGA) Land Pattern Design	44
7.4	Standards for Package-Level Substrate Design and Performance	33	8.1.2	Component Clearance	45
7.4.1	Qualification and Performance of Organic Structures for Flip Chip Mounting	33	8.1.3	Rigid Organic Substrate Design	45
7.4.2	Qualification and Performance for Organic Single and Multichip Mounting and Interconnecting Structures	33	8.1.4	Restriction of Hazardous Substances (RoHS)-Compliant Surface Finish Selection	47
7.4.3	Qualification and Performance Standard for Inorganic Mounting Structures	34	8.2	Flexible Circuit Substrate Design	48
7.4.4	Test Methods for Qualification and Evaluation of Flip Chip Mounting Structures	34	8.2.1	Material for Harsh Environments	48
7.4.5	Mechanical Performance Test Requirements	34	8.2.2	Rigid-Flex Substrates	48
7.5	Flip Chip Development and Performance Standards	34	8.3	Ceramic Substrate Design	49
7.5.1	Flip Chip Integrated Circuit (IC) Component Design	34	8.3.1	Thick-Film on Ceramic Substrates	49
7.5.2	Wafer Fabrication and Bond Site Planning	35	8.3.2	Thin Film on Ceramic Substrates	50
7.5.3	Wafer-Level Terminal Forming Methodologies	35	8.3.3	Multiple-Layer Ceramic Substrates	50
7.5.4	Molded Fan-Out Wafer-Level Process (FOWLP)	36	8.4	Substrate Design Guide Checklist	51
7.5.5	Design Standards for Wafer-Level Ball Grid Array (WLBGA)	36	9	FLIP CHIP AND DIE-SIZE DEVICE ASSEMBLY ...	51
7.5.6	Bond Pad and Array Planning	37	9.1	Substrate Preparation	51
7.5.7	Critical Factor: Bump Attachment and Bonding	39	9.2	Flip Chip and Die-Size Device Placement	51
7.5.8	Metallurgical Integrity	39	9.3	Attachment Processes	52
			9.3.1	Solder Attachment Process for Flip Chip	52
			9.3.2	Reflow Soldering	52
			9.3.3	Solder Alloys and Process Parameters	52
			9.3.4	Solder Stencil Development	53

9.4	Solder Process Profile Planning	54	10.8.2	Solder Interface Grain Structure Effects	67
9.4.1	Reflow Process Implementation	55	10.8.3	Global Expansion Mismatch	68
9.4.2	Solder Process Evaluation	55	10.8.4	Local Expansion Mismatch	68
9.5	Thermocompression and Ultrasonic Bonding ...	56	10.8.5	Internal Expansion Mismatch	68
9.6	Adhesive Interconnection	56	10.8.6	Solder Attachment Failure	68
9.6.1	Anisotropic Conductive Adhesives	56	11	RELIABILITY PREDICTION MODELING	68
9.6.2	Isotropic Conductive Adhesives	57	11.1	Large Temperature Excursions	69
9.6.3	Nonconductive Adhesive Process	57	11.2	Creep-Fatigue Modeling Creep	69
9.7	Cleaning	57	11.3	Statistical Failure Distribution and Failure Probability	69
9.7.1	No-Clean Flip Chip Processes	57	11.4	Damage Modeling	69
9.7.2	Aqueous Flip Chip Cleaning Technology	57	12	VALIDATION AND QUALIFICATION TESTING ...	70
9.8	Attachment Assessment	58	12.1	Screening Procedures	70
9.8.1	Optical Inspection	58	12.2	Evaluating Solder Joints	70
9.8.2	X-Ray Inspection	58	12.3	Testing Scenarios	70
9.9	Underfill (Flip Chip Encapsulation)	58	12.3.1	Critical Environmental Testing	70
9.9.1	Capillary Flow Underfill Process Overview	59	12.3.2	Die Testing for Known Good Die (KGD)	70
9.9.2	Fluxing (No Flow) Underfill	59	12.4	Inspection and Process Control Assurance	71
9.9.3	Removable/Reworkable Underfill	60	12.5	Total Quality Management and Manufacturing (TQMM)	71
9.9.4	Substrate Surface Compatibility	60	13	SUPPLY CHAIN ISSUES	71
9.10	Electrical Test	60	13.1	Supply Chain Traceability	71
9.11	Rework and Repair	60	13.2	Configuration Management	71
9.11.1	Hot-Air Process for Device Removal	60	APPENDIX A	Glossary	72
9.11.2	Laser Process for Device Removal	61	APPENDIX B	Acronyms	78
10	REQUIREMENTS FOR BOARD- AND MODULE-LEVEL RELIABILITY	61	Figures		
10.1	Robustness of Products to Use	61	Figure 3-1	Solid Copper Core Ball Contact	4
10.2	Chip Scale Package Robustness and Reliability	61	Figure 3-2	Flip Chip With a Ag-Coated Cu Core Terminal to Maintain Uniform Stand-Off Height	4
10.3	Reliability Factors	63	Figure 3-3	Solder-Bumped Wafer-Level Ball Grid Array (WLPGA)	5
10.3.1	Wear-Out Failures	63	Figure 3-4	Array-Configured Die-Size Ball Grid Array (BGA)	5
10.3.2	Creep	63	Figure 3-5	Face-Down Mounted Die (Flip Chip) on Organic Substrate	6
10.3.3	Electromigration	63	Figure 3-6	Face-Up Wire-Bond Chip Scale Package (CSP)	6
10.3.4	Corrosion	63	Figure 3-7	Narrow Opening in a Substrate Provides Access for Through-Window Wire-Bond Process	6
10.3.5	Thermomigration	64	Figure 3-8	Commercial Flip-Chip and Wafer-Level Semiconductor Package Innovations	7
10.4	Solder Bump Mechanical Reliability	64	Figure 3-9	Wire-Bond Pad to Array Redistribution Provides Wider Spacing and Larger Terminal Features	7
10.4.1	Strain	64			
10.4.2	Effect of Thermal Expansion Mismatch	64			
10.4.3	Temperature Cycling Frequency	65			
10.5	Wear-Out Mechanisms	65			
10.5.1	Reliability Factors	65			
10.5.2	Benefits of Reinforcement	66			
10.6	Event-Related Failures	66			
10.7	Design for Reliability (DfR)	66			
10.8	Damage Mechanisms and Failure of Solder Attachments	66			
10.8.1	Solder Joints and Attachment Types	67			

Figures

Figure 3-1	Solid Copper Core Ball Contact	4
Figure 3-2	Flip Chip With a Ag-Coated Cu Core Terminal to Maintain Uniform Stand-Off Height	4
Figure 3-3	Solder-Bumped Wafer-Level Ball Grid Array (WLPGA)	5
Figure 3-4	Array-Configured Die-Size Ball Grid Array (PGA)	5
Figure 3-5	Face-Down Mounted Die (Flip Chip) on Organic Substrate	6
Figure 3-6	Face-Up Wire-Bond Chip Scale Package (CSP)	6
Figure 3-7	Narrow Opening in a Substrate Provides Access for Through-Window Wire-Bond Process	6
Figure 3-8	Commercial Flip-Chip and Wafer-Level Semiconductor Package Innovations	7
Figure 3-9	Wire-Bond Pad to Array Redistribution Provides Wider Spacing and Larger Terminal Features	7

Figure 4-1	Bump Equivalent Circuit (Redistributed Chip) ..	8	Figure 5-8	Horizontal and Vertical Carriers for Transporting Wafers	25
Figure 4-2	Solder Bump Electrical Path (Redistributed Chip)	9	Figure 6-1	Low Input/Output (I/O) Flip Chip Device With Solder Bump Terminals	26
Figure 4-3	Final Metal Trace and Underlying Traces (Cross-Section)	10	Figure 6-2	High Input/Output (I/O) Flip Chip on Multilayer Ball Grid Array (BGA)	27
Figure 4-4	Thermal/Electrical Analogy	11	Figure 6-3	Laser Direct Imaging (LDI)	28
Figure 4-5	Bump Interconnect Equivalent Model	11	Figure 6-4	Offset-Printed Conductive Ink Pattern	29
Figure 4-6	Alignment to Visual/Sensitive Chip Structure	13	Figure 7-1	Die-Size Ball Grid Array (BGA) Package Examples	30
Figure 4-7	Minimum Pitch From Solder Bump to Passivation Seal	13	Figure 7-2	Die-Size Ball Grid Array (DSBGA) Package Outline Showing a Fully Populated Terminal Array (Bottom View)	31
Figure 4-8	Comparing Perimeter and Redistributed Terminal Sites	14	Figure 7-3	Ball Coplanarity	32
Figure 4-9	Redistribution of a Single Metal Layer Device	14	Figure 7-4	Terminal Depopulation From the Full Array ...	32
Figure 4-10	Passivation Cross-Section	14	Figure 7-5	Flip Chip Fan-Out on Substrate	34
Figure 4-11	Suggested Distribution of Redundant Bump Terminals	15	Figure 7-6	Comparing Perimeter Wire Bond Pad Layout Variations	35
Figure 4-12	Array Design Anticipating the Potential for Die Shrink	15	Figure 7-7	Comparing Wafer-Level Terminal Formation Methodologies	35
Figure 4-13	Signal and Power Distribution Positions	15	Figure 7-8	Molded Fan-Out Wafer-Level Process (FOWLP) Sequence	36
Figure 4-14	Nested I/O Terminals	16	Figure 7-9	Uniform Terminal Array Is a Result of Surface Redistribution	36
Figure 4-15	Typical Bump Passivation Reticle Mask Format for Peripheral and Array Terminal Variations	16	Figure 7-10	Fully Populated Array Matrix With Corner 'A1' Mark on the Outer Surface of the Die (Top View Left, Bottom View Right)	37
Figure 4-16	Product Unit Cell Plan	16	Figure 7-11	Comparing Passivation Patterns	39
Figure 4-17	Comparing Solder Ball Collapse After Reflow	17	Figure 7-12	Redistribution of Perimeter Bond Pads Into a Raised-Array Terminal Pattern	40
Figure 4-18	Land Pattern Planning for Flip Chip Attachment on a Ceramic-Based Substrate	17	Figure 7-13	Wafer-Level Ball Grid Array (WLBGA) Design Layout Guideline for a Staggered-Array Pattern	40
Figure 4-19	Mass Reflow Solder Bumping of the Die While in a Wafer Format	17	Figure 7-14	Terminal Array Accommodating Die Shrink ...	41
Figure 4-20	Au Stud-Bump Terminal Comparing a Wire Break-Off to a More Uniform Cut-Wire Profile	18	Figure 7-15	Underfill Material Applied to Mechanically Stabilize the Flip-Chip-Mounted Die	42
Figure 4-21	Surface Redistribution Layer of the Bond Sites to a Uniform Electroplated-Au Bump Terminal Array	19	Figure 7-16	Encapsulation Material Dispensing	43
Figure 4-22	Solder-Capped Cu Post or Pillar Terminal	20	Figure 7-17	JEDEC Standard Carrier Tray Designed for Array-Packaged Devices	43
Figure 5-1	Wafer-Level Testing Identifies Die Elements That Do Not Meet Established Functional Criteria	21	Figure 7-18	Tray Carrier With Smaller Partitions	44
Figure 5-2	Groove-Cutting and Wafer-Thinning Process Flow for Low-Stress Die Singulation	23	Figure 8-1	Sequential Build-Up Substrate Structure	45
Figure 5-3	Scribe and Break Singulation	23	Figure 8-2	Flip-Chip and SMT Mounted Onto a Rigid-Flex Substrate	48
Figure 5-4	Scribe and Break Singulation Aspect Ratio Consideration	23	Figure 8-3	Ceramic-Based Substrates	49
Figure 5-5	Thin Wafer	24	Figure 8-4	Flip Chip and SMT on a Ceramic-Based Substrate	49
Figure 5-6	Example Street Formed in Wafer Using the Deep Reactive-Ion Etching (DRIE) Process ..	24	Figure 8-5	Three-Layer, Low-Temperature Cofired Ceramic Substrate	50
Figure 5-7	Basic Die Singulation Process Using Deep Reactive-Ion Etching (DRIE) Ablation Process	24	Figure 9-1	Automated Placement System	51
			Figure 9-2	Flip Chip Attachment Process Using Flux Dipping of Terminals	52
			Figure 9-3	Laser-Cut Stencil Aperture	54
			Figure 9-4	Pb-Free Solder Process Profile	54

Figure 9-5	Reflow Solder of Flip Chip Die With Discrete SMT Devices	55
Figure 9-6	Comparison of SnPb and SAC Ball-to-Package Interface	55
Figure 9-7	Direct Die Attachment Using Solid-Au Bump	56
Figure 9-8	Comparison of Flip Chip Reflow Solder Attachment and Anisotropic Adhesive Joining Process	57
Figure 9-9	System for Evaluating Perimeter Terminal Site Interface	58
Figure 9-10	Edge-Dispensed Underfill	59
Figure 9-11	Component Spacing for Tool Access	60
Figure 9-12	Hot-Air Process for Device Removal	60
Figure 10-1	Cross-Section of Crack Formation Due To Coefficient of Thermal Expansion (CTE) Mismatch	64
Figure 10-2	Effects of Accumulating Fatigue Damage in Solder Joint Structures	67

Tables

Table 3-1	Comparative Table of Various Technologies for a 100 Lead 10x10 mm Die	5
Table 4-1	Final Metal Signal Trace (30 μ m) Resistances (Example)	9
Table 4-2	Final Metal Power Trace (60 μ m) Resistances (Example)	9
Table 4-3	Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip)	11
Table 4-4	Terminal Via and Final Metal Via Pitch	13
Table 4-5	Contact Pitch, Ball Size to Land Pattern Approximation (μ m)	17
Table 5-1	Bare Die Testing Levels	20
Table 7-1	JEDEC Standard Terminal Pitch (e) and Terminal Diameter (b) Variations for Die-Size Ball Grid Array (DSBGA) (mm)	31
Table 7-2	Maximum Permitted Matrix Sizes (mm) for Recommended Body Sizes for WLBGA Packages	38
Table 7-3	Comparing Wafer-Level Ball Grid Array (WLBGA) Terminal Pitch to Ball or Bump Terminal Diameter Range	38
Table 7-4	Nominal Ball or Bump Diameter and Minimum Land Diameter for Wafer-Level Ball Grid Array (WLBGA)	39
Table 8-1	Ball and Land Pattern Size Comparison	44
Table 8-2	Substrate Design Feature Characteristics	45
Table 8-3	IPC-4101 RoHS-Compliant Substrate Materials	47
Table 8-4	Physical Attributes of Nonreinforced Polyimide Films	48
Table 8-5	Thin-Film Circuit on Ceramic-Based Substrates	50
Table 9-1	Solder Alloy Examples	53
Table 10-1	Product Categories and Use Environments	62
Table 10-2	Coefficient of Thermal Expansion (CTE) for Typical Materials	64
Table 10-3	Typical Heights (Joined)	64

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Design and Assembly Process Implementation for Flip Chip and Die Size Components

1 SCOPE

This document describes the design and assembly challenges for implementing flip chip technology in a direct chip attach (DCA) assembly. The effect of bare-die or die-size components in a flip chip format has an impact on component characteristics and dictates the appropriate assembly methodology. This standard focuses on design, assembly methodology, critical inspection, repair and reliability issues associated with flip chip and die-size package technologies, including wafer-level ball grid array (WLBGA).

1.1 Target Audience and Intent The target audiences for this document are managers, design and process engineers as well as operators and technicians who deal with electronic assembly, inspection and repair processes. The intent is to provide useful and practical information to those who mount bare-die or die-size components in a DCA assembly or those who are considering flip chip process implementation.

1.2 Definition of Requirements The imperative form of action verbs is used throughout this document to identify acceptance requirements that may require compliance, depending on the Performance Classification of the hardware (see 1.3). To assist the User, these action verbs are in bold text.

- a) The words “**shall/shall not**” are used whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** or **shall not** requirement for a Performance Class may be considered if sufficient technical rationale/objective evidence is supplied to the User to justify the exception.
- b) The word “**should**” is used whenever a requirement is intended to express a provision that is nonmandatory and which reflects general industry practice and/or procedure.

1.3 Classification of Product The following is a general explanation of the three classes of hardware, (see J-STD-001 for details concerning the specific requirements for each of these classes).

IPC CLASS 1, General Electronic Products – Includes products suitable for applications in which the major requirement is function of the completed assembly.

IPC CLASS 2, Dedicated Service Electronic Products – Includes products for which continued performance and extended life is required and for which uninterrupted service is desired, but not critical. Typically, the end-use environment would not cause failures.

IPC CLASS 3, High-Performance Electronic Products – Includes products for which continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Each of these three classes most likely will have different reliability requirements as dictated by the end user and the intended use environment.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-A-610 Acceptability of Electronic Assemblies

1. www.ipc.org

IPC-TM-650 Test Methods Manual²

- 2.3.38 Surface Organic Contaminant Detection Test
- 2.3.39 Surface Organic Contaminant Identification Test (Infrared Analytical Method)
- 2.4.42.2 Die Shear Strength
- 2.6.7.2 Thermal Shock, Continuity and Microsection, Printed Board
- 2.6.9 Vibration, Rigid Printed Wiring

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments**IPC-HM-860** Specification for Multilayer Hybrid Circuits**IPC-1782** Standard for Manufacturing and Supply Chain Traceability of Electronic Products**IPC-2222** Sectional Design Standard for Rigid Organic Printed Boards**IPC-2223** Sectional Design Standard for Flexible Printed Boards**IPC-2224** Sectional Standard for Design of PWBs for PC Cards**IPC-2225** Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies**IPC-2226** Sectional Design Standard for High Density Interconnect (HDI) Boards**IPC-3406** Guidelines for Electrically Conductive Surface Mount Adhesives**IPC-4101** Specification for Base. Materials for Rigid and Multilayer Printed Boards**IPC-4552** Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Circuit Boards**IPC-4562** Metal Foil for Printed Board Applications**IPC-6013** Qualification and Performance Specification for Flexible Printed Boards**IPC-6015** Qualification and Performance Specification for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures**IPC-7091** Design and Assembly Process Implementation of 3D Components**IPC-7525** Stencil Design Guidelines**IPC-7711/21** Rework, Modification and Repair of Electronic Assemblies**IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments**2.2 Joint Industry Standards³****J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies**J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires**J-STD-003** Solderability Tests for Printed Boards**J-STD-004** Requirements for Soldering Fluxes**J-STD-005** Requirements for Soldering Pastes**J-STD-028** Performance Standard for Construction of Flip Chip and Chip Scale Bumps

2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/test-methods.aspx)

3. www.ipc.org

J-STD-030 Guideline for Selection and Application of Underfill Material for Flip Chip and Other Micropackages

J-STD-032 Performance Standard for Ball Grid Array Balls

J-STD-033 Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

J-STD-046 Customer Notification Standard for Product/Process Changes by Electronic Product Suppliers

2.3 JEDEC⁴

JEP95, Section 4.7 Die-Size Ball Grid Array Packages (DSBGA)

JEP95, Section 4.9 Generic Matrix Tray for Handling and Shipping (Low Stacking Profile for BGA Packages)

JEP95, Section 4.17 Ball Grid Array(BGA) Package Measuring and Methodology

JEP95, Section 4.18 Wafer Level Ball Grid Arrays (WLBGA)

JESD21 JEDEC Configurations for Solid State Memories

4. www.jedec.org

3 REQUIREMENTS AND TECHNOLOGY OVERVIEW

3.1 Terms and Definitions Refer to Appendix A for a glossary of terms applicable to this standard, as well as to IPC-T-50 for additional terms and definitions.

3.1.1 Acronyms and Abbreviations Refer to Appendix B for quick reference to acronyms and abbreviated periodic table elements used in this standard.

3.2 History of Flip Chip Mounting The flip chip process was established for applications requiring aggressive miniaturization. The process describes bond sites prepared with a compatible metallurgy and a bare semiconductor die face down and bonded directly to a substrate. Electrical interconnection from chip to substrate is most commonly achieved with alloy bumps provided on the wire-bond sites.

The bump alloy on the die is generally compatible with conventional reflow soldering processes. Flip chip is best suited for relatively low input/output (I/O) die; however, redistribution of peripheral-located wire-bond sites to a uniform area array format will enable the use of higher I/O die. Die-size packaging was developed later to provide a more uniform interface terminal configuration, more efficient testability and ease of handling in an assembly environment.

Flip chip solder bump interconnection technology is more than 45 years old. It was first conceived and developed by IBM for the Solid Logic Technology hybrid electronic circuitry in its System 360 computers. At that time, standard transistor packaging used hermetically sealed metal cans with glass-sealed wires emerging from a header upon which the Ge or Si chip was metallurgically back-bonded. Manual thermocompression wire bonding to the chip was the common technique. Although transistor technology was much more reliable than the vacuum tube technology that preceded it, the packaging and interconnection technologies were weak. Faulty manual wire bonds, AuAl intermetallic formation (purple plague) and Al corrosion of thin-film interconnections on the chip had significant reliability concerns, even in hermetic packages.

The first metallization layer (typically Cr) was used to create a good bond to the Al pad prepared for wire bond. Subsequent metal films, typically Cu and Au, were deposited to provide solderability for mounting the small ball terminals. Originally, the ball was an alloy of AuSn eutectic which melted at 360 °C; therefore, the pad was called ball-limiting metallurgy because the melted ball would not wet the glass beyond the area of the pad. The AuSn ball terminal was eventually replaced by a NiAu-plated solid Cu ball which was attached with a SnPb alloy to maintain a more uniform stand-off, which is shown in Figure 3-1.

The substrate developed to mount these bumped-die components required thick-film electrodes or wires be screened and fired onto alumina substrates. Originally, the thick film was glass-fritted AuPt paste; later, it became AgPd. The wiring pattern is hot-dip tinned with SnPb90 solder to improve conductance and to enable reflow solder interconnect of both active and passive components.

After each terminal site is fluxed, the bumped chip and other passive devices are placed face-down onto the solder-coated electrodes. Subsequently, the substrate is heated in a furnace to heat the solder to a liquidus state, thereby reflow soldering the device bump and joining the chip to the substrate.

A similar flip chip attachment solution was developed by Delco Electronics (General Motors). The only difference was that Delco coated the Cu ball contacts with a Ag alloy composition. The attachment was completed using a solder paste screen-printed onto the substrate and then reflow soldered. The Cu core bump maintained a uniform standoff height when attached to the substrate, as shown in Figure 3-2.

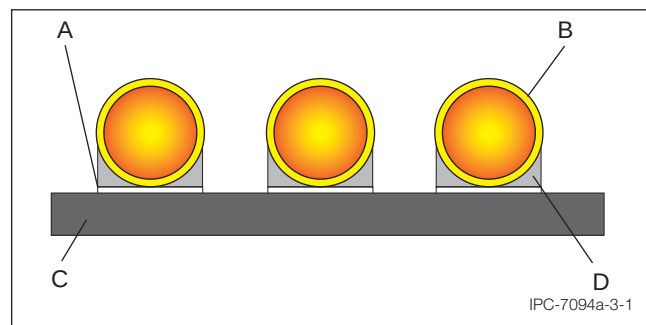


Figure 3-1 Solid Copper Core Ball Contact

- A – CrCuAu plated onto the AlSi pad
- B – NiAu plated on solid-Cu sphere
- C – Glass-passivated Si base
- D – Pb90Sn10 solder ball-to-die interface

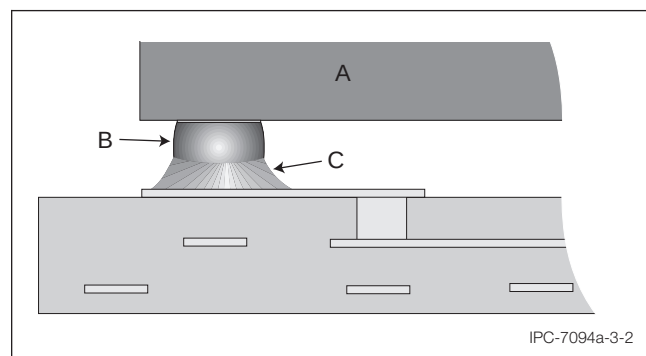


Figure 3-2 Flip Chip With a Ag-Coated Cu Core Terminal to Maintain Uniform Stand-Off Height

- A – IC device
- B – Ag bump
- C – Solder joint

3.2.1 Advantages of Flip Chip Mounting Because no intermediate packaging or leadframe are required, the die prepared for flip chip applications can enable increased circuit density and may contribute to improved high-frequency performance. As new generations of electronic products emerge, they often surpass the capability of existing packaging and interconnection technology and the infrastructure to support newer technology. This movement is occurring at all levels:

- IC
- IC package
- Module
- Hybrid
- PEB
- Connector
- Cable, which ties all the systems together

Interconnection density and methodology becomes the measure for successfully managing performance. The gap between printed boards and semiconductor technology (wafer-level integration) is greater than one order of magnitude in interconnection density capability, although the development of fine-pitch substrates and assembly technology has somewhat narrowed the gap. To ensure a satisfactory electrical interface, the die (typical of that shown in Figure 3-3) must be precisely aligned over the corresponding lands provided on the substrate.

All viable efforts are being used in filling this void utilizing uncased integrated circuits (flip chip) and incorporating more than one die or more than one part in the assembly process.

3.3 History of Die Size and Chip Scale Array Packaging

There have been many applications of flip chip technology; however, when handling and testing the uncased die, they are prone to cracking and surface damage. An alternative approach to bare-chip mounting is a package technology that maintains the small outline of the die but provides physical protection as well as a method for increasing both terminal size and pitch typical of that shown in Figure 3-4.

Table 3-1 provides a comparison of commonly used technologies.

Table 3-1 Comparative Table of Various Technologies for a 100 Lead 10x10 mm Die

Package Parameter	Bare Die (with wire bonds and pads)	Flip Chip	QFP	DSBGA	FBGA
Contact pitch	0.15 mm	0.25	0.30 mm	0.50 mm	0.50 mm
Footprint area	125 mm ²	120 mm ²	750 mm ²	150 mm ²	150 mm ²
Pkg/chip area	1.0 mm ²	1.0 mm ²	6.3 mm ²	≤ 1.1 mm ²	≥ 1.2 mm ²
Height	0.4 to 0.6 mm	0.5 to 0.7 mm	1.4 mm	≤ 1.0 mm	≥ 1.2 mm
Inductance nH (circuit length)	1-2 (0.75 mm wire)	0.1-0.2 (0.5 mm bump)	1-7 (3 mm lead)	0.5-2.1 (1 mm ball)	0.1-0.2 (1.2 mm ball)
Capacitance pF	0.2	0.03	0.5-1.0	0.05-0.2	0.05-0.3
PCB attachment	Epoxy + wire bond	Solder + underfill	Solder	Solder	Solder

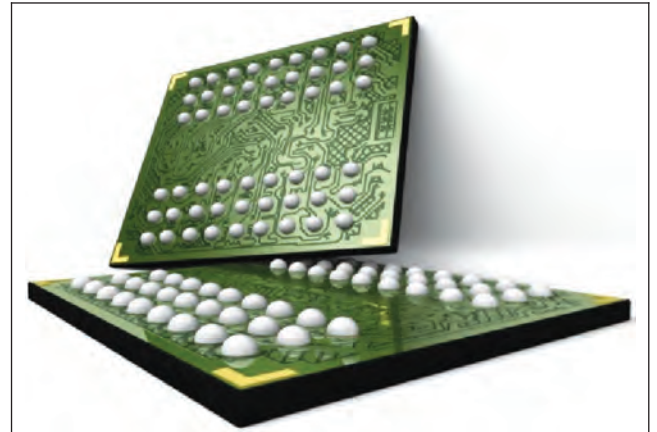


Figure 3-3 Solder-Bumped Wafer-Level Ball Grid Array (WLBGA)

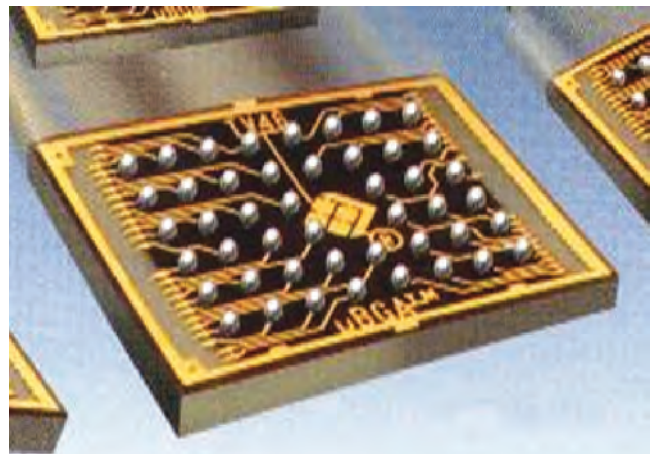


Figure 3-4 Array-Configured Die-Size Ball Grid Array (BGA)

Chip scale packages (CSPs) are often the same size or close to the same size as the die and are similar in appearance to the larger ball grid array (BGA) packages. Die-size BGA (DSBGA) and chip scale array packages are produced using widely differing constructions. The example shown in Figure 3-5 is an application that attaches a solder-bumped flip chip die element to an organic substrate (e.g., laminate, Si, glass, diamond, etc.). It contains an interconnection method designed to fan-out the bonding sites on the chip to a wider solder ball array pattern for printed board mounting.

Chip-to-substrate interconnection methods may include wire bonds, solder-capped Cu posts or solder bumps. Figure 3-6 illustrates a basic structure for a face-up wire-bond chip scale BGA format in which the package outline is slightly larger than the die. This is done to accommodate wire-bond interface between the die and substrate structure.

The package substrate has solder ball or bump terminals on its bottom surface for attachment to the printed board. Generally referred to as CSP or fine-pitch BGA (FBGA), the package assembly methodologies are often marketed under various trade names (see 3.3.2). The interface terminal pitch on all CSP devices can range from 0.3 mm to 0.8 mm.

3.3.1 Film-Based Package Substrate When developing a film-based substrate, package designers must first establish the die termination methodology. When the die is mounted with the active surface facing up (see Figure 3-6), the base material must accommodate wire-bond lands beyond the die outline. If the die is mounted on the substrate in the face-down orientation, several options are available. The die element can be furnished with preformed solder balls, solder bumps or solder-capped Cu posts at each terminal site. See Section 4 for details on alternate termination variations. Face-down die can also utilize wire-bond terminations. To accommodate wire-bond processing, an opening (window) is provided in the substrate to provide access to the wire-bond sites on the die surface (see Figure 3-7).

Figure 3-7 shows a single-metal conductor layer on a polyimide film base; however, the substrate can also be fabricated using thin reinforced glass/epoxy materials. The organic base material can be furnished more economically with two metal layers, which provide more efficient power and/or ground distribution and the ability to facilitate controlled impedance designs for enhanced performance. See Section 6 for information on substrate material variations.

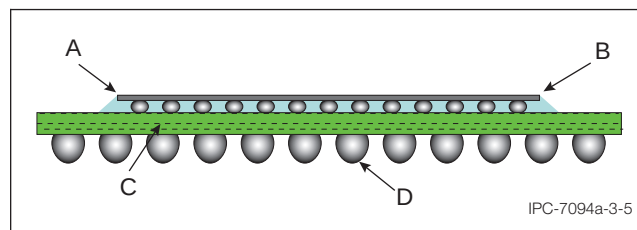


Figure 3-5 Face-Down Mounted Die (Flip Chip) on Organic Substrate

- A – Flip chip die element
- B – Polymer underfill
- C – Substrate
- D – Substrate-to-printed board solder ball contacts

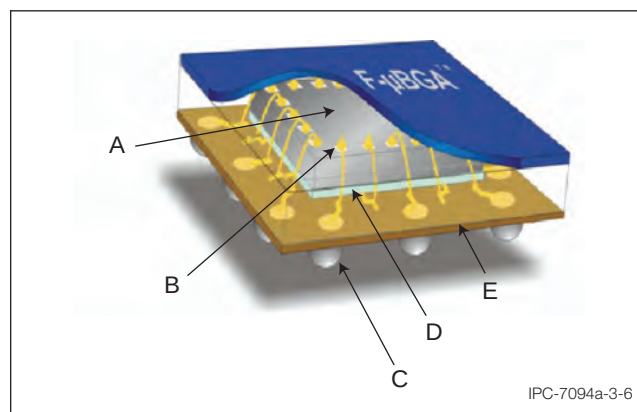


Figure 3-6 Face-Up Wire-Bond Chip Scale Package (CSP)

- A – Die element
- B – Au wire bond for die-to-substrate interface
- C – Solder ball contacts
- D – Die attach pad
- E – Package substrate

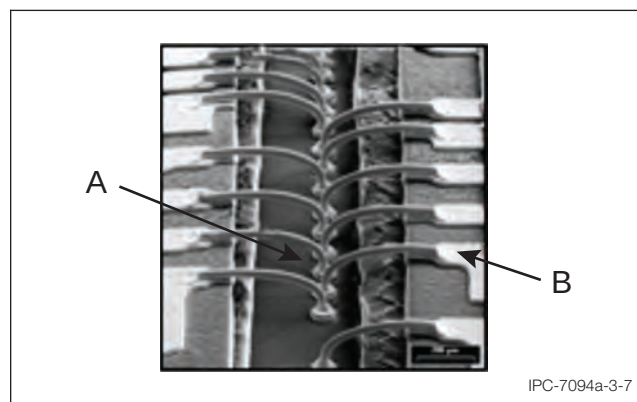


Figure 3-7 Narrow Opening in a Substrate Provides Access for Through-Window Wire-Bond Process
(Figure source: Invensas)

- A – Conventional ball bond on die land
- B – Wedge bond on bottom surface of substrate

3.3.2 Commercial Package Variations While flip-chip-configured semiconductors are classified as uncased die, several package assembly services have developed and/or adopted commercial package assembly innovations that maintain an outline that is not greater than the die outline (see Figure 3-8). The finished outline of the package, however, may be more defined by the number of terminals and the pitch required for die-to-board interface.

Another factor is the impact of die shrink. With each generation of a semiconductor products, developers will attempt to improve yield by reducing (shrinking) the die outline, thereby maximizing the number of die on the wafer. To maintain physical compatibility from one generation to another, the substrate outline and arrangement will remain constant.

The package-to-printed board interconnect for the examples in Figure 3-8 typically utilize Restriction of Hazardous Substances (RoHS)-compliant solder balls or bump terminals spaced at increments recommended in JEDEC Publication 95 for FBGA and DSBGA package families (see Section 7).

3.3.3 Redistribution The process for providing redistribution of wire-bond sites to a more uniform array format is performed while the die elements remain in the wafer format. The semiconductor's surface is insulated from the wiring pattern and conductor paths through a sequence of coating and plating processes. The finished conductor patterns ultimately connect to bump or ball terminals (see Figure 3-9).

Because conductor patterns can adjust the internal/external pad locations, this package does not impose any additional restrictions on semiconductor designers. The peripheral to area array redistribution allows the standard semiconductor developed for wire-bond processing to adapt to a uniform array pattern. In addition to the Cu conductor process detailed in the preceding, companies can provide thin-film conductor layers. Using a transfer process either at the wafer or bare-die level, multiple layers can be added to the semiconductor surface. Redistribution to a wider terminal-array pattern allows yield testing of the completed thin film add-on prior to transfer, and it minimizes IC exposure to processing. The solder bump terminals are simultaneously electroformed to make electrical connection from the IC chip pad to the redistribution lines and to produce the area array at the surface. The chip pad formation method is the photolithographic process made by thin-film patterning, dielectric etch and metal deposition.

As few as one and as many as four redistribution layers may be built-up on the wafer surface. Voltage layers can be isolated to provide low-inductance power supply and impedance control of the interconnect line from the point of the output of the chip driver to the substrate and into the receivers. An elastomeric mechanical buffer layer at the semiconductor-die-to-conductor interface enables reliability from thermal-cycle-induced solder connection fatigue failure due to chip and substrate CTE mismatch.

There are many proprietary techniques for packaging die. Some CSP assembly processes are broadly licensed and available from a wide number of semiconductor and assembly service providers, while others remain under the control of a single supplier. When selecting a chip-size package or a CSP methodology, users are encouraged to review reliability data to ensure the package technology meets environmental and performance criteria.

3.3.4 Advantages of Die-Size Package and Chip Scale Package (CSP) Technology It is important to compare many characteristics of flip chip and die-size package technology to select the most appropriate package technology. Some of the advantages of die-size packages and CSPs include:

- Can be the same size or very close to the size of uncased die element
- Furnish a uniform terminal array pattern for circuit routing efficiency
- Packaging bare die enables easier handling, testing and assembly

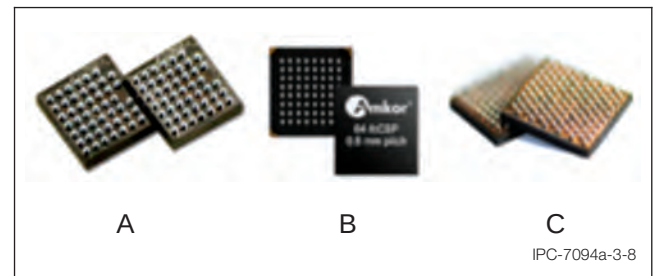


Figure 3-8 Commercial Flip-Chip and Wafer-Level Semiconductor Package Innovations

A – ASE Group WLCSP
B – Amkor Technologies fcCSP
C – STATS ChipPAC eWCSP

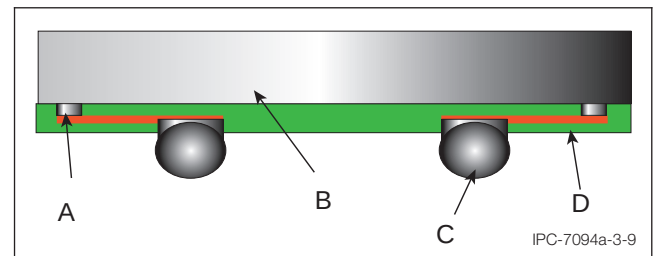


Figure 3-9 Wire-Bond Pad to Array Redistribution Provides Wider Spacing and Larger Terminal Features

A – Wire-bond pad
B – Semiconductor element
C – Ball or bump contact
D – Cu conductor

- Can be assembled onto printed boards using conventional surface mount technology (SMT) processes (although some package technologies may require underfill epoxy)
- Add minimal electrical and thermal parasitic
- Reliability data for several packages show results matching or exceeding leadframe packaged devices.

Section 4 provides additional detailed descriptions of these packaging technologies. See 3.2.1 for advantages of flip chips.

4 FLIP CHIP TECHNOLOGY

4.1 Electrical Design Considerations This section addresses electrical modeling, analysis considerations and design guidelines for chip bumping processes. It also describes substrates and packages for DCA, electrical models and combined noise analysis of a system.

Bumping technology offers significantly less inductance than wire-bond or ribbon-bond interconnects. Although die elements are primarily designed for wire-bond processing, they can be converted to bumped flip chip parts. To take full electrical advantage of the short coupling of the flip chip die, however, the chips should be initially designed for the bumping process. This allows optimization of internal chip wiring, circuit placement and optimized bump locations.

Whether using a common perimeter solder bump layout or designing a new array footprint, the designer must consider chip power, ground, signal and clock I/O to the interface criteria of the host package interposer or substrate structure. This is especially true when adapting the die- or package-level interposer to an existing host substrate. Also, the location and proximity of sensitive signals must be considered. Because bump pitch affects coupling noise, the designer must route the interface between die and interposer and/or substrate to ensure adequate isolation of sensitive signals.

4.1.1 Equivalent Circuitry The electrical path consists of wiring a via from the peripheral pad to the final metal redistribution trace, the final metal trace to the pad and the terminal via to the bump. The substrate metallization and associated wiring are part of the substrate electrical path. The bump electrical equivalent circuitry can be derived as shown in Figure 4-1 for first-order approximation.

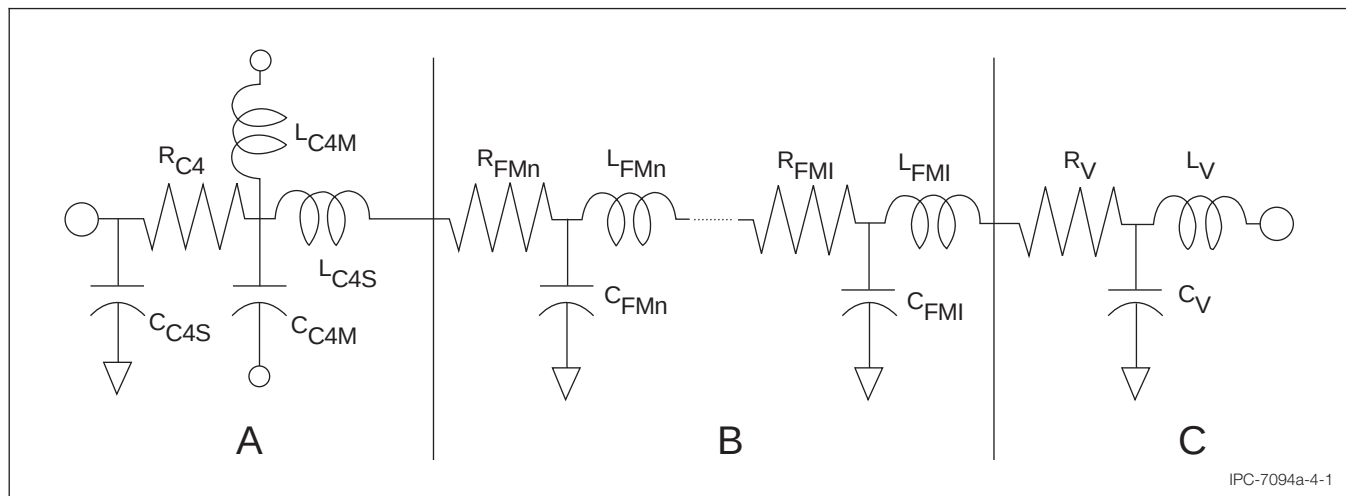


Figure 4-1 Bump Equivalent Circuit (Redistributed Chip)

A – C4 and terminal via
 B – Final metal trace and pad
 C – Wiring via

The wiring via and final metal (trace and pad) are modeled separately. The bump and the passivation opening are represented by equivalent lumped circuits, with both fringing and area capacitance accounted for in the circuits. It should be noted that the bump-to-chip and the final metal pad-to-chip area capacitances overlap. The designer needs to account for this coincidence in the model. One way to do this is to combine the effect of the two capacitors unless rise times become significantly short and/or chip traces become significantly long. Since the bump is relatively short compared to wire-bond or ribbon-bond interconnects, lumped element analysis can be used because distributed effects are minimal under most conditions.

For this example, the final metal is doped Al with the following parameters:

Surface resistivity (R_s)	= 0.037 Ω /square area (1- μm thick)
	= 0.028 Ω /square area (1.5- μm thick)
	= 0.018 Ω /square area (2- μm thick)
Signal Trace	= 30 μm
Power Trace	= 60 μm
Trace length	= 700 μm (minimum)
	= 3,350 μm (average)
	= 6,000 μm (maximum)
Trace thickness	= 1 μm , 1.5 μm and 2 μm

The largest final metal trace resistance (length = 6,000 μm ; width = 30 μm) can be calculated from Ohm's law.

$$R_{FM} = \frac{R_s \text{ Length}}{\text{Width}} = \frac{0.037 \Omega \cdot 6000 \mu\text{m}}{30 \mu\text{m}} = 7.4$$

Using the preceding value, Table 4-1 and Table 4-2 provide a quantitative view of how final metal resistance varies by thickness and length for signal and power traces.

Table 4-1 Final Metal Signal Trace (30 μm) Resistances (Example)

Final Metal Trace	Final Metal Signal Trace Resistance (Ω)		
	1 μm	1.5 μm	2 μm
700 μm	0.9	0.6	0.4
3350 μm	4.0	3.1	2.1
6000 μm	7.4	5.6	3.7

Table 4-2 Final Metal Power Trace (60 μm) Resistances (Example)

Final Metal Trace	Final Metal Signal Trace Resistance (Ω)		
	1 μm	1.5 μm	2 μm
700 μm	0.4	0.3	0.2
3350 μm	2.1	1.6	1.0
6000 μm	3.7	2.8	1.8

4.1.2 Final Metal Traces The final metal power, ground, clock and signal traces are a concern of any chip design, especially bump terminal redistribution design. Metal thickness has a major impact on final metal resistance (i.e., metal thickness is limited by the process capability for building-up conductor traces on the wafer surface). Typical elements shown in Figure 4-2 depict the physical solder bump electrical path for a peripheral pad chip redistributed for bumping technology and variations that can influence final metal resistance.

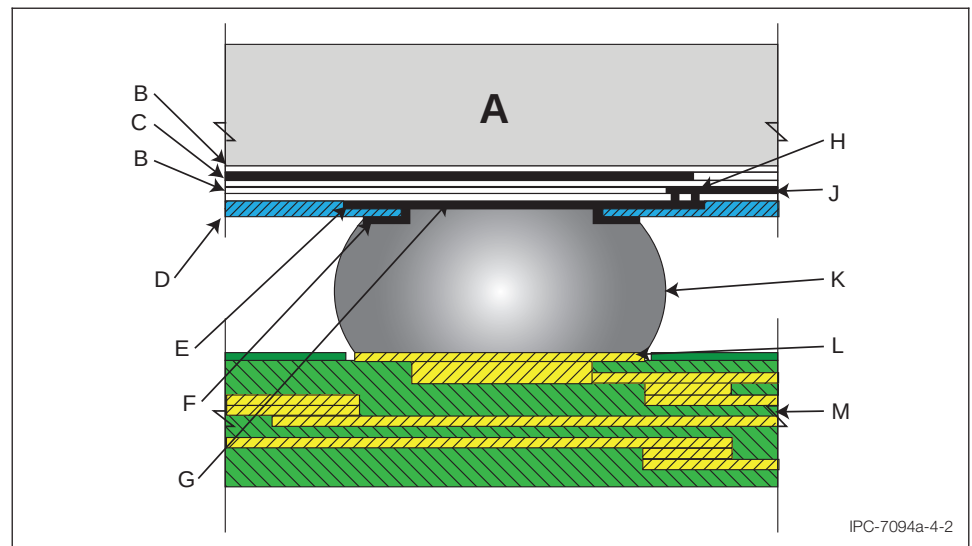


Figure 4-2 Solder Bump Electrical Path (Redistributed Chip)

A – Si	E – Final metal	J – Pad peripheral
B – Interlayer dielectric (ILD)	F – Metal pad limiting	K – Solder ball contact
C – Interlayer metallic (ILM)	G – Terminal via	L – Land pattern
D – Passivation	H – Interlayer wiring vias	M – Substrate

4.1.3 Inductance and Capacitance Calculation of final metal trace inductance and capacitance requires determination of self and mutual effects. These effects will be unique for each chip design. As shown in Figure 4-3, the orientation (parallel, orthogonal or between) of the final metal trace to underlying interlayer metal and ground planes will determine self and mutual capacitance.

Inductance is also influenced by orientation with respect to underlying metal and other final metal traces. Direction of current flow in these metal structures must be known so the designer can determine mutual inductance. To determine self-inductance, the appropriate current return path is needed.

Final metal trace capacitance consists of self and fringing capacitance. A first-order approximation of final metal total capacitance is shown below:

$$\text{Final metal trace capacitance} = (CA \times L \times W) + (CF \times L) \times 2$$

Where:

CA = Area capacitance (F/m²)

CF = Fringing capacitance (F/m)

L = Trace (m)

W = Trace (m)

For accurate modeling, coupling between final metal traces and underlying traces should be modeled using 2D/3D programs.

4.1.4 High-Frequency Performance Because the active surface of the die is face-down and near the active host substrate, the designer must define special consideration in trace routing on the chip, interposer and substrate. Changing signal levels on either the chip or the host substrate traces close to the chip are coupled. This coupling can create crosstalk, noises, electromagnetic fields (EMF), interference, etc., in the chip or substrate. Controlling the distance, the dielectric between chip and substrate traces and the characteristic impedance will help to reduce the effects of coupling.

4.2 Thermal Design The primary thermal path for uncased die is through the Si to the chip's backside surface. A percentage of thermal rise also will dissipate through the bump terminals. To this end, packaging methodology becomes the major component of thermal consideration and offers an added dimension of thermal management. Depending on the application, the designer has the option of selecting the thermal path.

The degree of consideration given to thermal design is dependent on three factors:

- Amount of energy or heat that must be dissipated
- Desired operating junction temperature of the chip
- Ambient temperature of the surrounding environment

Conduction, convection and radiation are the models for which heat can be dissipated. Conduction is the primary heat dissipation mode for bump interconnect. Convection is a small contributor, as illustrated in Figure 4-4; thermal and electrical analysis are analogous.

$$ER = L/(\sigma A)$$

$$TR = L/(kA)$$

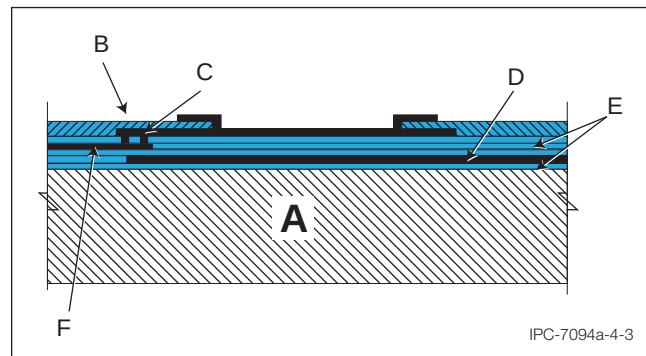


Figure 4-3 Final Metal Trace and Underlying Traces (Cross-Section)

A – Si
B – Passivation
C – Wiring via

D – ILM
E – ILD
F – Final metal

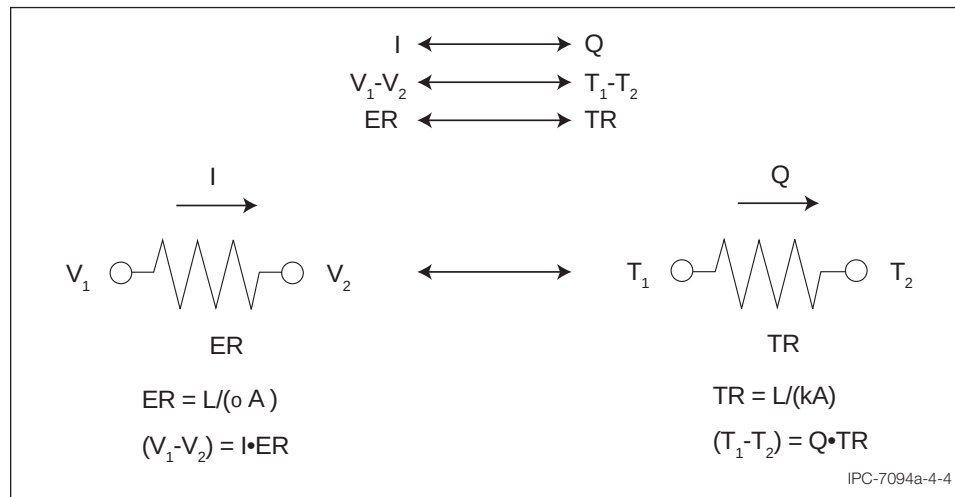


Figure 4-4 Thermal/Electrical Analogy

I – Current flow
 $V_1 - V_2$ – Voltage drop
 ER – Electrical resistance
 Q – Heat flow
 $T_1 - T_2$ – Temperature drop

TR – Thermal resistance
 σ – Electrical conductivity
 L – Conductor length
 A – Cross-sectional area of conductor
 k – Thermal conductivity

4.2.1 Bump Interconnect Thermal Model Bump thermal interconnects can be modeled as two cylinders between the chip power source and the substrate (see Figure 4-5). Cylinder 1 represents the innerlayer materials on the chip. Cylinder 2 represents the pad-limiting metals and bump size. The heat source is the device in the chip. Because there are several possible variations for bump terminal diameter, cylinder sizes vary accordingly.

Assuming cylinder 1 is SiO_2 ($k = 1.01 \text{ W/m K}$) and cylinder 2 is Sn3Pb97 solder ($k = 36 \text{ W/m K}$), the approximate interconnect thermal resistance can be calculated for each option (see Table 4-3).

It should be noted that cylinder 1 thermal resistance varies by the number and, specifically, the thickness (L) of inner layers on the chip, which is the main contributor to thermal resistance and should be modeled accurately. Furthermore, interface and bulk resistances have been combined to simplify calculations and illustrations. Bump terminal interconnect thermal resistance values for a typical single-, double- and triple-layer metal device are shown in Table 4-3. The reader is advised to consider these values are based on a 150- μm bump on Si where SiO_2 interlayer dielectric is modeled. Section 11 provides detailed information regarding physical and electrical modeling.

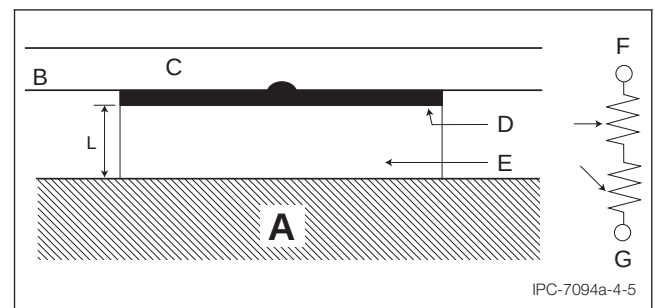


Figure 4-5 Bump Interconnect Equivalent Model

A – Substrate
 B – Si chip
 C – Heat source (junction)
 D – Cylinder 1
 E – Cylinder 2
 F – Heat source
 G – Substrate
 L – Thickness of inner layers (Table 4-3)

Table 4-3 Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip)

Interconnect Option	Diameter (m)	Cylinder I			Cylinder II			Total R (°C/W)
		L (m)	A(x ²) (nm ²)	R (°C/W)	L (m)	A(x ²) (nm ²)	R (°C/W)	
Option A	150	10	18	550	75	18	116	666
Option B	125	10	13	762	63	13	135	897
Option C	100	10	8	1238	50	8	174	1412
Option D (DCA)	150	10	18	550	≥ 75	18	≥ 116	≥ 666

4.3 Flip Chip Preparation for Mounting An IC prepared for flip chip mounting is basically a bare die with metallized terminals or bumped terminals ready for mounting. The terminal metallization is typically applied while the die elements remain in wafer form. There are numerous die attach techniques for joining the flip chip device to the substrate interconnections. These include reflow soldering, ultrasonic, thermocompression bonding and the use of anisotropically conductive and isotropically conductive polymer adhesives. Au-to-Au interface can be considered as well, using thermocompression and ultrasonic energy to complete the flip chip bonding process.

4.3.1 Design Guide Checklist Various design guidelines are applicable to the development of the basic die element, the uncased flip chip and the packaged die. The guidelines in some instances relate directly to wafer-level manufacturing conditions. In other instances, they apply to features required for mounting the component, terminal size, terminal pitch and array configurations. In any event, guidelines are furnished for very specific reasons. Designers should consider the following design guide checklist:

GUIDE 1 – Operating temperature must be considered when determining interconnect reliability. Devices requiring underfill may operate reliably at higher temperature than devices without underfill.

Reason: Solder creep at elevated temperatures is not well characterized. Applications will require evaluation and testing at operating temperature to determine expected interconnect reliability. There are five basic thermal and mechanical factors that affect solder bump fatigue:

- 1) Strain
- 2) Thermal activation
- 3) Thermal cycling frequency
- 4) Bump footprint
- 5) Chip underfill (once underfilled, underfill performance is key; not the solder)

GUIDE 2 – Solder and other alpha-emitting materials must be kept an appropriate distance from alpha-particle-sensitive chip circuitry. For example, a separation of 150 μm is required between Pb-rich bumps (e.g., SnPb97) and sensitive circuitry on polyimide-passivated devices.

Reason: Alpha particle emission rate of various materials may be too high for reliable operation of alpha-sensitive chip circuitry within close proximity. Measures such as thicker passivation on the die surface, modification of the alloy composition or metal shielding on the substrate can mitigate the effects of proximity.

GUIDE 3 – Redistribution designs must minimize the inductance and resistance to reduce sensitivity to electrostatic discharge (ESD).

Reason: Increased inductance and resistance of the redistribution line reduces the effectiveness of ESD circuits.

GUIDE 4 – Maximum current should be modeled for the interconnect system used.

Reason: Current density, therefore, reliability, varies with materials, construction, cross-sectional area, operating temperature, etc.

GUIDE 5 – Designs should conform to all applicable chip design and wafer fab specifications.

Reason: Design for manufacturability (DfM).

GUIDE 6 – The bump footprint should not be symmetrical with respect to the x or y axis unless other physical features are visible to define orientation.

Reason: To identify chip orientation for subsequent processing.

GUIDE 7 – At least two features are required on each edge of a chip positioned near the chip corners. Functional or non-functional bump terminals can be used to satisfy this requirement.

Reason: Needed for visual inspection and mechanical support of the chip required during joining to maintain parallelism to the substrate.

GUIDE 8 – It is recommended that bump terminal diameters on flip chip devices conform to the mandates of the chosen bump pitch to ensure reliable connection without risking shorting between bump terminals. Some desirable bump terminal sizes are 100 μm , 125 μm , 150 μm and 250 μm .

Reason: To conform with individual suppliers' processes and anticipated industry standards (e.g., JEDEC).

GUIDE 9 – A minimum number of bump terminals may be required for manufacturability and reliability.

Reason: To withstand dynamic and steady-state mechanical forces.

GUIDE 10 – In most applications, only one bump terminal diameter per chip/wafer should be used.

Reason: Varying bump diameter may impair chip attach. Although not recommended, specialized applications requiring multiple bump sizes per chip/wafer exist.

GUIDE 11 – The minimum bump pitch should be held at 250 μm when possible to facilitate the assembly of standardized substrates. (Multiple minimum pitches will cause confusion.)

Reason: Minimum terminal pitches prevent terminal-to-terminal, terminal-to-trace and trace-to-trace shorting and provide the distance needed to effectively clean joining flux (if applicable).

GUIDE 12 – Location of terminal bumps near areas requiring visual recognition will depend on final bump size, as illustrated in Figure 4-6.

Reason: This enables alignment tolerance so misaligned terminal bumps do not block or cover areas needed for visual or optical recognition.

GUIDE 13 – The minimum distance from the center of the passivation opening to the passivation seal at the edge of the chip is 50 % of the final bump terminal diameter, plus the maximum alignment tolerance, plus the desired minimum stand-off between bump terminals and chip seal (Figure 4-7).

Reason: Minimum pitch required for solder bump terminal alignment tolerance.

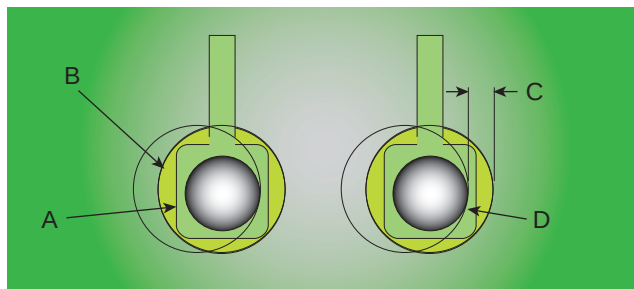


Figure 4-6 Alignment to Visual/Sensitive Chip Structure

A – Bond pad
B – Ball contact
C – Maximum alignment tolerance
D – Passivation opening

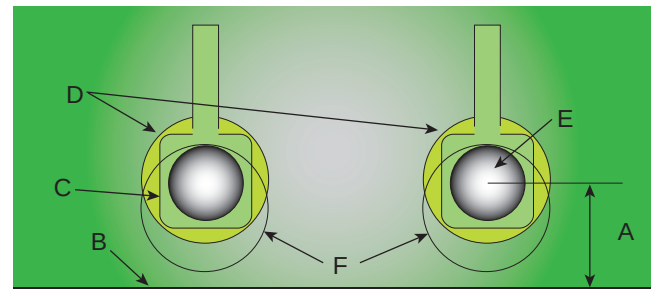


Figure 4-7 Minimum Pitch From Solder Bump to Passivation Seal

A – Terminal-to-edge die
B – Passivation seal
C – Bond pad
D – Aligned ball contacts
E – Passivation opening
F – Misaligned ball contacts

GUIDE 14 – Every bump terminal must be connected to a corresponding substrate metal pad.

Reason: Metallurgical attachment of every bump terminal to both chip and substrate is required for flip chip interconnect integrity.

GUIDE 15 – Vias under final metal wiring must be spaced away from the edges of the passivation opening. Examples of minimum spacing values used by IBM and Motorola are shown in Table 4-4.

Reason: Intersection of the edge of the passivation opening with the underlying via topography results in steep features that are difficult to cover with pad-limiting metallurgy (PLM) and may induce stress-related defects.

Table 4-4 Terminal Via and Final Metal Via Pitch

Description	Size	Tolerance
Passivation opening dimensions	50 μm	$\pm 1 \mu\text{m}$
Passivation opening (edge vs. stacked wiring)	2	Minimum
Passivation opening (edge vs. common wiring)	10	Minimum

GUIDE 16 – The edge of the PLM as patterned should not transect an underlying step feature (e.g., via edge). The importance of this guideline increases with increasing step height and slope.

Reason: Pad-limiting larger metal can cause stresses when positioned over irregular surfaces.

GUIDE 17 – Practical test cell bumps should be identical to bumps on product die.

Reason: This provides correlation between test cell bumps and active product bumps.

4.3.2 Final Metal Final metal is the top layer of metallization (typically Al) on a chip. It may be the first layer or the fourth, depending on the device complexity. The solder bump terminal connects downward through the final metal to the chip. All electrical paths, to and from the chip, travel through the final metal. Redistribution, illustrated in Figure 4-8, is the relocation of original terminal locations to preferred bump sites. This requires a new redistribution metal layer that becomes final metal, illustrated in Figure 4-9.

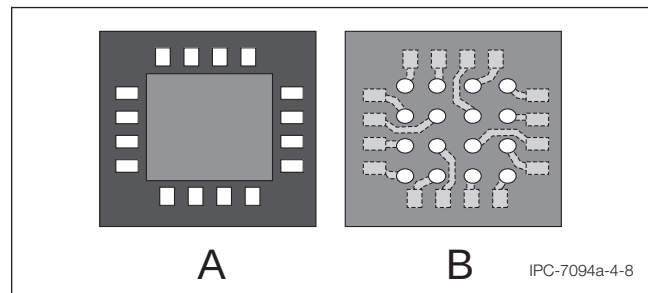


Figure 4-8 Comparing Perimeter and Redistributed Terminal Sites

A – Bare IC chip with peripheral bond pads

B – Chip I/O redistributed on die surface to array

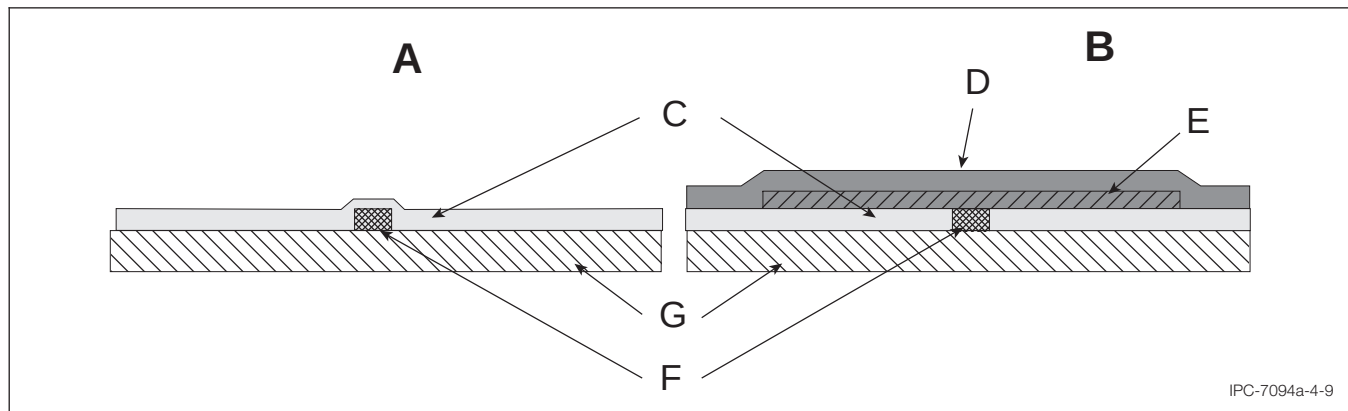


Figure 4-9 Redistribution of a Single Metal Layer Device

A – Original device

B – Redistributed device

C – Original chip passivation

D – Final chip passivation

E – Final metal

F – Metal 1

G – Si

4.3.3 Surface Passivation Passivation consists of a layer of protective films that coat the final metal and chip. These films can vary with semiconductor technology (e.g., complementary metal-oxide semiconductor (CMOS) bipolar CMOS, etc.) and with the wafer fabrication facility. These films are deposited and imaged with standard wafer processing techniques. There are many types of passivation in practice, some of which are Si nitride, Si oxynitride, spin-on-glass, polyimide and sputtered SiO_2 . It must be noted that sidewall profile is critical. Figure 4-10 shows an example of surface passivation.

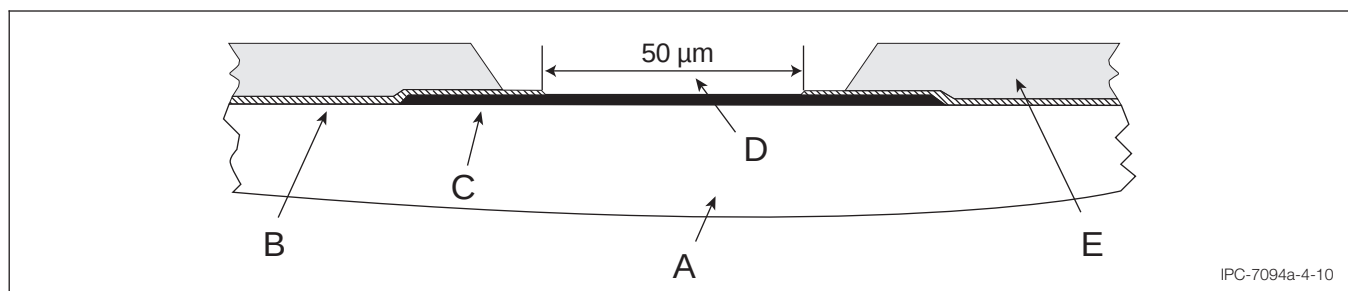


Figure 4-10 Passivation Cross-Section

A – Si

B – Chip passivation

C – Final metal pad

D – Passivation opening

E – Polyimide

Polyimide is recessed from the chip passivation because the same mask is used to pattern the chip and passivation layer, although different processing is used for each layer.

4.3.4 Footprint Population The number of bump terminals required varies with electrical, thermal and mechanical requirements. Besides electrical connections, additional bump terminals may be included for heat dissipation or mechanical support (e.g., outriggers, chip orientation or future design migration). Each application has its own unique characteristics. This makes it impossible to establish a general methodology for terminal population; however, there are various strategies that can be employed depending on the application.

See 4.3.4.1 through 4.3.4.4 for examples of terminal population design variations and suggested approaches for selecting them.

4.3.4.1 Redundant Bump Terminals Redundant bump terminals are often included for power and critical signals. The chip area will support a larger footprint, but the resulting distance to neutral point (DNP) may negatively impact reliability. In this approach, the outermost rows of terminal bumps join chips and endure the most stress. As the DNP increases, the stress in the outer rows increases. By placing redundant terminal bumps in the outer rows and critical bumps in the inner rows; chip functionality will not be compromised if any redundant bump terminals in the outer rows fail. The design should include enough redundant bump terminals to allow for potential loss. Figure 4-11 shows how this might be accomplished.

4.3.4.2 Die Shrink Consideration Recognizing that the uncased die will likely be subject to some level of refinement and area reduction (die shrink) by the manufacturer, it will be necessary to establish the terminal matrix well inside the anticipated die perimeter. With this factor in mind, the package designer should attempt to provide terminal spacing for the array pattern that can allow at least one generation of die shrink without affecting the user's next level of assembly. As the die shrinks, it may be necessary to adjust both terminal size and spacing. Specifically, when the bump or ball terminal count is high, it may not be possible to utilize the established array variations; however, the package engineer will need to consider the next level of interconnect technology.

To reduce the potential for large-scale redesign of the next-level substrate it is suggested that the array pattern locate the critical signal terminal bumps in the chip's interior. Use outer rows for redundant and mechanical bumps.

When shrink occurs, the outer less essential rows may be lost, but the critical bump terminals will not be affected. As the chip shrinks so does the DNP, making the loss of redundant and mechanical bumps less of an issue. This is illustrated in Figure 4-12. Several companies have developed and registered die-size array packages with a terminal pitch ≤ 0.40 mm. To achieve further reductions in terminal pitch, manufacturers will need to adapt even smaller terminal features for mounting.

4.3.4.3 Input/Output (I/O) Drivers on the Periphery Some chip designs require I/O drivers be located on the periphery with other circuits internal to the chip. In addition, redundant connections for power and signals may be desired. When positioning I/O drivers on the chip periphery, shorter interconnection lengths will help to minimize parasitic effects. Bump terminals should be located as close to the pertinent circuitry as possible. Figure 4-13

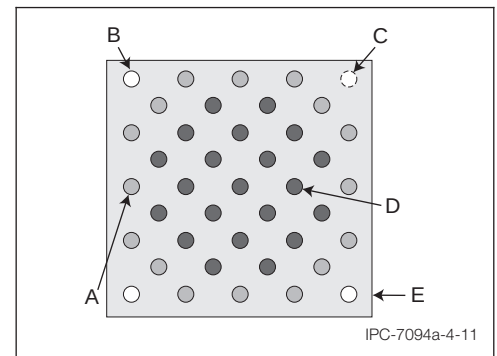


Figure 4-11 Suggested Distribution of Redundant Bump Terminals

- A – Redundant contacts
- B – Mechanical contacts
- C – Optional contact depopulation to define orientation
- D – Critical contacts
- E – Die outline

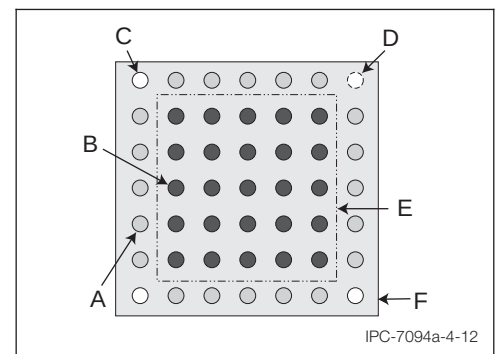


Figure 4-12 Array Design Anticipating the Potential for Die Shrink

- A – Redundant contacts
- B – Critical contacts
- C – Mechanical contacts
- D – Optional contact depopulation to define orientation
- E – Projected second-generation die shrink outline
- F – Die outline

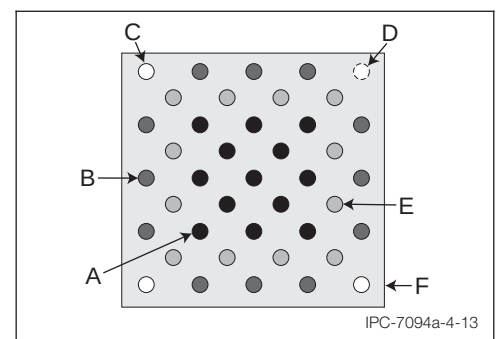


Figure 4-13 Signal and Power Distribution Positions

- A – Power and ground contacts
- B – Output contacts
- C – Mechanical contacts
- D – Optional contact depopulation to define orientation
- E – Input contacts
- F – Die outline

shows redundant power and ground bumps that are centrally located above the internal circuitry to minimize distribution lengths. Input bumps are placed near the input circuitry; output bumps are placed near the output drivers.

4.3.4.4 Isolating Sensitive Input/Output (I/O) In some chips, it is important to electrically isolate a sensitive I/O position from crosstalk or other noise. The approach to doing this is to surround the area with power and ground bumps as shown in Figure 4-14.

The designer should exercise caution when placing bump terminals of different electrical potentials in close proximity, because they could cause shorting problems with dense wafer probes. Bump pitch should be maximized to compensate for this potential hazard.

4.4 Design Output Requirements There is a minimum amount of information that should be provided to a designer for the designer to produce a bump terminal design, including:

- Final metal mask
- Passivation mask
- Unit cell plan

It should be noted that the mask requirements are wafer fabrication dependent. One should consult the supplying wafer fabrication group for specific information. In addition, each plan is typically a computer-aided design (CAD) file and may include specific drawings. The most prevalent format in use is GDSII, though others are possible.

4.4.1 Final Metal Reticle Mask This mask will conform to the wafer fabrication reticle or mask requirements.

4.4.2 Passivation (Terminal Via) Reticle Mask and Plan A suggested alignment target format is shown in Figure 4-15. In this example, the fiducial marks represent the chip passivation edges. A nonwetable metal appears everywhere except the terminal via sites. The as-drawn dimensions of the terminal vias are wafer fab dependent.

Positive photoresist is used with this type of reticle mask. Terminal via sizing may require compensation for etch bias depending on the wafer fab etching process. The designer should consult with the wafer fabricator to determine the specific design requirements. The bump passivation plan is a CAD file containing the terminal via location data needed for the bump mask design.

4.4.3 Unit Cell Design A drawing and/or CAD file is required for each type of unit cell plan (suitable surface composition analysis technique and test method) as illustrated in Figure 4-16. This information is needed for generating the wafer step plan and bump mask design.

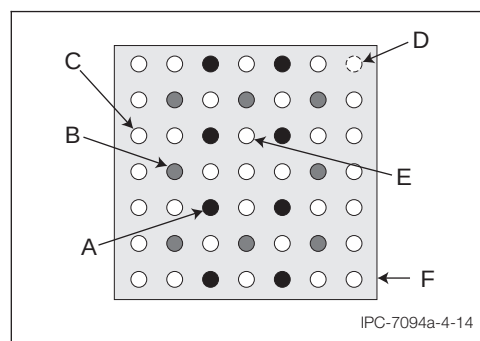


Figure 4-14 Nested I/O Terminals

- A – Ground contacts
 B – Power contacts
 C – I/O contacts
 D – Optional contact depopulation to define orientation
 E – Nested I/O contacts
 F – Die outline

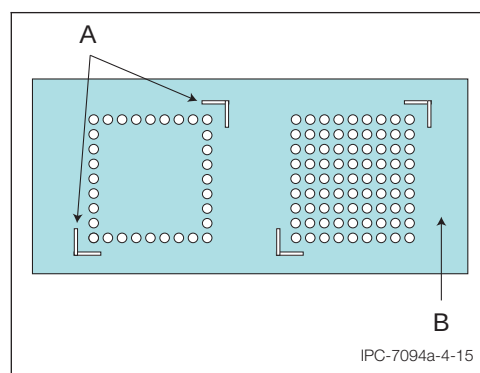


Figure 4-15 Typical Bump Passivation Reticle Mask Format for Peripheral and Array Terminal Variations

- A – Fiducial alignment targets
 B – Terminal site

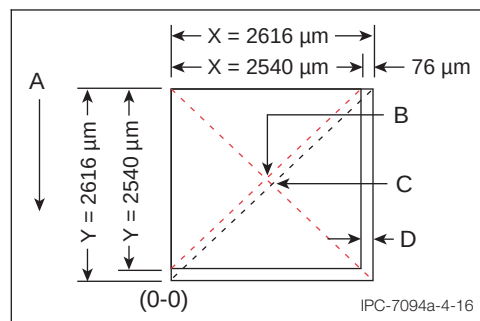


Figure 4-16 Product Unit Cell Plan

- A – Major flat
 B – Center of product cell
 C – Center of product unit cell
 D – Kerf scribe

4.5 Land Pattern Design The land pattern for flip chips and die-size array packages is simply a circle of coated Cu foil for which diameter is the same or slightly smaller than the bump or ball terminal diameter. Table 4-5 and Figure 4-17 compare variations of contact features and the typical effect of reflow soldering with eutectic or near-eutectic alloy (collapsible) solder ball contacts.

The surface coating on the conductor circuit land is typically one of the common solder-compatible alloy compositions or an organic solder protective coating.

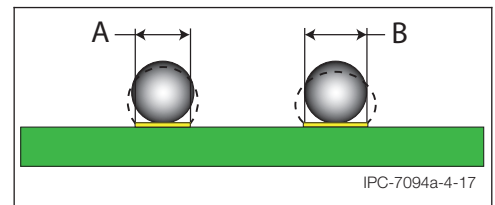


Figure 4-17 Comparing Solder Ball Collapse After Reflow

A – Slightly smaller land (preferred)
B – Same size land

Table 4-5 Contact Pitch, Ball Size to Land Pattern Approximation (μm)

Contact Pitch	Nominal Bump or Ball Diameter	Land Diameter Reduction	Nominal Land Size	Land Size Variation
500	300	20 %	250	200 to 250
400	250	20 %	200	170 to 200
300	200	20 %	150	120 to 150
250	150	10 %	125	100 to 125

4.5.1 Land Pattern for Ceramic Substrate Design For perimeter-type flip chip attachment, the land pattern may be defined by a basic solder mask opening over the conductive area. Figure 4-18 shows a top view of a ceramic-based substrate land pattern configuration.

4.5.2 Solder Bumping The most common bumping process begins with stencil printing solder paste on each terminal site while the die remains in the wafer-level form. The solder paste is a powdered alloy composition combined with a fluxing material that, when heated to a liquidus state, forms a semispherical bump terminal. The joining process occurs within the elevated temperature. The time needed to reach the liquidus of the solder alloy and the peak temperature and time above liquidus must be adjusted for the alloy composition of the terminal material and individual wafer mass and complexity.

4.5.3 Solder Paste Deposition Direct deposition of solder paste on each terminal site is an alternate method for creating solder bump terminals. The powdered alloy composition is combined with a fluxing material and then dispensed onto individual terminal sites while the die elements remain in the wafer format. Typical of the solder paste printing method described in 4.5.2, the composite material, when heated to liquidus, forms a semispherical bump profile typical of that detailed in Figure 4-19.

Mass reflow soldering in a production environment may utilize a simple surface conduction process, energy furnished by infrared (IR) or forced-air convection. The ramp rate from ambient to 125 °C is < 60 seconds; however, the actual duration of time in ramping the temperature to the level in which the alloy converts from a solid state to a liquid state may require several minutes.

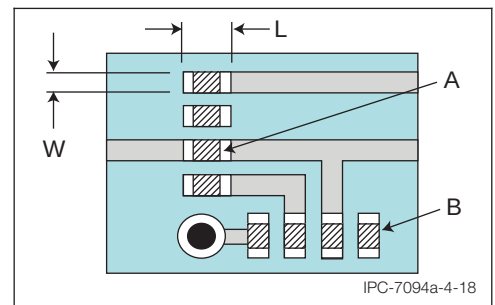


Figure 4-18 Land Pattern Planning for Flip Chip Attachment on a Ceramic-Based Substrate

A – Post outline
B – Land area
L – Two to three times post length (typically 300 μm)
W – Post width (typically 100 μm) Figure

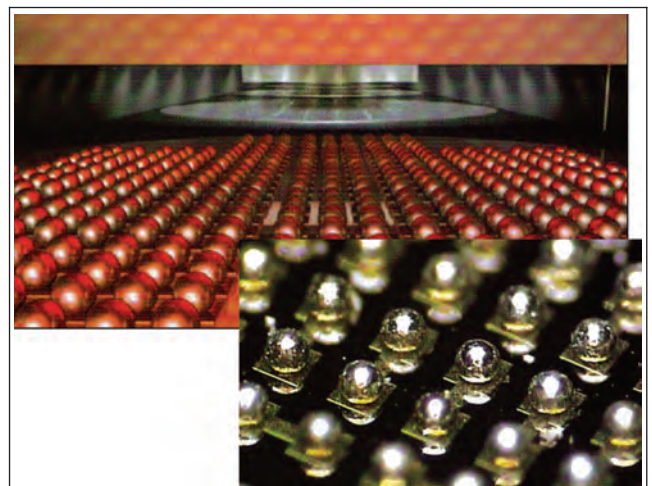


Figure 4-19 Mass Reflow Solder Bumping of the Die While in a Wafer Format

(Source: BTU)