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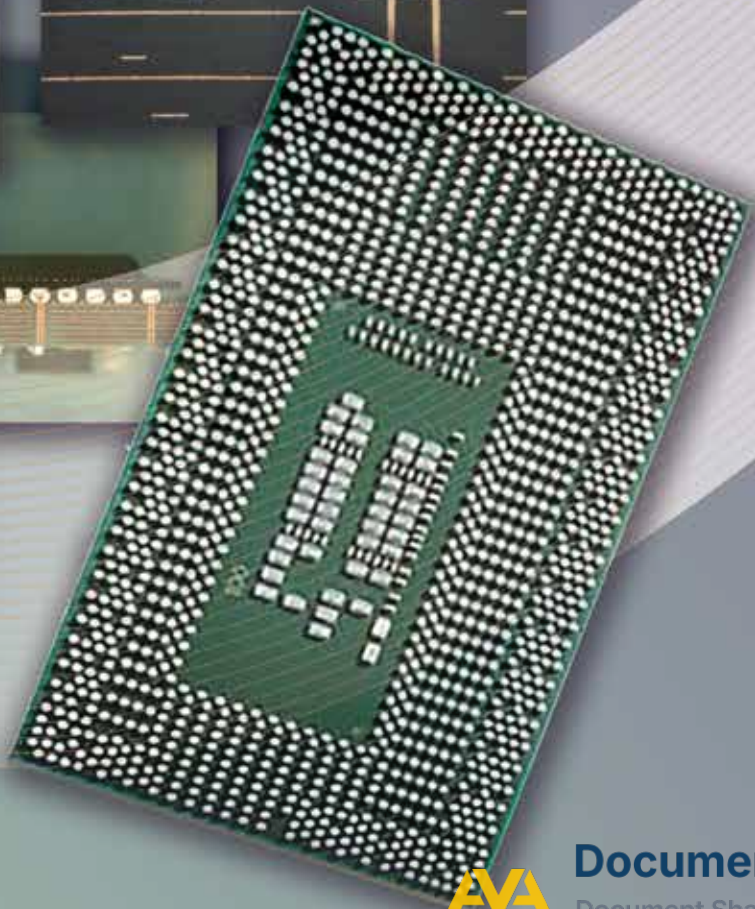
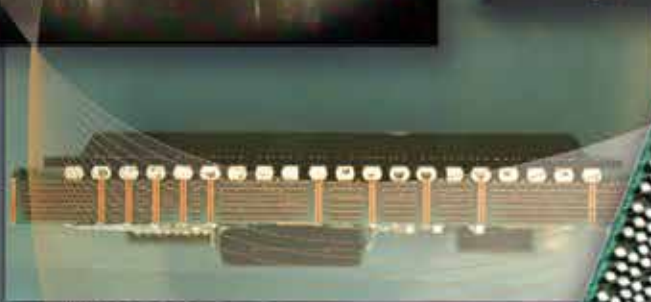
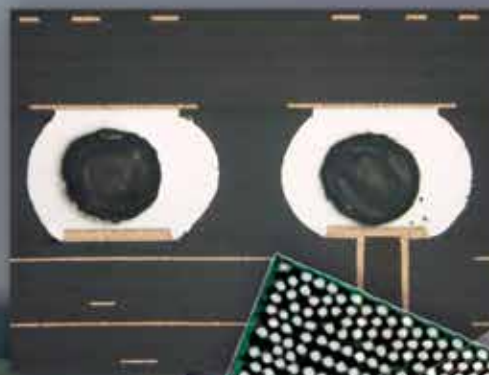
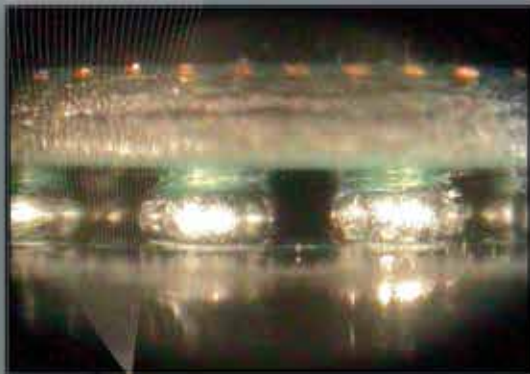
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Design and Assembly Process Implementation for Ball Grid Arrays (BGAs)

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IPC-7095D-WAM1

Design and Assembly Process Implementation for Ball Grid Arrays (BGAs)

Developed by the Ball Grid Array Task Group (5-21f) of the
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Users of this publication are encouraged to participate in the
development of future revisions.

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Design and Assembly Process Implementation for Ball Grid Arrays (BGAs)

1 SCOPE

This standard describes design and assembly implementation for ball grid array (BGA) and fine-pitch BGA (FBGA) technology, focusing on inspection, repair and reliability issues associated with design and assembly of printed boards using these packages.

1.1 Purpose The purpose of this standard is to provide useful and practical information to those who use or are considering using BGAs. The target audiences for this document are managers, designers and process engineers who are responsible for design, assembly, inspection and repair processes of printed boards and printed board assemblies.

1.1.1 Intent This document describes how to successfully implement robust design and assembly processes for printed board assemblies using BGAs as well as ways to troubleshoot some common anomalies which can occur during BGA assembly. For accept/reject criteria and requirements for BGA assemblies, see J-STD-001 and IPC-A-610.

1.1.2 Interpretation of “Shall” The imperative form of the verb “**shall**” is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a “**shall**” requirement may be considered if sufficient data are supplied to justify the exception. To assist the reader, the word “**shall**” is presented in bold characters.

The words “should” and “may” are used whenever it is necessary to express nonmandatory provisions. “Will” is used to express a declaration of purpose.

1.1.3 Presentation All dimensions and tolerances in this specification are expressed in hard SI (metric) units and bracketed soft imperial [inch] units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions < 1 mm [0.0394 in] will be expressed in micrometers and microinches.

1.1.4 Use of “Lead” For readability and translation, this document uses the word lead only to describe leads of a component (sometimes referred to as terminations).

1.1.5 Abbreviations and Acronyms Periodic table elements are abbreviated in this standard. See Appendix B for full spellings of abbreviations (including elements) and acronyms used in this standard.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-A-610 Acceptability of Electronic Assemblies

IPC-TM-650 Test Methods Manual²

2.4.42 Torsional Strength of Chip Adhesives

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-SM-817 General Requirements for Dielectric Surface Mounting Adhesives

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies

IPC-HDBK-830 Guidelines for Design, Selection and Application of Conformal Coatings

IPC-1401 Corporate Social Responsibility and Sustainability Protocols for Electronic Manufacturing Industry

IPC-1601 Printed Board Handling and Storage Guidelines

IPC-1751 Generic Requirements for Declaration Process Management

1. www.ipc.org

2. Current and revised IPC Test Methods are available on the IPC Web site (www.ipc.org/test-methods.aspx)

- IPC-1752** Materials Declaration Management
- IPC-2221** Generic Standard on Printed Board Design
- IPC-2222** Sectional Design Standard for Rigid Organic Printed Boards
- IPC-2226** Sectional Design Standard for High Density Interconnect (HDI) Boards
- IPC-4101** Specification for Base Materials for Rigid and Multilayer Printed Boards
- IPC-4552** Performance Specification for Electroless Nickel/Immersion Gold (ENIG) Plating for Printed Boards
- IPC-4553** Specification for Immersion Silver Plating for Printed Boards
- IPC-4554** Specification for Immersion Tin Plating for Printed Boards
- IPC-4761** Design Guide for Protection of Printed Board Via Structures
- IPC-6012** Qualification and Performance Specification for Rigid Printed Boards
- IPC-7091** Design and Assembly Process Implementation of 3D Components
- IPC-7094** Design and Assembly Process Implementation for Flip Chip and Die Size Components
- IPC-7351** Generic Requirements for Surface Mount Design and Land Pattern Standard
- IPC-7525** Stencil Design Guidelines
- IPC-7526** Stencil and Misprinted Board Cleaning Handbook
- IPC-7530** Guidelines for Temperature Profiling for Mass Soldering (Reflow & Wave) Processes
- IPC-7711/7721** Rework, Modification and Repair of Electronic Assemblies
- IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments
- IPC/JEDEC-9702** Monotonic Bend Characterization of Board-Level Interconnects
- IPC/JEDEC-9703** Mechanical Shock Test Guidelines for Solder Joint Reliability
- IPC/JEDEC-9704** Printed Wiring Board Strain Gage Test Guideline
- IPC/JEDEC-9706** Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection
- IPC/JEDEC-9707** Spherical Bend Test Method for Characterization of Board Level Interconnects
- IPC-9708** Test Methods for Characterization of Printed Board Assembly Pad Cratering
- IPC-9709** Test Guidelines for Acoustic Emission Measurement during Mechanical Test

2.2 Joint Standards³

- J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies
- J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires
- J-STD-005** Requirements for Soldering Pastes
- J-STD-020** Handling Requirements for Moisture Sensitive Components
- J-STD-030** Selection and Application of Board Level Underfill Materials
- J-STD-033** Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices
- J-STD-609** Marking and Labeling of Components, Printed Board and Printed Board Assemblies to Identify Lead (Pb), Pb-Free and Other Attributes

2.3 JEDEC⁴

- JEP95 Section 4.5** Fine Pitch (Square) Ball Grid Array Package (FBGA)
- JEP95 Section 4.6** Fine Pitch (Rectangular) Ball Grid Array Package (FRBGA)
- JEP95 Section 4.7** Die-Size Ball Grid Array Package (DSBGA)
- JEP95 Section 4.9** Generic Matrix Tray for Handling and Shipping (Low Stacking Profile for BGA Packages)
- JEP95 Section 4.10** Generic Matrix Tray for Handling and Shipping

3. www.ipc.org

4. www.jedec.org

JEP95 Section 4.14 Ball Grid Array Package (BGA)

JEP95 Section 4.17 Ball Grid Array (BGA) Package Measurement and Methodology

JESD22-A102 Unbiased Autoclave Test Method

JESD22-B108 Coplanarity Test for Surface-Mount Semiconductor Devices

JESD22-B112 High Temperature Package Warpage Measurement Methodology

JESD22-B115 Solder Ball Pull

JESD22-B117 Solder Ball Shear

JESD94 Application Specific Qualification Using Knowledge Based Test Methodology

JESD217 Test Methods to Characterize Voiding in Pre SMT Ball Grid Array Packages

2.4 EIA⁵

EIA-481 8 mm Through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling

3 SELECTION CRITERIA AND MANAGING BGA IMPLEMENTATION

3.1 Terms and Definitions Terms and definitions **shall** be in accordance with 3.1.1 through 3.1.4 and IPC-T-50.

3.1.1 Solder-Mask-Defined (SMD) BGA Pad A printed board pad with a solder mask aperture diameter equal to the diameter of the pad on the BGA.

3.1.2 Non-Solder-Mask Defined (NSMD) BGA Pad A printed board pad with a solder mask aperture diameter larger than the diameter of the pad on the BGA. Also known as Cu-defined BGA pad.

3.1.3 Nonwet Open (NWO) One metallurgical mass formed from a BGA ball and reflowed solder paste (or flux) which has incomplete or no wetting to the printed board land.

3.1.4 Head-on-Pillow (HoP) A solder joint comprised of two metallurgically distinct masses formed from a BGA ball and reflowed solder paste which has incomplete or no coalescence.

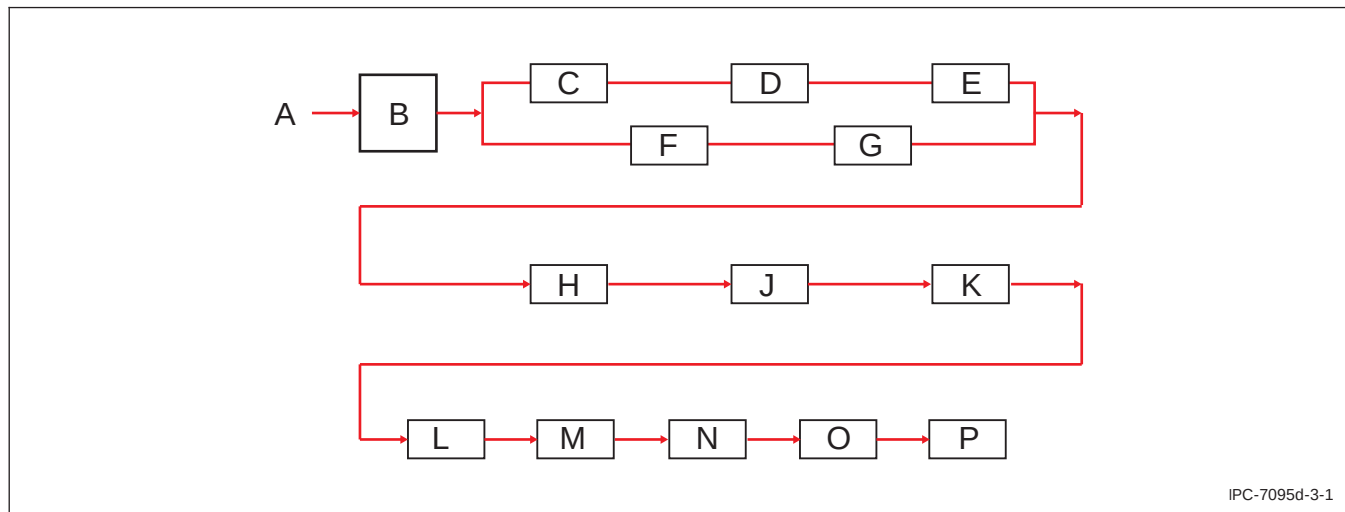
3.2 Overview Every electronic system consists of interfaces and the printed board assembly. Typically, the complexity of these systems is reflected in both the type of components used and their interconnecting structure. The more complex the components, as judged by the physical size and the number of input/output (I/O) terminals, the more complex the interconnecting substrate. Cost and performance drivers for end products have resulted in increased component density and a greater number of components attached to a single printed board assembly, while the available mounting area has decreased. In addition, the number of functions per device has increased, which is accommodated by using increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges for assemblers and printed board manufacturers who encounter handling, coplanarity and alignment problems.

Component packaging, microprocessor and memory package requirements affect the remaining electronic assembly packaging issues. The driving forces for component packaging are thermal management, electrical performance, dynamic warpage reduction, reliability, real estate constraints and cost. Peripheral devices with 1-mm pitch have become common, but this package cannot accommodate more than 84 pins. Larger peripheral pin-count devices require lead pitches of 0.65 mm, 0.5 mm or 0.3 mm.

Although pitches < 1 mm are useful for reducing package size, some manufacturers find it difficult to achieve increased density. At these fine pitches, leads are very fragile and susceptible to damage (e.g., lead coplanarity, lead bending and sweep). To place these packages, a pick-and-place machine with a vision system and waffle pack handlers is necessary. These two equipment features, however, can add substantial capital equipment costs.

BGAs were developed to overcome the assembly challenges presented by these fine-pitch, high-lead-count peripheral devices. Figure 3-1 shows an example of the package manufacturing process for BGAs.

5. <https://www.ecianow.org/standards-practices/standards/>



IPC-7095d-3-1

Figure 3-1 BGA Package Manufacturing Process

A – Start	F – Chip attach using flip chip process	L – Perform AOI
B – Known good die	G – Underfill die	M – Perform electrical test
C – Die attach	H – Apply flux or paste on BGA substrate lands	N – Inspect
D – Wire bond	J – Place balls on BGA substrate lands	O – Pack
E – Mold package	K – Reflow balls on BGA substrate lands	P – Ship

The use of solder bump interconnections instead of leads on BGAs eliminates problems associated with lead damage and coplanarity. BGA pitches from 1 mm to 1.5 mm have more than 250 μm of stand-off height, which significantly reduces problems with paste printing, placement, reflow and cleaning. BGAs provide much shorter signal paths compared to fine-pitch devices. Shorter signal paths can be very critical in high-speed applications. The termination types also play a role in the spacing between adjacent I/Os.

Internal or user design guidelines should indicate the importance of allowing added spacing between fine-pitch devices and the mounting substrate. With the exception of no-clean fluxes, cleaning problems arise with fine-pitch devices which sit almost flush ($< 250 \mu\text{m}$) to the printed board assembly. For proper cleaning, a stand-off of 0.4 mm to 0.5 mm is desirable. The need to meet this requirement will be based on the size of the BGA package, since smaller x-y profiles allow easier penetration of the cleaning solutions.

3.3 Description of Assembly Infrastructure Incorporating BGAs into electronic assemblies requires dedicated engineering resources to develop, implement and integrate the processes into the assembly operation. Even though BGAs can leverage SMT infrastructure, there are technical considerations that must be addressed to ensure successful implementation of BGA components into existing product configurations.

3.3.1 Land Patterns and Printed Board Considerations Land patterns are important to manufacturing because land dimensions affect the consistency and reliability of the resulting solder joint as well as cleaning and testability. Land pattern design for BGAs is even more critical because of the increased difficulty in solder joint inspection and rework/repair. Land pattern design issues for BGAs need to be understood. This is essential to ensure proper solder joint formation, prevent defects (e.g., bridging and opens) and achieve optimal reliability.

IPC-7351 contains land pattern guidelines based on three density levels. BGA lands can be SMD lands, in which the solder mask overlaps the land, or metal-defined lands, in which the solder mask stays away from the land. There are pros and cons for each approach, and the choice often depends on the BGA pitch (impacts land size) or size (impacts part mass).

These conditions help define:

- *Thermal Stress Reliability* – The metal-defined land helps avoid the possibility of a stress crack in the collapsed ball.
- *Mechanical Shock Reliability* – SMD lands helps secure the land to the laminate.

In addition to land design, one should keep in mind that the inner rows of BGA pins require additional layers for interconnection. Increasing the number of pins (vias) affects layer count due to the reduction of routing channels. Higher layer counts mean higher cost of the printed board.

BGAs and column grid arrays (CGAs) were standardized in 1992 with 1.5-mm, 1.27-mm and 1-mm pitches. FBGA package standards have established pitches of 1 mm, 0.8 mm, 0.75 mm, 0.65 mm and 0.5 mm; pitch configurations are defined in

small as 0.4 mm, 0.3 mm and 0.25 mm. Although standard configurations for BGAs and their associated land patterns exist (described in IPC-7351), some component manufacturers have modified the standard configurations to improve the interconnection capability in the component substrate. Tailoring standard geometries makes it important to check the manufacturer's data sheet to determine the exact characteristics of the pitch, ball size and depopulation (removed balls).

The concern in using these very complex parts relates to printed board design and assembly issues. The concern with design is properly interconnecting all the leads and having sufficient room for routing conductors. The concern with assembly is attaching all the leads to the mounting structure with high solder joint yield, avoiding open solder joints (head-on-pillow (HoP) and nonwet open (NWO)) or shorts (solder bridging between neighboring joints).

3.3.2 Technology Comparison

3.3.2.1 Multichip Module (MCM) and System in Package (SiP) Small, handheld portable systems (e.g., cell phones) result in the need for chips to be mounted on top of each other. The principles used to mount a single chip into an organic carrier package can also be used to connect several chips together. This technique is referred to as multichip module (MCM) or system in package (SiP). Ball size and pitch continue to be the primary process factors for individual components or those that encompass more than one semiconductor die. Table 3-1 shows examples of an attempt to establish a definition for MCMs housing more than one die. Initially, the chips were mounted on the same plane (horizontally). Figure 3-2 is an example of one such product using the area array concepts for interconnection.

Table_3-1 Multichip Module (MCM) Definitions

MCM	Technology Description	Attributes
Type 1	Common technology package	Multiple same type chips, in plane
Type 1S	Common technology package	Multiple same type chips, stacked
Type 1F	Common technology package	Multiple same type chips, folded
Type 2	Mixed-technology package	Mixed integrated circuit (IC) technology package, in plane
Type 2S	Mixed-technology package	Mixed IC technology package, stacked
Type 2F	Mixed-technology package	Mixed IC technology package, folded
Type 3	SiP	Mixed ICs and discrete devices, in plane
Type 3S	SiP	Mixed ICs and discrete devices, stacked
Type 4	Optoelectronic SiP	Mixed-technology for optoelectronics

3.3.2.2 Microprocessors Microprocessors typically have 40% to 60% of their I/O dedicated to power and ground. For example, a package might have a total of 1,300 I/O to 1,400 I/O of which the signal count is between 600 I/O and 700 I/O. Application-specific ICs (ASICs) may differ in that I/O apportionment.

The signal I/O escape wiring, and their interconnection to other high-I/O packages, will also require high density interconnect (HDI) technology. As the number of I/O on a chip increases, the body size of the single-chip package may become unacceptably large and could require reassessment of the overall package solution. This could include considering MCM packaging as an alternative.

The signal I/O count for high-performance BGAs is about two and a half times that commonly required for BGAs used in handheld products. The interconnection density requirement is linearly proportional to the number of signal I/O per package and inversely proportional to the center-to-center pitch between adjacent packages. A 2.5 X increase in signal I/O from 500 pins to 1,300 pins per package at the same package-to-package pitch will require a printed board with a 2.5 X increase in wiring density and a proportional increase in the density of the interlevel vias or plated-through holes (PTHs). This may require a reduction in the PTH/via pitch and an increase in the number of signal layers in the printed board.

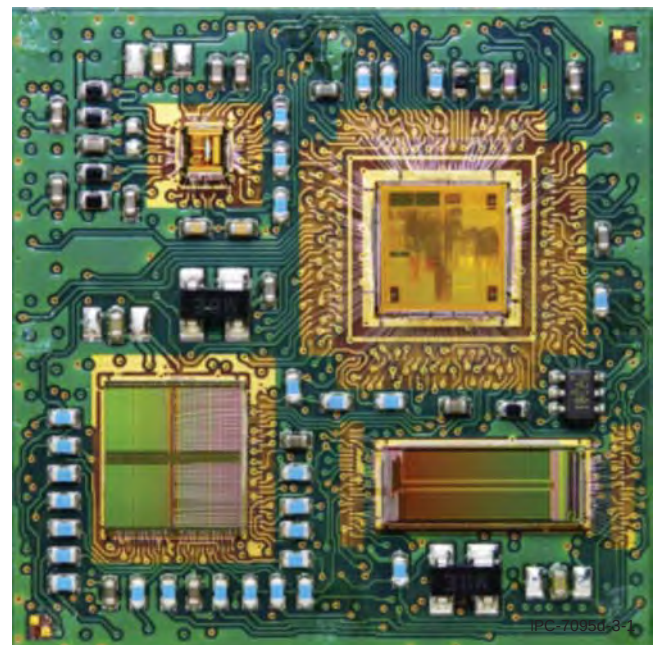


Figure 3-2 Multichip Module (MCM) Type 2S-L-WB

3.3.2.3 Escapes and Routing Considerations More functions are going into the silicon, which increase component package size and complexity. The higher I/O demand will require multilayer or HDI (microvia) designs to support the required wiring and to provide escape routing from the internal connections of array component patterns to the printed board. Using both sides of the printed board to place all the components may be required by the design. There will also be an increased demand on the printed board to handle the required power dissipation.

Using high-I/O components like BGAs and FBGAs creates the challenge of routing all the required signal, power and ground I/O balls to the printed board without increasing board complexity, therefore, increasing cost. Innovative package pin assignments and package configuration considerations (e.g., pitch, ball size, ball count and depopulation) can make printed board routing easier.

Two interconnection signal layers can be sufficient for trace escape from the inner rows within the BGA land pattern array, even when the BGA has very high ball counts, providing the pin assignments are properly planned and the escape routing is carefully designed. Table 3-2 is an illustration of the number of escapes possible on two layers of circuitry vs. the array size and the number of conductors between lands/vias.

Note: As the number of I/O increases, the ability to escape diminishes, so more layers may be required.

Table 3-2 appears to indicate two routing layers are insufficient to escape any array $> 16 \times 6$ (256 balls). In reality, a significant number of the balls will be used for power and ground connections and will require no conductor routing. They can be directly connected to the appropriate plane through land-to-via (dog bone). It is important to keep in mind poor placement of the signal or power/ground balls can waste available routing channels and significantly reduce the total number of signal I/Os that can be routed out in a given number of layers.

Table 3-2 Number of Conductors vs. Array Size on Two Layers of Circuitry

Array Size	Total Leads	Number of Conductors Between Vias (• •)		
		1	2	3
		• •	• •	• •
14 X 14	196	192	196	196
16 X 16	256	236	256	256
19 X 19	361	272	316	352
21 X 21	441	304	356	400
25 X 25	625	368	436	496
31 X 31	961	464	556	640
35 X 35	1,225	528	638	736

Placing signal pin assignments on the outer rows of an array package and using the inner balls for power and ground will facilitate escape routing. However, the corner balls of large array packages are more susceptible to mechanical failure, so it may be preferable to use these for redundant ground connections. The number of rows of signal I/O that can be routed out will depend on the desired number of conductor routing layers in the printed board and the number of conductors that can be routed between lands and vias.

Figure 3-3 shows examples of conductor and space widths that will fit between adjacent lands with various pitches and land diameters. Note that as ball pitch decreases, conductor width and spacing for a given number of conductors per channel also decrease, making it more difficult and costly to produce the printed board.

To reduce layer counts, designers can use balls anywhere packages. Balls anywhere packages are application-specific and customized based on the board design. The user will need to work with the chip supplier to obtain balls anywhere packages (see 6.2.6).

3.3.2.4 Wire Bonding Using 150- μm conductors and spaces is quite cost effective, but printed board cost begins to increase significantly for 100- μm conductors and spaces. Using an organic interconnecting substrate to mount the bare die within a plastic BGA requires the mounting lands on the substrate to match the bonding lands on the die.

The bonding lands are typically positioned for wire bonding, because this is the most popular technique. Thermally conductive adhesive is one method used to attach the back of the die to the substrate. Depending on the number of I/O and the lead pitch, multilayer substrate fabrication techniques may be used to translate a peripheral bonding land die to an area array matrix of bumps, balls or columns (see Figure 3-4).

Chip-bonding lands in an array format permit the mounting of the die in flip chip configurations. The die is mounted opposite to that which is wire bonded, and the bumps of the die make direct contact with the substrate being used.

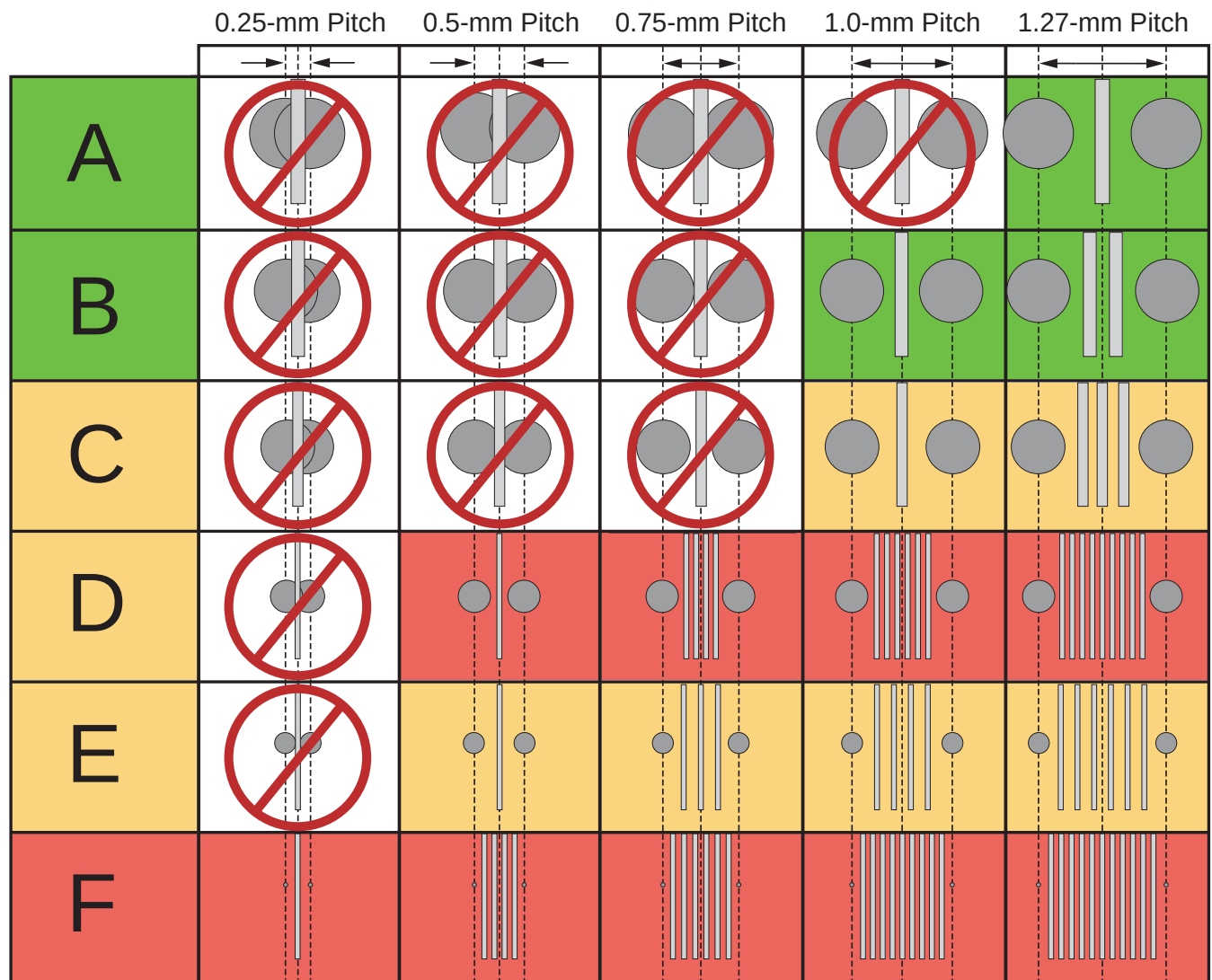


Figure 3-3 Conductor Width-to-Pitch Relationship

A – Conventional FR-4 (125 μ m line / 125 μ m space / 700 μ m land)
 B – Conventional FR-4 (125 μ m line / 125 μ m space / 600 μ m land)
 C – High-density FR-4 (100 μ m line / 100 μ m space / 600 μ m land)

D – Next-generation FR-4 (60 μ m line / 50 μ m space / 300 μ m land)
 E – Typical microvia (75 μ m line / 100 μ m space / 200 μ m land)
 F – Next-generation microvia (50 μ m line / 50 μ m space / 50 μ m land)

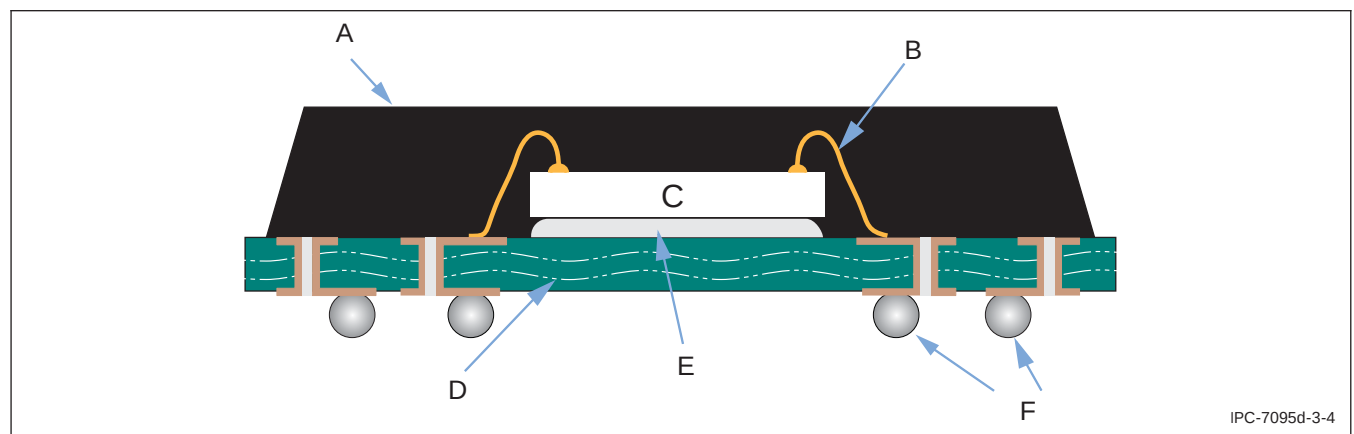


Figure 3-4 Wire-Bonded Ball Grid Array (BGA)

A – Overmolded epoxy
 B – Wire bonds
 C – Silicon die
 D – Substrate
 E – Die attach
 F – Solder balls

IPC-7095d-3-4

die pattern to the BGA pattern. This creates routing challenges for organic high-density microcircuit printed boards. Under-fill is usually required to accommodate and soften the mismatch between the coefficient of thermal expansion (CTE) of the chip and the CTE of the organic multilayer printed board (see Figure 3-5).

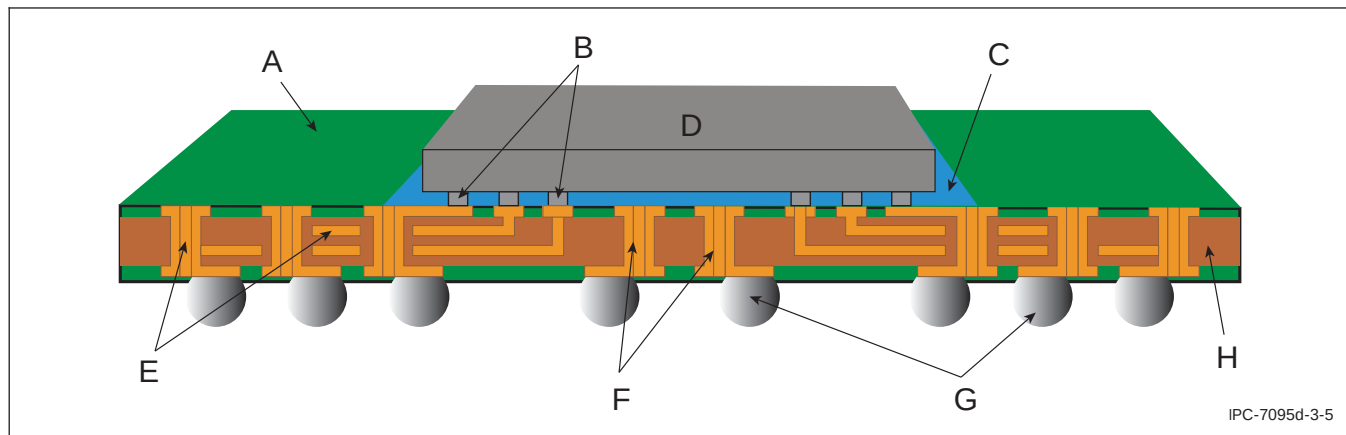


Figure 3-5 Flip Chip Bonded Ball Grid Array (BGA)

A – Solder mask
 B – High-melt-temperature solder or z-axis interconnection material
 C – Epoxy underfill
 D – IC chip

E – Copper circuitry and plated vias
 F – Thermal vias
 G – Solder balls
 H – High-performance laminate

3.3.3 Assembly Equipment Impact Surface mount technology (SMT) has advanced to a stage where most electronic components manufactured today are only available in SMT form. Manufacturing products with SMT in any significant volume requires automation. For low-volume SMT manufacturing, a manually operated machine or a single-placement machine may be sufficient. High-volume SMT manufacturing requires special solder paste deposition systems, multiple and various placement machines, in-line solder reflow systems and cleaning systems.

BGA repair and inspection are rather difficult, particularly for components with large body sizes or finer ball pitches. Rework machines with paste deposition, preheat and vision capability may not be required, but they are very helpful. X-ray and optical inspection (endoscope) capabilities can also benefit process development.

3.3.4 Stencil Requirements Stencil thickness and land size will determine paste volume, which is very critical for ceramic BGAs. Generally, on larger BGA components with 1.25-mm and 1-mm pitch, the aperture is large enough that stencil clogging, print registration and definition are less of a problem than with quad flat pack (QFP) components. Stencil thickness may need to be reduced when using finer-pitch BGA parts.

Matching solder paste stencil openings to the requirements of fine-pitch BGAs requires an understanding of the relationship between the stencil aperture and the size of the particles in the paste. IPC-7525 provides good descriptions to help make the appropriate relationship decisions for land patterns for parts which continue to reduce in size and be placed in closer proximity to each another.

3.3.5 Inspection Requirements As with any SMT part, BGAs should not be moved after component placement because this may smear the paste and cause solder bridges. Even if some misalignment is visually observed, many parts will self-align during reflow if their terminations are no more than 50 % off the land. If a BGA has a gross misalignment problem, it should be removed before reflow and then attached to the printed board assembly during rework. Assembled BGAs should be inspected for possible insidious defects (e.g., HoP) which may not result in an electrical test failure.

3.3.6 Test Before using BGAs, test strategies need to be developed. Direct probing on BGA solder joints is not possible, so test points should be designed. However, on high-density and complex BGAs, there may be insufficient test points to cover all critical I/Os. Some alternative test strategies may be needed, such as designing BGA components with boundary scan capability designed into them, which reduces the number of I/O fan-out probe points. Other efforts to build test capability on top of BGAs have not been proven to be good solutions because of the pressure exerted on the BGA and its solder balls.

3.4 Time-to-Market Readiness Before introducing BGA printed board assemblies into an end-product, it is important to address not only the technical issues, but also the possible business implications. When technology and product are concurrently developed, integration and validation issues may adversely impact time-to-market. It is preferable to first develop the

validate the technology before implementing it on a product. Otherwise, if a problem develops in the product or technology, the deadline for product shipment may be missed. To ensure time-to-market readiness, BGA implementation methodology and process steps should be analyzed.

3.5 Methodology Several factors must be considered when making design decisions to balance size, cost and functionality. The product must also be able to perform reliably over its expected lifespan in its intended environment. Package selection may be influenced by these reliability factors and environmental conditions (e.g., temperature, vibration, shock and humidity). Environmental and regulatory factors should also be considered.

3.6 Process Step Analysis There are several available paths to effectively utilizing BGAs. The length of each path depends on the company's design and assembly facilities and how quickly the company can be production ready. The following is an example of one approach:

1. Select a list of candidate products for BGAs.
2. Develop an equipment list based on the projected volume needs.
3. Organize a team representing design, production, test, quality and purchasing. This team is responsible for component and equipment selections and review. If sufficient in-house expertise does not exist, it may be desirable to use a reputable training center or consultant to save cost and time.
4. Develop a comprehensive BGA design guide that stresses manufacturability. Use existing standards where possible.
5. Design the candidate products, starting with the conversions of existing products using fine-pitch components.
6. Determine the need for Pb-free products, including the alloy used on the part as well as the surface finish needed on the mounting substrate.
7. Conduct rigorous assembly and test reviews. Carefully monitor component purchasing to ensure components have the specified package, shipping method, metallization, solderability and orientation in the shipping containers.
8. Develop comprehensive workmanship standards and a process control system that is statistically sound.
9. Design the remaining candidate products.

With the major emphasis on using parts that meet customer requirements and conform to new environmental regulations, many customers require reports listing all materials used at the component level and for completed assemblies. This requirement to establish a formal declaration system has been in place since the automotive industry was challenged by the end-of-life European Union directives. To help facilitate this reporting, IPC has developed materials declaration procedures (IPC-1751 and IPC-1752) and have encouraged software providers to make tools available that meet the requirements of those standards.

3.7 BGA Limitations and Issues Even though BGA technology has moved into the mainstream, there are still business and technical decisions and issues which must be resolved. Areas of special concern are:

- Visual inspection
- Moisture sensitivity
- Rework
- Cost
- Availability
- Voids in BGAs
- Open joint (BGA or package-on-package (PoP) BGA)
- HoP and NWO phenomena
- Standards and their adoption
- Reliability concerns

Adopting BGA technologies requires dedicated engineering resources to develop and implement a consistently reliable process.

3.7.1 Visual Inspection BGA packages may not be suitable for companies that rely on visual inspection to ensure quality and repair. BGA solder joint arrays cannot be inspected unless X-ray or optical inspection techniques are used. To benefit from the use of BGAs, the manufacturer must maintain a robust process control. Due to resources required (equipment, time and training), some companies find implementing such tight process control to be a difficult endeavor.

Some visual inspections of BGAs can identify problems with solder joints. These would show good flow on an uncollapsed ball with ceramic BGAs and collapsed balls on plastic BGAs on the outer rows of the BGA. Visual inspection of the outer rows serves as an indicator of some of these problems. Examples are BGA alignment with the lands on the outer rows or how the BGA is sitting on the board—level or skewed.

3.7.2 Moisture Sensitivity Plastic BGAs are moisture sensitive. This makes them susceptible to warpage, swelling, pop-corning or cracking if they are not properly baked and kept dry prior to assembly. Component storage and handling procedures are critical for any moisture-sensitive component, including leaded SMT devices, but it is critical for BGAs.

Component moisture sensitivity is tested using J-STD-020 and is determined by the package thickness. The moisture sensitivity level must be determined for each BGA package type. It is critical to know at which of the applicable temperatures (220 °C, 235 °C, 245 °C, 250 °C or 260 °C) the BGA was classified. The classification of the package type may drop several levels if the higher temperature is used.

Due to improvements in molding compounds and laminate systems, most laminate-based BGAs can be mounted and qualified for temperatures above 220 °C. Hermetic ceramic BGAs are not moisture sensitive, so they can be mounted using any of the higher temperatures. If a manufacturer will use Pb-free solder, it is important to test and verify at a higher temperature (e.g., 260 °C), because the higher temperatures for Pb-free applications can create major issues with BGAs and all other SMT devices.

3.7.3 BGA and Board Coplanarity and Warpage The plastic BGA package is also susceptible to warpage (the package edges lift up), which can result in no connections on the outer rows. The edges may also bend down, thus such terms as concave (also known as frowning) or convex (also known as smiling) BGAs have been used to identify these conditions. The convex (smiling) BGA puts a stress on the balls at the outer rows, while the concave (frowning) BGA puts the stress on the connection of the inter-row ball locations. Package warpage is of real concern in flux-only applications during rework. Large die sizes can cause CTE mismatch between the printed board and the package laminate material, which can create package warpage (see Figure 3-6).

Thermally unbalanced package designs, particularly those with heat spreaders on the top, will warp according to the classic bimetal effect.

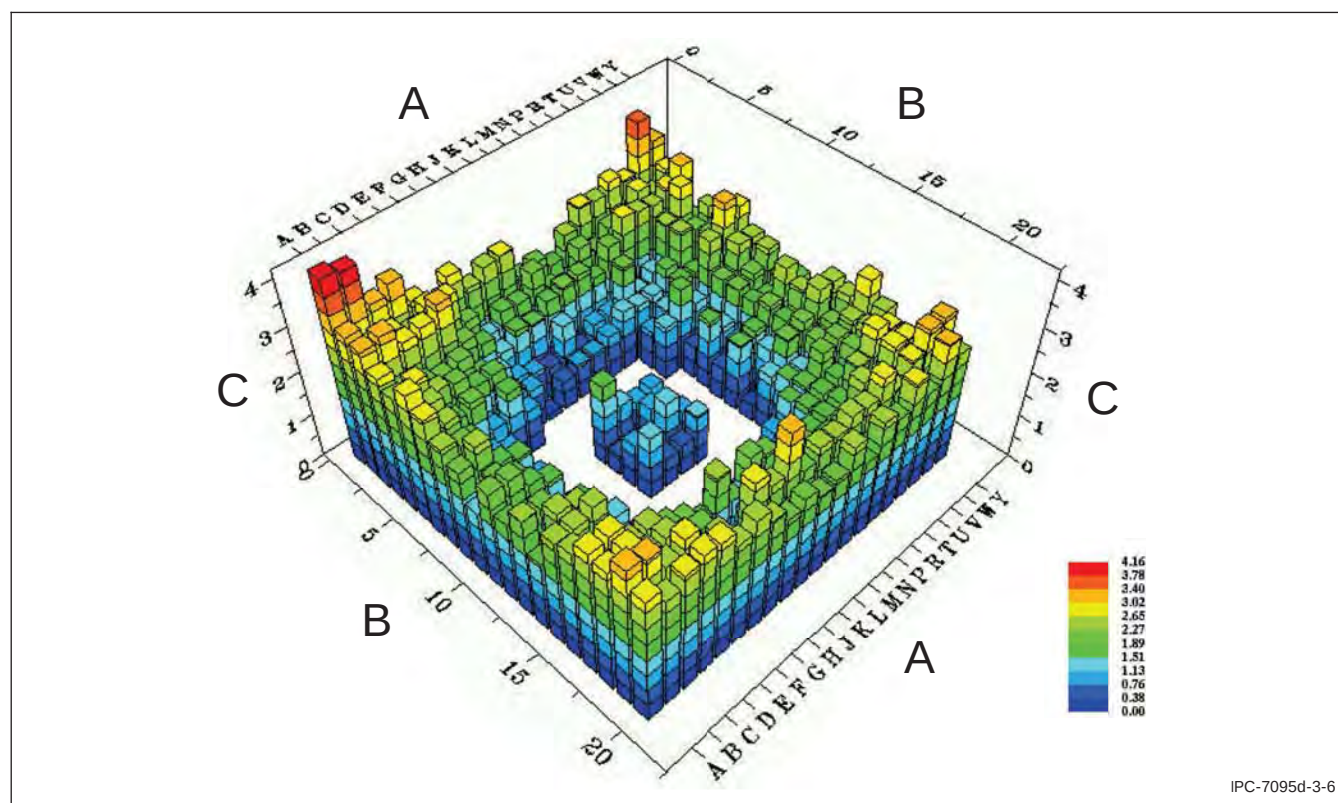


Figure 3-6 BGA Warpage

A – Row B – Columns C – BGA coplanarity

3.7.4 Rework Although BGAs do not require nearly as much rework as fine-pitch lead-frame devices, reworking these devices can be difficult. Tools and techniques include manual and automated techniques, reballing the BGA or redressing the land pattern. Several factors must be addressed during the rework operation. These are:

- Number of heat cycles
- Ball collapse during reballing
- No damage to pads on BGA interposer
- Proper land redressing and no damage to lands on the printed board
- Appropriate reflow temperature for reattachment based on alloy used
- Proper cleaning to remove flux residue unless no-clean flux is used
- Removal of underfill or corner-applied adhesives, if present
- Determine if the cost of rework, BGA and/or board assembly is worthwhile

See 7.9 for further details on repair and rework of BGAs.

3.7.5 Cost BGAs have a slight cost differential compared to fine-pitch peripheral packages. Competitive pressure keeps bringing costs lower to meet new targets. Additional costs accrue with increased board layer counts that BGAs require; however, there are many advantages to the interconnecting concepts and the performance characteristics resulting from BGA implementation.

The following are some key reasons for higher BGA package cost:

- Higher-cost substrate (fine line/space)
- High- T_g bismaleimide-triazine (BT) resin
- Thermal enhancements
- Electrical enhancements
- Very fine external pitches
- Thin profile heights
- Multiple die in a package
- Use of stiffener to mitigate dynamic package warpage

The industry continues to address these issues and make progress with them.

Because there are no standard pin count BGA designs, every die has different requirements. Each package/die combination is unique; therefore, economies of scale that manufacturers can achieve with perimeter-leaded packages are not necessarily seen with area array devices.

3.7.6 Voids in BGAs Many companies use boundary scan, in-circuit test (ICT), automated X-ray inspection (AXI), and automated optical inspection (AOI) individually or in combination to improve process control for BGA solder joints. Some look for voids through X-ray systems (see 7.3) to identify defects or verify against accept/reject threshold, because some level of voiding in any kind of solder joint may be inevitable. There is no direct correlation to specify the amount of voiding against reliability performance under thermal or mechanical stress. Other factors such as stand-off, solder mask aperture, land design, etc., are more dominant influencing factors for reliability.

Generally, voids are created during the SMT reflow process due to materials and process effects. Such voids are termed process or macro voids. However, there are many other sources of voids beyond those from the SMT process. These sources are discussed in detail in 7.5.

The requirement and accept/reject criteria established in J-STD-001 and IPC-A-610, respectively, represent a consensus for best practices. Values above this level can occur for design-induced voids (e.g., unfilled microvia in land). In such cases other acceptance criteria need to be established between the manufacturer and the user, taking the end-use environment into consideration. In the absence of design-induced voids, voiding levels > 30 % are not expected under normal circumstances. Appendix A provides support in establishing process improvement goals.

3.7.7 Pad Cratering Pad cratering is a separation of the pad from the printed board resin/weave composite or within the composite immediately adjacent to the pad. It is also known as a laminate crack. Examples of pad cratering are shown in cross-section pictures of BGA solder joints in Figure 3-7 (red arrows).

Pad cratering was first observed during the transition to Pb-free solders. New laminate resin systems were formulated to meet the high-temperature requirements of Pb-free solder and were stiffer and more brittle than those used for SnPb solders. Being more prone to cracking, these laminates failed when subjected to high dynamically induced mechanical stresses during such printed board assembly operations as ICT, board depanelization and connector insertion. They also failed during shock and vibration stresses imposed during shipment and product use in the field.



Figure 3-7 Examples of Pad Cratering

There are several possible failure modes for a BGA solder joint. Figure 3-8 highlights the location of pad cratering in relation to other forms of solder joint failures. See Location 5 for the pad crater failure mode. It occurs between the land pad and the printed board laminate. The failure between the component substrate and the component pad at Location 1 is also very similar to pad cratering, but this type of failure is usually attributed to the component packaging process rather than printed board assembly. The occurrence of failure in Location 1 is usually discovered during component reliability evaluations or during the classification conditioning described in 3.7.2.

Table 3-3 lists IPC standards related to characterization and assessment of printed board interconnects for their propensity to pad cratering.

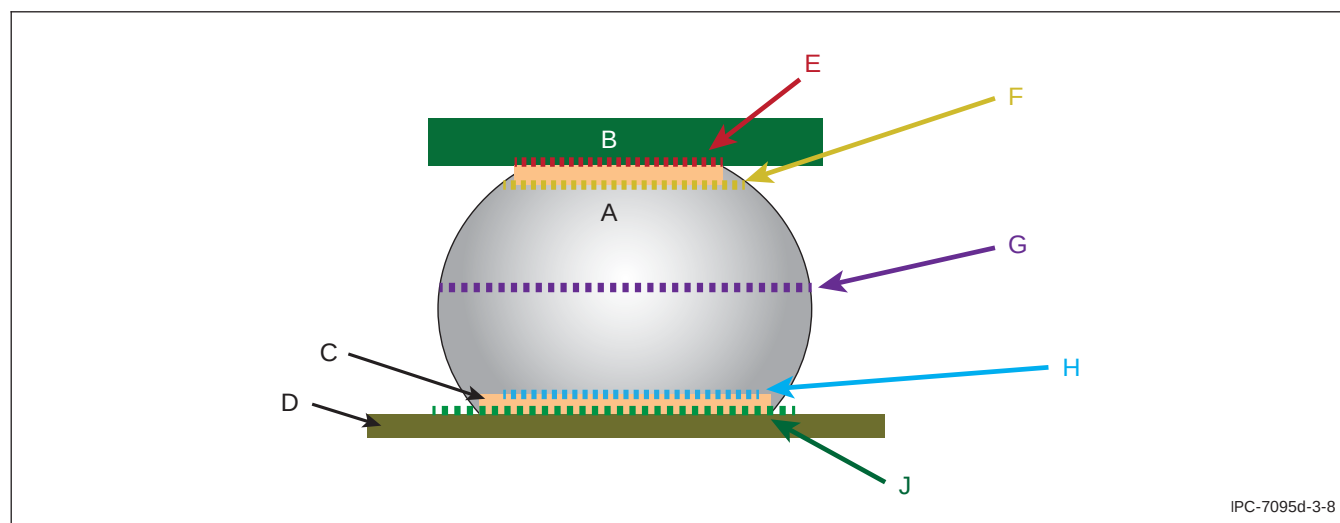


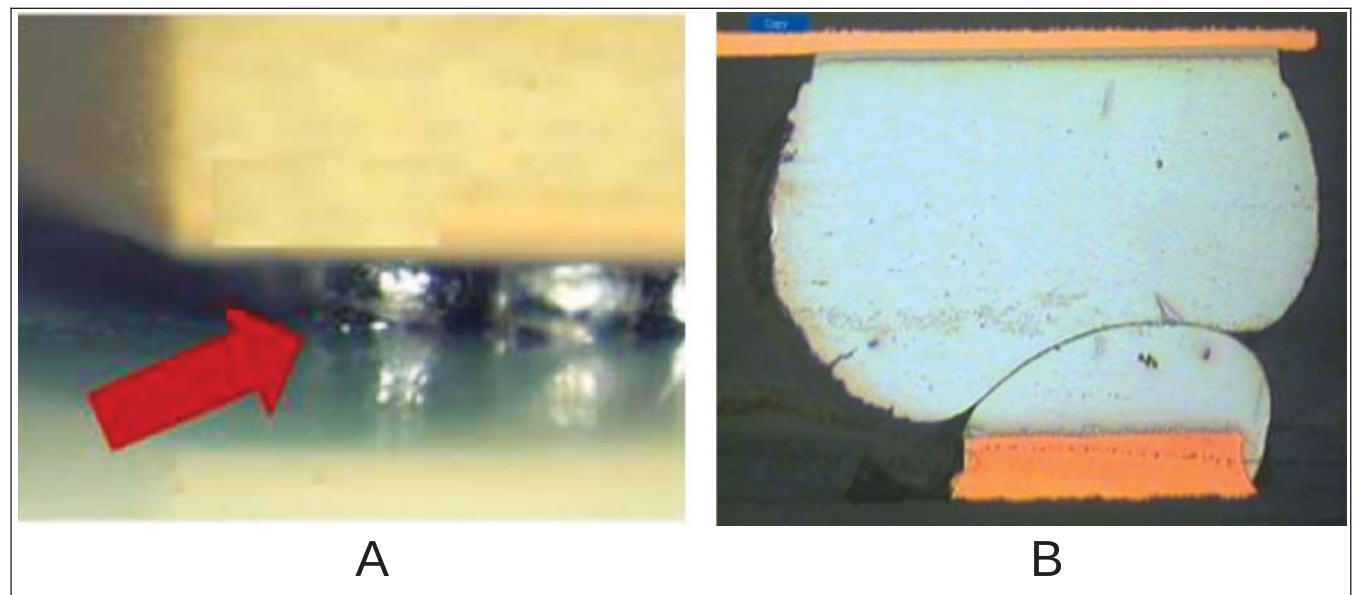
Figure 3-8 Various Possible Failure Modes for a BGA Solder Joint

- A – Solder ball
- B – Component substrate
- C – Land pad
- D – Printed board
- E – Failure between component substrate and pad (Location 1)
- F – Failure between substrate pad and ball (Location 2)
- G – Failure within solder, typically seen after thermocycle (Location 3)
- H – Failure between ball and pad (Location 4)
- J – Failure between pad and board (pad cratering) (Location 5)

Table 3-3 List of IPC Standards Related to Pad Cratering

Standard Number	Description
IPC/JEDEC-9702	Characterizes the fracture strength of a component's board-level interconnects.
IPC/JEDEC-9703	Mechanical shock test guidelines for assessing solder joint reliability of printed board assemblies, from component to system level.
IPC/JEDEC-9704	Specifies a methodology for strain gage placement and subsequent testing of printed boards using strain gages. The method describes specific guidelines for strain gage testing of printed boards during the printed board manufacturing process, including assembly, test, system integration and other types of operations that may induce board flexure.
IPC/JEDEC-9706	Establishes metrology guidelines to electrically and reliably detect solder joint opens on flip chip, BGA and SMT board assemblies during mechanical shock or drop event.
IPC/JEDEC-9707	Characterizes the maximum allowable strain that a SMT device's board-level interconnects can withstand in flexural loading.
IPC-9708	Provides test methods to evaluate the susceptibility of printed board assembly materials and designs to cohesive dielectric failure underneath SMT pads. The test methods can be used to rank order and compare different printed board materials and design parameters, but they do not define acceptance criteria.
IPC-9709	Establishes an acoustic emission method to evaluate the performance and reliability of surface-mount attachments of electronic assemblies during mechanical loading.

3.7.8 Head-on-Pillow (HoP) Defect HoP defect is a solder joint comprised of two metallurgical distinct masses formed from the BGA ball and reflowed solder paste with incomplete or no coalescence. This defect is also known as head-in-pillow, ball-in-cup, ball-in-socket and hidden pillow. Figure 3-9 shows two views of HoP defects.

**Figure 3-9 Corner View (Left) and Cross-Section View (right) of a Head-on-Pillow (HoP) Solder Joint Defect**

A – Corner view B – Cross-section view

As shown in the cross-section view in Figure 3-9, the two masses of solder are touching but have not coalesced into one. This defect may not result in an electrical open, because with some pressure on the BGA package, the contact resistance between the two masses may be low enough to pass ICT requirements. If the two masses of solder are separated by a gap, the defect is called a HoP open. Figure 3-10 shows an example of a HoP open defect. This defect will fail ICT requirements.

**Figure 3-10 Cross-Section View of a Head-on-Pillow (HoP) Open Defect**

The root cause of HoP is the formation of a gap between the molten solder ball and molten solder paste deposit on the lands. If this gap does not form during reflow soldering, the HoP defect will not form, unless there is either contamination or excessive oxidation on the solder ball.

The following are some solutions to mitigate HoP:

- Increase the solder paste volume printed on the lands by opening-up the stencil aperture.
- Use solder pastes that maintain their activity late into the reflow process to promote coalescence of the solder ball and solder paste masses, even when the printed board assembly is cooling down from the peak reflow temperature region.
- Equilibrate the temperature across all solder balls of the BGA during reflow.
- Use a nitrogen atmosphere during reflow.
- Use pallets during reflow to minimize board warpage, which causes the formation of the gap.

See also 7.8.5.

3.7.9 Nonwet Open (NWO) Defect NWO is a joint comprised of one metallurgical mass formed from the BGA ball and reflowed solder paste (or flux) with incomplete or no wetting to the land. There will be no evidence of solder on the land. This defect is also known as nonwet, hanging ball, ball on pad and ball on land. Figure 3-11 shows various views of NWO defects.

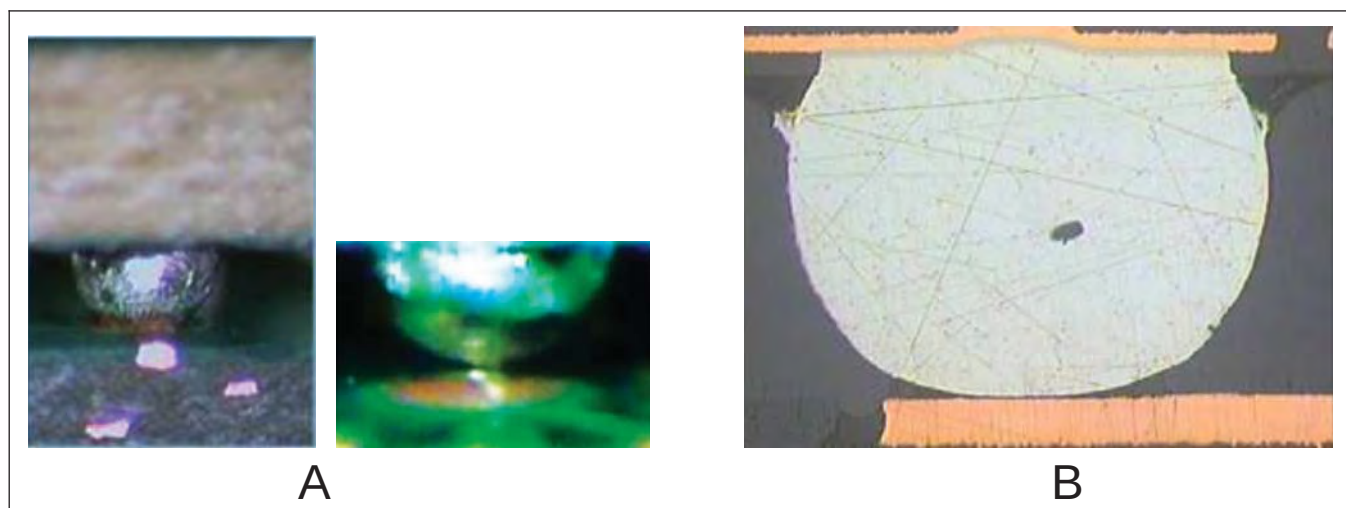


Figure 3-11 Examples of Nonwet Open (NWO) Defects in Side View and Cross-Section View

A – Side views

B – Cross-section view

There are many root causes of NWO:

- The stencil aperture can become clogged during solder paste printing and leave little or no paste on the land.
- Contamination on the land, which will prevent wetting of the molten solder to the land.
- Warpage of the BGA package during reflow can lift the ball and the solder paste stuck to the ball up and away from the land. When in the reflow zone of the oven, this solder paste will coalesce with the solder ball to form one mass without wetting the land.

NWO defects caused by package warpage can be reduced and eliminated using methods similar to those used to mitigate HoP:

- Change the solder paste formulation so it adheres stronger to the land than to the solder ball during reflow.
- Print more solder paste on the land to increase adhesion force of the solder paste deposit to the land. Use pallets to decrease the warpage of the printed board during reflow and to lower the risk of separating the ball from the land.

See also 7.8.6.

3.7.10 Reliability Concerns In general, the reliability of the solder attachment can be optimized by developing a thorough understanding of the product's operational use environment and by following the guidance outline in the design for reliability (DfR) procedure suggested in IPC-D-279. This section covers reliability concerns specific to BGA components. These concerns can be separated into BGA component reliability and the reliability of the BGA solder attachment to the interconnecting substrate, usually an organic printed board.

Component reliability issues are mitigated through proper mounting of the die to the interposer. Wire bonding is well known, often quite refined and can afford high yields. Another popular technique is to mount the bare die face down onto the interposer in a flip chip configuration. Using flip chip processes requires a tighter control of the land positions on the interposer so the lands line up properly with the bonding sites on the bare die. In addition, if the interposer is made of organic materials, the attachment process also requires underfill to minimize the fatigue damage caused by a CTE mismatch between the silicon die and interposer.

Solder joint fatigue for BGAs at the board assembly level is mitigated by minimizing the CTE mismatch between the package substrate and the printed board. Solder joints in the corner of BGA packages and under the die shadow are at the highest risk for fatigue failure because CTE mismatch is the highest at these locations. Increasing the package stand-off height is one way to minimize solder joint fatigue risk. Another way is to use board-level underfills, similar to what is done for the first-level interconnect between the silicon die and the organic package substrate. See 7.2.2 for more details on underfills.

Brittle fracture of solder joints during mechanical shock and drop stresses also is mitigated by using board-level underfills. However, since the underfill application process can take an inordinate amount of time, corner-bond and edge-bond processes are used in market segments in which the products are prone to shock and drop events. In corner- and edge-bond processes, an adhesive is applied to only the corners or edges of the BGA component substrate and is then cured. See 7.2.2.2 for more details on corner and edge bonding.

The risk of Sn whiskers and Au embrittlement should be considered when selecting surface finishes. Thick Au ($> 0.25 \mu\text{m}$) as a surface finish should be avoided to mitigate the risk of Au embrittlement of the solder. Excessive thickness of other noble metals as a surface finish should also be avoided. See 5.3 for more information on surface finishes.

4 COMPONENT CONSIDERATIONS

4.1 Semiconductor Packaging Comparisons and Drivers There are many types of package formats for ICs, but there are only four types of terminal shapes:

- 1) In-line pin (single and dual)
- 2) Pin grid array (PGA) and BGA
- 3) J-lead
- 4) Gull-wing lead

J-leads and gull-wing leads are the most common lead configurations for SMT plastic-packaged ICs. Gull-wing is the most commonly used of the two. One of the biggest problems with higher-pin-count, fine-pitch gull-wing leads is their fragility and, because of this, their susceptibility to lead damage (e.g., coplanarity, lead bending and sweep). Lead damage is one of the leading causes of defects in fine-pitch, gull-wing packages. Although gull-wing devices are the most commonly used lead form for low- and high-pin-count packages, BGA devices have broad acceptance due to their physical robustness, pin-for-pin density increase, size reduction opportunities and enhanced electrical performance.

Regarding performance, BGA signal paths can be much shorter than those of fine-pitch gull-wing packages, which is advantageous in high-speed applications. BGAs have also exhibited very high board-level assembly process yields due to their ability to self-align during reflow. Because their array format can be scaled up to accommodate high I/O within a small form factor, BGAs have proven to be a practical solution to higher-pin-count packaging.

4.1.1 Package Feature Comparisons Designs and configurations of area array component terminations have evolved significantly from the simple ball being attached to a land on the package substrate. The BGA configuration is the most basic and widely used termination design for area array packages. A solder ball is reflow soldered onto the land of a package substrate using either flux or solder paste. This package, with balls on its underside, can then be subsequently reflow soldered to printed boards using standard SMT soldering process. The solder balls melt fully and collapse when forming the solder joint.

The solder grid array termination design dispenses with the solder ball and prints only solder paste on the package land. The resulting solder bump is then reflow soldered on printed boards to form the solder joint using standard SMT soldering process.

Another technique is the use of ceramic interposers for producing grid array packages. The ceramic ball grid array (CBGA) termination design is similar to the BGA design, but the ball (typically PbSn10) used in this concept does not melt fully and collapse during assembly. Due to the wide mismatch in expansion between the ceramic substrate and the package substrate, the CBGA is not recommended for use in high-temperature applications.

printed board laminate, a high stand-off height needs to be maintained for the solder joint to provide adequate reliability. The noncollapsing Pb-free solder ball (formerly high Pb) provides this requirement.

To address the need to mount a ceramic package on an organic printed board and accommodate the differences in respective CTEs, a column of solder provides the attachment termination. The ceramic column grid array (CCGA) termination design is an extension of the CBGA. CCGAs use a PbSn10-cast column or PbSn20 Cu wrap column instead of a high-melt ball. This creates a higher stand-off and more flexible interconnection, resulting in a significant increase in reliability. This high-Pb alloy also has been supplanted by a Pb-free alloy for applications that prohibit the use of Pb.

Some packages use a Cu pillar (μ PILR) to reduce z-height expansion. Additionally, some connectors use an enhanced fillet termination (solder charge) to provide a larger area for solder to wet.

See Figure 4-1 for examples of termination types.

4.1.2 BGA Package Influencers The emphasis on faster, smaller and lighter electronics systems is making component, printed board and system packaging more complex. The increase in assembly complexity is due in part to the wide use of small-outline SMT packages, the key to miniaturization of electronics products. Device contact pitch also plays a critical role in the complexity of manufacturing processes. For example, with the adoption of finer contact pitches, greater precision is demanded for each process in the assembly sequence (e.g., pick-and-place, solder paste printing and reflow). Inspection, rework and repair also must be more precise.

Key issues to address when selecting BGA component packaging:

- Thermal and electrical performance
- Spatial constraint
- Cost

The component packaging requirement varies for different types of systems. For example, high-end microprocessors run at higher frequencies and require thermally and electrically enhanced packages.

Thermal enhancements include:

- Heat slugs
- Heat spreaders
- Heat sinks
- Integrated fin-fans (fans mounted on heat sink)

Electrical enhancements include:

- Multilayer packages
- Higher-pin-count packages
- In-package capacitance

Hermetic ceramic packages are generally used for in-package capacitance applications.

4.1.3 Cost Concerns Lead-frame ICs have traditionally maintained a relatively low manufacturing cost. This is due to the very high volume of products being offered in a limited package configuration. This enables the manufacturer to utilize common tooling and molding processes for a diverse number of customer applications. The array package format, however, is more often designed and engineered for a specific product application.

The initial cost for BGA devices with a pin count < 200 will most likely be greater than lead-frame packaging. This is due in part to the unique single-application substrate design and additional package assembly process steps. Cost parity between lead frame ICs and BGAs is generally reached when the device requires ≥ 200 I/Os.

4.1.4 Component Handling BGAs can be furnished in a carrier tray or tape-and-reel. EIA-481 standard embossed tape-and-reel format is often specified when IC components are relatively small and/or are required for very high-volume applications. JEDEC-registered carrier trays are furnished to meet industry-developed design guidelines (see JEP 95, Section 4.9 and Section 4.10) with a fixed length, width and thickness. Plastic-packaged ICs, including BGAs, are susceptible to moisture retention that can damage the package during reflow. To protect the devices from undue physical contact and exposure to humidity, the loaded carrier trays are shipped in a sealed electrostatic discharge (ESD) and vacuum-purged moisture-resistant envelope. Trays should remain sealed until ready for board-level assembly (see 4.8.5).

Package Type	Termination Cross-Section Before Reflow	Termination Cross-Section After Reflow
BGA		
Solder Grid Array		
CBGA		
CCGA		
Solder Charge SMT		
μPILR		

Figure 4-1 Termination Types for Area Array Packages

A – Package substrate

D – Land

G – Solder joint

K – Ceramic package substrate

N – Socket terminal

B – Solder ball

E – Printed board

H – Fillet

L – Column

O – Stamped solder preform

C – Solder mask

F – Solder bump

J – High-Pb solder ball

M – Socket body



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The user should specify plastic-encased BGAs to be furnished in tray format rather than tape-and-reel. The tray carrier will accommodate the potential need to bake-out devices prone to moisture absorption. For example, if plastic BGAs are exposed to ambient conditions beyond their floor life, they will likely require baking before assembly. The plastic tray carriers developed for bake-out are rated to withstand 125 °C. Tape-and-reel materials cannot be exposed to temperatures > 50 °C without damage occurring to the carrier tape. Baking a moisture-sensitive BGA in tape format could take several days.

4.1.5 Thermal Performance Continually improving microprocessor performance and increasing clock speeds have led to power increases. Problems associated with higher power are mitigated with die shrink, which is made possible by the reduction of transistor feature sizes in contemporary semiconductor processes and the associated trend towards lower power supply voltages. As device geometry shrinks, field intensities increase, promoting a reduction in supply voltages to avoid destructive effects.

CBGAs are commonly used for high-wattage packages, because they provide greater thermal conductivity than plastic packages. Thermally enhanced plastic packages can also accommodate up to 30 watts by incorporating integral metal heat spreaders.

4.1.6 Spatial Constraint Spatial constraint is one of the important driving forces in reducing component package size. This has contributed to the widespread usage of SMT devices, which are not only smaller in size, but enable component mounting on both sides of the printed board. As pin counts increase, however, even with SMT, conductor-to-conductor pitch must decrease to keep the size of the package within a practical range for manufacturing.

As BGA contact pitch package decreases, the opportunity for placing more components in a specific area increases. Printed board real estate can support more functions per unit area, but components such as fine-pitch BGAs require narrower conductors and closer conductor spacing for interconnection. For assemblies with very high component density, a greater number of conductive layers may be required to maintain a smaller form factor.

4.1.7 Electrical Performance With increasing frequency, the need for improved impedance control and minimal package insertion loss is a concern. When impedance control requirements are imposed, one must consider the need for terminations to prevent or dampen reflections. These terminations, if performed in parallel to source and/or load points on critical signals, will increase power consumption.

Electrical performance drivers include:

- Signal integrity
- Operating frequency
- Power
- Pin count

High-frequency operations increase power consumption with the square of frequency. Low-power semiconductor development has increased to reduce the average power consumption of complex digital ICs. Fortunately, as IC processes mature, the power per logic operation decreases by smaller device feature sizes. In the case of ceramic packages, even with increase in bond lands for high-speed devices, the pin count growth required for power and ground distribution is kept to a minimum by exploiting the intrinsically high package capacitance and using package-mounted bypass capacitors.

4.1.8 Mechanical Performance The susceptibility of BGA assemblies to other failure modes caused by mechanical shock, vibration and/or bending also should be assessed. Procedures described in IPC/JEDEC-9702, IPC/JEDEC-9703, IPC/JEDEC-9704, IPC/JEDEC-9707 and IPC-9708 provide guidance in completing assessments such as mechanical shock, bend testing and employment of an *in-situ* method for continuous evaluation. The interconnect failure modes from these types of exposures extend beyond solder joint failure. One other failure mode that may be observed through this type of mechanical testing is land cratering, which is the fracturing of the resin layer in the printed board under the BGA land. These cracks initiate at the edge of a BGA land and can continue to propagate through the underlying resin layer. The fracture may follow various paths. There may be an adhesive failure between the Cu land and the underlying resin, or there may be a cohesive failure due to a fracture entirely within the resin layer or through a connecting trace.

Electrical failure will occur when the conductor trace leading to the BGA land fractures. Depending on the location of the mechanical loading, the trace fracture may occur either before or after the land crater fracture propagates under the BGA land. This phenomenon can result in the risk of latent defects, which creates long-term reliability exposure. A land crater may be initiated during mechanical handling of assembly processing, but it may not be detectable at test by electrical means.

Subsequent thermomechanical exposure may result in the propagation of the crack through a conductor and later electrical failure in the field. Even if the conductor does not crack, the laminate crack creates the potential for increased moisture ingress, which could result in conductive anodic filament (CAF) formation.

4.2 Die Mounting in the BGA Package There are many ways a die is mounted in a BGA. The three main variations can be differentiated by the medium of signal transmission from the die to the solder ball array. In the basic three designs, the signal is carried by wire, conductive material (flip chip) or conductive ribbon-lead. The substrate can be ceramic or organic. The package properties will depend on the properties of the substrate material and its dimensional parameters. This section describes the more common methodologies for die-to-package assembly.

4.2.1 Wire Bonding There are two main forms of wire-bonded BGAs:

- 1) Chip-on-board (COB) – active surface of the die faces away from the substrate
- 2) Board-on-chip (BOC) – active surface of the die faces the substrate

In both structures, the bond pads on the die are generally furnished at the periphery, and the wire bonds are made from the die periphery to the lands on the substrate surrounding the die.

The die can be attached to the substrate using conductive or nonconductive adhesive. Use of electrically conductive adhesive is specified when the die backside requires an electrical connection. The drawback to this is the substrate area smaller than and equivalent to the size of the die cannot be accessed for in-package circuit routing. If the die does not require a backside electrical connection, a nonconductive adhesive can be used to place the die on the substrate. In this case, the area under the die can be used for signal routing.

The adhesive selected for die attach must not adversely affect the mechanical integrity of the traces or the integrity of the electrical signal. After die attach and adhesive curing, the die is ready for electrical interface to the substrate base. The bond pads on the die are electrically connected to the bond pads on the substrate using Au wire or Al wire when feasible. The traces on the substrate route the signals from wire bond pads to the BGA on the bottom of the substrate through plated vias. After the wire bonding process, the die and bond area is typically protected by encapsulation. Encapsulation material can be applied in the form of glob-top or molded in a press. An alternative to encapsulation is the attachment of a premolded cover after assembly.

In BOC (die face-down structure), the bond pads on the die can be located at the die periphery or in a row or rows at the center of the die. The substrate is designed with a narrow slot to accommodate the row or rows of bond pads on the die. The die-to-substrate adhesive is placed to the right and left of the bond pads. The adhesive can be applied in paste or film. The active (circuit) side of the die is attached face-down onto the substrate with the substrate slot exposing the bond pads on the die typical of that shown in Figure 4-2.

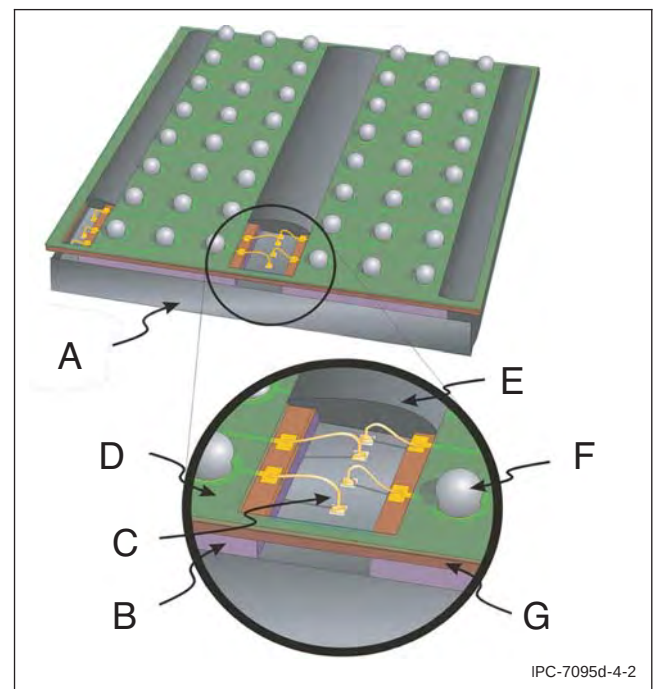


Figure 4-2 Board-on-Chip (BOC) BGA Construction

- A – Silicon chip
- B – Adhesive
- C – Wirebonds
- D – Solder mask
- E – Encapsulant
- F – Solder ball
- G – Polyimide film

After die attachment and adhesive cure, the bond pads on the die are wire bonded to the corresponding pads surrounding the slot on the substrate. Following wire bonding, the wires and exposed die surface are encapsulated for protection. Note that one or more grid array rows will need to be depopulated to allow the slot in the substrate for wire bonding to the die. Also note that wire bonding is accomplished at the center of the die and does not require additional peripheral area around it for die-to-substrate interface. Figure 4-3 illustrates the top and bottom of a mold-encapsulated BGA package.

4.2.2 Flip Chip Flip chip (direct chip attach) design eliminates the need for wires and die attach. In this design, a pre-bumped die is flipped circuit-side down, and then the lands on the circuit side of the die are brought into contact with corresponding lands on a substrate by using solder or conductive adhesive. The die bond pads, however, are not immediately compatible with solder or conductive adhesive attachment processes. Solder bumping with a solder-compatible alloy composition before sawing the die wafer is one of the most common procedures. The solder material and the bumped-pad structure materials are chosen to optimize electrical and mechanical connection typical of that shown in Figure 4-4.

Conductive adhesive or polymer attachment can be adapted as well; however, the die bump contact may require a noble alloy that is compatible with the conductive alloy particles in the adhesive. This alloy bump or ball can be applied to the die bond pads by plating or ball bonding. If a solder or an isotropic conductive adhesive is used, the gap between the die and the substrate may require an under-die filling with epoxy to ensure mechanical integrity of the die-to-substrate interface. Use of an anisotropically conductive material eliminates the need for added underfill. After attaching the die to the substrate, it is typically encapsulated, coated or over-molded for protection.

4.2.3 Changing BGA Termination Materials Most commercial array-configured components are furnished with a Sn-rich, Pb-free ball contact to be compliant with Restriction of Hazardous Substances (RoHS) regulations. Several electronic market segments remain exempt from Pb-free restrictions, especially products that operate in harsh environments and/or have life-critical functionality. While these market segments can use Pb solder, it is increasingly difficult to procure commercial BGA components which are not in ROHS-compliant configurations. When the specific alloy furnished on the BGA component is not compatible with an application or corresponding SMT processing, manufacturers may choose to mitigate risks by changing the BGA termination alloy. This involves removal of the existing contact (deballing) and replacement (reballing) with the preferred alloy.

4.2.3.1 Deballing For low-volume applications, the original solder ball can be removed using solder wicking or a hot-air desoldering tool. Solder wicking can work well, but the technician performing the task must avoid scratching or lifting the lands on the component. As an alternative, hot-air desoldering systems specifically developed for BGA rework can be used. When a greater number of components require reballing, automated wave solder deball systems, robotic hot-air excavation or a solder-dip process may prove more efficient. No matter the method used, the cleaner the lands, the better the result obtained when reballing.

4.2.3.2 Reballing Reballing is significantly more complex. The components must first be prebaked to ensure any moisture that may have been absorbed from the ambient atmosphere is eliminated. Moisture retained within a BGA can become gaseous during reballing, which will cause severe structural failure.

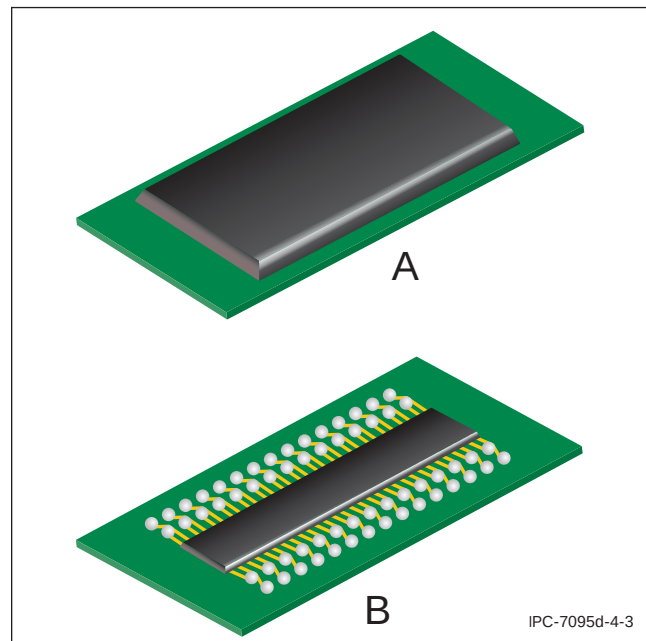


Figure 4-3 Top of Molded Board-on-Chip (BOC) BGA
A – Top B – Bottom

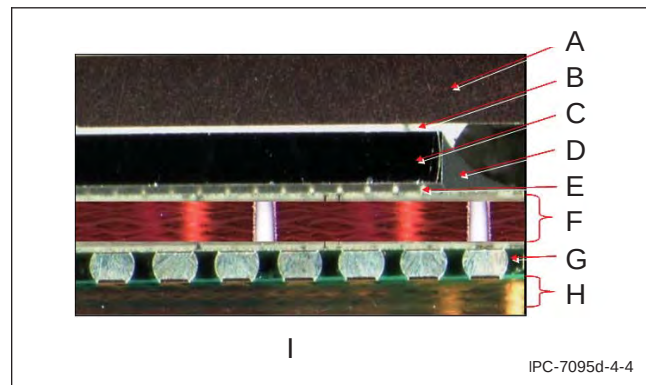


Figure 4-4 Flip Chip (Bumped Die) on a BGA Substrate
A – Heat spreader E – Flip chip solder balls
B – Thermal paste F – Package substrate
C – Die G – BGA solder balls
D – Underfill H – Printed board

BGA reballing equipment suppliers recommend a bake-out process (see J-STD-033). Preformed arrays provide spheres of the preferred alloy that are already configured in the desired array. Many array configurations are available, and the cost is low for small quantities since there is minimal tooling cost. The preformed arrays use either water-soluble paper or a temporary polymer carrier to retain the tiny spheres in position during reflow soldering onto the BGA.

This reballing method requires subsequent component cleaning and baking to dry the BGA again before use. Bench-top rework and repair systems also enable efficient deballing and reballing, but operator skill will be critical. Fully automated BGA reballing systems, due to their cost, will likely be justified only for very high-volume or sustained-use applications.

The reballing process has been shown to be reliable, provided strict procedures (including the number of reflows) are followed. The advantage of using a reballed BGA is the component is transparent to a SnPb soldering process. The disadvantages, however, are the cost and time required to reball the component, as well as the potential for package warpage when the component is exposed to excessive temperature. Additionally, package warpage increases the potential for HoP solder process defects.

Be aware that the reballing process effectively eliminates component traceability and revokes any regular or extended warranty that is normally provided by the original manufacturer regarding component use and storage. Consult the original manufacturer to determine if there might be some limitations concerning additional reflow and reprocessing of the BGA terminations.

If the process for efficiently changing solder ball alloy is beyond the capability for a company, a broad range of service sector solutions exist.

4.2.4 Options for Nonreballed BGAs The disadvantages of reballing may motivate the assembler to evaluate options that do not involve this process. This section explains the options for using a Pb-free BGA in a SnPb soldering process.

4.2.4.1 Two-Stage Process In the two-stage assembly process, a standard SnPb reflow process is used for assembly of all components on the board except Pb-free components, which are installed in the second assembly stage.

STAGE 1: Solder paste is printed onto printed board land patterns followed by placement of all components except Pb-free BGAs. The assembly is then processed using a conventional SnPb reflow process (210 °C to 220 °C peak).

STAGE 2: Flux (not solder paste) is selectively applied at BGA sites. Pb-free BGAs are then placed and selectively soldered using standard Pb-free process profile (240 °C to 245 °C peak). Selective soldering is completed using either hot-air or laser-assisted process, which selectively heats only the Pb-free BGAs.

The key advantage of the two-stage assembly process is the integrity and reliability of both SnPb and Pb-free components remain intact, since they experience only the profiles for which they are designed. The disadvantages of this method are:

- Some component fabricators may void their component warranties.
- Processing will require additional resources.
- Overall process lead time may increase.
- The assembler will need selective soldering capability (hot-air repair tool or selective laser soldering system) in house.

In addition, the potential impact of higher process temperatures to the printed board and adjacent component should be considered.

4.2.4.2 Mixed-Eutectic and Near-Eutectic Solder Processing Another alternate to reballing is to use a hot (compromise) reflow profile during the SnPb soldering process to create a mixed-metallurgy solder joint. This process may result in a fully mixed (homogeneous) solder joint or a segregated one, depending on the parameters of the reflow profile and relative volumes of solder alloys. SnPb solder paste materials are typically eutectic, requiring a maximum profile temperature of ~ 220 °C to coalesce and complete the joining process. The typical Pb-free solder reflow, however, requires a temperature range of 235 °C to 245 °C to ensure uniform alloy fusion, well above the 220 °C SnPb solder process reflow profile limit. Some high-performance product design teams have conducted testing and worked with their component fabricators to develop acceptable hot reflow profiles that do not introduce component integrity concerns.

Although component materials are generally robust enough to withstand the extended temperature spike, some component fabricators may void their component warranties if the assembly process temperature exceeds 220 °C.

The advantages of using a hot profile are minimal process parameters changes and low cycle time impact. The disadvantages of using a hot profile are the time and costs associated with the additional due diligence reliability testing and laborious reflow profile generation required to demonstrate component/solder joint integrity acceptability.

Figure 4-5A shows a typical SnPb eutectic solder joint with uniform microstructure. Figure 4B shows a Pb-free solder joint with a mixed-metallurgy microstructure exhibiting segregated regions of Pb-free and SnPb solder.

The main disadvantage of the segregated mixed-alloy microstructure is the solder joint will be compromised, likely requiring the use of an underfill material to physically reinforce the package-to-printed board solder joint interface.

4.2.4.3 Underfill for Mixed-Alloy Soldering The use of an underfill is one methodology for reinforcing Pb-free BGA components assembled using SnPb solder. Underfill material also reduces the impact of mismatch stresses (due to CTE differences) on the solder joints by directly coupling the BGA component to the printed board.

Advantages of using an underfill are reduced costs and greater availability of standard Pb-free-configured BGAs. Disadvantages of using an underfill are the materials cost and time associated with dispensing and curing the material. Furthermore, if the underfill formulation is not reworkable, the printed board assembly becomes nonrepairable (see IPC-SM-817 and J-STD-030 for guidance).

4.3 Standardization

4.3.1 Industry Standards for BGAs BGA packaging standardization considers several physical variables including the diameter of the individual ball and the positional accuracy of the ball in relationship to a true position within the component outline.

For more detail regarding package variation, mechanical feature dimensions and allowable physical tolerances, refer to the JEDEC guidelines for BGA packaging described in 4.3.1.1 through 4.3.1.4.

4.3.1.1 BGA Package JEP95, Section 4.14 defines a BGA and CGA family. A BGA or CGA is a square or rectangular 1.5-mm-pitch, 1.27-mm-pitch and sub-1-mm-pitch package with an array of metallic balls or columns on the underside of the package. The main body of the package has a metallized circuit pattern applied to a dielectric structure. Semiconductor die are attached to either the top or bottom surface of this package body. An array pattern of metallized balls/columns on the underside of the dielectric forms the mechanical and electrical connection from the package body to a mating feature (e.g., printed board). The surface that contains the die may be encapsulated by various techniques to protect the semiconductor.

4.3.1.2 Fine-Pitch BGA (FBGA) Package JEP95, Section 4.5 defines an FBGA package as a reduced-pitch (< 1 mm) version of a BGA package. The carrier body of the package has a metallized circuit pattern applied to a dielectric structure. One or more semiconductor devices are attached to either the top or bottom surface of this dielectric carrier.

On the underside of the dielectric carrier is an array pattern of metallized balls which form the mechanical and electrical connection from the package body to a mating feature (e.g., printed board). The surface that contains the die may be encapsulated by various techniques to protect the semiconductor. The requirements for a square FBGA package family allows three optional contact pitch variations (0.5 mm, 0.65 mm and 0.8 mm) and defines four device profile (height) variations. Additionally, a 0.75-mm contact pitch has been included on the die-size BGA (DSBGA) package guideline, which provides four pitch variations for the die-size device family.

The total profile height of the FBGA (measured from the seating plane to the top of the component) is > 1.7 mm. The low-profile fine-pitch BGA (LFBGA) is a reduced-height version of an FBGA. The total profile height of LFBGAs is ≤ 1.2 mm, as measured from the seating plane to the top of the component. Thin-profile fine-pitch BGA (TFBGA) is a reduced-height version of an FBGA, with a total profile height of ≤ 1 mm, as measured from the seating plane to the top of the component. Very-thin-profile fine-pitch BGA (VFBGA) is a reduced-height version of an FBGA with a total profile height ≤ 0.8 mm, as measured from the seating plane to the top of the component.

The JEDEC design guide for FBGA allows the manufacturer the option to increase ball diameter as the spacing or pitch between ball contact centers increase, as compared in Table 4-1. The JEDEC FBGA and fine-pitch reeling guide.

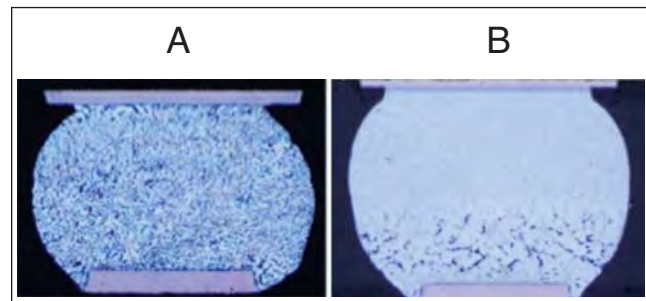


Figure 4-5 BGA Solder Joints Using SnPb – (A) and Mixed-Metallurgy (B) (Pb-Free Alloy in a SnPb Process) With Partially Mixed SnPb in a SAC Ball

(FRBGA) design guide does not support 0.75-mm pitch BGAs; however, the industry has registered some nonconforming parts with that pitch, but they are not JEDEC packages.

Table 4-1 JEDEC Standard JEP95-1/5 Allowable Ball Diameter Variations for FBGA

Ball Pitch (mm)	Ball Diameter (mm)		
	Min	Nom	Max
0.30	Not defined in JEP95-1/5		
0.40	0.20	0.25	0.30
0.50	0.25	0.30	0.35
0.65	0.25	0.30	0.35
0.65	0.35	0.40	0.45
0.80	0.25	0.30	0.35
0.80	0.35	0.40	0.45
0.80	0.45	0.50	0.55

The larger ball diameter option has been allowed to accommodate packages using rigid interposer structures. The larger diameter ball may compensate to a degree, for the wide mismatch of CTE between the silicon die and the rigid printed board structure.

4.3.1.3 Fine-Pitch Rectangular BGA (FRBGA) Package JEP95, Section 4.6 defines a FRBGA, which has an array of metallic balls on the underside of the package. The substrate or carrier of the package has a rectangular shape with a metallized circuit pattern applied to one or both sides of a dielectric structure. Generally described with the same general terms noted in JEP95, Section 4.5, the body size for an FRBGA is defined by the D and E dimensions. Dimension D is the size of the body when measured parallel to the major axis of the package, and dimension E is the size measured parallel to the minor axis. For rectangular packages, D will have a larger value than E.

4.3.1.4 Die-Size BGA (DSBGA) Package JEDEC Publication JEP95, Section 4.7 defines a DSBGA. A DSBGA has an array of metallic balls on the underside of the package. The substrate or carrier of the package may have a square or rectangular shape with a metallized circuit pattern applied to either or both sides of a dielectric structure. The semiconductor die is attached to the top surface of this dielectric carrier.

On the underside of the dielectric, the array pattern of metallized balls provides the mechanical and electrical connection from the package body to the next-level component (e.g., a printed board). The surface to which the die is attached may be encapsulated by various techniques to protect the semiconductor. The size of the substrate or carrier is as close to the die size as practically possible.

A DSBGA is a type of BGA package in which the body size is defined to coincide as closely as possible with a specific die size. This package is sometimes called a real-chip-size BGA or chip scale package (CSP). The dimensions of the package body accommodate assembly only of a die with a specific size; these body dimensions will change because of changes in die size. The outline of the package may be square or rectangular, but this aspect ratio may also change as a given package is redesigned to conform to a new die size. The aspect ratio will likely differ for devices of the same functionality from multiple suppliers. The controlling factor for the standardization of DSBGA packages is the size and aspect ratio of the ball array.

The D and E dimensions define the body size of a DSBGA package. For packages with a rectangular ball matrix, the matrix determines the orientation of the dimensions. Dimension D is the body size measured parallel to the major axis of the ball matrix; dimension E is the body size measured parallel to the minor axis of the ball matrix. For rectangular packages, D will not necessarily have a larger value than E, as would be the case for an FRBGA package per JEP95, Section 4.6. A DSBGA package with a square ball matrix should follow the usual JEDEC convention, in which D is greater than E. The maximum values for both D and E are defined in JEDEC 95 using 0.5-mm increments. The values are determined by rounding the actual DSBGA body size upward to the next 0.5-mm boundary. Therefore, when using this procedure, D and E values have the form y.00 or y.50.

The array pitch for a DSBGA package will not necessarily be equal for the D and E matrix dimensions. When the pitches are not equal, ball dimensions and tolerances for the smaller of the two pitches will govern the definition of related package dimensions and tolerances. The controlling pitch of the array of balls on a DSBGA package is always < 1 mm. The contact pitch variations for the DSBGA described in JEP95, Section 4.7, are 0.8 mm, 0.75 mm, 0.65 mm, and 0.5 mm.

4.3.2 BGA Package Pitch BGAs are divided into two groups of pitches. The first group includes plastic and ceramic package outlines, which allow 1.5-mm, 1.27-mm and 1-mm contact pitch variations. The second group is designated as fine-pitch which allow ball contact pitch variations of 0.8 mm, 0.75 mm, 0.65 mm, 0.5 mm, 0.4 mm, 0.3 mm and 0.25 mm for DSBGAs. Few component manufacturers are currently providing parts with 1.5-mm pitch, because the pressure is on form factor to keep BGAs as small as possible. Although ball pitch ≤ 0.4 mm is allowed, the applications may be limited for conventional SMT assembly due to difficulty in processing. Pitch plays a large role in the determination of which ball diameters can be used in various combinations. Table 4-2 shows the characteristics of balls that are used with pitches of 0.5 mm through 1.5 mm for plastic BGAs (PBGAs), while Table 4-3 shows the pitches for DSBGAs.

Table 4-2 Ball Diameter Sizes for Plastic BGAs (PBGAs)

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.75	0.90 to 0.65	1.5, 1.27
0.60	0.70 to 0.50	1.0
0.50	0.55 to 0.45	1.0, 0.8
0.45	0.50 to 0.40	1.0, 0.8, 0.75
0.40	0.45 to 0.35	0.8, 0.75, 0.65
0.30	0.35 to 0.25	0.8, 0.75, 0.65, 0.5

Although not mandatory, nonsymmetrical ball patterns have the added advantage of enabling automated orientation detection during assembly. One example is to omit one of the corner balls in an otherwise symmetrical array.

Table 4-3 Ball Diameter Sizes for Die-Size BGAs (DSBGAs)

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.25	0.28 to 0.22	0.4
0.20	0.22 to 0.18	0.3
0.15	0.17 to 0.13	0.25

4.3.2.1 Land Pattern Design The land pattern of the component substrate (where the ball is attached) and the land pattern of the mounting structure (e.g., printed board) should be as similar in diameter as possible. Component manufacturers have determined that the printed board land pattern or the land on the component should be slightly less than the ball diameter. The amount of reduction is based on the original ball size, which is used to determine the average land. In determining the relationship between nominal characteristics, a manufacturing allowance for land size has been determined to be 0.1 mm between the maximum material condition (MMC) and least material condition (LMC) for ball diameters ≥ 0.4 mm and less for balls < 0.4 mm.

Table 4-4 provides data on BGA land patterns and their variation to accommodate nine ball diameters.

Table 4-4 Land Pattern Design

Nominal Ball Diameter (mm)	Reduction	Nominal Land Diameter (mm)	Land Variation (mm)
0.75	25 %	0.55	0.60 to 0.50
0.60	25 %	0.45	0.50 to 0.40
0.50	20 %	0.40	0.45 to 0.35
0.45	20 %	0.35	0.40 to 0.30
0.40	20 %	0.30	0.35 to 0.25
0.30	20 %	0.25	0.25 to 0.20
0.25	20 %	0.20	0.20 to 0.17
0.20	15 %	0.15	0.15 to 0.12
0.15	15 %	0.10	0.10 to 0.08

Many component manufacturers use SMD lands (see 6.2.2). When this technique is used, the nominal land diameter should be increased by the amount of solder mask encroachment on the land (usually ~ 0.1 mm). The opening in the solder mask window then represents the diameter to which the ball will become attached, while the actual land is slightly larger to accommodate the SMD land concepts. It should be noted that routing density is decreased, since the land is larger.

4.3.3 BGA Package Outline

BGA body sizes are divided into two outline groups: square and rectangular.

The square outline package family size ranges from as small as 4 mm × 4 mm to as large as 50 mm × 50 mm. In fine-pitch variations package sizes increase in 1-mm increments. In ranges larger than 21 mm × 21 mm, the body size increase in increments of 2 mm to 2.5 mm, and pitches are in the regular range. Rarely will any of the fine-pitch parts be found in sizes > 21 mm × 21 mm.

The rectangular BGA family has the same size ranges from 4 mm to 50 mm but varies by each application. This group can have many more variations than the square group. Rectangular sizes typically are found to follow no fixed incremental progression. This group is normally driven by the memory applications and closely follows the die sizes. Rectangular sizes are normally standardized in small-application-specific families. FBGA components (≤ 0.8 mm) rarely exceed 21 mm in body size.

FBGAs are 0.5-mm to 0.8-mm pitch solder balled array packages that have fixed package dimensions D and E. Dimension D is the body size measured parallel to the major axis of the ball matrix; dimension E is the body size measured parallel to the minor axis of the ball matrix. The FBGA is more like the plastic and ceramic BGA families, having fixed body dimensions. Although the FBGA outline is typically only 20 % larger than the die, it will not change shape with every die shrink.

DSBGAs are 0.3-mm- to 0.5-mm-pitch solder balled array packages that have variable package dimensions D and E. The DSBGA takes the shape of the die, which normally makes it a rectangular outline. It is widely used in Flash and dynamic random-access memory (DRAM) memory devices. The rectangular die size outline will likely change D and E dimensions with every die shrink.

4.3.4 Ball Size Relationships

The trend toward higher-pin-count ICs and smaller package outlines has enabled companies to improve both product functionality and performance. The total variation of the system considers three major issues:

- 1) Positioning
- 2) Ball tolerance
- 3) Substrate tolerance

All three attributes added together result in a worst-case analysis; however, as with other land patterns, a statistical average is determined by using the root mean square (RMS) value.

Table 4-5 assists the user in calculating variations in land pattern geometry for a wide range of BGA applications. It also shows the total variation in the system for each of the nine ball sizes. As noted, the standard nominal dimension for ball contact diameters are 0.15 mm, 0.2 mm, 0.25 mm, 0.3 mm, 0.4 mm, 0.45 mm, 0.5 mm, 0.6 mm and 0.75 mm. Ball contact size for array packages are influenced by the limit established for overall package height, ball contact pitch and the desire to maximize solder joint reliability.

Table 4-5 Land-to-Ball Calculations for BGA Packages (mm)

Land Size		Location Allowance	Ball Variation	Ball Size			% Reduction from Nom.	Variation Allowance
MMC	LMC			Nominal	MMC	LMC		
0.60	0.50	0.10	0.25	0.75	0.90	0.65	25 %	0.25
0.50	0.40	0.10	0.20	0.60	0.70	0.50	25 %	0.20
0.45	0.35	0.10	0.10	0.50	0.55	0.45	20 %	0.17
0.40	0.30	0.10	0.10	0.45	0.50	0.40	20 %	0.17
0.35	0.25	0.10	0.10	0.40	0.45	0.35	20 %	0.17
0.25	0.20	0.05	0.10	0.30	0.35	0.25	20 %	0.15
0.20	0.17	0.05	0.06	0.25	0.28	0.22	20 %	0.08
0.15	0.12	0.05	0.04	0.20	0.22	0.18	15 %	0.07
0.10	0.08	0.05	0.04	0.15	0.17	0.13	15 %	0.07

4.3.5 Package-on-Package (PoP) BGA PoP innovations are proving to be preferred for a broad range of SiP applications and addressing spatial constraints. User companies have realized that complex mixed-technology functions can be produced with higher yield and more economically if the semiconductors are individually prepackaged and tested before joining. The most common solution for PoP applications utilizes package sections designed around the existing JEDEC FBGA standard array packaging format (see Figure 4-6). Stacking prepackaged die has less risk because the individual packages are fully tested before conversion to the stacked PoP format.

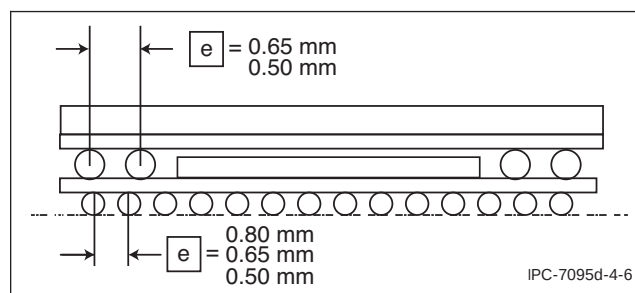


Figure 4-6 JEDEC Standard Format for Package-on-Package Components

Source: JEDEC Publication 95-4.22

The decision to join one package to another before or during board-level assembly may be influenced by the requirement for in-process configuration flexibility. For example, the base package can be furnished by one vendor, while the memory sections of the stack are supplied by one to three other vendors. This is because memory functions are available from a greater number of sources, and the testing for memory is somewhat specialized. Furthermore, the concern of ownership of total quality and reliability can be alleviated.

Logic device suppliers are responsible for the logic. Memory manufacturers are responsible for the respective memory. Printed board assemblers are responsible for only the surface-mount attachment of the two. This alternative has two benefits. It allows the user to specify multiple variations (e.g., different memory functions, data rate, etc.) as well as accommodating secondary sources of supply.

4.3.6 Coplanarity A critical issue in SMT packages is the limits for coplanarity of the contacts. The coplanarity requirements in a BGA package are very different from other lead-frame packaged SMT components. Coplanarity for any BGA is the distance of component contact surface above a common seating plane. Noncoplanarity, a simplified term, is the maximum distance between the lowest and the highest contact when the package rests on a perfectly flat surface. This definition represents a package sitting on a printed board on at least three locations.

Coplanarity tolerance defines the distance from the seating plane to the highest point of the package. This dimension includes the stand-off height, package body thickness and (if present) lid thickness. The measurement criteria do not include attached features such as heat sinks or other components. An integral heat slug, however, is not considered an attached feature. If the package happens to be a laminate-substrate-based BGA, additional coplanarity issues can be expected due to problems associated with adapting larger substrates and maintaining flatness within the tolerances. This, in part, is the reason why the PBGA package coplanarity requirement is established at 150 μm . Most suppliers would like the allowable BGA coplanarity limit to be $\sim 200 \mu\text{m}$, but users prefer the maximum to be $\leq 100 \mu\text{m}$ (see 4.6.2.6 and 4.8.4). There are different coplanarity requirements for different types of BGAs. Table 4-6 shows a sampling of JEDEC-registered BGA package outlines.

Table 4-6 Examples of JEDEC-Registered BGA Outlines

Registered Outline	Package Type	Coplanarity
MO-151	PBGA	0.20 mm
MO-156/MO-157	CBGA	0.15 mm
MO-195	FBGA	0.08 mm

Coplanarity values may vary from JEDEC outline to outline because of the ball metallurgy. In low-temperature, eutectic solder balls (183 $^{\circ}\text{C}$ melting point), balls collapse during the assembly operation; therefore, the coplanarity requirement is not as tight as a high-temperature solder ball (302 $^{\circ}\text{C}$ melting point) in which the balls do not collapse during the assembly operation.

While coplanarity can act as an indicator of SMT attachment capability, the transient behavior of BGAs that takes place during reflow processing can affect SMT placement yield. Hence, accept/reject guidelines should consider both room-temperature and high-temperature coplanarity responses using JESD22-B108 and JESD22-B112, respectively. A device that appears to be nonconforming at room temperature may produce yield results that meet manufacturer's yield metrics.

4.4 Component Packaging Style Considerations JEDEC design guidelines for BGAs do not define specific materials or methods of assembly. Base materials will vary from one supplier to another depending on application. The base structure is most likely reinforced organic laminate, nonreinforced polyimide film or ceramic. Ceramic-based BGA packages are often supplied with noncollapsing solder balls made of high-temperature solder (SnPb10) with a melting point of 302 $^{\circ}\text{C}$.

BGA connectors typically utilize a liquid crystal polymer resin for the housing due to its temperature capability and flatness characteristics. Ball size will vary with pitch and package size. Larger packages will usually have larger ball sizes, which improve reliability. Since the ceramic package is relatively very flat and tolerances in ball diameters are very narrow, coplanarity requirements can be relatively narrow as well. The supplier of the ceramic-based package will generally furnish recommendations for selecting a suitable solder paste composition for board-level assembly.

4.4.1 Solder Ball Alloys Solder ball composition is defined by the overall printed board assembly technology (e.g., SnPb or Pb-free) and the package type (e.g., ceramic or laminate substrate). The alloy composition selected for balls on reinforced-laminate- and polyimide-film-based BGAs can vary widely. Many are furnished with a SnPb eutectic solder having a melting (liquidus) point of 183 °C (179 °C for eutectic solder with 2% Ag). The balls are commonly applied to the package substrate using only flux and a reflow soldering temperature of 215 °C to 220 °C to complete the joining process.

Component manufacturers should establish a method to clearly identify the metallurgy of the solder alloy used for BGA balls, accompanied by a part number change. J-STD-609 provides a convenient method for identifying the BGA ball alloy. Users may choose to verify the BGA alloy using screening methods such as X-ray fluorescence.

4.4.1.1 SnPb Alloys Although not in wide use for most commercial applications, SnPb alloys can be adapted for both solder ball and solder joining materials. One common alloy composition is SnPb37 eutectic, with a liquidus temperature of 183 °C. The eutectic Ag alloy composition, SnPb36Ag2, has a liquidus temperature of 179 °C and is an acceptable alternative to eutectic SnPb37. Ceramic BGAs, when used in SnPb technology, often employ a high-Pb alloy of PbSn10 composition to provide the required solder joint reliability. This alloy does not melt during the SnPb reflow process, but when it is attached to the printed board with eutectic SnPb37 it provides a reliable interconnect.

4.4.1.2 Pb-Free Alloys In compliance with the RoHS directive, companies manufacturing electrical and electronic assemblies and electrical components must use Pb-free materials for ball contacts and package-to-substrate joining. Although many Pb-free alloy compositions are available, most manufacturers have adopted Sn as the primary element and include Ag or a combination of Ag and Cu to the Sn alloy.

Typical Pb-free alloy compositions include SnAg3Cu0.5 (SAC305), SnAg3.8Cu0.7 (SAC387) or SnAg4Cu0.5 (SAC405). These solders have liquidus temperatures in the range of 217 °C to 227 °C and require peak reflow temperatures from 240 °C to 260 °C, depending on the overall mass of the assembly being processed. Depending on the specific alloy composition, the liquidus point of the solder ball can vary by as much as 10 °C (see Table 4-7).

Table 4-7 Pb-Free Alloy Variations

Composition	Alloy	Liquidus Temperature	Reflow Temperature
SnAg3.5	SnAg	221 °C	240 °C to 250 °C
SnCu0.7	SnCu	227 °C	245 °C to 255 °C
SnAg4.7Cu1.7	SnAgCu*	216 °C	237 °C to 247 °C
SnAg4Cu1	SnAgCu*	218 °C	238 °C to 248 °C
SnAg3Cu0.5	SnAgCu*	218 °C	238 °C to 248 °C
SnAg4Cu0.5	SnAgCu	218 °C	238 °C to 248 °C
SnAg3.8Cu0.7	SnAgCu	218 °C	238 °C to 248 °C
SnAg3.2Cu0.5	SnAgCu	218 °C	238 °C to 248 °C
SnAg3.5Cu0.75	SnAgCu*	218 °C	238 °C to 248 °C

* May be covered by patents

Within the SnAgCu (SAC) system, addition of other alloying elements can affect solder under-cooling, formation of various intermetallics, unusual matrix properties and changes in solder microstructure. Great care must be taken when introducing new alloys into BGAs and new alloyed BGAs into the assembly process. Outside the SAC system, various alloy systems containing Bi, In, Sb or Zn have been developed. The underlying metallurgy of each system differs, which drives the physical properties and mechanical behavior, which then affects assembly process parameters and solder joint reliability.

4.4.1.3 Low-Temperature Solders

4.4.1.3.1 Drivers for Low-Temperature Solders There are three drivers for using low-temperature solders:

- 1) **Economic** – Using lower-melting-temperature solders can result in considerable energy savings due to lower peak reflow soldering temperatures. These cost savings result primarily from the smaller current draw required to operate the ovens during reflow. This is a direct result of the temperatures of the oven zones being set to a lower value.

- 2) Environmental – Using lower-temperature solders decreases greenhouse gas production and reduces the impact of the product lifecycle on the environment.
- 3) Solder joint yield improvement – Increasing demand for consumer products (e.g., smart phones and wearables) has fostered the need for light-weight, ultra-thin electronic packages which still require high performance.

Reduction in package thickness creates new challenges for reflow soldering assembly. CTE mismatches among materials used in these electronic packages results in warpage increases when using SAC reflow temperatures. This warpage leads to yield-lowering defects such as HoP, NWO and solder bridging.

Reducing the peak reflow temperature improves the SMT solder joint yield margin, particularly for BGA solder joints, by reducing the package's dynamic warpage and keeping the ball and paste in contact during reflow.

Figure 4-7 shows dynamic warpage of a flip chip BGA package over a temperature range of 25 °C to 260 °C. In the 160 °C to 180 °C range (peak reflow temperature range for SnBi solder pastes), the package warpage is 30 % to 50 % lower than at ~ 260 °C, which is near the peak reflow temperature for SAC solder pastes.

4.4.1.3.2 Choice of Low-Temperature Solder Alloys The solder alloy(s) chosen for use in low temperature soldering have a boundary on their liquidus temperatures on the high and low ends. If the liquidus temperature is too high, most benefits of low-temperature solders will not be realized. Conversely, the liquidus temperature should be higher than the operating temperatures in the field for products in which low-temperature solder is used.

Figure 4-8 shows low-temperature solder alloy systems (SnBi, SnIn, SnZn and In) with a liquidus ~ 100 °C to 200 °C and which do not contain Pb or Cd (excluded for environmental reasons) and Au (excluded for economic reasons). These alloys can be eutectic or off-eutectic (hypoeutectic or hypereutectic with respect to their main elemental ingredient). Off-eutectic compositions typically have a melting range between the solidus and liquidus temperatures (also called a pasty range). They could also have additional elements added to them to impart certain desirable properties (i.e., reduction of liquidus temperatures).

4.4.1.4 SnBi Solder Alloy System The mobile computer market uses SnBi systems because of the familiarity with this solder system in high-volume manufacturing. It has been used for several years in TVs, white goods and LED products because certain ingredient components cannot withstand higher reflow temperatures incumbent to using current Pb-free solders such as those in the SAC alloy system.

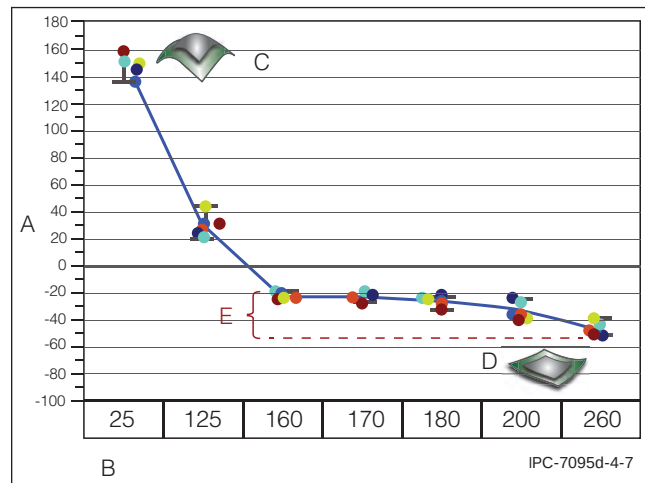


Figure 4-7 Dynamic Warpage Plot with Temperature for a Flip Chip BGA Package

A – Dynamic warpage (μm)
B – Temperature
C – Convex (+) warpage
D – Concave (-) warpage
E – ~ 30 % to 50 % reduction

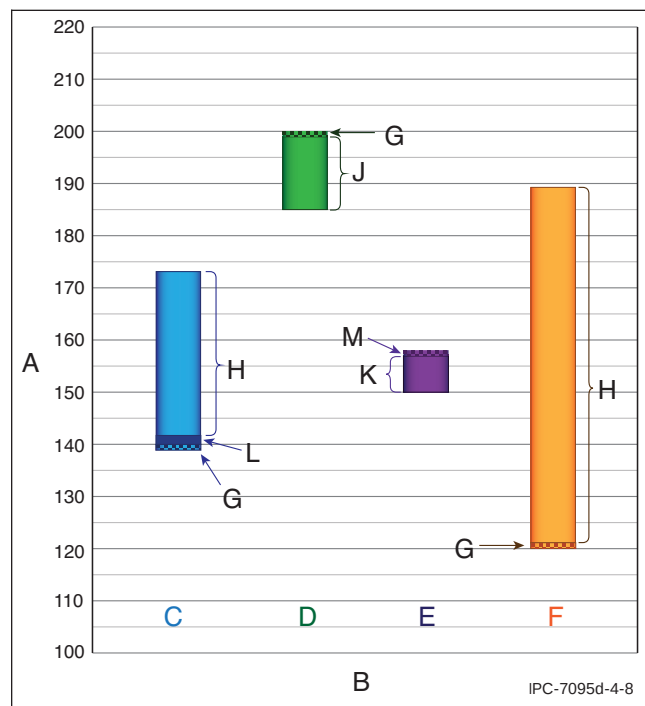


Figure 4-8 Low-Temperature Alloys with Liquidus Temperatures Between 100 °C and 200 °C and Which Do Not Contain Pb, Cd or Au

A – Liquidus temperature (°C)
B – Alloy system
C – BiSn
D – SnZn
E – In
F – InSn
G – Eutectic
H – Off-eutectic alloys
J – Alloys with Bi and In
K – Alloys with Bi
L – BiSnAg
M – In metal

Figure 4-9 shows a phase diagram for a SnBi alloy system. As is apparent, this phase diagram is very similar to the SnPb phase diagram; the eutectic composition is BiSn42. The phase diagram indicates hypoeutectic and hypereutectic compositions and their pasty range. See IPC-7530 for information on phase diagrams.

Figure 4-10 illustrates the typical microstructure for SnBi solders. This microstructure is also very similar to that of SnPb solders. It is a two-phase mixture, with the darker phases being Sn rich and the lighter phases being Bi rich. Depending on the cooling rate of the solder joints, the phase morphology can be lamellar, nodular or a mixture of the two.

This SnBi alloy system has drawbacks. Solder joints made with eutectic SnBi solders are prone to failures when subjected to mechanical and drop shock forces. This is primarily due to the inherent brittleness of the Bi phase within the microstructure. Bi has a rhombohedral crystal structure that has very few slip planes for dislocation movement. The larger the number of slip planes available for dislocation motion, the higher the ductility of the material.

The market segment initially targeting low-temperature SnBi solders has a high risk for its products being dropped when in use (i.e., dropped mobile device). Therefore, to lower the risk of solder joint failures under mechanical shock and drop, two pathways for solder joint enhancement have been investigated:

- 1) Enhancing the ductility of the basic SnBi solder alloy
- 2) Use of polymeric reinforcement of the solder joints

4.4.1.4.1 Ductility Enhancement of SnBi Solders Multiple strategies are being implemented to improve the ductility of SnBi solders. These include:

- Decreasing the Bi content in the solder alloy. This decrease reduces the volume of the brittle phase (Bi) and increases the volume of the ductile phase (Sn) in the solder.
- Strengthening the Sn phase by adding specific elements to the solder. This is termed solid-solution strengthening.
- Strengthening the Sn phase by adding specific elements that precipitate out into the microstructure. This is termed precipitation hardening.
- Refining the microstructure (grain size or morphology) by adding specific elements in small concentrations. These effects change the deformation mechanism within the solder from the classic dislocation slip to cooperative grain boundary sliding. Adding these elements also reduced the segregation of the Bi at the solder-termination interfacial regions through which brittle cracks predominantly propagate.
- Modifying the Bi phase by alloying with other element(s). This modification makes the Bi-containing phase less brittle.

4.4.1.4.2 Polymeric Reinforcement of SnBi Solder Joints Polymeric reinforcement of SnBi solder joints use cured polymeric materials (e.g., epoxy) as an external reinforcement. This external reinforcement strengthens the solder joints by lowering the risk of crack formation and propagation within the solder when mechanical shock forces are applied to the assembly.

These polymeric reinforcements are used for BGAs and other area array component solder joints in the form of board-level underfills. One major detriment of underfills in high-volume manufacturing is that they adversely affect throughout time

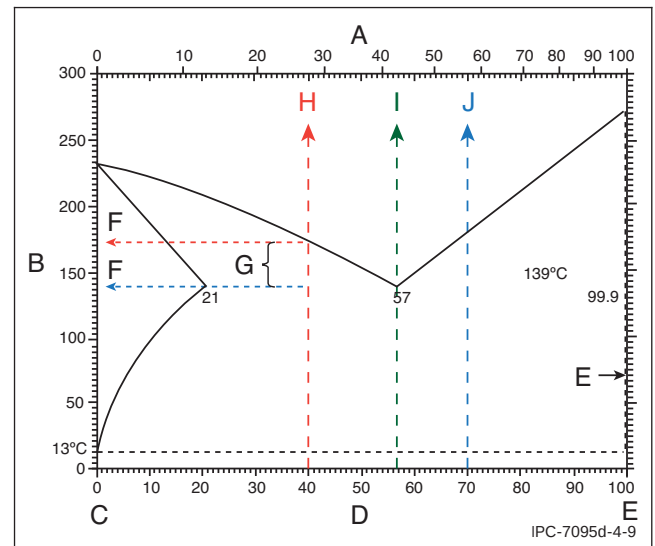


Figure 4-9 SnBi Phase Diagram

A – Atomic % Bi
B – Temperature (°C)
C – Sn
D – Weight percent Bi
E – Bi
F – T_m
G – Pasty range
H – Hypoeutectic
I – Eutectic
J – Hypereutectic

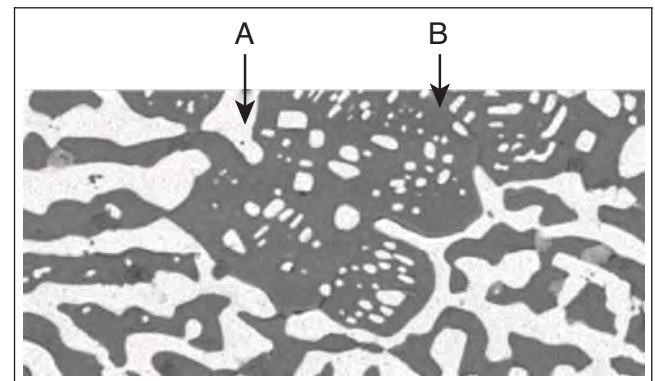


Figure 4-10 Typical Microstructure of SnBi Solder Alloy

A – Bi
B – Sn

This is because underfills first must be dispensed at specific locations where the BGAs are present after the board has been reflow soldered, and then they must be cured in a subsequent step. Energy expenditure of the curing ovens is another detriment for the underfill process.

An alternative polymeric option for strengthening SnBi solder joints is to use low-temperature resin-containing solder pastes, also known as joint reinforced pastes (JRP). These solder pastes contain an uncured resin within their flux component. During the reflow process, when the solder paste melts, this resin is displaced away from the molten solder and externally coats the molten solder. As the reflow process proceeds, the molten solder wets the metallic terminations, followed by gelling and curing of the resin component within the flux. After reflow, the cured resin forms a fillet around the solder joints, providing the necessary mechanical reinforcement. The JRP process essentially creates a partial underfill of BGAs during the reflow process without the need for additional dispensing and curing steps.

4.4.2 Ball Attach Process The package substrate is typically fabricated in a strip format containing multiple packages (see Figure 4-11). Ball contact placement is performed after the balls have gone through wire bonding and plastic molding or encapsulation processing. Both automated and semiautomated ball placement is being utilized for volume BGA assembly. Alloy spheres of the desired size (see Table 4-1) are attached by gang placement machines, individually placed using automated systems or dispensed in mass with a stencil-like fixture. For companies doing development or for low-volume placement, a simple template fixture can be provided for precise ball positioning.

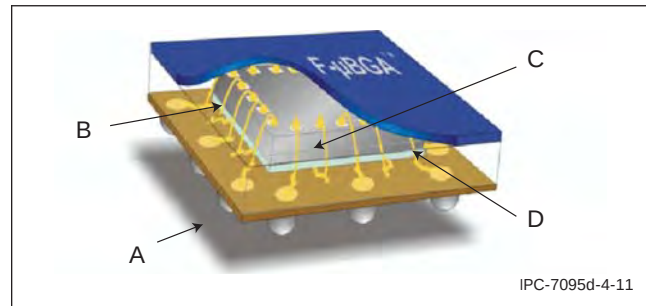


Figure 4-11 Plastic Ball Grid Array (PBGA) Package
 A – Package substrate
 B – Die
 C – Wire bond
 D – Package substrate

The overall ball attachment process, however, is the same. To begin, solder paste or flux is applied onto the contact pattern. The solder paste or flux holds the balls in place during reflow soldering. Reflow soldering of the ball to the substrate is often performed in a nitrogen gas environment. The nitrogen gas environment helps provide consistent ball quality and keeps the surface from oxidizing during reflow; however, nitrogen gas may not be necessary for reflow attachment of the package to the printed board. Eutectic solder balls provide a controlled collapse which during reflow soldering promotes self-alignment (compensating for some misplacement during assembly).

There are some issues to consider when using PBGAs. The first is moisture sensitivity. Moisture-sensitive components around other components being removed and replaced during rework must be dried in advance and/or protected from the heat of the rework activity. If the plastic-cased BGA is to be reused, special care will be required to reball the BGA after the package is detached from the printed board assembly. Moisture sensitivity is not the case with high-melting-point non-collapsing balls used on CBGAs, and the balls do not melt during rework.

The PBGA is also susceptible to warpage when exposed to temperatures required for solder attachment. The edges of the package tend to lift up or curve down during reflow soldering and can severely disturb or interrupt the electrical interface between package and printed board assembly. Larger packages are even more susceptible to warpage than smaller packages. Package warpage is caused by CTE mismatch between the substrate structure, the mold compound and the silicon die inside. This problem may become more acute when the die is large or when the BGA has a heat spreader.

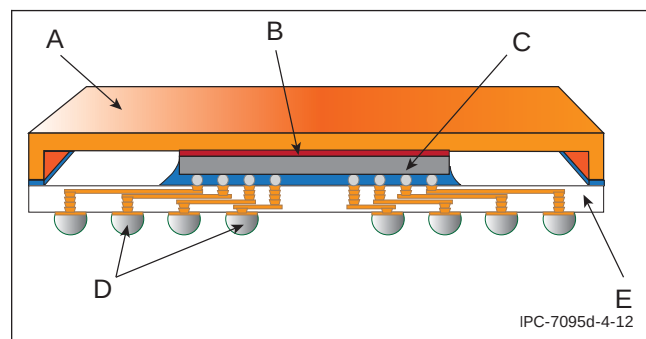


Figure 4-12 Cross-Section of a Thermally Enhanced Ceramic Ball Grid Array (CBGA) Package
 A – Metal alloy heat spreader
 B – Thermal interface material
 C – Flip chip semiconductor chip
 D – Solder balls
 E – Ceramic alumina substrate base

4.4.3 Ceramic Ball Grid Array (CBGA) Internal connections in ceramic-based packages can be wire bond or flip chip. Figure 4-12 shows flip chip bonding inside the package. The package can be furnished with the die mounted on the top surface of the substrate (cavity up) or with the die mounted to the substrate's lower surface (cavity down). The solder balls

generally used for ceramic packages typical of that illustrated in Figure 4-13 are a high-temperature alloy composition (SnPb10) with a melting point of 302 °C. The ball attachment alloy, however, may be a eutectic solder (SnPb37).

Although polymer encapsulation (over-molding) is widely used to encase the die area, some CBGAs are hermetic (do not absorb moisture). Since solder balls adapted for these products often have a high melting point, they do not collapse during rework. The disadvantage of CBGAs is that their high thermal mass will be slightly different than plastic-packaged ICs and can make solder reflow profile development more difficult. Because of the CTE mismatch between the ceramic-based package and the printed board, solder joints may need to be physically reinforced. After soldering and cleaning, it is a common practice to apply an epoxy-based underfill between ceramic substrate interposer and organic printed board materials.

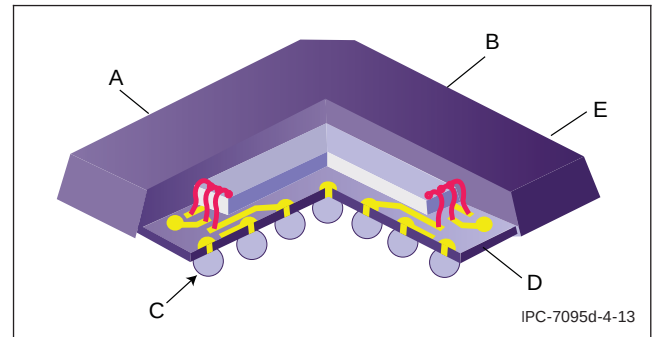


Figure 4-13 Ceramic Ball Grid Array (CBGA) Package with Molded Polymer Encapsulation

- A – Encapsulant
- B – Chip
- C – Solder ball (Pb-free)
- D – Ceramic substrate (double-sided)
- E – Bonding wire

4.4.4 Ceramic Column Grid Arrays (CCGAs) Solder columns are noncollapsible surface-mountable interconnects for large ceramic IC packages (21 mm to 52.5 mm). CCGAs are typically 1-mm and 1.27-mm pitch. Experimentation in industry indicates it is feasible to support solder columns for narrower-pitch CCGA components, down to 0.8 mm and eventually smaller pitches.

Solder columns absorb more extreme CTE mismatch between the IC package and the printed board. CTE mismatch is pervasive due to joining materials of different properties in IC packages and the printed board. The CTE mismatch differential between a ceramic IC package and a printed board is roughly 10 ppm/°C in the x/y-axis, rising above 50 ppm/°C in the z axis as temperatures exceed the T_g rating of the printed board. As the IC package increases in size, the differentials of CTE mismatch become more significant, especially when the package experiences repeated wide temperature cycles from -40 °C to 125 °C. Stress due to an extreme CTE mismatch often results in solder joint failure and electrical failure between a large CBGA IC package and the printed board.

Solder columns, which are nominally 2.2-mm long (see Figure 4-14) provide more compliancy than solder balls to reduce stress caused by CTE mismatch. Solder columns absorb stress and increase solder joint reliability under harsh operating conditions.

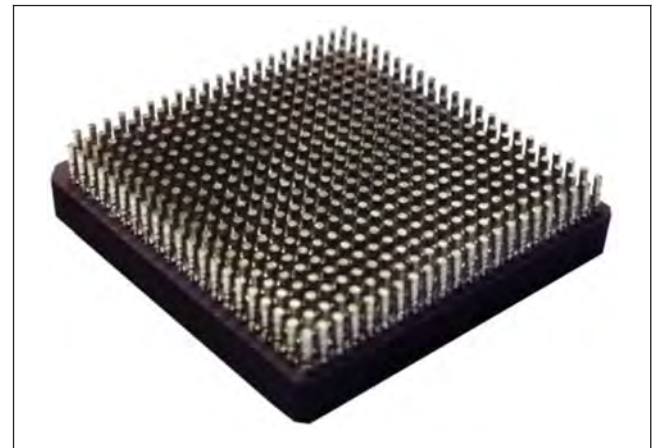


Figure 4-14 Typical Ceramic Column Grid Array (CCGA) With Cu Ribbon Wrap

(Figure source: Source Actel)

Older solder columns constructed of plain PbSn10 wire (or cast) without Cu wrapping may degrade electrical performance, especially at higher frequencies. Columns increase the overall package profile height, as compared to BGA components.

Solder columns are available in a variety of lengths, from 1 mm to 2.54 mm, while the nominal length 2.2 mm tends to be the industry norm. Longer columns (3.81 mm) are useful for raising IC packages with bottom-mounted decoupling capacitors off the printed board.

The diameter of the solder column should be 75 % of the landing pad diameter to allow a proper annular solder fillet to form around both ends of the solder columns after joining the IC package to the printed board. Solder columns are available with diameters as small as 0.2 mm and as large as 0.56 mm (0.89 mm for certain applications). Solder columns with a 0.5-mm diameter tend to be the industry norm for 1-mm- and 1.27-mm-pitch ceramic IC packages. Solder columns with diameters 0.3 mm to 0.38 mm are required for commercial 1-mm-pitch organic substrates (PBGA without solder balls), since many PBGA-style pads have 0.5-mm SMD openings.

While BGAs with SMD pads are not optimal, solder columns have been successfully attached to organic PBGA substrates, as illustrated in Figure 4-15. Solder columns are constructed of high-melting-point solder alloys and do not collapse during reflow of printed boards with eutectic (SnPb37) or SAC Pb-free alloy solder pastes.

Solder columns with high-temperature alloys, including PbSn20, PbSn15 and PbSn10, are available wound with an outer layer of oxygen-free (OFHC-101 or alloy CDA101) Cu. A thin outer layer of Cu ribbon (0.025 mm to 0.05 mm) is spirally wrapped around the column. Columns are coated with eutectic SnPb37 to cover the Cu ribbon and form a lap joint between the Cu to the solder column, as shown in Figure 4-16.

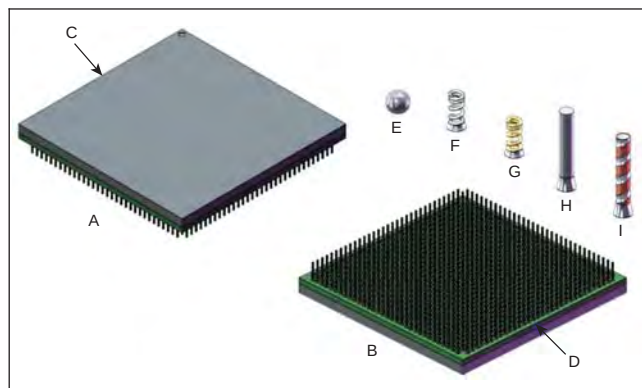


Figure 4-15 Plastic BGA (PBGA) with Variety of Columns
(Figure source: TopLine)

- | | |
|-----------------------|----------------------|
| A – Top view | F – Microcoil (SnPb) |
| B – Pad view | G – Microcoil (NiAu) |
| C – Heat spreader | H – PbSn10 |
| D – Plastic substrate | I – PbSn20 |
| E – Solder ball | |

Solder columns constructed with electroplated Cu over PbSn10 core provide 30 % lower thermal resistance than Cu-wrapped columns to conduct heat away from the bottom of the IC package to the ground plane of the printed board, as illustrated in Figure 4-17.

Microcoil springs, introduced by NASA, provide an alternative to traditional solder columns. The base material is BeCu electroplated with a choice of SnPb40 or SnAu. The Au-plated version provides a Pb-free solution when combined with SAC305 fillets.

Coils are 0.5 mm in diameter by 1.27 mm long (free-load length) for use with 1-mm-pitch ceramic IC packages. A smaller coil with 0.4-mm diameter and 1-mm length is used when attaching to organic PBGA substrates with 0.5-mm-diameter solder-mask-defined pads.



Figure 4-16 Typical Solder Column with Cu Ribbon Wrap
(Figure source: TopLine)

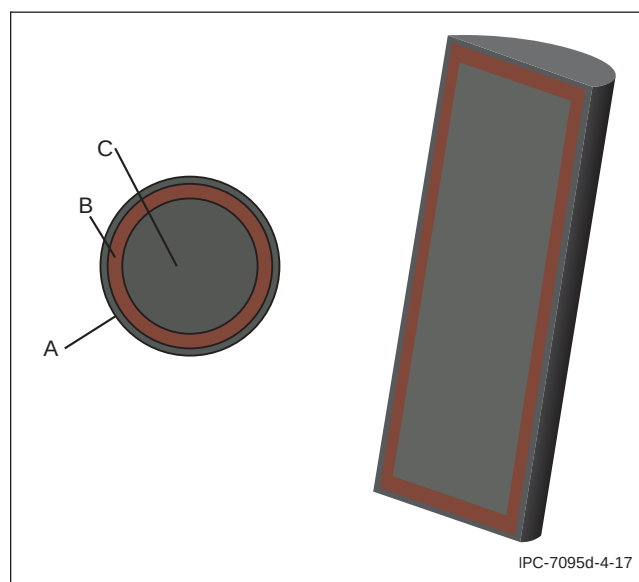


Figure 4-17 Section View of PbSn10 Solder Column with Electroplated Cu Covered with SnPb40 Outer Layer
(Figure source: TopLine)

- | |
|--------------------------------|
| A – Deposited SnPb40 |
| B – Cu plate |
| C – Solder alloy core (PbSn10) |

See Figure 4-18, Figure 4-19, Figure 4-20 and Figure 4-21.



Figure 4-18 SnPb-Plated Microcoil (Left) and Au-Plated Microcoil (Right)

(Figure source: TopLine)

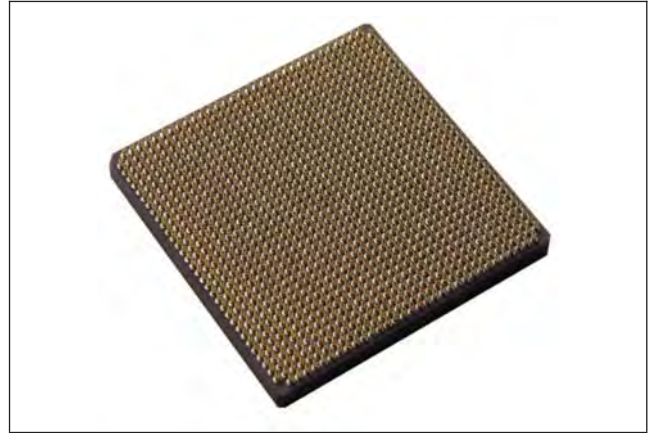


Figure 4-19 Au-Plated Microcoil Spring on Column Grid Array (CGA1152) Ceramic IC Package

(Figure source: TopLine)

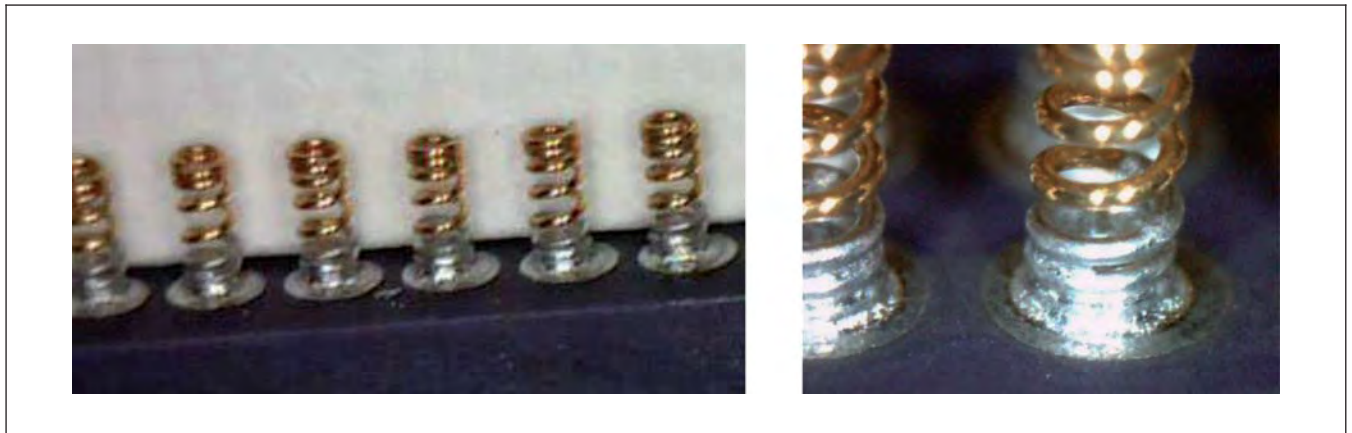


Figure 4-20 Microcoil Spring with SAC305 Fillet on Column Grid Array (CGA) Package

(Figure source: TopLine)

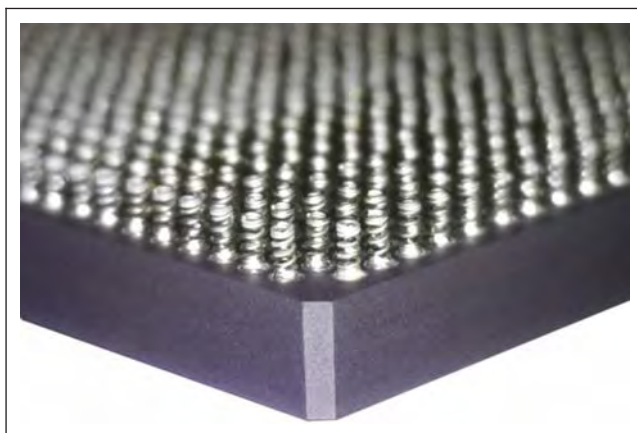


Figure 4-21 Microcoil Spring (Electroplated SnPb40) Column Grid Array (CGA1152) With SnPb37 Fillet

(Figure source: TopLine)

Table 4-8 provides data on land patterns and their variation to accommodate 10 column diameters for CGAs.

Table 4-8 Column Grid Array (CGA) Land Size Approximation

Nominal Column Diameter (mm)	Pad Enlargement	Nominal Land Diameter (mm)	Land Variation (mm)
0.56	33 %	0.75	0.75 to 0.90
0.51	37 %	0.67	0.67 to 0.75
0.40	33 %	0.53	0.53 to 0.67
0.38	33 %	0.50	0.50 to 0.53
0.30	33 %	0.40	0.40 to 0.50
0.25	40 %	0.35	0.35 to 0.40
0.20	40 %	0.28	0.28 to 0.35
0.15	40 %	0.21	0.21 to 0.28
0.125	40 %	0.175	0.175 to 0.21
0.10	50 %	0.15	0.15 to 0.175

Solder columns ≥ 0.51 mm in diameter are normally attached to NSMD lands. Solder columns ≤ 0.4 mm in diameter are often attached to SMD lands. In either case, the PCB land is always larger than the diameter of the solder column. When possible, it is best to increase the size of the land to the upper range of the land variation shown in Table 4-8.

Table 4-9 Summarizes 10 types of column constructions for CGAs.

Table 4-9 Column Grid Array (CGA) Alloy and Construction Styles

Description	Base Material	Secondary Material	Plating	Column Diameter	SnPb	Pb-Free
Solder cast column	PbSn10	–	–	0.51 mm	Yes	See Note
Solder wire column	PbSn15	Cu	SnPb37	0.30 mm to 0.56 mm	Yes	No
Solder wire column	PbSn20	Cu	SnPb37	0.30 mm to 0.56 mm	Yes	No
Solder wire column	PbSn10	Cu	SnPb37	0.30 mm to 0.56 mm	Yes	No
Microcoil spring	BeCu	–	SnPb40	0.40 mm to 0.51 mm	Yes	No
Microcoil spring	BeCu	–	NiAu	0.40 mm to 0.51 mm	No	Yes
Cu column	Cu	–	Sn100	0.10 mm to 0.25 mm	No	Yes
Cu column	Cu	–	SnPb40	0.10 mm to 0.25 mm	Yes	No
Cu-braided solder wire	PbSn10	Cu	Sn6Pb37	0.30 mm to 0.51 mm	Yes	No
Cu-braided solder wire	PbSn10	Cu	SAC305	0.30 mm to 0.51 mm	Yes	See Note

Table note: PbSn10 solder may be exempt from RoHS restrictions for certain industries under category 7a. Suggest monitoring updates to RoHS for discontinuation of “exempt” status.

The CGA columns shown in Table 4-9 are available in a variety of materials and constructions. The common characteristic among the CGAs is the requirement to reduce stress caused by CTE mismatch between the device package and printed board. Column diameter is selected based on the pad diameter available on the component. Typically, smaller-pitch components have smaller-diameter land pads.

To minimize column collapse, care must be taken to reflow heavy CGA components at the lowest practical temperature. Research is ongoing to investigate other Pb-free column materials.