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Generic Requirements for Surface Mount Design and Land Pattern Standard

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Association Connecting Electronics Industries



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Generic Requirements for Surface Mount Design and Land Pattern Standard

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of the Printed Board Design Committee (1-10) of IPC

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Users of this publication are encouraged to participate in the
development of future revisions.

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Generic Requirements for Surface Mount Design and Land Pattern Standard

1 SCOPE

This document provides generic requirements on land pattern geometries used for the surface attachment of electronic components, as well as surface mount design recommendations for achieving the best possible solder joints to the devices assembled.

1.1 Purpose The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet to meet the requirements of IPC J-STD-001, and also to allow for inspection, testing, and rework of those solder joints. Designers can use the information contained herein to establish standard land pattern geometries not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the printed board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Land patterns become a part of the printed board circuitry and they are subject to the producibility levels and tolerances associated with fabrication and assembly processes. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns.

In addition to the land pattern geometries required for proper solder joint formation, other mounting conditions must be considered, such as solder mask clearance, solder paste stencil aperture sizes, clearance between adjacent components, clearance between the bottom of the component and the printed board surface (if relevant), keep-out areas (if relevant), and suitable rules for adhesive applications. These additional features become part of the overall land pattern standard for each component type.

Note 1: The dimensions used for component descriptions have been extracted from standards listed in Section 2. Designers should refer to the manufacturer's data sheet for specific component package dimensions.

Caution: Users should be aware that individual component data sheets may not meet standardized component outlines (e.g., JEDEC standard component outlines).

Note 2: Elements of the mounting conditions, particularly the courtyard, given in this standard are related to the reflow soldering process. Adjustments for wave or other soldering processes, if applicable, have to be carried out by the user. This may also be relevant when solder alloys other than eutectic tin lead solders are used.

Note 3: This standard assumes that even under worst case tolerance conditions the opportunity for an acceptable solder fillet will be maintained.

Note 4: Heat dissipation aspects have not been taken into account in this standard. Greater mass may require slower process speed to allow heat transfer.

Note 5: For surface mount components, the solder joints provide not only the electrical connection, but the mechanical support as well. Heavier components (greater weight per land) require larger lands; thus, adding additional land pattern surface will increase surface area of molten solder to enhance capabilities of extra weight. In some cases the lands shown in this standard may not apply for a particular application and may need to be increased in a land pattern library; in these cases, considering additional measures may be necessary.

1.2 Documentation Hierarchy This standard identifies the generic physical design principles involved in the creation of land patterns for surface mount components, and is supplemented by a shareware IPC-7351 Land Pattern Calculator that provides, through the use of a graphical user interface, the individual component dimensions and corresponding land pattern recommendations based upon families of components. The IPC-7351 Land Pattern Calculator is provided on CD-ROM as part of this standard. Updates to land pattern dimensions, including patterns for new component families, can be found on the IPC website (www.ipc.org) under the "Knowledge" menu, within "PCB Tools and Calculators." See Appendix B for more information on the IPC-7351 Land Pattern Calculator.

1.2.1 Component and Land Pattern Family Structure The IPC-7351 provides the following number designation within this standard for each major family of surface mount components to indicate similarities in solder joint engineering goals:

IPC-7352 – Discrete Components (CAP, CAPAE, RES, IND, DIO, LED, SODFL, SOTFL)

IPC-7353 – Gullwing Leaded Components, Two Sides (SOP, SOIC, SOD, SOT, TO)

IPC-7354 – J-Leaded Components, Two Sides (SOJ)

IPC-7355 – Gullwing Leaded Components, Four Sides (QFP, CQFP)

IPC-7356 – J-Leaded Components, Four Sides (PLCC)

IPC-7357 – Post Leads, Two Sides (DIP)

IPC-7358 – Area Array Components (BGA, FBGA, CGA, LGA)

IPC-7359 – No Lead Components (QFN, SON, LCC, DFN, PQFN, PSON)

Note: None of the families provided above are intended for release as separate publications from this standard. They are intended only to group together component families that share similar solder joint engineering goals.

1.3 Performance Classification This standard recognizes that electrical and electronic products are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of product between classes.

Process Indicator imperfections are permitted and are deliverable.

The user is responsible for defining the product class. The procurement documentation package **shall** state the product class and any exceptions to specific parameters, where appropriate.

Criteria defined in this document reflect three classes, which are as follows:

Class 1 General Electronic Products – Includes limited life products suitable for applications where the requirement is function of the completed product.

Class 2 Dedicated Service Electronic Products – Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical.

Class 3 High Reliability Electronic Products – Includes products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, and the product must function when required.

The IPC-7351 land patterns have the capability of accommodating all three performance classifications.

1.3.1 Producibility Levels When appropriate this standard will provide three design producibility levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

Level A General Design Producibility – Preferred

Level B Moderate Design Producibility – Standard

Level C High Design Producibility – Reduced

The producibility levels are not to be interpreted as a design requirement, but a method of communicating the degree of difficulty of a feature between design and fabrication/assembly facilities. The use of one level for a specific feature does not mean that other features must be of the same level. Selection should always be based on the minimum need, while recognizing that the precision, performance, conductive pattern density, equipment, assembly and testing requirements determine the design producibility level. The numbers listed within the tables of IPC-7351 are to be used as a guide in determining what the level of producibility will be for any feature. The specific requirement for any feature that must be controlled on the end item **shall** be specified on the master drawing of the printed board or the printed board assembly drawing.

Classification of producibility levels should not be confused with density levels of land pattern geometries described in 1.4.

1.4 Land Pattern Determination This standard discusses two methods of providing information on land patterns.

1. Exact details based on industry component specifications, board manufacturing and component placement accuracy capabilities.

These land patterns are restricted to a specific component, and have an identifying IPC-7351 land pattern name.

2. Equations can be used to alter the given information to achieve a more robust solder connection, when used in particular situations where the equipment for placement or attachment are more or less precise than the assumptions made when determining the land pattern details (see 3.1.2).

Three land pattern geometry variations are supplied for each of the device families; maximum land protrusion (Density Level A), median land protrusion (Density Level B) and minimum land protrusion (Density Level C). Before adapting the minimum land pattern variations the user should consider product qualification testing based on the conditions shown in Table 3-24.

Density Level A: Maximum (Most) Land Protrusion – For low-density product applications, the ‘maximum’ land pattern condition has been developed to accommodate wave or flow solder of leadless chip devices and leaded gull-wing devices. The geometry furnished for these devices, as well as inward and “J”-formed lead contact device families, may provide a wider process window for reflow solder processes as well.

Density Level B: Median (Nominal) Land Protrusion – Products with a moderate level of component density may consider adapting the ‘median’ land pattern geometry. The median land patterns furnished for all device families will provide a robust solder attachment condition for reflow solder processes and should provide a condition suitable for wave or reflow soldering of leadless chip and leaded gull-wing type devices.

Density Level C: Minimum (Least) Land Protrusion – High component density typical of portable and hand-held product applications may consider the ‘minimum’ land pattern geometry variation. Selection of the minimum land pattern geometry may not be suitable for all product use categories.

The use of classes of performance (1, 2, and 3) is combined with that of component density levels (A, B, and C) in explaining the condition of an electronic printed board assembly. As an example, combining the description as Levels 1A or 3B or 2C, would indicate the different combinations of performance and component density to aid in understanding the environment and the manufacturing requirements of a particular printed board assembly.

Although all three land pattern geometry variations are considered compliant for lead free soldering processes, the Density Level C variant will require more processing capability to ensure a proper wetting of the lead free alloy. See 3.2.3 for further information on land pattern design in lead free soldering environments.

1.5 Terms and Definitions Terms and definitions used herein are in accordance with IPC-T-50 except as otherwise specified.

Note: Any definition denoted with an asterisk (*) is a reprint of the term defined in IPC-T-50.

***As Agreed Between User and Supplier (AABUS)** Indicates additional or alternate requirements to be decided between the user and the supplier in the procurement documentation. Examples include contractual requirements, modifications to purchase documentation and information on the drawing. Agreements can be used to define test methods, conditions, frequencies, categories or acceptance criteria within a test, if not already established.

***Assembly** – A number of parts, subassemblies or combinations thereof joined together. (Note: This term can be used in conjunction with other terms listed herein, e.g., “Printed Board Assembly.”)

***Automatic Test Equipment (ATE)** – Equipment that automatically analyzes functional or static parameters in order to evaluate performance.

***Base Material** – The insulating material upon which a conductive pattern may be formed. (The base material may be rigid or flexible, or both. It may be a dielectric or insulated metal sheet.)

***Basic Dimension** – A numerical value used to describe the theoretical exact location of a feature or hole. (It is the basis from which permissible variations are established by tolerance on other dimensions in notes or by feature control symbols.)

***Blind Via** – A via extending only to one surface of a printed board.

***Buried Via** – A via that does not extend to the surface of a printed board.

***Castellation** – A recessed metalized feature on the edge of a leadless chip carrier that is used to interconnect conducting surface or planes within or on the chip carrier.

***Chip Carrier** – A low-profile, usually square, surface-mount component semiconductor package whose die cavity or die mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package. (It may be leaded or leadless.)

***Chip-On-Board (COB)** – A printed board assembly technology that places unpackaged semiconductor dice and interconnects them by wire bonding or similar attachment techniques. Silicon area density is usually less than that of the printed board.

***Coefficient of Thermal Expansion (CTE)** – The linear dimensional change of a material per unit change in temperature. (See also “Thermal Mismatch (Expansion)”).

***Component** – An individual part or combination of parts that, when together, perform a design function(s). (See IPC-T-50 for additional term references.)

***Component Mounting Site** – The location on a Package Interconnect (P&I) structure that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component.

***Conductive Pattern** – The configuration or design of the conductive material on a base material. (This includes conductors, lands, vias, heatsinks and passive components when these are an integral part of the printed board manufacturing process.)

***Conductor** – A single conductive path in a conductive pattern.

***Constraining Core** – A supporting plane that is internal to a packaging and interconnecting structure. (See also “Supporting Plane”).

Courtyard – The smallest rectangular area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundaries.

Courtyard Excess – The area between the rectangle circumscribing the land pattern and the component, and the outer boundary of the courtyard. The courtyard excess may be different in the x-and y-direction.

Courtyard Manufacturing Zone – The area that provides a minimum electrical and mechanical clearance (courtyard excess) around the combined component body and land pattern boundaries.

***Double-Sided Assembly** – A packaging and interconnecting structure with components mounted on both the primary and secondary sides. (See also “Single-Sided Assembly”).

***Dual-Inline Package (DIP)** – An electronic device package with a rectangular housing and two parallel rows of electrical connecting pins, usually protruding from the longer sides of the package and bent downward.

***Fine-Pitch Technology (FPT)** – A surface-mount assembly technology with component terminations on less than 0.625 mm [0.025 in] centers.

***Fiducial (Mark)** – A printed board artwork feature(s) that is created in the same process as the conductive pattern and that provides a common measurable point for component mounting with respect to a land pattern or land patterns.

***Flat Pack** – A rectangular component package that has a row of leads extending from each of the longer sides of its body that are parallel to the base of its body.

***Footprint** – See “Land Pattern.”

***Grid** – An orthogonal network of two sets of parallel equidistant lines that is used for locating points on a printed board.

***Heel Fillet** – The solder fillet formed in the land area behind the lead.

***In-Circuit Testing (ICT)** – The application of test signals directly to a device’s input terminals and sensing the results directly from the device’s output terminals.

***Infrared Reflow (IR)** – Remelting of solder using infrared heating as the primary source of energy.

***Integrated Circuit (IC)** – A combination of inseparable associated circuit elements that are formed in place and interconnected on or within a single base material to perform a particular electrical function.

***Jumper wire** – A discrete electrical connection that is part of the original design and is used to bridge portions of the basic conductive pattern formed on a printed board.

***Land** – A portion of a conductive pattern usually used for the connection and/or attachment of components.

***Land Pattern** – A combination of lands that is used for the mounting, interconnection and testing of a particular component.

***Leadless Chip Carrier** – A chip carrier whose external connections consist of metallized terminations that are an integral part of the component body. (See also “Leaded Chip Carrier.”)

Leaded Chip Carrier – A chip carrier whose external connections consist of leads that are around and down the side of the package. (See also “Leadless Chip Carrier.”)

***Least Material Condition (LMC)** – The condition in which a feature of size contains the least amount of material within the stated limits of size.

***Master Drawing** – A control document that shows the dimensional limits or grid locations that are applicable to any and all parts of a product to be fabricated, including the arrangement of conductors and nonconductive patterns or elements; the size, type, and location of holes; and all other necessary information.

***Maximum Material Condition (MMC)** – The condition in which a feature of size contains the most amount of material within the stated limits of size.

***Mixed Component-Mounting Technology** – A component mounting technology that uses both through-hole and surface-mounting technologies on the same packaging and interconnecting structure.

***Module** – A separable unit in a packaging scheme.

***Multilayer Printed Circuit Board Assembly** – An assembly that uses a multilayer printed circuit board for component mounting and interconnecting purposes.

***Nominal** – The design target dimension for a physical characteristic of a product or a feature to which a tolerance may be applied that establishes the limits of variation from the target that are acceptable.

***Organic Solderability Preservative (OSP)** – An organic compound that reacts selectively with copper surfaces forming a thin, uniform film that prevents copper oxidation and helps maintain solderability after extended printed board storage.

***Packaging and Interconnecting Assembly** – The general term for an assembly that has components mounted on either or both sides of a packaging and interconnecting structure.

***Packaging and Interconnecting Structure** – The general term for a completely processed combination of base materials, supporting planes or constraining cores, and interconnection wiring that are used for the purpose of mounting and interconnecting components.

***Plated-Through Hole (PTH)** – A hole with plating on its walls that makes an electrical connection between conductive patterns on internal layers, external layer, or both, of a printed board.

***Primary Side** – The side of a packaging and interconnecting structure that is so defined on the master drawing. (It is usually the side that contains the most complex or the most number of components.)

***Printed Board (PB)** – The general term for completely processed printed circuit and printed wiring configurations. (This includes single-sided, double-sided and multilayer boards with rigid, flexible, and rigid-flex base materials.)

***Printed Board Assembly** – The generic term for an assembly that uses a printed board for component mounting and interconnecting purposes.

***Printed Circuit Board Assembly** – An assembly that uses a printed circuit board for component mounting and interconnecting purposes.

***Printed Wiring** – A conductive pattern that provides point-to-point connections but not printed components in a predetermined arrangement on a common base. (See IPC-T-50 for additional term references.)

Profile Tolerance – A group of powerful geometric tolerances that control the size, location, orientation, and form of a feature. Profile tolerances can be either independent or related.

***Regardless of Feature Size** – A geometric tolerance or datum reference that applies at any increment of size of a feature that is within its size tolerance.

***Registration** – The degree of conformity of the position of a pattern (or portion thereof), a hole, or other feature to its intended position on a product.

***Secondary Side** – That side of a packaging and interconnecting structure that is opposite the primary side. (It is the same as the “solder side” on through-hole mounting technology.)

***Single-Inline Package (SIP)** – A component package with one straight row of pins or wire leads.

***Single-Sided Assembly** – A packaging and interconnecting structure with components mounted only on one side. (See also “Double-Sided Assembly.”)

Static Charge – An electrical charge that has accumulated or built up on the surface of a material

Static Electricity Control – A technique where materials and systems are employed to eliminate/discharge static electricity build-up by providing continuous discharge paths

***Supported Hole** – A hole in a printed board that has its inside surfaces plated or otherwise reinforced.

***Supporting Plane** – A planar structure that is a part of a packaging and interconnecting structure in order to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics. (It may be either internal or external to the packaging and interconnecting structure.) (See also “Constraining Core.”)

***Surface Mount Technology (SMT)** – The electrical connection of components to the surface of a conductive pattern that does not utilize component holes.

***Tented Via (Type I Via)** – A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are desposited in the hole. It may be applied to one side or both.

***Thermal Mismatch (Expansion)** – The absolute difference between the thermal expansion of two components or materials. (See also “Coefficient of Thermal Expansion (CTE).”)

***Through Connection** – The electrical connection to connect conductor patterns on the front side through to the back side of a printed board. (See IPC-T-50 for additional term references.)

***Through-Hole Technology (THT)** – The electrical connection of components to a conductive pattern by the use of component holes.

Toe Fillet – The solder fillet formed in the land area in front of the lead termination.

***Tooling Feature** – A physical feature that is used exclusively to position a printed board or panel during a fabrication, assembly or testing process. (See IPC-T-50 for additional term references.)

***Via** – A plated-through hole that is used as an interlayer connection, but in which there is no intention to insert a component lead or other reinforcing material. (See also “Blind Via” and “Buried Via.”)

1.6 Revision Level Changes Changes made to this revision of the IPC-7351 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the figure or table header.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-A-610 Acceptability of Printed Board Assemblies

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-S-816 SMT Process Guideline and Checklist

IPC-1902 Grid System for Printed Circuits

IPC-2221 Generic Standard on Printed Board Design

IPC-2226 Sectional Design Standard for High Density Interconnect (HDI) Printed Boards

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-4761 Design Guide for Protection of Printed Board Via Structures

IPC-6012 Qualification and Performance Standard for Rigid Printed Boards

IPC-7095 Design and Assembly Process Implementation for BGAs

IPC-7525 Stencil Design Guidelines

IPC-7530 Guidelines for Temperature Profiling for Mass Soldering Processes

IPC-7711/21 Rework and Repair Guide

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

2.2 Electronic Industries Association²

EIA-481 Tape and Reel Specification

2.3 Joint Industry Standards (IPC)¹

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

J-STD-033 Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

2.4 International Electrotechnical Commission³

IEC-61188 Printed Boards and Printed Board Assemblies Design and Use

2.5 Joint Electron Device Engineering Council (JEDEC)⁴

Publication 95 JEDEC Registered and Standard Outlines for Solid State Products

1. www.ipc.org
2. www.eia.org
3. www.iec.ch
4. www.jedec.org

3 DESIGN REQUIREMENTS

3.1 Dimensioning Systems This section describes a set of dimensional criteria for components, land patterns, positional accuracy of the component placement capability and for the development of acceptable solder joints commensurate with reliability or product performance analysis.

Profile tolerances are used in the dimensioning system to define the size range between maximum and minimum component/lead dimensions without ambiguity. The profile tolerance is intended to control both size and position of the land. Figure 3-1 shows the profile tolerancing method.

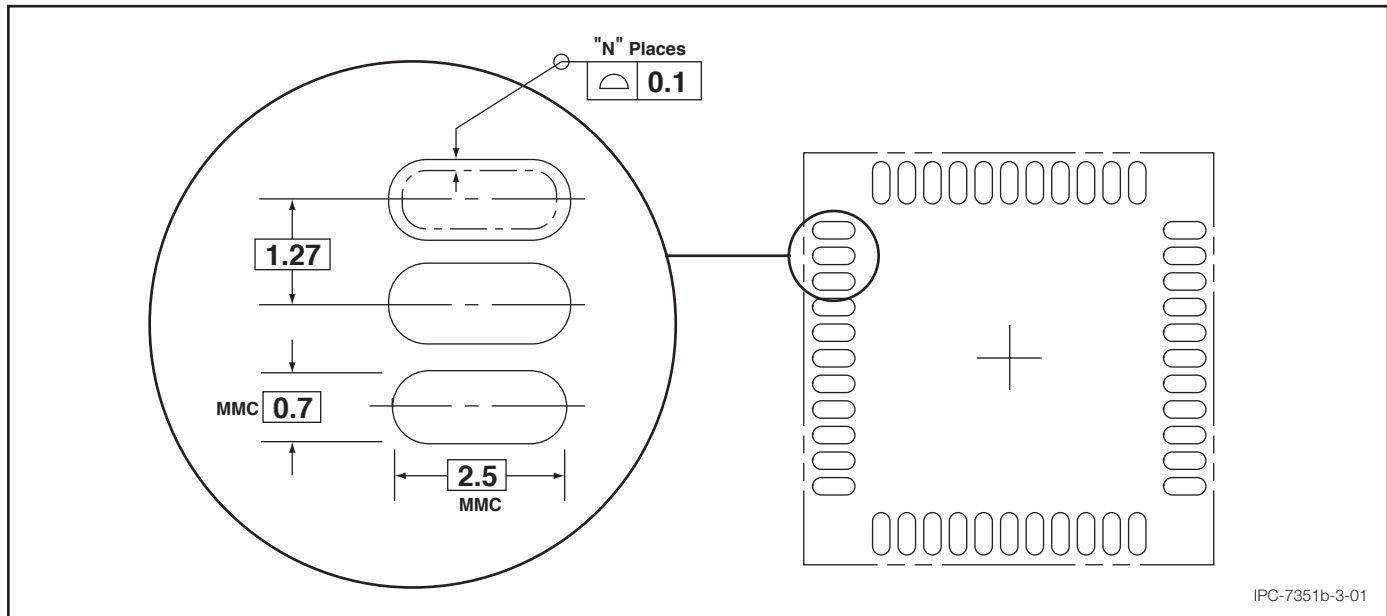


Figure 3-1 Profile Tolerancing Method

The use of the profile dimensioning system requires an understanding of the concepts. The use of a set of requirements are adopted and invoke the following rules, unless otherwise modified:

- All dimensions are basic (nominal)
- Limits of size control form as well as size
- Perfect form is required at maximum dimensions
- Datum references and position tolerances apply at maximum dimensions, and are dependent on feature size
- Position dimensions originate from maximum dimensions
- Tolerances and their datum references other than size and position apply regardless of feature size (RFS)

The dimensioning concepts used for this system of analysis consider the assembly/attachment requirements as their major goal. Specification (data) sheets for components or dimensions for land patterns on printed boards may use different dimensioning concepts, however, the goal is to combine all concepts into a single system. Users are encouraged to establish the appropriate relationship between their dimensioning system(s) and the profile dimensioning system and analysis concepts described herein to allow for ease of tailoring these concepts for robust process performance. As an example, if the tolerance used for positioning is larger than the machine tolerance used in production, a single dimensional change could modify the land pattern.

3.1.1 Component Tolerancing The component manufacturers and industry standards organizations are responsible for the dimensioning and tolerancing of electronic components (see 3.1.5.2). The basic dimensions and tolerance limits published in the specifications have been converted to a functional equivalent using the profile tolerancing method with all components shown with their basic dimensions as limit dimensions (maximum or minimum size). Profile tolerances are unilateral, and are described to reflect the best condition for solder joint formation.

The concept for component dimension evaluations is based on evaluating the surfaces of the component termination and component lead or contact that are involved in the formation of the acceptable solder joint. Component manufacturers provide dimensions for their parts showing either the limits of size (max/min) or they provide a nominal size and then put a tolerance on that nominal dimension. In order to facilitate the dimensioning system, these dimensions and their associated tolerances are converted to minimum and maximum size. If only a nominal dimension is provided the variation on the dimension must be determined empirically in order to establish the appropriate land pattern.

As an example, a size C3216 capacitor has a manufactured nominal dimension for its length of 3.2 mm. The tolerance described by the manufacturer is ± 0.2 mm. Thus, the minimum dimension of "L" is 3.0 mm with a unilateral tolerance of 0.4 mm, resulting in its maximum dimension being 3.4 mm.

Figure 3-2 shows the characteristics for the 3216 capacitor. Item A in Figure 3-2 shows the component manufacturer's dimensions for the length of the capacitor. Item B in Figure 3-2 shows the component length at its minimum size in the converted dimensions of the system using profile tolerancing. Item C in Figure 3-2 shows the land pattern at its maximum size. These conditions provide for an optimum toe fillet.

Similar concepts are applied to leaded surface mount parts. The critical dimensional characteristics identified are those that relate to the formation of the toe and heel solder fillet. For components with gull-wing leads, the basic dimensions apply across the outer extremities of the part for toe land projection; and within the inside of the formed radius of opposing leads for heel solder fillet formation.

The outer dimensions of leaded or even leadless chip carriers are usually easy to determine since these are readily available from the component manufacturer or standards organization. The inner (heel-to-heel) dimensions are rarely provided in industry standards or manufacturers' specifications. These dimensions are more difficult to determine, not only because of the form of the lead, termination, or castellation but also because the inner dimensions must be derived by subtracting the sum of the dimensions of the leads (with all their inherent tolerances) from the overall dimensions of the part.

Item A in Figure 3-3 shows the concept for the manufacturer's dimensions and tolerances for a gull-wing SOIC. Item B in Figure 3-3 shows the converted dimensions to be considered in the overall mounting system requirements.

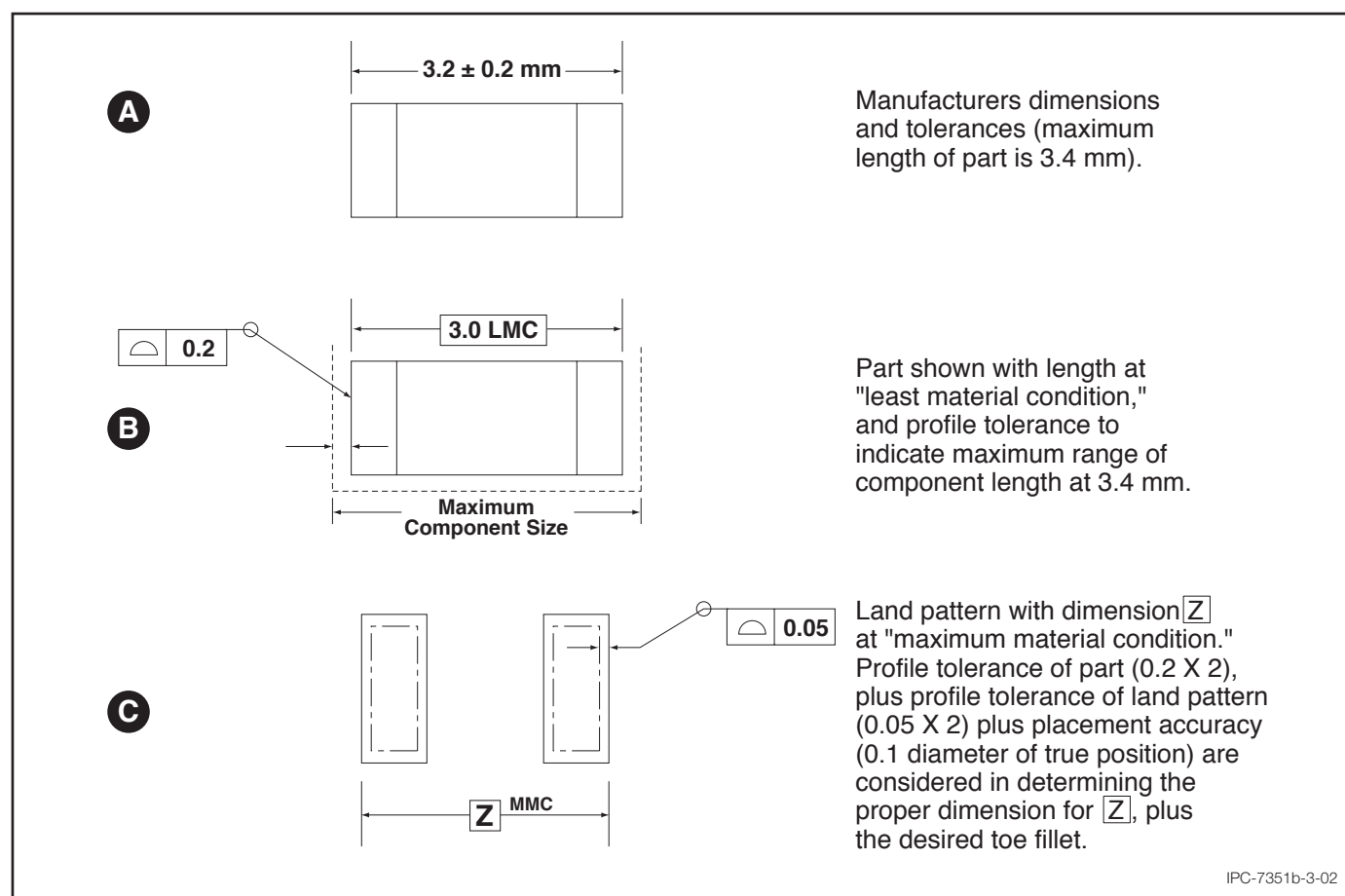


Figure 3-2 Example of 3216 (1206) Capacitor Dimensioning for Optimum Solder Fillet Condition

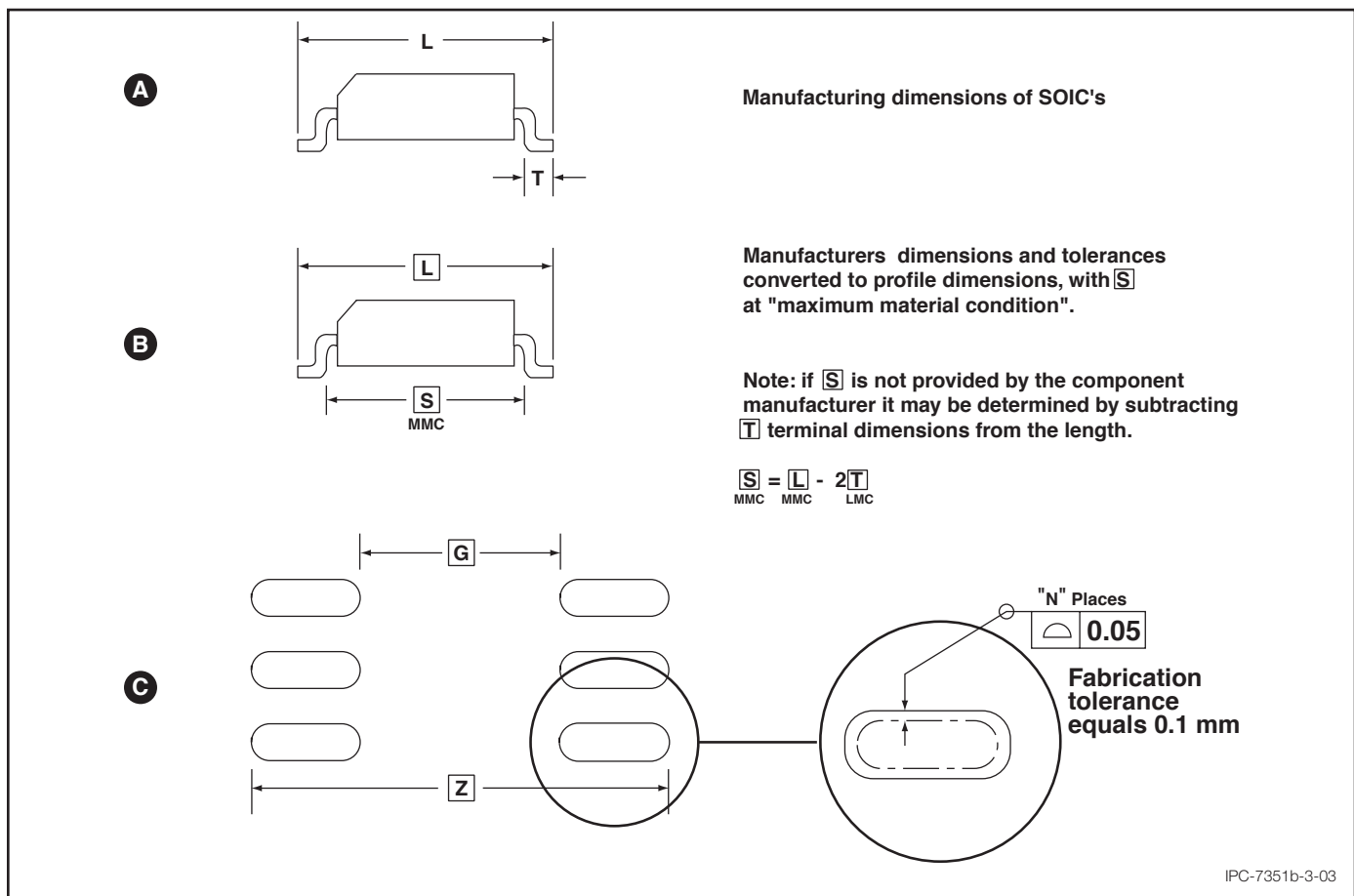


Figure 3-3 Profile Dimensioning of Gull-Wing Leaded SOIC

Item C in Figure 3-3 shows the land pattern dimensions. The basic dimensions define the minimum length as measured across the two outer extremities. As component tolerances for "L" increase the maximum length, the opportunity for the toe fillet is subsequently reduced.

The inner dimensions between heel fillets on opposing sides are the most important. Inner dimensions are derived by:

- Establishing the maximum outline of the component as measured from lead termination end to lead termination end. (This dimension is shown as "L," and is provided by the manufacturer).
- Establishing the minimum amount of the lead length as measured across the "footprint" (from heel to toe for gull-wing leads). (This dimension is "T," and is provided by the manufacturer).
- Subtracting twice the minimum lead length of (T) from the maximum overall component length of (L) to arrive at the maximum length inside the leads across the length of the component (the inner dimension between opposing heel fillets). Including the tolerances on dimensions (L) and subtracting the maximum dimension of $T \times 2$ will yield the minimum dimension between opposing heels. This signifies the worst-case tolerance analysis.
- Three sets of tolerances are involved in the analysis described within three tolerances on the overall component, plus the tolerances for the lead on each end. Since not all three tolerances are considered at their worst case, a recommended method for determining the statistical impact is to summarize the squares of the tolerances and take the square root of their sum as the RMS (root-mean-square) tolerance difference.

For example,

$$\text{RMS tolerance accumulation} = \sqrt{(L_{\text{tol}})^2 + 2(T_{\text{tol}})^2}$$

Where:

$$L_{\text{tol}} = L_{\text{max}} - L_{\text{min}}$$

$$T_{\text{tol}} = T_{\text{max}} - T_{\text{min}}$$

tol = tolerance

max = maximum

min = minimum

As an example, the SOIC with 16 leads has the following limits for the “L” (component length) and “T” (terminal length) dimensions:

$$L_{\text{min}} = 5.8 \text{ mm}, L_{\text{max}} = 6.2 \text{ mm}$$

$$L_{\text{tol}} = L_{\text{max}} - L_{\text{min}} = 6.2 \text{ mm} - 5.8 \text{ mm} = 0.4 \text{ mm}$$

$$T_{\text{min}} = 0.4 \text{ mm}, T_{\text{max}} = 1.27 \text{ mm}$$

$$T_{\text{tol}} = T_{\text{max}} - T_{\text{min}} = 1.27 \text{ mm} - 0.4 \text{ mm} = 0.87 \text{ mm}$$

Therefore, the calculations for “S” minimum and maximum dimensions are as follows:

$$S_{\text{min}} = L_{\text{min}} - 2T_{\text{max}} = 5.8 \text{ mm} - 2(1.27 \text{ mm}) = 3.26 \text{ mm}$$

$$S_{\text{max}} = L_{\text{max}} - 2T_{\text{min}} = 6.2 \text{ mm} - 2(0.4 \text{ mm}) = 5.40 \text{ mm}$$

$$S_{\text{tol}} = S_{\text{max}} - S_{\text{min}} = 5.4 \text{ mm} - 3.26 \text{ mm} = 2.14 \text{ mm}$$

The difference between S_{min} and S_{max} is 2.14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-case scenario for the tolerance range for “S” can also be calculated by adding the tolerances for the component length and the two terminals:

$$S_{\text{tol}} = L_{\text{tol}} + 2T_{\text{tol}} = 0.4 \text{ mm} + 2(0.87 \text{ mm}) = 2.14 \text{ mm}$$

In order to arrive at a more realistic tolerance range, the RMS value is calculated using the tolerances on the dimensions involved (“L” and “T”):

$$S_{\text{tol}}(\text{RMS}) = \sqrt{(L_{\text{tol}})^2 + 2(T_{\text{tol}})^2} = \sqrt{0.4^2 + 2(0.87)^2} = 1.30 \text{ mm}$$

The difference between worst case and the RMS value is $2.14 - 1.30 = 0.84$. This variation is the difference between the two methods for tolerance analysis. In order to derive a new maximum and minimum dimension for “S” to determine land patterns, half of this difference is subtracted from the worst case S_{max} ($5.4 - 0.42 = 4.98$); and half the difference is added to the worst case S_{min} ($3.26 + 0.42 = 3.68$). Thus, 4.98 to 3.68 becomes the variation (Max/Min) for the S dimension.

This technique is used so that a more realistic S_{max} dimension is used in the land pattern equations for calculating G_{min} (minimum land pattern gap between heel fillets).

3.1.1.1 Solving for Dimension “Z” It should be noted that there are various options to determine the tolerances for the component (C), the fabrication allowance (F), and the placement tolerance (P). In determining the calculations for the example in Figure 3-3 for the dimension “Z,” one would note that the component “SO16” has an L_{max} equal to 6.20 mm, and an L_{min} equal to 5.80 mm. With the assumption that “F” is equal to 0.1 mm and “P” is equal to 0.2 mm, the following conditions would be used for determining the “Z” dimension:

$$Z_{\text{max}} = L_{\text{min}} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$Z_{\text{max}} = 5.80 \text{ mm} + 2J_T + \sqrt{0.4^2 + 0.1^2 + 0.2^2}$$

In the above example, the two joints should be rounded to a realistic number. Normally a total Z dimension of 7.0 mm would be acceptable for a density level B land pattern providing a 0.4 mm land protrusion at either end of the SO16 component.

3.1.2 Land Tolerancing Profile tolerancing is used for lands in a manner similar to that of the components. All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Unilateral tolerances are intended to reduce the land size and thus result in a lesser area for solder joint formation. In order to facilitate companion dimension systems, the land pattern is dimensioned across outer and inner extremities.

The dimensioning concept in this standard uses limiting dimensions and geometric tolerancing to describe the allowable maximum and minimum dimensions of the land pattern. When lands are at their maximum size, the result may be a minimum acceptable space between lands; conversely when lands are at their minimum size, the result may be a minimum acceptable land pattern necessary to achieve the minimum required land protrusion. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this document is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions, etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis (see Table 3-1).

3.1.3 Fabrication Allowances Figure 3-3 shows the land pattern for an SOIC with gull-wing leads intended to be a companion to the chip component dimensioning concepts shown previously in Figure 3-2. The basic “L” dimension is across the outer extremities of the component lead or terminal.

For the land pattern, dimension “Z” is at maximum size, while the inner extremities (dimension “G”) are dimensioned at minimum size. Unilateral tolerances decreased the basic dimension for “Z” while increasing the basic “G” dimension. This action results in a reduced land pattern at Least Material Condition (LMC). Thus, processing target values should be as close as possible to the basic “Z” and “G” dimensions at Maximum Material Condition (MMC). This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

The variation between the dimensions Z, G, and X are indicated as a fabrication allowance (F). This fabrication allowance represents the maximum variation between the largest land pattern size (MMC) and the least land pattern size (LMC). This does not include material movement as described in 3.1.4, which is included in the assembly tolerancing since machine vision capability reevaluates the true position of the land pattern.

3.1.4 Assembly Tolerancing Another part of the equation is the assembly variation defined by the letter “P.” This variation represents the location of the component in relation to its true position as defined by the design. The term diameter of true position (DTP) is used to describe this variation and is a single number that can be used in the dimensional tolerance analysis.

As an example, for establishing the target heel protrusion dimensions of the example shown in Figure 3-3, the following conditions would be true:

Where:

J is 0.5 mm (target heel fillet)

C is S_{tol} (RMS) = 1.29 mm (see previous calculations from component dimensions)

F is 0.1 mm (assumed fabrication tolerance)

P is 0.05 mm (assumed assembly equipment placement tolerance)

Therefore:

$$G_{min} = 4.98 \text{ mm} - 2(0.5 \text{ mm}) - \sqrt{(1.29)^2 + (0.1)^2 + (0.05)^2} = 2.25 \text{ mm}$$

Another major condition for multiple-leaded components that must be considered in land pattern design is lead, termination, or castellation pitch. The pitch describes the basic dimension of the spacing of one component lead termination or castellation to its adjacent counterpart(s). No tolerance is assigned to pitch in the profile dimensioning concept. Differences in pitch are included in the width dimensions of the lead, termination, or castellation which are dimensioned as basic at the minimum size.

3.1.5 Dimension and Tolerance Analysis In analyzing the design of a component/land pattern system, several things come into play, including the size and position tolerances of the component lead or termination, the tolerances of the land pattern, and the placement accuracy of the man/machine to center the part to the land pattern. The result is the land area available for a solder joint that provides a proper formation of a toe, heel, or side fillet.

System equations have been developed for chip components and multiple leaded parts. These concepts assume that the target values of parts and land patterns are maximized to reflect solder joint formation (i.e., outer dimensions of components at minimum size with outer dimensions of land patterns at maximum size). The equations use the following symbols:

C is the unilateral profile tolerance(s) for the component

F is the unilateral profile tolerance(s) for the printed board land pattern

P is the diameter of true position placement accuracy to the center of the land pattern

With the assumption that a particular solder joint or solder volume is desired for every component, some methods use the worst-case criteria for determining a dimension. This would require that “C,” “F,” and “P” be added to the minimum dimension of the component length plus the solder joint requirements, in order to determine the maximum dimension of the outer land pattern.

Experience shows that the worst-case analysis is not always necessary; therefore statistical methods are used by taking the square root of the sum of the squares of the tolerances. This method assumes that all features will not reach their worst case. The equations for determining component land pattern requirements are as follows:

$$Z_{\max} = L_{\min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$G_{\min} = S_{\max} - 2J_H - \sqrt{C_S^2 + F^2 + P^2}$$

$$X_{\max} = W_{\min} + 2J_S + \sqrt{C_W^2 + F^2 + P^2}$$

Where:

Z is the overall length of land pattern

G is the distance between lands of the pattern

X is the width of land pattern

L is the overall length of component

S is the distance between component terminations

W is the width of the lead or termination

J is the desired dimension of solder fillet or land protrusion:

J_T is the solder fillet or land protrusion at toe

J_H is the solder fillet or land protrusion at heel

J_S is the solder fillet or land protrusion at side

C is the component tolerances:

C_L is the tolerance on component length

C_S is the tolerance on distance between component terminations

C_W is the tolerance on the lead width

F is the printed board fabrication (land pattern geometric) tolerances

P is the part placement tolerance (placement equipment accuracy)

The formula (the square root of the sum of the squares) is identical for both toe and heel solder joint formation (different tolerances are used, however). However, the desired solder joint dimension and the square root of the sum of the squares are added for outer land pattern dimensions and subtracted for inner land pattern dimensions. The result provides the final land pattern dimensions Z, G, and X.

The same concept is true for chip, multiple leaded or lead-less components. Additionally, pitch with lead-to-land overlap (M) can be evaluated as well as the space (N) to reflect the clearance between a lead, termination, or castellation and the adjacent land(s). These latter values are not used in the equations to determine the land pattern sizes, but may be used to limit lead-to-adjacent land proximity and to adjust lead-to-land overlap (see Figure 3-4).

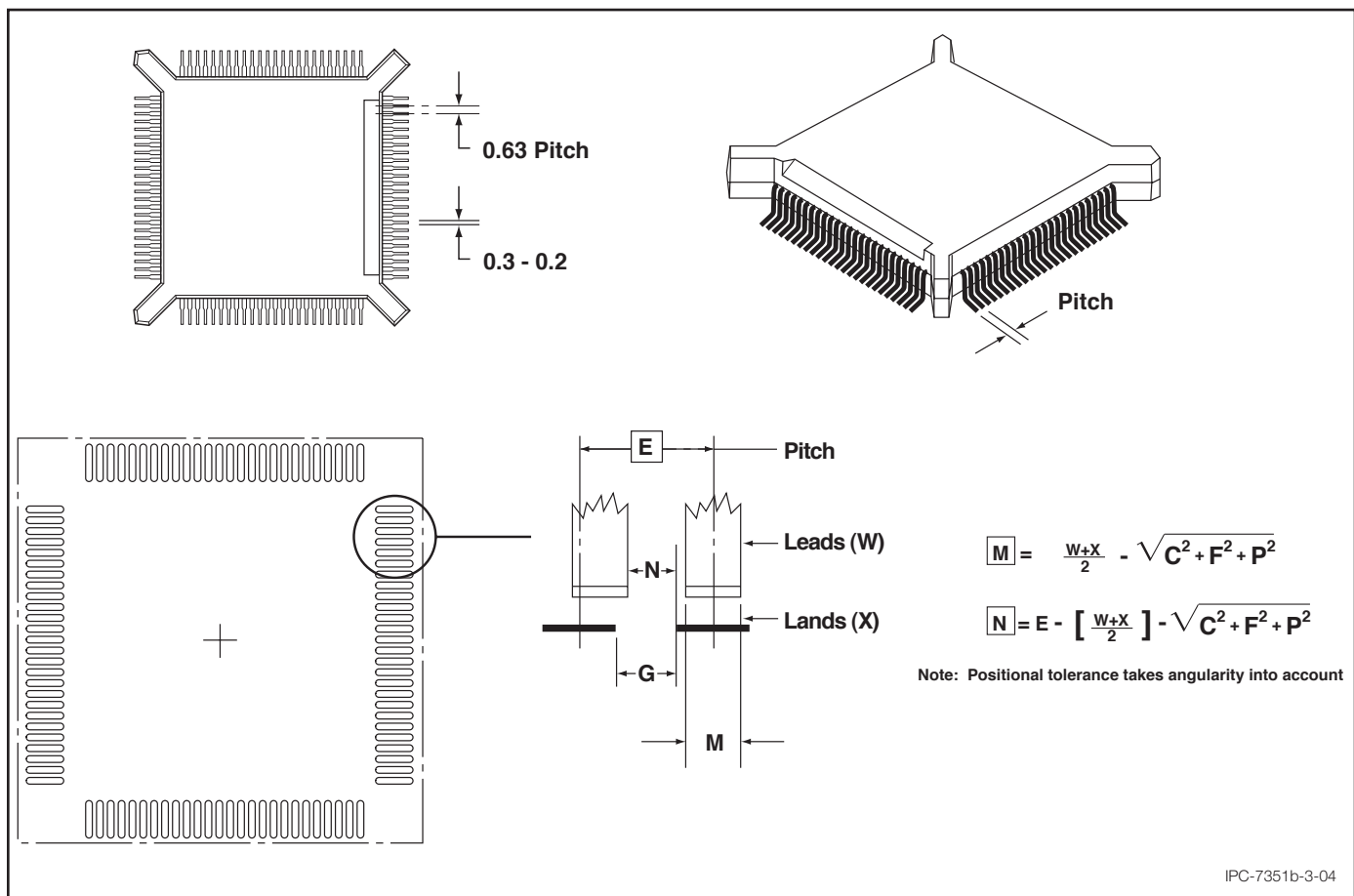


Figure 3-4 Pitch for Multiple Leaded Components

The equations for determining if the clearance “N” or the attachment overlap “M” are sufficient is as follows:

$$M = \left[\frac{W + X}{2} \right] - \sqrt{C^2 + F^2 + P^2}$$

$$N = E - \left[\frac{W + X}{2} \right] - \sqrt{C^2 + F^2 + P^2}$$

3.1.5.1 Tolerance and Solder Joint Analysis The following tolerance concepts are used to determine the land patterns for electronic components. These concepts are detailed in Table 3-1 and reflect the tolerances on the component, the tolerances on the land pattern (on the interconnecting substrate), and the accuracy of the equipment used for placing components.

Solder joint minimums are shown for toe, heel and side fillets. These conditions are minimums, since the equations in 3.1.5 address the component, printed board, and placement accuracy tolerances (sum of the squares). The minimum solder joint or land protrusion is increased by the amount that the tolerance variation does not use up. The courtyard excess is added to the maximum dimension that the land pattern or component occupies. The courtyard excess number is added to each side of the dimension in question. It is intended that this addition provides sufficient room for electrical and physical clearance between components and/or land patterns. Since the total of all the number calculations may not result in a reasonable numerical equivalent, a suggested round-off (up or down) feature has been added to the tables to identify a rounding up value for the final number to be used in the design.

Table 3-1 Tolerance Analysis Elements for Chip Devices

Tolerance Element	Detailed Description
Component Tolerance	The difference between the MMC and the LMC of each component dimension, length, width and distance between terminations or leads. This number is the “C” tolerance in the equations.
Printed Board Tolerance	The difference between the MMC and the LMC of each land pattern dimension. This number is the “F” tolerance in the equations.
Positional Accuracy	Positional accuracy is defined as diameter of true position (DTP). This is the variation of the part centroid related to the land pattern theoretical center (includes feature location tolerance from Table 3-26).
Toe Fillet	The land protrusion beyond the lead or termination extremities (see Table 3-2 through Table 3-22).
Heel Fillet	The land protrusion beyond the internal lead or termination dimensions (see Table 3-2 through Table 3-22).
Side Fillet Width	The land protrusion to either side of the lead or termination (see Table 3-2 through Table 3-22).

The land pattern libraries included within the IPC-7351 LP Calculator provide an analysis of tolerance assumptions and resultant solder joints based on the finished land pattern dimensions. Tolerances for component dimensions, the land pattern dimensions (fabrication tolerances on the interconnecting substrate), and the component placement equipment accuracy are all taken into consideration. These tolerances are addressed in a statistical model, and assume even distribution of the tolerances for component, fabrication and placement accuracy.

Individual tolerances for fabrication (“F”) and component placement equipment accuracy (“P”) are assumed to be as given in the IPC-7351 land pattern libraries. These numbers may be modified based on user equipment capability or fabrication criteria. For example, many printed board fabricators will compensate for etch factors and increase or “swell” land features. In such instances, the combination of etch factor compensation by the printed board fabricator and the IPC-7351 default “F” tolerance results in what can be described as “double etch compensation” where the land size is increased beyond expectation. In these instances, the fabrication tolerance in the “Calculator Settings” menu of the IPC-7351 LP Calculator should be set to 0.0 mm.

Component tolerance ranges (C_L , C_S , and C_W) are derived by subtracting minimum from maximum dimensions given. The user may also modify these numbers, based on experience with their suppliers.

The dimensions for minimum solder fillets at the toe, heel, or side (J_T , J_H , J_S) have been determined based on industry empirical knowledge and reliability testing. Solder joint strength is greatly determined by solder volume. An observable solder fillet is necessary for evidence of proper wetting. Thus, the values in the IPC-7351 land pattern libraries usually provide for a positive solder fillet. Nevertheless, if the user of any of the three land pattern geometry variations desires a more robust process condition for placement and soldering equipment, individual elements of the analysis may be changed to new and desired dimensional conditions. This includes component, printed board or placement accuracy spread, as well as minimum solder joint or land protrusion expectation. In addition, this standard recognizes the need to have different goals for the solder fillet or land protrusion conditions.

Table 3-2 through Table 3-22 indicate the principles used for the three goals established by this standard. They reflect maximum (most), median (nominal) and minimum (least) material conditions for the land protrusions used to develop land patterns for surface mounting various lead or terminations of components. Unless otherwise indicated, the IPC-7351 identifies all three goals as Density Levels A, B, or C.

Several component families have a different concept for developing a land pattern. Effectively, there are no toe, side or heel fillets; rather the land periphery is similar about the entire termination. Whether round or rectangular, once the tolerance is assigned it applies to the periphery of the lands for that particular part. Thus the term “Periphery” is used to signify that the principles occur all around the termination. This is applicable to Table 3-17 through Table 3-19, and Table 3-21. See 15.4 and 15.5 for further information.

Note: A caution is provided in using the information presented in Table 3-2 and Table 3-3. Due to a reduced component standoff height (less than 0.15 mm) on some components, caution is recommended in determining the land pattern length for gull wing components to ensure that any solder paste that touches the package body as a result of the heel fillet extending under the package body does not result in solder bridging among the component leads. Excessive tolerance ranges for the component dimensions may result in an overly robust land pattern where the heel fillet extends under the component body. In such cases, the combination of a large land pattern, a small component seating plane (stand-off between the surface of the printed board and the bottom of the gull wing device) and excessive solder paste thickness may result in some solder adhering to the component body during placement, causing bridging between adjacent component leads after reflow.

Table 3-2 Flat Ribbon L and Gull-Wing Leads (greater than 0.625 mm pitch) (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.35	0.15
Heel (J_H) ¹	0.45	0.35	0.25
Side (J_S)	0.05	0.03	0.01
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Small Outline Integrated Circuit SOIC Construction and land pattern development are described in 9.1			
Small Outline Package SOP Construction and land pattern development are described in 9.2			
Quad Flat Pack QFP Construction and land pattern development are described in 11.1 and 11.2			
Ceramic Quad Flat Pack CQFP Construction and land pattern development are described in 11.3			
Small Outline Transistor SOT Construction and land pattern development are described in 8.6, 8.7, 8.9, and 8.10			
Small Outline Diode SOD Construction and land pattern development are described in 8.8			

Note 1. For gull wing components where dimension S_{min} is less than or equal to dimension A_{max} , use the following heel fillet goals:

Density Level A - 0.25 mm

Density Level B - 0.15 mm

Density Level C - 0.05 mm

Note 2. This does not apply to gull wing components where the lead terminals have a tolerance T1 that is greater than 0.5 mm.

Table 3-3 Flat Ribbon L and Gull-Wing Leads (less than or equal to 0.625 mm pitch) (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.35	0.15
Heel (J_H) ¹	0.45	0.35	0.25
Side (J_S)	0.01	-0.02	-0.04
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Small Outline Package SOP Construction and land pattern development are described in 9.3			
Quad Flat Pack QFP Construction and land pattern development are described in 11.2			

Note 1. For gull wing components where dimension S_{min} is less than or equal to dimension A_{max} , use the following heel fillet goals:

Density Level A - 0.25 mm

Density Level B - 0.15 mm

Density Level C - 0.05 mm

Note 2. This does not apply to gull wing components where the lead terminals have a tolerance T1 that is greater than 0.5 mm.

Table 3-4 J Leads (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Heel (J_H) (to find Z dim)	0.55	0.35	0.15
Toe (J_T) (to find G dim)	0.10	0.00	-0.10
Side (J_S)	0.05	0.03	0.01
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Plastic Leaded Chip Carrier PLCC Construction and land pattern development are described in 12.1			
Small Outline J-leaded SOJ Construction and land pattern development are described in 10.1			

Table 3-5 Rectangular or Square-End Components (Capacitors and Resistors) Equal to or Larger than 1608 (0603) (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.35	0.15
Heel (J_H)	0.00	0.00	0.00
Side (J_S)	0.05	0.00	-0.05
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Chip Resistor RESC Construction and land pattern development are described in 8.1			
Chip Capacitor CAPC Construction and land pattern development are described in 8.2			
Chip Inductor INDC Construction and land pattern development are described in 8.3			

Table 3-6 Rectangular or Square-End Components (Capacitors and Resistors) Smaller than 1608 (0603) (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.30	0.20	0.10
Heel (J_H)	0.00	0.00	0.00
Side (J_S)	0.05	0.00	-0.05
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.02, 1.04, 1.06		
Courtyard excess	0.2	0.15	0.1
Chip Resistor RESC Construction and land pattern development are described in 8.1			
Chip Capacitor CAPC Construction and land pattern development are described in 8.2			
Chip Inductor INDC Construction and land pattern development are described in 8.3			

Table 3-7 Cylindrical End Cap Terminations (MELF) (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.60	0.40	0.20
Heel (J_H)	0.2	0.1	0.02
Side (J_S)	0.1	0.05	0.01
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Metal Electrode Lead Face Resistor RESMELF Construction and land pattern development are described in 8.5			
Metal Electrode Lead Face Diode DIOMELF Construction and land pattern development are described in 8.5			

Table 3-8 Leadless Chip Carrier with Castellated Terminations (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Heel (J_H) (to find Z dim)	0.65	0.55	0.45
Toe (J_T) (to find G dim)	0.25	0.15	0.05
Side (J_S)	0.05	-0.05	-0.15
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Leadless Ceramic Chip Carrier LCC Construction and land pattern development are described in 15.1			
Leadless Ceramic Chip Carrier Side Pin 1 LCCS Construction and land pattern development are described in 15.1			



Table 3-9 Concave Chip Array Component Lead Package (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.45	0.35
Heel (J_H)	-0.05	-0.07	-0.10
Side (J_S)	-0.05	-0.07	-0.10
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Resistor Chip Array Concave RESCAV Construction and land pattern development are described in 14.5.1			
Capacitor Chip Array Concave CAPCAV Construction and land pattern development are described in 14.5.1			
Inductor Chip Array Concave INDCAV Construction and land pattern development are described in 14.5.1			
Oscillator Side Concave OSCSC Construction and land pattern development are described in 14.5.1			

Table 3-10 Convex Chip Array Component Lead Package (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.45	0.35
Heel (J_H)	-0.05	-0.07	-0.10
Side (J_S)	-0.05	-0.07	-0.10
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Resistor Chip Array Convex Version E RESCAXE Construction and land pattern development are described in 14.5.2			
Resistor Chip Array Convex Version S RESCAXS Construction and land pattern development are described in 14.5.2			

Table 3-11 Flat Chip Array Component Lead Package (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.45	0.35
Heel (J_H)	-0.05	-0.07	-0.10
Side (J_S)	-0.05	-0.07	-0.10
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Resistor Chip Array Flat RESCAF - Construction and land pattern development are described in 14.5.3			
Capacitor Chip Array Flat CAPCAF - Construction and land pattern development are described in 14.5.3			
Inductor Chip Array Flat INDCAF - Construction and land pattern development are described in 14.5.3			

Table 3-12 Butt Joints (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	1.0	0.8	0.6
Heel (J_H)	1.0	0.8	0.6
Side (J_S)	0.3	0.2	0.1
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	1.5	0.8	0.2
Dual in line Butt Mounted DIPB - Construction and land pattern development are described in 13.0			

Table 3-13 Inward Flat Ribbon L-Leads
(Molded Inductors, Diodes & Polarized Capacitors) (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T) (to find G dim)	0.25	0.15	0.07
Heel (J_H) (to find Z dim)	0.8	0.5	0.2
Side (J_S)	0.01	-0.05	-0.10
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Molded Polarized Capacitor CAPMP Construction and land pattern development are described in 8.4			
Molded Inductor INDM Construction and land pattern development are described in 8.4			
Molded Diode DIOM Construction and land pattern development are described in 8.4			

Table 3-14 Flat Lug Leads (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.55	0.35	0.15
Heel (J_H)	0.45	0.35	0.25
Side (J_S)	0.05	0.03	0.01
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Generic DPAK TO - Construction and land pattern development are described in 8.11			

Note 1. Depends on thermal requirements.

Table 3-15 Quad Flat No-Lead (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.40	0.30	0.20
Heel (J_H)	0.00	0.00	0.00
Side (J_S)	-0.04	-0.04	-0.04
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Quad Flat No Lead QFN Construction and land pattern development are described in 15.2			

Note 1. The rationale for the relatively large negative heel stems from the tolerances for the lead lengths as also being relatively large. In order to maintain a minimum clearance of 0.20 mm to the thermal tab it becomes necessary to trim the heel by -0.2 mm. Without a thermal tab the heel can usually be increased to as much as 0.50 mm.

Table 3-16 Small Outline No-Lead (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.40	0.30	0.20
Heel (J_H)	0.00	0.00	0.00
Side (J_S)	-0.04	-0.04	-0.04
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Small Outline No Lead SON Construction and land pattern development are described in 15.3			

Note 1. With a thermal tab the heel can usually be increased to as much as 0.1 mm.

Table 3-17 Ball Grid Array Components (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Periphery Collapsing Ball	25% reduction below nominal ball diameter	20% reduction below nominal ball diameter	15% reduction below nominal ball diameter
Periphery Non Collapsing Ball or Column	15% increase above the nominal ball or column diameter	10% increase above the nominal ball or column diameter	5% increase above the nominal ball or column diameter
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	2.00	1.00	0.50
Ball Grid Array BGA Construction and land pattern development are described in 14.1.1 & 14.1.2			

Table 3-18 Small Outline and Quad Flat No-Lead with Pullback Leads (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Periphery	0.05	0.00	-0.05
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Pullback Small Outline No-lead PSON - Construction and land pattern development are described in 15.4			
Pullback Quad Flat No-lead PQFN - Construction and land pattern development are described in 15.4			
Dual Small Outline No-lead DFN - Construction and land pattern development are described in 15.5			

Table 3-19 Corner Concave Component Oscillator Lead Package (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Outer Periphery ¹	0.35	0.25	0.15
Inner Periphery ²	0.10	0.00	-0.05
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	0.5	0.25	0.1
Concave Corner Oscillator OSCCC Construction and land pattern development are described in 14.5.1			

Note 1. The edge of the land associated with the outside of the component body.

Note 2. The edge of the land under the component body.

Table 3-20 Aluminium Electrolytic Capacitor and 2-pin Crystal (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.70	0.50	0.30
10.0 mm or higher	1.00	0.70	0.40
Heel (J_H)	0.00	-0.10	-0.20
10.0 mm or higher	0.00	-0.05	-0.10
Side (J_S)	0.50	0.40	0.30
10.0 mm or higher	0.60	0.50	0.40
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess	1.0	0.50	0.25
Aluminum Electrolytic Capacitor (CAPAE) Construction and land pattern development are described in 8.12			

Table 3-21 Column and Land Grid Array (unit: mm)

Lead Part	Median (Nominal) Density Level B
Periphery	0.00
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15
Courtyard excess	1.00
Column Grid Array (CGA) Construction and land pattern development are described in 14.1.3	
Land Grid Array (LGA) Construction and land pattern development are described in 14.1.4	

Table 3-22 Small Outline Components, Flat Lead (unit: mm)

Lead Part	Maximum (Most) Density Level A	Median (Nominal) Density Level B	Minimum (Least) Density Level C
Toe (J_T)	0.30	0.20	0.10
Heel (J_H)	0.00	0.00	0.00
Side (J_S)	0.05	0.00	-0.05
Round-off factor	Round off to the nearest two place decimal, i.e., 1.00, 1.05, 1.10, 1.15		
Courtyard excess ¹	0.2	0.15	0.1
Small Outline Diode, Flat Lead (SODFL) and Small Outline Transistor, Flat Lead (SOTFL) construction and land pattern development are described in 8.13.			

Note 1. SODFL and SOTFL components are micro-miniature (SOTFL 6 pin is 1.6 x 1.6 mm and SODFL is 1.6 x 0.8 mm) and require a smaller courtyard.

3.1.5.2 Component Dimensions Illustrations of component dimensions are provided in the IPC-7351 Land Pattern Calculator. The standards organizations provide many more dimensions to define the requirements for manufacturing the specific components in a family class; only those dimensions that are necessary for land pattern development are repeated within the IPC-7351 Land Pattern Calculator. At times, the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturer's data sheet. Component dimensions are provided according to the concepts of MMC and LMC. Both conditions are presented in the IPC-7351 Land Pattern Calculator. The component manufacturers may not always dimension their components in accordance with the limits shown in the IPC-7351 Land Pattern Calculator. However, these limits may be used as criteria for go/no-go acceptance of the component. The LMC dimensions are those that have been used in the equations described in 3.1 for determining the recommended land pattern.

Dimensions that have had their tolerance spread reduced are so indicated in the tables. Parts that are available with shape characteristics or tolerance limits that fall outside the recommended norms require land patterns that must be altered slightly from those presented.

Users of these specialized parts are encouraged to develop their own land patterns which then become unique to a specific component vendor part. A dimensioning system with specific equations has been provided to facilitate unique land pattern development or enhance process usage.

3.1.5.3 Land Pattern Dimensions Land pattern dimensions are provided in the IPC-7351 Land Pattern Calculator according to the concepts of MMC.

Sometimes a dimension is presented as a minimum distance. This occurs when defining a space(s) that exists between lands at MMC. The printed board manufacturer may not always inspect the printed board in accordance with the limit concepts provided in this standard. However, these limits may be used as the criteria for go/no-go acceptance of the printed board land pattern. The dimensions provided in this standard are those that have been used in the equations described in 3.1.5 for determining the recommended land patterns. The MMC for each land pattern analysis level describes the most robust joint or land protrusion for that level land pattern.

Note: It is the responsibility of the user to verify the SMT land patterns used for achieving an undisturbed mounting process, including testing and an ensured reliability for the product stress conditions in use. In addition the size and shape of the proposed land pattern may vary according to the solder mask aperture, the size of the land pattern extension (dog bone), the via within the extension, or if the via is in the land pattern itself. Also, the usage of oblong, or rounded, land pattern pads is considered advantageous for lead free soldering processes in comparison with rectangular pads, as the oblong shape provides for a pull of the solder on the pad. An exception to this rule occurs when the heel portion of the land pattern has to be trimmed due to the component body standoff being less than the paste mask stencil thickness or the heel having to be trimmed due to “Thermal Pad” interference. In these two cases, the rectangular pad shape is preferred to compensate for the reduction in copper area of the land pattern pad length.

3.1.5.4 Courtyard Determination The courtyard, or “courtyard excess”, of any land pattern is the smallest area that provides a minimum electrical and mechanical clearance of both the component maximum boundary extremities and/or the land pattern maximum boundary extremities. The intent of the courtyard is to aid the designer in determining the minimum area occupied by the combination of component and land pattern. The information provided in Table 3-2 through Table 3-22 is intended to relate to those excesses that should be added to the maximum dimension to derive the appropriate courtyard condition.

As an example, if a component was the major determining factor of the boundary condition, it would have the excess added to the dimensions. The same holds true for a land pattern that has the greater extremities. If either dimension were 14.5 mm, and the excess from Table 3-2 through Table 3-22 indicated an excess of 0.8 mm, the resulting courtyard would theoretically be 16.1 mm. The tables further define a round-up feature. If the round-up were recommended as being to the nearest 0.5 mm, the courtyard would become 16.5 mm.

It should be noted that 16.5 mm is a number that, when divided by 2 to obtain the component centroid, provides 2 decimal places to the right of the number. It therefore may be appropriate to keep this number in an even approximation such as 16.6 mm. This would provide 8.3 mm to either side of the center of the component to help designers position the component in relation to some grid or placement algorithm.

When manufacturing allowances must be considered in the design process the courtyard represents the starting point of the minimum area needed for the component and the land pattern. Manufacturing, assembly and testing representatives should assist in determining the additional room needed to accommodate placement, testing, modification and repair. This manufacturing allowance is usually dependent on the density and complexity of the product, and is not defined in this document. The manufacturing allowance is determined by application and manufacturing process requirements (see Figure 3-5).

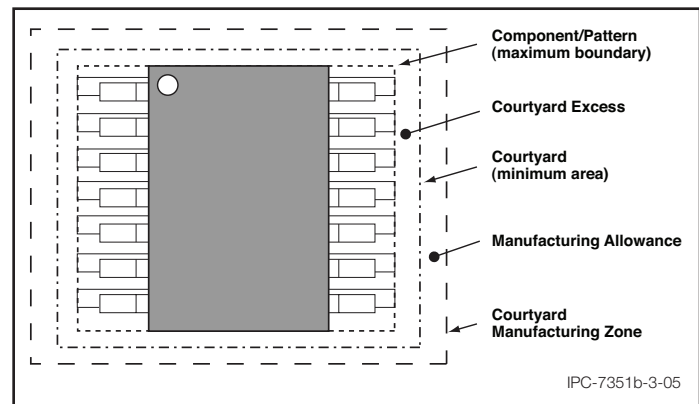


Figure 3-5 Courtyard Boundary Area Condition

3.1.5.5 Land Pattern Naming Convention Each land pattern in the IPC-7351 has received a name containing a prefix for the device type, a pin pitch, a nominal lead span corresponding to the “L” dimension (or a pair of nominal lead spans for components with termination leads on four sides), and a pin quantity. In the case of ball grid array (BGA) packages, the column and row numbers are given as there are no end termination lead spans. The purpose of the number is to aid in communication between engineering, design, and manufacturing. Specific syntax explanations include:

The + (plus sign) stands for “in addition to” (no space between the prefix and the body size).

Note: This character is used within Table 3-23 to illustrate the land pattern naming convention concept, but is not itself used within the individual land pattern names in the IPC-7351 Land Pattern Calculator.

The - (dash) is used to separate the pin qty.

The X (capital letter X) is used instead of the word “by” to separate two numbers such as height X width like “Quad Packages.”

The _ (underscore) is the separator between pin Qty in Hidden & Deleted pin components.

The suffix letters of L, M and N are reserved by IPC. The suffix letters “L,” “M,” and “N” have been reserved to signify when the land protrusion is at their minimum (least), maximum (most), or median (nominal) protrusion or use environment as follows:

M – Maximum (Most) Material Condition (Density Level A)

N – Median (Nominal) Material Condition (Density Level B)

L – Minimum (Least) Material Condition (Density Level C)

Note 1: Ball Grid Array (BGA) packages may feature land pattern names that indicate a difference in pitch between pads in the row axis vs. pads in the column axis. These are often referred to as “dual pitch BGA”. For example, the BGA land pattern name of BGA48C100X80P6X8_900X1200X120 conveys that the pitch is 0.100 mm in the row axis and 0.80 mm in the column axis.

Note 2: Ball Grid Array (BGA), Dual Flat No-Lead (DFN), Column Grid Array (CGA), Land Grid Array (LGA), Pullback Quad Flat No-Lead (PQFN) and Pullback Small Outline No-Lead (PSON) all have a different concept for developing a land pattern. Effectively, there are no Toe, Side or Heel fillets; rather the land periphery is similar about the entire termination. Whether round or rectangular, once the tolerance is assigned it applies to the periphery of the lands for that particular part.

Note 3: A variation code for the thermal tabs underneath components is outside the scope of IPC-7351 land pattern naming convention. The variances in thermal tab sizes and frequencies per component would quickly make a variation code assignment within the land pattern naming convention unmanageable.

The BGA has a circular periphery that is based on the reduction of the land pattern based on the nominal ball diameter of the BGA as provided by the supplier. The “L”, “M”, and “N” dimensions are based on the land diameter reduction and the amount of excess room provided by the courtyard.

M = 1.5, and 1.27 Pitch; Courtyard = 2.0 mm

N = 1.0, 0.8, 0.65, and 0.5 Pitch; Courtyard = 1.0 mm

L = 0.4, 0.3, and 0.25 Pitch; Courtyard = 0.5 mm

The Pullback lands show a relationship between the part termination and the land pattern. The “L”, “M”, and “N” dimensions are based on the amount of pull back that the land provides about the periphery of the Termination.

Where ever no difference occurs between the “L”, “M”, and “N” dimensions the tables defining the tolerance goals show the same number.

Additional suffixes for alternate components that do not follow JEDEC, EIA or IEC standards are as follows:

“A” – Alternate Component (used for SOP and QFP when component tolerance or height is different)

“B” – Second Alternate Component

Suffixes for reverse pin order are as follows:

20RN = 20 pin part, Reverse Pin Order, Nominal Environment

Suffixes for hidden pins are as follows:

20_24N = 20 pin part in a 24 pin package. The pins are numbered 1 – 24 the hidden pins are skipped. The schematic symbol displays up to 24 pins.

Suffixes for deleted pins are as follows:

24_20N = 20 pin part in a 24 pin package. The pins are numbered 1 – 20. The schematic symbol displays 20 pins.

Additional suffixes for JEDEC and EIA Standard parts that have several alternate packages are as follows:

AA, AB, AC JEDEC or EIA Component Identifier (used primarily on Chip Resistors, Inductors and Capacitors).

The naming conventions provided in Table 3-23 will not be modified except in situations where a conflict among land pattern names must be resolved. Naming conventions may be added to the table as new component families are generated. The most current naming convention listing can be found on the IPC website (www.ipc.org) under the “Knowledge” tab and within “PCB Tools and Calculators”.

Table 3-23 IPC-7351 Land Pattern Naming Convention

Component, Category	Land Pattern Name
Ball Grid Array's	BGA + Pin Qty + C or N + Pitch P + Ball Columns X Ball Rows _ Body Length X Body Width X Height
BGA w/Dual Pitch	BGA + Pin Qty + C or N + Col Pitch X Row Pitch P + Ball Columns X Ball Rows _ Body Length X Body Width X Height
BGA w/Staggered Pins	BGAS + Pin Qty + C or N + Pitch P + Ball Columns X Ball Rows _ Body Length X Body Width X Height
BGA Note: The C or N = Collapsing or Non-collapsing Balls	
Capacitors, Chip, Array, Concave	CAPCAV + Pitch P + Body Length X Body Width X Height - Pin Qty
Capacitors, Chip, Array, Flat	CAPCAF + Pitch P + Body Length X Body Width X Height - Pin Qty
Capacitors, Chip, Non-polarized	CAPC + Body Length + Body Width X Height
Capacitors, Chip, Polarized	CAPCP + Body Length + Body Width X Height
Capacitors, Chip, Wire Rectangle	CAPCWR + Body Length + Body Width X Height
Capacitors, Molded, Non-polarized	CAPM + Body Length + Body Width X Height
Capacitors, Molded, Polarized	CAPMP + Body Length + Body Width X Height
Capacitors, Aluminum Electrolytic	CAPAE + Base Body Size X Height
Ceramic Flat Packages	CFP127P + Lead Span Nominal X Height - Pin Qty
Column Grid Array, Circular Lead	CGA + Pin Qty + C + Pitch P + Pin Columns X Pin Rows _ Body Length X Body Width X Height
Column Grid Array, Square Lead	CGA + Pin Qty + S + Pitch P + Pin Columns X Pin Rows _ Body Length X Body Width X Height
Crystals (2 leads)	XTAL + Body Length X Body Width X Height
Dual Flat No-lead	DFN + Body Length X Body Width X Height - Pin Qty
Diodes, Chip	DIOC + Body Length + Body Width X Height
Diodes, Molded	DIOM + Body Length + Body Width X Height
Diodes, MELF	DIOMELF + Body Length + Body Diameter
Diodes, Side Concave, 2 Pin	DIOSC + Body Length X Body Width X Height - Pin Qty
Diodes, Side Concave, 4 Pin	DIOSC + Pitch P + Body Length X Body Width X Height - Pin Qty
Dual-Inline Package (Butt Mounted)	DIP + Pitch P + Lead Span Nominal X Height - Pin Qty
Fuses, Molded	FUSM + Body Length + Body Width X Height
Inductors, Chip	INDC + Body Length + Body Width X Height
Inductors, Molded	INDM + Body Length + Body Width X Height
Inductors, Precision Wire Wound	INDP + Body Length + Body Width X Height
Inductors, Chip, Array, Concave	INDCAV + Pitch P + Body Length X Body Width X Height - Pin Qty
Inductors, Chip, Array, Flat	INDCAF + Pitch P + Body Length X Body Width X Height - Pin Qty
Land Grid Array, Circular Lead	LGA + Pin Qty + C + Pitch P + Pin Columns X Pin Rows _ Body Length X Body Width X Height
Land Grid Array, Square Lead	LGA + Pin Qty + S + Pitch P + Pin Columns X Pin Rows _ Body Length X Body Width X Height
Land Grid Array, Rectangle Lead	LGA + Pin Qty + R + Pitch P + Pin Columns X Pin Rows _ Body Length X Body Width X Height
LED's, Molded	LEDM + Body Length + Body Width X Height
LED's, Side Concave, 2 Pin	LEDSC + Body Length X Body Width X Height - Pin Qty
LED's, Side Concave, 4 Pin	LEDSC + Pitch P + Body Length X Body Width X Height - Pin Qty
Oscillators, Side Concave	OSCSC + Pitch P + Body Length X Body Width X Height - Pin Qty
Oscillators, J-Lead	OSCL + Pitch P + Body Length X Body Width X Height - Pin Qty
Oscillators, L-Bend Lead	OSCL + Pitch P + Body Length X Body Width X Height - Pin Qty
Oscillators, Corner Concave	OSCCC + Body Length X Body Width X Height
Plastic Leaded Chip Carriers	PLCC + Pitch P + Lead Span L1 X Lead Span L2 Nominal X Height - Pin Qty
Plastic Leaded Chip Carrier Sockets Square	PLCCS + Pitch P + Lead Span L1 X Lead Span L2 Nominal X Height - Pin Qty
Quad Flat Packages	QFP + Pitch P + Lead Span L1 X Lead Span L2 Nominal X Height - Pin Qty
Ceramic Quad Flat Packages	CQFP + Pitch P + Lead Span L1 X Lead Span L2 Nominal X Height - Pin Qty
Quad Flat No-lead	QFN + Pitch P + Body Width X Body Length X Height - Pin Qty + Thermal Pad
Pull-back Quad Flat No-lead	PQFN + Pitch P + Body Width X Body Length X Height - Pin Qty + Thermal Pad
Quad Leadless Ceramic Chip Carriers	LCC + Pitch P + Body Width X Body Length X Height - Pin Qty
Quad Leadless Ceramic Chip Carriers (Pin 1 on Side)	LCCS + Pitch P + Body Width X Body Length X Height - Pin Qty
Resistors, Chip	RESC + Body Length + Body Width X Height
Resistors, Molded	RESM + Body Length + Body Width X Height
Resistors, MELF	RESMELF + Body Length + Body Diameter
Resistors, Chip, Array, Concave	RESCAV + Pitch P + Body Length X Body Width X Height - Pin Qty
Resistors, Chip, Array, Convex, E-Version (Even Pin Size)	RESCAXE + Pitch P + Body Length X Body Width X Height - Pin Qty
Resistors, Chip, Array, Convex, S-Version (Side Pins Diff)	RESCAXS + Pitch P + Body Length X Body Width X Height - Pin Qty
Resistors, Chip, Array, Flat	RESCAF + Pitch P + Body Length X Body Width X Height - Pin Qty
Small Outline Diodes, Flat Lead	SODFL + Lead Span Nominal + Body Width X Height
Small Outline IC, J-Leaded	SOJ + Pitch P + Lead Span Nominal X Height - Pin Qty
Small Outline Integrated Circuit, (50 mil Pitch SOIC)	SOIC127P + Lead Span Nominal X Height - Pin Qty
Small Outline Packages	SOP + Pitch P + Lead Span Nominal X Height - Pin Qty
Small Outline No-lead	SON + Pitch P + Body Width X Body Length X Height - Pin Qty + Thermal Pad
Pull-back Small Outline No-lead	PSOP + Pitch P + Body Width X Body Length X Height - Pin Qty + Thermal Pad
Small Outline Transistors, Flat Lead	SOTFL + Pitch P + Lead Span Nominal X Height - Pin Qty
SOD (Example: SOD3717X135 = JEDEC SOD123)	SOD + Lead Span Nominal + Body Width X Height
SOT89 (JEDEC Standard Package)	SOT89
SOT143 & SOT343 (JEDEC Standard Package)	SOT143 & SOT343
SOT143 & SOT343 Reverse (JEDEC Standard Package)	SOT143R & SOT343R
OT23 & SOT223 Packages (Example: SOT230P700X180-4)	SOT + Pitch P + Lead Span Nominal X Height - Pin Qty
TO (Generic DPAK - Example: TO228P970X238-3)	TO + Pitch P + Lead Span X Height - Pin Qty

Notes:

1. All dimensions are in Metric Units
2. All Lead Span and Height numbers go two places past the decimal point and "include" trailing Zeros
3. All Lead Span and Height numbers go two place before the decimal point and "remove" leading Zeros
4. All Chip Component Body Sizes are one place to each side of the decimal point
5. All Pitch Sizes are two places to the right & left of decimal point with no leading Zeros but include trailing zeros