



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-7912A

End-Item DPMO for Printed Circuit Board Assemblies

IPC-7912A

January 2004

A standard developed by IPC

Supersedes IPC-7912
July 2000

2215 Sanders Road, Northbrook, IL 60062-6135

Tel. 847.509.9700 Fax 847.509.0700

www.ipc.org



Documents

Document Sharing Hub

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee (TAEC) that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.

Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/790-5372.

Thank you for your continued support.



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-7912A

End-Item DPMO for Printed Circuit Board Assemblies

Developed by the DPMO and Assemblies, Attributes and Variables
Identification Task Group (5-22g) of the Assembly and Joining
Processes Committee (5-20) of IPC



Supersedes:

IPC-7912 - July 2000

Users of this publication are encouraged to participate in the
development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798



This Page Intentionally Left Blank



Documents
Document Sharing Hub

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the DPMO and Assemblies, Attributes and Variables Identification Task Group (5-22g) of the Assembly and Joining Processes Committee (5-20) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Assembly and Joining Processes Committee

Chair
James F. Maguire
Intel Corporation

DPMO and Assemblies, Attributes and Variables Identification Task Group

Co-Chairs
Tom Olafsson
Teradyne Inc.

Greg Hurst
BAE SYSTEMS

Technical Liaisons of the IPC Board of Directors

Nilesh S. Naik
Eagle Circuits Inc.

Sammy Yi
Flextronics International

DPMO and Assemblies, Attributes and Variables Identification Task Group

Michael Aldrich, Analog Devices Inc.
Pierre Audette, Nortel Networks
Bill F. Barthel, Plexus Corp.
Gerald Leslie Bogert, Bechtel Plant Machinery, Inc.
Richard Bradford, Raytheon Company
Rex L. Breunsbach, Electronic Controls Design Inc. (ECD)
Fritz R. Byle, Kester Northrop Grumman
Alan S. Cash, Northrop Grumman Corporation
Yves Desrochers, Nortel Networks
Ashok Dhawan, C-MAC Electronic Systems Inc.
Darrin Dodson, Alcatel USA
Adele Doucet, Nortel Networks
Jean-Yves Gagne, Nortel Networks
Candace M. Garcia, Sypris Electronics, LLC
Denis Gignac, Nortel Networks
John Gonser, Harris Corporation, GCSD
Marsha Hall, Techdyne, Lytton Inc.
Greg Hurst, BAE SYSTEMS
Les Hymes, The Complete Connection

David Ingraham, OSDA Contract Services Inc.
Ed Irons, Harris Corporation, GCSD
James Jenkins, Harris Corporation, GCSD
Dr. Thomas N. Kennedy, Soletron Corporation
Frank N. Kimmey, C.I.D.+, PowerWave
Tim Kruse, Plexus NPI Plus
Harjinder Ladhar, Soletron Corporation
Richard Latta, Plexus Corp.
Doug A. Lishka, The Boeing Company
Jeffery J. Luttkus, Lockheed Martin Space Systems Company
James F. Maguire, Intel Corporation
Chris McManus, Delta Group Electronics
Stephen Meeks, Jr., White Electronic Designs Corporation
Jay Messner, The Boeing Company
James H. Moffitt, Moffitt Consulting Services
Graham Naisbitt, Concoat Limited
John S. Norton, Xerox Corporation
Michaela Nyland, Phoenix International Corp.

Tom Olafsson, Teradyne Inc.
Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information
Mel Parrish, Soldering Technology International
Scott B. Penin, Paradigm Manufacturing LLC
Thomas Perea, Honeywell Inc.
Frank M. Piccolo, Adeptron Technologies Corporation
Curtis L. Putnam, Boeing Company
Guy M. Ramsey, ACI/EMPF
Peter Randklev, Benchmark Electronics Inc.
Mark Rusciolelli, Nexus Custom Electronics Inc.
Vit Sklenar, Robert Bosch (Australia) Pty.
John W. Smith, Siemens
Jorgen Svensson, Sony Ericsson Mobile Communications AB
Richard Vernon, Phoenix International Corp.
John M. Weckwerth, Jabil Circuit, Inc.
Robert Willis, The SMART Group
Don Youngblood, Honeywell Inc.

Table of Contents

1 OVERVIEW	1	4.2 Assumptions	2
1.1 Scope	1	4.3 DPMO Index	3
1.2 Purpose	1	4.3.1 Calculation of Component DPMO	3
1.3 Terms and Definitions	1	4.3.2 Calculation of Placement DPMO	3
1.3.1 DPMO.....	1	4.3.3 Calculation of Termination DPMO	3
1.3.2 DPMO Index	1	4.3.4 Calculation of Assembly DPMO	3
2 APPLICABLE DOCUMENTS	1	4.4 Calculation Examples	3
3 CATEGORIZATION OF OPPORTUNITIES AND DEFECTS	1	APPENDIX A	6
3.1 Component Opportunities (o_c).....	1	APPENDIX B	7
3.2 Component Defect (d_c)	1		
3.3 Placement Opportunity (o_p)	1		
3.4 Placement Defect (d_p)	2		
3.5 Termination Opportunity (o_t)	2		
3.6 Termination Defect (d_t)	2		
3.7 Assembly Opportunity (o_a)	2		
3.8 Assembly Defect (d_a)	2		
3.9 Listing of Countable Defects	2		
4 CALCULATION OF END-ITEM METRICS	2		
4.1 DPMO Calculation	2		

Figures

Figure 4-1	Calculations for Completed Electronic Assemblies: Conceptual Diagram	2
Figure 4-2	Example One	3
Figure 4-3	Example Two	4

Tables

Table 4-1	Example One	3
Table 4-2	Example Two	4

End-Item DPMO for Printed Circuit Board Assemblies

1 OVERVIEW

1.1 Scope This document is intended to define standard methods for the categorization of defects related to electronic printed board assemblies (PBAs). This document will provide consistent methodologies for calculating the following benchmark indices:

- Defects Per Million Opportunities Index (DPMO Index)
- Component DPMO
- Placement DPMO
- Termination DPMO
- Assembly DPMO

DPMO as applied in this standard is a measurement taken on completed product. Only those defects detected or discovered at an assembly's completed product evaluation are to be included in the calculations. A companion standard, IPC-9261 *In-Process DPMO and Estimated Yield for PWAs* is used to develop DPMO indices for measuring in-process assembly steps.

It is recognized that a manufacturing index can be obtained through a variety of methods. Overall Manufacturing Index (OMI) is explained in detail in Appendix B.

This document is intended to be used in conjunction with assembly acceptance standards such as IPC/EIA J-STD-001 or IPC-A-610. This document is for benchmarking and is NOT intended to describe how to track or otherwise log defect types or drive corrective action. In-process DPMO is outside the scope of this document.

Note: The intent of this document is to define “how” to arrive at several DPMO related indices. There is no intent to dictate the “number” of assemblies or data points that are needed to calculate these indices. Users of this document are cautioned when comparing one manufacturer's indices to one another due to differences in assembly complexity and the amount of data that may have been used in a computation.

1.2 Purpose To define a consistent method for calculating DPMO on completed electronic assemblies in order to benchmark the electronic assembly process.

- It is assumed that each printed board assembly that is inspected will be 100% inspected for all defects identified in Appendix A and only inspected PBAs will be used to determine opportunity count.
- 100% inspection efficiency is assumed.

1.3 Terms and Definitions

1.3.1 DPMO (Defects per Million Opportunities) is defined as the number of defects divided by the number of defect opportunities, multiplied by 1,000,000.

1.3.2 DPMO Index DPMO Index is defined as the total number of defects on a completed assembly divided by the total number of opportunities for that assembly, multiplied by 1,000,000.

2 APPLICABLE DOCUMENTS¹

IPC/EIA J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

IPC-A-610 Acceptability of Electronic Assemblies

3 CATEGORIZATION OF OPPORTUNITIES AND DEFECTS

3.1 Component Opportunities (o_c) The term “component” is defined as each device or piece of hardware that may be assembled onto a printed wire board (PWB). Solder, glue dots, and other similar assembly materials are not to be included in this DPMO calculation. The PWB is considered to be one component.

The total opportunity count for each “component” is one. An electronic component with multiple leads still counts as one. Processes, such as cleaning operations, do not add component opportunity counts. The finished PWA is not an opportunity.

3.2 Component Defect (d_c) A component defect is damage to a component exceeding the limits of the component specification, or those described in IPC/EIA J-STD-001 or IPC-A-610, and/or damage that results in non-usability of that component. Component defects include both visible defects and non-visible defects (physical/electrical). Even though a component may have more than one component defect; any one or combination of multiple component defects on any single component will have a maximum defect count of one for that component.

Example: A component could be both dimensionally incorrect and have major surface flaws, however, these result in a defect count of one.

3.3 Placement Opportunity (o_p) The term “placement” refers to the proper placement of components based on the bill of materials. Nonpopulated component locations each

1. www.ipc.org

count as one placement opportunity. The PWB does not have a placement opportunity. This is because the printed wiring board has no “placement” of its own. Therefore, the number of placement opportunities will be one less than the number of components. The total opportunity count for each placed component is one.

3.4 Placement Defect (d_p) A placement defect is any component presence and/or positioning error that has occurred during an assembly operation that violates the dimensional criteria specified for that component in IPC/EIA J-STD-001 or IPC-A-610. Example: exceeding maximum side or toe overhang. Even though a component may have more than one placement defect, any one or combination of multiple placement defects on any single component will have a maximum defect count of one for that placement.

Example: A rectangular component could exhibit both a violation of maximum toe overhang and maximum side overhang; however, this results in a defect count of one.

3.5 Termination Opportunity (o_t) The term “termination” is defined as any hole, land or other surface (such as component to component attachment) to which a component is electrically terminated. The termination opportunity count includes nonpopulated component lands, excluding via holes. Include any terminal onto which a wire is electrically attached.

The total opportunity count for each “termination” is one; e.g., a 208 lead component will have 208 opportunities. A wire typically will have one termination at each end for a total of two opportunities. Note that if a single component termination connects to multiple lands on the PWB (i.e., split pad or shield) then only count the terminations of the component, not the number of lands. In this case you would count only one termination opportunity. In the event of a defect to either one or both of the split pads, the maximum count of defects would be one.

3.6 Termination Defect (d_t) A termination defect is any electrically joined termination that violates the requirements specified in IPC/EIA J-STD-001.

A single connection may exhibit more than one defect, however any one or combination of multiple termination defects on any single termination will have a maximum defect count of one. If two terminations are shorted by one solder bridge, each termination is counted as a defect.

Example: An “L” lead may exhibit both insufficient heel solder and insufficient side joint length, however, one defect is counted.

3.7 Assembly Opportunity (o_a) An assembly opportunity is an overall opportunity for a defect that is not captured within termination, component and placement opportunity categorization. Examples of processes that provide such opportunities are conformal coating and cleaning. Whether considering one or multiple processes, each PWA has only one assembly opportunity.

3.8 Assembly Defect (d_a) An assembly defect is a defect that applies once to a PWA. Examples would be solder balls or a board flooded in the wave. Each assembly defect should be logged at the process step where the defect is found. It is recognized that the total number of assembly defects for a series of processes may exceed the number of opportunities in extreme cases. This result is expected (more than one assembly defect per assembly, on average) and would impact a combined DPMO including the result. The intent of this document is not to rely on such combined metrics.

3.9 Listing of Countable Defects Appendix A provides a complete listing of the defects that may be counted.

4 CALCULATION OF END-ITEM METRICS

4.1 DPMO Calculation Figure 4-1 provides users with a graphical representation of DPMO.

Note: The DPMO index will be dominated by processes having higher opportunity counts (typically terminations).

4.2 Assumptions The following lists assumptions for calculation of end-item metrics:

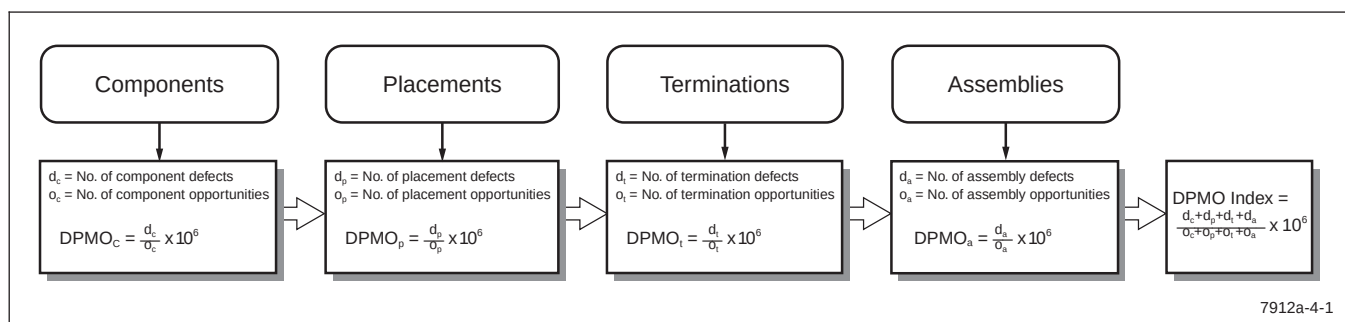


Figure 4-1 Calculations for Completed Electronic Assemblies: Conceptual Diagram