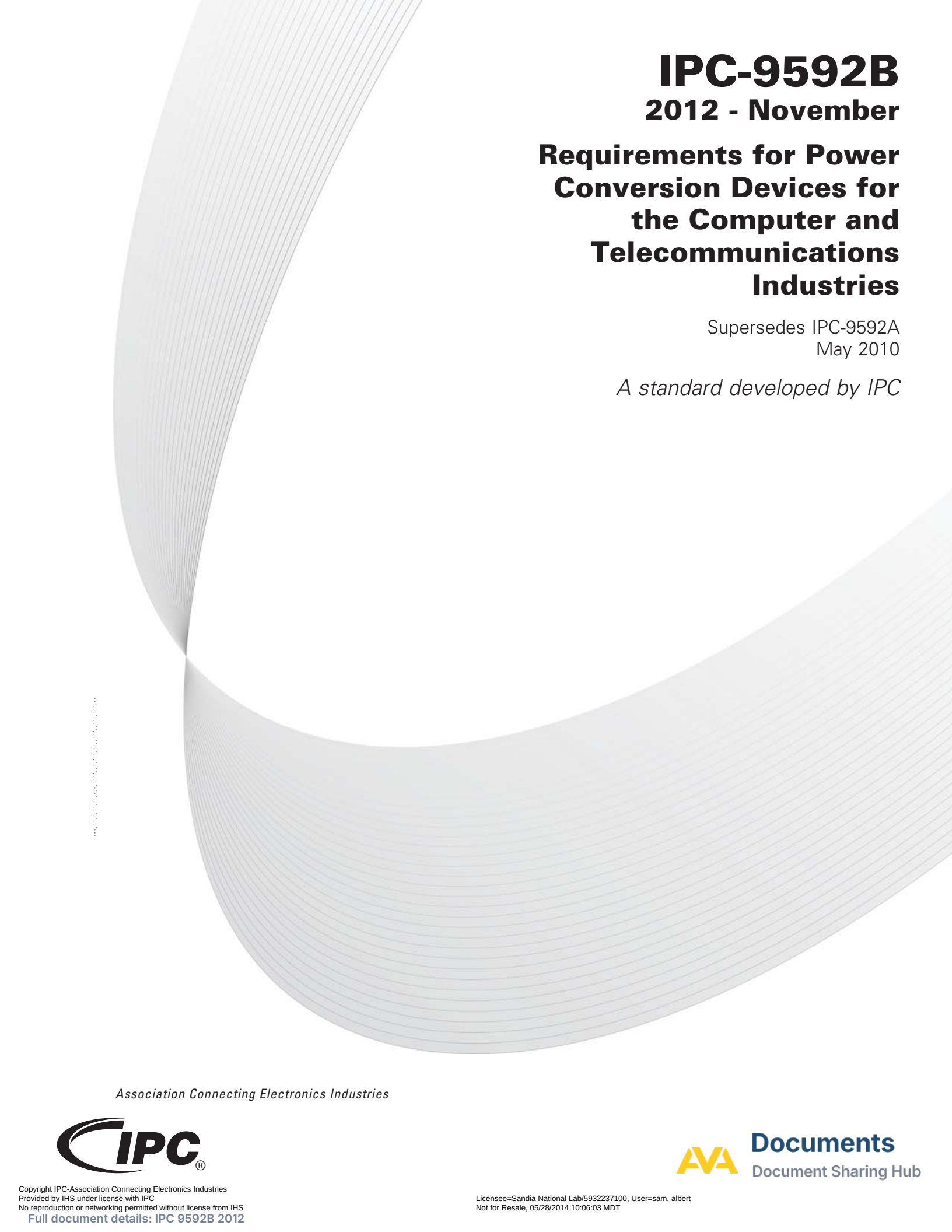




# **IPC-9592B**

## **2012 - November**

### **Requirements for Power Conversion Devices for the Computer and Telecommunications Industries**

Supersedes IPC-9592A  
May 2010

*A standard developed by IPC*

*Association Connecting Electronics Industries*



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IPC-9592B

# Requirements for Power Conversion Devices for the Computer and Telecommunications Industries

Developed by the Power Conversion Devices Standard Subcommittee (9-82) of IPC

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Users of this publication are encouraged to participate in the development of future revisions.

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## Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the Power Conversion Devices Standard Subcommittee (9-82) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of IPC extend their gratitude.

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# Table of Contents

|                                                                     |    |                                                                                                    |    |
|---------------------------------------------------------------------|----|----------------------------------------------------------------------------------------------------|----|
| <b>1 SCOPE</b> .....                                                | 1  | 3.3.6.1 ac to dc and dc to dc PCD Data Sheet .....                                                 | 13 |
| 1.1 Statement of Scope .....                                        | 1  | 3.4 Material Control and Labeling .....                                                            | 13 |
| 1.2 Description .....                                               | 1  | 3.5 Revision Control .....                                                                         | 14 |
| 1.3 Purpose .....                                                   | 1  | <b>4 DESIGN FOR RELIABILITY</b> .....                                                              | 14 |
| 1.4 Order of Precedence When Purchasing .....                       | 1  | 4.1 Reliability Prediction (FIT) .....                                                             | 14 |
| <b>2 APPLICABLE DOCUMENTS AND TERMS AND DEFINITIONS</b> .....       | 2  | 4.2 Component Selection .....                                                                      | 14 |
| 2.1 IPC .....                                                       | 2  | 4.3 Metal Corrosion with PCD Electronic Assembly .....                                             | 15 |
| 2.2 International .....                                             | 2  | 4.3.1 Corrosion Testing .....                                                                      | 15 |
| 2.2.1 Canadian Standards Association (Canada) .....                 | 2  | 4.3.2 Appropriate Printed Circuit Board Surface Finishes .....                                     | 15 |
| 2.2.2 International Organization for Standardization ....           | 2  | 4.3.2.1 Surface Finishes for the Computer Industry .....                                           | 15 |
| 2.2.3 GB China .....                                                | 2  | 4.3.2.2 Surface Finishes for Telecommunication Industry .....                                      | 15 |
| 2.2.4 International Electrotechnical Commission .....               | 2  | 4.3.3 Surface Finishes for Assembly Parts, ECM as a Failure Mechanism and Conformal Coatings ..... | 15 |
| 2.2.5 Norma Oficial Mexicana .....                                  | 3  | 4.3.3.1 Components (Thick Film) .....                                                              | 15 |
| 2.2.6 European Norm .....                                           | 3  | 4.3.3.2 Connectors .....                                                                           | 15 |
| 2.3 United States .....                                             | 3  | 4.3.3.3 Electrochemical Migration Failures .....                                                   | 16 |
| 2.3.1 TELCORDIA .....                                               | 3  | 4.3.3.4 Conformal Coatings .....                                                                   | 16 |
| 2.3.2 JEDEC .....                                                   | 4  | 4.4 Derating Guidelines .....                                                                      | 17 |
| 2.4 Terms, Definitions and Acronyms .....                           | 4  | 4.4.1 Derating Documentation Requirements .....                                                    | 17 |
| <b>3 PRODUCT SPECIFICATION AND DOCUMENTATION REQUIREMENTS</b> ..... | 9  | 4.5 Design Failure Modes and Effects Analysis (DFMEA) .....                                        | 18 |
| 3.1 Product Classification System .....                             | 9  | 4.6 Voltage Spacing Design Requirements .....                                                      | 20 |
| 3.1.1 Class I General or Standard PCDs .....                        | 9  | 4.7 Moisture Sensitivity Level (MSL) Rating of Surface Mount Power Conversion Devices (PCDs) ..... | 20 |
| 3.1.2 Class II Enhanced or Dedicated Service PCDs ...               | 9  | 4.7.1 Application of MSL Guidelines During Assembly of PCDs .....                                  | 20 |
| 3.1.3 ac to dc and dc to dc PCDs .....                              | 9  | 4.7.2 Applicability of MSL Requirements .....                                                      | 21 |
| 3.1.4 Three Categories of Product .....                             | 9  | 4.7.3 Identification of MSL Rating .....                                                           | 21 |
| 3.2 Documentation Requirements .....                                | 9  | 4.7.4 Packaging Requirements .....                                                                 | 21 |
| 3.3 Data Sheet Information - Form, Fit and Function .....           | 10 | 4.7.5 Handling Requirements for BMP Users .....                                                    | 21 |
| 3.3.1 Input Power Specifications .....                              | 10 | 4.7.6 Qualification Testing for MSL .....                                                          | 21 |
| 3.3.1.1 ac to dc PCD Data Sheet .....                               | 10 | <b>5 DESIGN AND QUALIFICATION TESTING</b> .....                                                    | 21 |
| 3.3.1.2 dc to dc PCD Data Sheet .....                               | 10 | 5.1 Design Verification Testing (DVT) .....                                                        | 22 |
| 3.3.2 Logic, Indicator, and Control Specifications .....            | 11 | 5.1.1 Scope of Testing .....                                                                       | 22 |
| 3.3.3 Output Specifications .....                                   | 11 | 5.1.2 Sample Size .....                                                                            | 22 |
| 3.3.3.1 ac to dc PCD Data Sheet .....                               | 11 | 5.1.3 Test Methods .....                                                                           | 22 |
| 3.3.3.2 dc to dc PCD Data Sheet .....                               | 12 | 5.1.4 Test Conditions and Limits .....                                                             | 22 |
| 3.3.3.3 ac to dc and dc to dc PCD Data Sheet .....                  | 13 | 5.1.5 DVT Report .....                                                                             | 22 |
| 3.3.4 Reliability .....                                             | 13 |                                                                                                    |    |
| 3.3.4.1 ac to dc and dc to dc PCD Data Sheet .....                  | 13 |                                                                                                    |    |
| 3.3.5 Safety and Regulatory .....                                   | 13 |                                                                                                    |    |
| 3.3.5.1 ac to dc and dc to dc PCD Data Sheet .....                  | 13 |                                                                                                    |    |
| 3.3.6 Physical Dimensions and Electrical Connections .....          | 13 |                                                                                                    |    |



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|                                                                                                   |    |                                                                                        |    |
|---------------------------------------------------------------------------------------------------|----|----------------------------------------------------------------------------------------|----|
| 5.1.6 Design Verification Testing -<br>ac Input Parameters .....                                  | 22 | 5.2.3.3.2 Minimum Requirements for<br>Thermocouples .....                              | 26 |
| 5.1.6.1 Test Conditions .....                                                                     | 22 | 5.2.3.3.3 Minimum Reporting Requirements for<br>Vibration and Thermal Monitoring ..... | 26 |
| 5.1.6.2 Parameters to Be Measured .....                                                           | 22 | 5.2.3.4 Laboratory Test Equipment .....                                                | 26 |
| 5.1.7 Design Verification Testing - dc<br>Input Parameters .....                                  | 23 | 5.2.3.4.1 Source and Loading .....                                                     | 26 |
| 5.1.7.1 Test Conditions .....                                                                     | 23 | 5.2.3.4.2 Monitoring Capability .....                                                  | 27 |
| 5.1.7.2 Parameters to Be Measured .....                                                           | 23 | 5.2.3.4.3 Additional Hardware .....                                                    | 27 |
| 5.1.8 Design Verification Testing - Overall<br>Input to Output Parameters .....                   | 23 | 5.2.3.4.4 Minimum Reporting Requirements for<br>Laboratory Equipment .....             | 27 |
| 5.1.8.1 Test Conditions .....                                                                     | 23 | 5.2.3.5 Sample Size .....                                                              | 27 |
| 5.1.8.2 Parameters to Be Measured .....                                                           | 23 | 5.2.3.6 Functional Test Requirements .....                                             | 27 |
| 5.1.9 Design Verification Testing - dc<br>Output Parameters .....                                 | 23 | 5.2.3.6.1 Pre-Test Verification .....                                                  | 27 |
| 5.1.9.1 Test Conditions .....                                                                     | 23 | 5.2.3.6.2 Thermal Step Stress/Combined<br>Environment/Rapid Thermal Cycle .....        | 27 |
| 5.1.9.2 Parameters to Be Measured .....                                                           | 23 | 5.2.3.6.3 Vibration Step Stress .....                                                  | 27 |
| 5.1.10 Design Verification Testing -<br>Protection Features .....                                 | 23 | 5.2.3.6.4 Monitoring .....                                                             | 27 |
| 5.1.10.1 Test Conditions .....                                                                    | 24 | 5.2.3.7 Test Reporting and Documentation<br>Requirements .....                         | 27 |
| 5.1.10.2 Parameters to Be Measured .....                                                          | 24 | 5.2.3.8 Root Cause Analysis and<br>Corrective Actions .....                            | 28 |
| 5.1.11 Design Verification Testing - Input and<br>Output Signals and Indicators .....             | 24 | 5.2.4 Temperature, Humidity and Bias (THB) .....                                       | 29 |
| 5.1.11.1 Test Conditions .....                                                                    | 24 | 5.2.4.1 Purpose .....                                                                  | 29 |
| 5.1.11.2 Parameters to Be Measured .....                                                          | 24 | 5.2.4.2 Applicability .....                                                            | 29 |
| 5.1.12 Design Verification Testing - Other Electrical<br>Parameters, Features and Functions ..... | 24 | 5.2.4.3 Sample Size .....                                                              | 29 |
| 5.1.12.1 Current Sharing .....                                                                    | 24 | 5.2.4.4 Test Procedure .....                                                           | 29 |
| 5.1.12.2 Test Conditions .....                                                                    | 24 | 5.2.4.5 Pass Criteria .....                                                            | 29 |
| 5.1.12.3 Test Procedure .....                                                                     | 24 | 5.2.5 High Temperature Operating Bias (HTOB) .....                                     | 29 |
| 5.1.13 Design Verification Testing - Hot Swap .....                                               | 24 | 5.2.5.1 Purpose .....                                                                  | 29 |
| 5.1.13.1 Test Conditions .....                                                                    | 24 | 5.2.5.2 Applicability .....                                                            | 30 |
| 5.1.13.2 Test Procedure .....                                                                     | 24 | 5.2.5.3 Sample Size .....                                                              | 30 |
| 5.1.14 Design Verification Testing - Mechanical<br>Compliance .....                               | 24 | 5.2.5.4 Procedure .....                                                                | 30 |
| 5.2 Environmental Stress Testing (EST) .....                                                      | 25 | 5.2.5.5 Pass Criteria .....                                                            | 30 |
| 5.2.1 EST Purpose .....                                                                           | 25 | 5.2.6 Temperature Cycling Test .....                                                   | 30 |
| 5.2.2 Test Sequence for EST .....                                                                 | 25 | 5.2.6.1 Purpose .....                                                                  | 30 |
| 5.2.2.1 Module Preconditioning .....                                                              | 25 | 5.2.6.2 Applicability .....                                                            | 31 |
| 5.2.3 Highly Accelerated Life Test (HALT) .....                                                   | 25 | 5.2.6.3 Sample Size .....                                                              | 31 |
| 5.2.3.1 Scope and Purpose .....                                                                   | 25 | 5.2.6.4 Procedure .....                                                                | 31 |
| 5.2.3.2 HALT Chamber Equipment Requirements .....                                                 | 26 | 5.2.6.5 Monitoring .....                                                               | 31 |
| 5.2.3.2.1 Chamber Thermal and Vibration<br>Capability .....                                       | 26 | 5.2.6.6 Pass Criteria .....                                                            | 32 |
| 5.2.3.2.2 Chamber Minimum Reporting<br>Requirements .....                                         | 26 | 5.2.7 Power and Temperature Cycling (PTC) Test .....                                   | 32 |
| 5.2.3.3 Vibration and Thermal Monitoring<br>Capability .....                                      | 26 | 5.2.7.1 Purpose .....                                                                  | 32 |
| 5.2.3.3.1 Minimum Requirements for<br>Accelerometers .....                                        | 26 | 5.2.7.2 Applicability .....                                                            | 32 |
|                                                                                                   |    | 5.2.7.3 Sample Size .....                                                              | 32 |
|                                                                                                   |    | 5.2.7.4 Procedure .....                                                                | 32 |
|                                                                                                   |    | 5.2.7.5 Pass Criteria .....                                                            | 32 |
|                                                                                                   |    | 5.2.8 Shock and Vibration .....                                                        |    |



|                                                 |    |                                                                      |    |
|-------------------------------------------------|----|----------------------------------------------------------------------|----|
| 5.2.8.1 Purpose .....                           | 33 | 5.2.14.4.1 Purpose .....                                             | 39 |
| 5.2.8.2 Testing Overview .....                  | 33 | 5.2.14.4.2 Applicability .....                                       | 39 |
| 5.2.8.3 Test Sequence .....                     | 33 | 5.2.14.4.3 Sample Size .....                                         | 39 |
| 5.2.8.4 Pass Criteria .....                     | 33 | 5.2.14.4.4 Test Method .....                                         | 39 |
| 5.2.8.5 Test Equipment .....                    | 33 | 5.2.14.4.5 Pass Criteria .....                                       | 39 |
| 5.2.8.6 Device Mounting .....                   | 33 | 5.3 Electromagnetic Susceptability (EMS) and<br>Other Tests .....    | 39 |
| 5.2.9 Random Vibration - Operating .....        | 33 | 5.3.1 Conducted Continuous Wave .....                                | 39 |
| 5.2.9.1 Purpose .....                           | 33 | 5.3.1.1 Purpose .....                                                | 39 |
| 5.2.9.2 Applicability .....                     | 33 | 5.3.1.2 Applicable Devices .....                                     | 39 |
| 5.2.9.3 Sample Size .....                       | 33 | 5.3.1.3 Sample Size .....                                            | 39 |
| 5.2.9.4 Test Method .....                       | 33 | 5.3.1.4 Test Method .....                                            | 39 |
| 5.2.9.5 Pass Criteria .....                     | 35 | 5.3.1.5 Pass Criteria .....                                          | 39 |
| 5.2.10 Random Vibration - Non-Operating .....   | 35 | 5.3.2 Radiated Immunity .....                                        | 40 |
| 5.2.10.1 Purpose .....                          | 35 | 5.3.2.1 Purpose .....                                                | 40 |
| 5.2.10.2 Applicability .....                    | 35 | 5.3.2.2 Applicable Devices .....                                     | 40 |
| 5.2.10.3 Sample Size .....                      | 35 | 5.3.2.3 Sample Size .....                                            | 40 |
| 5.2.10.4 Test Method .....                      | 35 | 5.3.2.4 Test Method .....                                            | 40 |
| 5.2.10.5 Pass Criteria .....                    | 36 | 5.3.2.5 Pass Criteria .....                                          | 40 |
| 5.2.11 Shock - Operating .....                  | 36 | 5.3.3 Conducted Electrical Fast Transient (EFT) .....                | 40 |
| 5.2.11.1 Purpose .....                          | 36 | 5.3.3.1 Purpose .....                                                | 40 |
| 5.2.11.2 Applicability .....                    | 36 | 5.3.3.2 Applicable Devices .....                                     | 40 |
| 5.2.11.3 Sample Size .....                      | 36 | 5.3.3.3 Sample Size .....                                            | 40 |
| 5.2.11.4 Test Method .....                      | 36 | 5.3.3.4 Test Method .....                                            | 40 |
| 5.2.11.5 Pass Criteria .....                    | 36 | 5.3.3.5 Pass Criteria .....                                          | 40 |
| 5.2.12 Free Fall .....                          | 36 | 5.3.4 Conducted Surges .....                                         | 40 |
| 5.2.12.1 Purpose .....                          | 36 | 5.3.4.1 Purpose .....                                                | 40 |
| 5.2.12.2 Applicability .....                    | 36 | 5.3.4.2 Applicable Devices .....                                     | 41 |
| 5.2.12.3 Sample Size .....                      | 36 | 5.3.4.3 Sample Size .....                                            | 41 |
| 5.2.12.4 Test Method .....                      | 36 | 5.3.4.4 Test Method .....                                            | 41 |
| 5.2.12.5 Pass Criteria .....                    | 37 | 5.3.4.5 Pass Criteria .....                                          | 41 |
| 5.2.13 Drop Test .....                          | 37 | 5.3.5 Ring Waves .....                                               | 41 |
| 5.2.13.1 Purpose .....                          | 37 | 5.3.5.1 Purpose .....                                                | 41 |
| 5.2.13.2 Applicability .....                    | 37 | 5.3.5.2 Applicable Devices .....                                     | 41 |
| 5.2.13.3 Sample Size .....                      | 37 | 5.3.5.3 Sample Size .....                                            | 41 |
| 5.2.13.4 Test Method .....                      | 37 | 5.3.5.4 Test Method .....                                            | 41 |
| 5.2.13.5 Pass Criteria .....                    | 37 | 5.3.5.5 Pass Criteria .....                                          | 41 |
| 5.2.14 Other Environmental Stress Testing ..... | 38 | 5.3.6 Electrostatic Discharge - Packaged<br>Power Devices .....      | 41 |
| 5.2.14.1 Corrosion Resistance .....             | 38 | 5.3.6.1 Purpose .....                                                | 41 |
| 5.2.14.2 Dust Resistance .....                  | 38 | 5.3.6.2 Applicable Devices .....                                     | 41 |
| 5.2.14.3 SMT Attachment Reliability .....       | 38 | 5.3.6.3 Sample Size .....                                            | 41 |
| 5.2.14.3.1 Purpose .....                        | 38 | 5.3.6.4 Test Method .....                                            | 41 |
| 5.2.14.3.2 Applicability .....                  | 38 | 5.3.6.5 Pass Criteria .....                                          | 42 |
| 5.2.14.3.3 Sample Size .....                    | 38 | 5.3.7 Electrostatic Discharge - Board Mounted<br>Power Devices ..... |    |
| 5.2.14.3.4 Test Method .....                    | 38 |                                                                      |    |
| 5.2.14.3.5 Pass Criteria .....                  | 39 |                                                                      |    |
| 5.2.14.4 Through Hole Pin Solderability .....   | 39 |                                                                      |    |



|                                                                |    |                                                                                                     |     |
|----------------------------------------------------------------|----|-----------------------------------------------------------------------------------------------------|-----|
| 5.3.7.1 Purpose .....                                          | 42 | 6.5 Qualification of Change .....                                                                   | 49  |
| 5.3.7.2 Sample Size .....                                      | 42 | 6.5.1 Content of each Product Change<br>Notice (PCN)/End of Life (EOL)/<br>Product Alert (PA) ..... | 49  |
| 5.3.7.3 Test Method .....                                      | 42 | 6.5.1.1 Product Alerts (PA) .....                                                                   | 49  |
| 5.3.7.4 Pass Criteria .....                                    | 42 | 6.5.1.2 End of Life .....                                                                           | 49  |
| 5.3.8 Power Line Disturbance Immunity - ac Input ...           | 42 | 6.5.1.3 Changes Requiring a PCN (include<br>but are not limited to): .....                          | 49  |
| 5.3.8.1 Purpose .....                                          | 42 | <b>7 MANUFACTURING CONFORMANCE TESTING</b> .....                                                    | 50  |
| 5.3.8.2 Applicability .....                                    | 42 | 7.1 Manufacturing Conformance Tests .....                                                           | 50  |
| 5.3.8.3 Sample Size .....                                      | 42 | 7.2 Early Manufacturing Conformance Test<br>Requirements .....                                      | 50  |
| 5.3.8.4 Conditions for All Tests .....                         | 42 | 7.3 Final Assembly Test Requirements .....                                                          | 50  |
| 5.3.8.5 Short Term Input Undervoltage<br>and Overvoltage ..... | 42 | 7.3.1 Functional Tests .....                                                                        | 50  |
| 5.3.8.6 Input Undervoltage - Performance Level B ...           | 42 | 7.3.2 Stress Tests (Short Term Reliability Tests -<br>BI/HASS) .....                                | 51  |
| 5.3.8.7 Immunity to Slow Reduction of<br>Input Voltage .....   | 43 | 7.3.3 Ongoing Reliability Testing (ORT) .....                                                       | 51  |
| 5.3.9 Electromagnetic Emissions .....                          | 43 | 7.3.4 Safety Tests .....                                                                            | 51  |
| 5.3.9.1 Devices with ac Input .....                            | 43 | 7.3.5 Final QA Cosmetic/Mechanical Audit .....                                                      | 52  |
| 5.3.9.1.1 Conducted Emissions .....                            | 43 | 7.3.5.1 QA Out of Box Audit (OBA) .....                                                             | 52  |
| 5.3.9.1.2 Harmonic Input Current .....                         | 43 | <b>APPENDIX A</b> .....                                                                             | 53  |
| 5.3.9.1.3 Radiated Emissions .....                             | 43 | <b>APPENDIX A-1</b> .....                                                                           | 67  |
| 5.3.9.2 Packaged Power Devices with dc Input .....             | 43 | <b>APPENDIX B</b> .....                                                                             | 70  |
| 5.3.9.2.1 Conducted Emissions .....                            | 44 | <b>APPENDIX C</b> .....                                                                             | 75  |
| 5.3.9.2.2 Radiated Emissions .....                             | 44 | <b>APPENDIX C-1</b> .....                                                                           | 76  |
| 5.3.9.3 Board Mounted Power Devices<br>with dc Input .....     | 44 | <b>APPENDIX C-2</b> .....                                                                           | 78  |
| 5.3.9.3.1 Conducted Emissions .....                            | 44 | <b>APPENDIX C-3</b> .....                                                                           | 79  |
| 5.3.9.3.2 Radiated Emissions .....                             | 44 | <b>APPENDIX C-4</b> .....                                                                           | 81  |
| 5.3.10 Acoustic Noise .....                                    | 44 | <b>APPENDIX D</b> .....                                                                             | 92  |
| 5.3.10.1 Purpose .....                                         | 44 | <b>APPENDIX E</b> .....                                                                             | 110 |
| 5.3.10.2 Applicability .....                                   | 44 |                                                                                                     |     |
| 5.3.10.3 Sample Size .....                                     | 44 |                                                                                                     |     |
| 5.3.10.4 Test Method .....                                     | 44 |                                                                                                     |     |
| 5.3.11 Product Safety .....                                    | 44 |                                                                                                     |     |
| 5.3.12 Regulatory: “Green” .....                               | 44 |                                                                                                     |     |
| <b>6 QUALITY PROCESSES</b> .....                               | 44 |                                                                                                     |     |
| 6.1 Quality Management Systems .....                           | 44 |                                                                                                     |     |
| 6.1.1 Process Failure Modes and Effects Analysis .....         | 45 |                                                                                                     |     |
| 6.1.2 Statistical Process Control .....                        | 45 |                                                                                                     |     |
| 6.1.3 Process Capability Assessment .....                      | 46 |                                                                                                     |     |
| 6.1.4 Measurement Capability Assessment .....                  | 46 |                                                                                                     |     |
| 6.1.5 Corrective Action Process .....                          | 46 |                                                                                                     |     |
| 6.1.6 Calibration .....                                        | 47 |                                                                                                     |     |
| 6.1.7 Continuous Improvement .....                             | 47 |                                                                                                     |     |
| 6.1.8 Process Quality Metrics .....                            | 47 |                                                                                                     |     |
| 6.2 Sub-Tier Supplier .....                                    | 47 |                                                                                                     |     |
| 6.3 Materials Traceability Requirements .....                  | 48 |                                                                                                     |     |
| 6.4 Change Authorization .....                                 | 48 |                                                                                                     |     |

### Figures

|            |                                                                                        |    |
|------------|----------------------------------------------------------------------------------------|----|
| Figure 4-1 | DFMEA Worksheet Form Used by Many<br>Companies .....                                   | 19 |
| Figure 4-2 | DFMEA Severity, Occurrence and Detection<br>Ranking Chart Used by Many Companies ..... | 19 |
| Figure 4-3 | Uninsulated Conductor Voltage-Spacing<br>Requirements .....                            | 20 |
| Figure 5-1 | Class I PCDs Operating Vibration Test:<br>Acceleration vs. Frequency .....             | 34 |
| Figure 5-2 | Class II PCDs Operating Vibration Test:<br>Acceleration vs. Frequency .....            | 34 |
| Figure 5-3 | Class I PCDs Non-Operating Vibration:<br>Acceleration vs. Frequency .....              | 35 |
| Figure 7-1 | Typical Manufacturing Conformance<br>Test Flow .....                                   | 11 |



|              |                                                                |     |            |                                                                                                                                                            |    |
|--------------|----------------------------------------------------------------|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| Figure C-4-1 | Ripple Test Setup for dc Output Measurement .....              | 84  | Table 5-13 | Required Performance Levels for Conducted Continuous Wave Testing .....                                                                                    | 39 |
| Figure C-4-2 | Timing Definition Guideline .....                              | 86  | Table 5-14 | Required Performance Levels for Radiated Immunity Testing .....                                                                                            | 40 |
| Figure D-1   | Graphical Display of Typical HALT .....                        | 92  | Table 5-15 | Required Performance Levels for Conducted Electrical Fast Transient Testing .....                                                                          | 40 |
| Figure D-2   | Operating and Destruct Margin .....                            | 94  | Table 5-16 | Required Performance Levels for Conducted Surges Testing .....                                                                                             | 41 |
| Figure D-3   | Low Temperature Limits Test .....                              | 94  | Table 5-17 | Required Performance Levels for Ring Waves Testing .....                                                                                                   | 41 |
| Figure D-4   | High Temperature Limits Test .....                             | 96  | Table 5-18 | Required Performance Levels for Electrostatic Discharge Testing - Packaged Power Devices .....                                                             | 42 |
| Figure D-5   | Rapid Thermal Transitions Test .....                           | 98  | Table 5-19 | Minimum Passing Voltage for Electrostatic Discharge Testing - Board Mounted Power Devices .....                                                            | 42 |
| Figure D-6   | Random Vibration Step Test .....                               | 99  | Table 5-20 | Minimum Requirements to Meet Performance Level A When Device is Tested for Short Term Input Undervoltage and Overvoltage .....                             | 43 |
| Figure D-7   | Typical Input Voltage Test Profile .....                       | 101 | Table 5-21 | Minimum Requirements to Meet Performance Level B When Device is Tested for Input Undervoltage (perform all combinations of % reduction and duration) ..... | 43 |
| Figure D-8   | Input Voltage Cycle .....                                      | 102 |            |                                                                                                                                                            |    |
| Figure D-9   | Typical Output Load Test Profile .....                         | 103 |            |                                                                                                                                                            |    |
| Figure D-10  | Output Load Cycle .....                                        | 103 |            |                                                                                                                                                            |    |
| Figure D-11  | A Typical Combined Stress Test Profile .....                   | 105 |            |                                                                                                                                                            |    |
| Figure D-12  | One Cycle of Combined Stress Test Profile .....                | 105 |            |                                                                                                                                                            |    |
| Figure D-13  | Example Showing HASA Thermal Plus Vibration Test Profile ..... | 108 |            |                                                                                                                                                            |    |
| Figure E-1   | Input Power Cycling Diagram .....                              | 112 |            |                                                                                                                                                            |    |
| Figure E-2   | Unpowered Thermal Cycle Profile .....                          | 112 |            |                                                                                                                                                            |    |

### Tables

|            |                                                              |    |             |                                                                             |     |
|------------|--------------------------------------------------------------|----|-------------|-----------------------------------------------------------------------------|-----|
| Table 4-1  | MSL Levels per the Table 5.1 in IPC/ JEDEC J-STD-020 .....   | 21 | Table A-1   | Derating Guidelines for Capacitors .....                                    | 54  |
| Table 5-1  | Minimum Sample Size for HALT Tests .....                     | 27 | Table A-2   | Derating Guidelines for Resistors .....                                     | 56  |
| Table 5-2  | Minimum Sample Size for THB Tests .....                      | 29 | Table A-3   | Derating Guidelines for Diodes and Transistors .....                        | 58  |
| Table 5-3  | Minimum Sample Size for HTOB Tests .....                     | 30 | Table A-4   | Derating Guidelines for Magnetics .....                                     | 60  |
| Table 5-4  | Sample Sizes for Temperature Cycling Tests .....             | 31 | Table A-5   | Derating Guidelines for Microcircuits and Hybrid Microcircuits .....        | 62  |
| Table 5-5  | Minimum Number of Cycles for Temperature .....               | 31 | Table A-6   | Derating Guidelines for Miscellaneous Electricals and Electronics .....     | 63  |
| Table 5-6  | Temperature Limits for Temperature Cycling Tests .....       | 31 | Table A-1-1 | Conversions Between MTBF, AFR and FIT ...                                   | 68  |
| Table 5-7  | Inspection Cycles for Temperature Cycling Test .....         | 31 | Table D-1   | Cycle Details .....                                                         | 107 |
| Table 5-8  | Minimum Sample Size for Power and Temperature Tests .....    | 32 | Table E-1   | Acceptable Failure Rates for Test Time Reduction/Sampling/Elimination ..... | 111 |
| Table 5-9  | Steps Required for Power and Temperature Cycling Tests ..... | 32 | Table E-2   | BI Time Reduction Requirements .....                                        | 113 |
| Table 5-10 | Operating Vibration Profile Charts .....                     | 35 | Table E-3   | HASS Thermal Cycle Count Reduction Requirements .....                       | 114 |
| Table 5-11 | Non-Operating Vibration Profile Charts .....                 | 36 |             |                                                                             |     |
| Table 5-12 | Height of Fall for Free Fall Testing .....                   | 37 |             |                                                                             |     |



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# Requirements for Power Conversion Devices for the Computer and Telecommunications Industries

## 1 SCOPE

**1.1 Statement of Scope** This document standardizes the requirements for power conversion devices (PCDs) for the computer and telecommunications industries. The phrase “power conversion devices” refers to ac to dc and dc to dc modules, converters and power supplies. This specification sets the requirements for design; qualification testing; conformance testing and manufacturing quality/reliability processes, but does not include the functional requirements of the specific equipment.

**1.2 Description** Power Conversion Devices (PCDs) addressed in this document are used in the electronics industry to provide conversion of main power sources, usually ac, to lower dc voltages either for direct use of electronic circuits, or as a secondary source for additional dc to dc PCDs to provide several dc voltage levels for various electronic devices in a product. Any deviations due to applicable regulatory standard updates take precedence over this document.

**Performance Parameters** are comprised of mechanical, electrical, environmental, quality/reliability and regulatory requirements:

Mechanical requirements include form and size, connector and wiring configurations and cooling needs.

Electrical requirements define the electrical interface, including power source (ac or dc), input voltage, frequency and current needs, output voltages and current capabilities and, where applicable, logic controls.

Environmental requirements entail both operating and shipping temperatures, humidity, shock and vibration limits.

Quality/Reliability Assurance requirements include definitions and requirements for the design and testing of the quality and reliability of PCDs.

Regulatory requirements are international standards for safety, electronic interference and environmental impact of PCDs.

**Methods** This document describes specific methods to meet the defined performance parameters. These methods are **Design for Reliability**, **Design Qualification Testing**, **Manufacturing Conformance Testing**, and **Quality Processes**. In addition, this document provides guidance to improve corrosion resistance of PCDs used in harsh environments and specifies key **Regulatory Requirements** pertaining to PCDs.

**1.3 Purpose** The purpose of this document is to create a set of consistent specifications and methods to assure suitability, quality, safety and reliability of PCDs for the electronics industry. These specifications will apply to suppliers of PCDs, including their design and testing, and will provide guidelines for the end user to ensure adequate specifications for use in their products. All of the specifications and requirements defined in this document are intended to be part of suppliers' PCDs certifications outlined by the customers and will ship with first article and any design changes to the PCD, on request by the user.

**1.4 Order of Precedence When Purchasing** In the event of conflict when this document is utilized for purchasing a product addressed by this IPC standard, the following order of precedence **shall** apply:

- a. Purchase order.
- b. Master drawing.
- c. This standard.
- d. Applicable documents (see Section 2).

## 2 APPLICABLE DOCUMENTS AND TERMS AND DEFINITIONS

### 2.1 IPC<sup>1</sup>

**IPC J-STD-001** Requirements for Soldered Electrical and Electronic Assemblies

**IPC/ECA J-STD-002** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

**IPC J-STD-004** Requirements for Soldering Fluxes

**IPC/JEDEC J-STD-020** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

**IPC/JEDEC J-STD-033** Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

**IPC-T-50** Terms and Definitions for Interconnecting and Packaging Electronic Circuits

**IPC-A-610** Acceptability of Electronic Assemblies

**IPC-6012** Qualification and Performance Specification for Rigid Printed Boards

**IPC-9591** Performance Parameters (Mechanical, Electrical, Environmental and Quality/Reliability) For Air Moving Devices

**IPC-9701** Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

### 2.2 International

#### 2.2.1 Canadian Standards Association (Canada)<sup>2</sup>

**CAN/CSA C22.2 No. 60950-1** Safety of Information Technology Equipment, Including Electrical Business Equipment

#### 2.2.2 International Organization for Standardization<sup>3</sup>

**ISO 3741** Determination of sound power levels of noise sources - Precision methods for broad-band sources in reverberation rooms (equivalent to ANSI/NAIS S12.51)

**ISO 3744** Determination of sound power levels of noise sources using sound pressure - Engineering method in an essentially free field over a reflecting plane (equivalent to ANSI/NAIS S12.54)

**ISO 7779** Acoustics - measurement of airborne noise emitted by information technology and telecommunications equipment

**ISO 9001** Quality management systems - Requirements

**ISO 9296** Acoustics - Declared noise emission values of computer and business equipment

**ISO 10302** Method for the measurement of airborne noise emitted by small air-moving devices (equivalent to ANSI S12.11)

#### 2.2.3 GB China<sup>4</sup>

**GB 4943-2001** Safety of Information Technology Equipment (Including Electrical Business Equipment)

#### 2.2.4 International Electrotechnical Commission<sup>5</sup>

**IEC 60028-2-27** Environmental Testing - Part 2.27 Test Ea and guidance: Shock

**IEC 60068-2-31** Environmental Testing - Part 2.31 Test Ee: Drop and topple, primarily for equipment-type specimens

**IEC 60068-2-32** Environmental Testing - Part 2.32 Test Ed: Freefall

1. [www.ipc.org](http://www.ipc.org)

2. [www.csa.org](http://www.csa.org)

3. [www.iso.org](http://www.iso.org)

4. [www.bzcbs.com](http://www.bzcbs.com)

5. [www.iec.ch](http://www.iec.ch)

**IEC 60068-2-64** Environmental Testing - Part 2.64 Test Fh: Vibration, broad-band random (digital control) and guidance

**IEC 60529** Degrees of Protection Provided by Enclosures (equivalent to EN 60529)

**IEC 60812** Analysis Techniques for System Reliability - Procedure for Failure Mode and Effects Analysis (FMEA)

**IEC 60950-1** Safety of Information Technology Equipment, Including Electrical Business Equipment, including all national deviations as specified in the current CB Bulletin

**IEC 61000** Electromagnetic Compatibility (EMC) - consists of over 30 documents covering electromagnetic and radio interference, power line interference, ESD, immunity and ground (earth connection) testing

**IEC 61000-3-2** Electromagnetic Compatibility (EMC) - Part 3-2 Limits - Limits for Harmonic Current Emissions (Equipment Input Current  $\leq 16A$  per Phase)

**IEC 61000-4-2** Electromagnetic Compatibility (EMC) - Part 4-2 Testing and Measurement Techniques - Electrostatic Discharge Immunity Test

**IEC 61000-4-3** Electromagnetic compatibility (EMC) - Part 4-3 Testing and measurement techniques - Radiated, radio-frequency, electromagnetic field immunity test

**IEC 61000-4-4** Electromagnetic compatibility (EMC) - Part 4-4 Testing and measurement techniques - Electrical fast transient/burst immunity test

**IEC 61000-4-5** Electromagnetic compatibility (EMC) - Part 4-5 Testing and measurement techniques - Surge immunity test

**IEC 61000-4-6** Electromagnetic compatibility (EMC) - Part 4-6 Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields

**IEC 61000-4-11** Electromagnetic compatibility (EMC) - Part 4-11 Testing and measurement techniques - Voltage dips, short interruptions and voltage variations immunity tests

**IEC 61000-4-12** Electromagnetic compatibility (EMC) - Part 4-12 Testing and measurement techniques - Oscillatory waves immunity test

**IEC 62040-1-1** 1st edition and IEC 62040-1-2 1st edition Components and Subassemblies used in Uninterruptible Power Systems (and their equivalent adapted standards such as EN 62040-1-1 or UL 1778, etc., in different countries)

### **2.2.5 Norma Oficial Mexicana<sup>6</sup>**

**NOM-019-SCFI** Safety of Data Processing Equipment

### **2.2.6 European Norm<sup>7</sup>**

**EN 50116** Information Technology Equipment. Routine Electrical Safety Testing in Production

**EN 55022** Information Technology Equipment - Radio Disturbance Characteristics - Limits and Methods of Measurement

**EN 55024** Information Technology Equipment - Immunity Characteristics - Limits and Methods of Measurement

## **2.3 United States**

### **2.3.1 TELCORDIA<sup>8</sup>**

**GR-78-CORE** Generic Requirements for the Physical Design and Manufacture of Telecommunications Products and Equipment

6. [www.normex.com.mx](http://www.normex.com.mx)

7. [www.ansi.org](http://www.ansi.org)

8. [www.telcordia.com](http://www.telcordia.com)



**GR-1274-CORE** Generic Requirements for Reliability Qualification Testing of Printed Wiring Assemblies Exposed to Hygroscopic Dust

**SR332** Reliability Prediction Procedure for Electronic Equipment

### 2.3.2 JEDEC<sup>9</sup>

**EIA/JESD22-A101** Steady State Temperature Humidity Bias Life Test

**JESD22-A108** Temperature, Bias and Operating Life

**JESD22-A114** Electrostatic Discharge (ESD) Sensitivity Testing - Human Body Model (HBM)

**JESD47** Stress-Driven Qualification of Semiconductor Circuits

**2.4 Terms, Definitions and Acronyms** The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined below.

**AABUS** – (As an Acronym): As Agreed Between User and Supplier

– (As a Term): Indicates additional or alternate requirements to be decided between the user and the supplier in the procurement documentation. Examples include contractual requirements, modifications to purchase documentation and information on the drawing. Agreements can be used to define test methods, conditions, frequencies, categories or acceptance criteria within a test, if not already established.

**Accelerometer** – Instruments used for measuring and analyzing acceleration and vibration. The two types of accelerometers used during HALT are Control Accelerometers and UUT Accelerometers.

**AFR** – Annualized Failure Rate: The average failure rate of a population of products normalized to a year.

**ASD** – Acceleration Spectral Density.

**AST** – Accelerated Stress Testing.

**AQL** – Average Quality Level.

**Arrhenius Relationship** – Mathematical model for relation of failure rate to temperature.

**ATE** – Automated Test Equipment.

**Baseplate** – A mounting surface used to conduct heat away from a PCD.

**BI** – Burn-In.

**BIA** – Burn-In audit.

**BOM** – Bill of Material.

**BMP** – Board Mount Power: Refers to encapsulated and open PWB power converters that are mounted on larger PWBs.

**CIP** – Continuous Improvement Process.

**Corrective Action (CA)** – A change implemented in a design or process to eliminate a product weakness or flaw. Corrective actions may include changes in parts or material sources, product design, and production process changes.

**Cp** – Process Capability: An indicator of process capability using the ratio of specification width to process variation.

**Cpk** – Process Capability Index: Adjustment of Cp for the effect of a noncentered distribution. Measures how close a process is running to its specification limits, relative to the natural variability of the process and center of the distribution.

**CTE** – Coefficient of Thermal Expansion

**Cross Regulation** – In a multiple output power supply, the change in output voltage at one output caused by the load change on another output (adapted from the PSMA Handbook of Terms).

9. [www.jedec.org](http://www.jedec.org)

**Custom** – Product developed and qualified to meet customer specific requirements.

**DFMEA** – Design Failure Modes and Effects Analysis.

**DL** – Destruct Limit: The stress level at which a product will fail. When the stress level is reduced, the failure will not recover (i.e., this is a hard failure).

**DPMO** – Defects per Million Opportunities.

**DVT** – Design Verification Test: A qualification test to assess if design specifications are met.

**Dwell Time** – The amount of time a stress is held stationary while the UUT is being exercised. The dwell time will be calculated after thermal equilibrium is reached. It does not include ramp time.

**EDVT** – Electrical Design Verification Test: A qualification test to assess if electrical design specifications are met.

**EFT** – Electrical Fast Transient.

**EMC** – Electro-Magnetic Compatibility.

**EMI** – Electro-Magnetic Interference.

**EN** – European Norm.

**ESD** – Electro-Static Discharge.

**EST** – Environmental Stress Testing.

**FET** – Field Effect Transistor: includes power MOSFETS commonly used in power converters.

**FIT** – Failures in Time (Reliability):  $1 \text{ FIT} = 1 \text{ Failure}/1,000,000,000 \text{ devices hours}$ . The FIT rate (measured) =  $\Sigma \text{ Failures} \div \Sigma \text{ Operating Hours} * 10^9$  and the relationship of FIT to MTBF is:  $\text{MTBF} = 10^9 / \Sigma \text{ FIT}$  (Also, see MTBF)

**Fit (as part of Form, Fit and Function)** – The suitability or readiness of a product for a particular application, including environmental extremes, marginal parameters, physical and signal compatibility with interfacing systems and surroundings, level of performance, safety margins, reliability, maintainability and installability.

**Form (as part of Form, Fit and Function)** – The weight, density, chemical or material composition, size, shape, structure, appearance, protocol, pattern, composition, configuration and marking/identification of a product.

**Function (as part of Form, Fit and Function)** – The set tasks or purposes for which a product is used by the customer, including all the tasks generally accepted for the product and those specifically designated by the customer.

**Functional Test** – A test on the UUT that measures functionality, UUT operation, and critical parameters to determine if UUT fails to perform to specifications or degradation has occurred within the UUT.

**Fundamental Limit of the Technology (FLT)** – The last stress point beyond which failures can no longer be accelerated before unrealistic failure modes start being introduced. For example, the FLT for a piece of plastic material is the point at which the state of the plastic starts to change and soften. Up to this point, the plastic exhibits an elastic behavior, but beyond it, permanent changes occur in the material.

**Grms** – Root Mean Square value of G, where G is acceleration due to gravity - a measure of dynamic acceleration used in vibration testing.

**HALT** – Highly Accelerated Life Test: Design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits.

**HASA** – Highly Accelerated Stress Audit: Performed via sample testing as opposed to 100% that is done with HASS.

**HASS** – Highly Accelerated Stress Screening: Used to improve the robustness/reliability of a product through test-fail-fix process where the applied stresses may be beyond the specified operating limits (OL) determined by HALT. This is applied to 100% of the manufactured units.

**High Line** – For devices designed to operate from ac sources, the highest rated nominal input voltage. For devices designed to operate from dc sources, the maximum rated input voltage.

**Hipot** – High Potential Testing.

**Hot Swap** – To remove or insert a PCD from or into a system that is operating.

**HTOB** – High Temperature Operating Bias.

**IEC** – International Electrotechnical Commission.

**IFIR** – Initial Field Incident Rate: The defect rate experienced in the first 30 to 90 days of field usage and is the customer's initial experience with the product. The timeframe depends on the user's point of view and needs. That is, if the user is a retail consumer, then 30 days is most common because such consumers begin using the product upon delivery. For commercial or industrial users, the timeframe is more likely 60 to 90 days, where the final product may not be put into service for some number of weeks after the product is delivered and the final commercial rack-mounted device is assembled and placed into service.

**LDL** – Lower Destruct Limit, e.g., -50 °C (also, see DL).

**Life Test** – A test run specifically to determine reliability (or failure rate) over time of a component or product.

**Line Regulation** – The change in output voltage for a specified change in the input voltage, at specified loads with all other factors constant, sometimes expressed as a percentage (adapted from the PSMA Handbook of Terms).

**Load Regulation** – The change in output voltage when a load is changed from one specified steady-state value to another, with all other factors held constant (adapted from the PSMA Handbook of Terms).

**LOL** – Lower Operational Limit, e.g., -20 °C (see OL).

**Low Line** – For devices designed to operate from ac sources, the lowest rated nominal input voltage. For devices designed to operate from dc sources, the minimum rated input voltage.

**LSL** – Lower Specification Limit.

**LTR** – Long Term Reliability: Described as one or more of the following: a) Expected annual failure rate over the usable service life, expressed as a percent per year; b) Expected service life of a product in a given use condition; c) End of life is characterized where it exceeds the annual steady state failure rate by 20%; or d) Service life, expressed in years, for a given use condition.

**LTPD** – Lot Tolerance Percent Defects.

**LRR** – Line Reject Rate: The defect rate experienced at the OEM manufacturing line (not at the PCD supplier's manufacturing line). It defines the number of failed PCD units during the manufacturing and testing of the OEM PCD system. For an item that does not enter the OEM manufacturing process (referred to as a drop shipped PCD from the PCD manufacturer directly to the OEM's customer, there is no LRR metric.

**Maverick Control** – The control process utilized to reduce or eliminate a maverick product.

**Maverick Product** – Product that exhibits significant anomalous characteristics that may cause a higher than normal level of failure anywhere in the user's application or manufacturing line.

**MAX** – The maximum value of a specified parameter.

**MIN** – The minimum value of a specified parameter.

**MSL** – Moisture Sensitivity Level.

**MTBF** – Mean Time Between Failure (Hours):  $MTBF \text{ (measured)} = \Sigma \text{ Operating Hours} \div \Sigma \text{ Failures}$ . For a population of products, MTBF **shall** apply *during* useful life when failure rates are relatively constant. MTBF is *not* a measure of how long a power supply can be expected to survive. (MTBF may be estimated from methods such as Telcordia SR332, or from hardware tests.)

**MTR** – Manufacturing Test Requirement.

**OBA** – Out of Box Audit.

**OCP** – Overcurrent Protection.

**Operational Limit (OL)** – The stress level prior to where one or more of the UUT's operating characteristics are no longer within specification. For vibration, the Operating Limit is also known as the Vibration Operating Limit (VOL). For temperature, the two types of Operating Limits are Upper Operating Limit (UOL) and Lower Operating Limit (LOL).

**ORT** – Ongoing Reliability Test.

**OTP** – Overtemperature Protection.

**OVP** – Overvoltage Protection.

**PARD** – Periodic and Random Disturbance.

**PCB** – Printed Circuit Board (preferred term): Same meaning as PWB (Printed Wiring Board).

**PCD** – Power Conversion Device: Refers to ac to dc and dc to dc modules, converters and printed circuit board assemblies.

**Performance Level A** – No Effect: “Normal performance within limits specified by the manufacturer, requestor or purchaser.”

**Performance Level B** – Temporary Effect, Self Recovering: “Temporary loss of function or degradation of performance which ceases after the disturbance ceases, and from which the equipment under test recovers its normal performance, without operator intervention.”

**Performance Level C** – Needs Help to Recover: “Temporary loss of function or degradation of performance, the correction of which requires operator intervention.”

**Performance Level D** – Damaged Beyond Recovery: “Loss of function or degradation of performance which is not recoverable, owing to damage to hardware or software, or loss of data.”

**PFMEA** – Process Failure Modes and Effects Analysis.

**POL** – Point of Load.

**Power Spectral Density (PSD)** – A measurement of the amplitude and frequency content of a random vibration spectrum, expressed in units of g<sup>2</sup>/Hz. This is also commonly referred to Acceleration Spectral Density (ASD).

**Power Train** – Components that directly transform input power into output power in a PCD.

**Product Family** – Products will be considered similar and of the same family if they use the same power train topology and component set and have printed circuit boards with equivalent minimum spacings with only minor differences for output voltage and alarm/communication functions. In addition, similar products must have equivalent mechanical dimensions with an exception for pin length on BMP devices.

**Product Specification** – The comprehensive description of form, fit and function for a product, often expressed in a product data sheet (although some data sheets are only excerpts of key specifications).

**PSD** – Power Spectral Density.

**PWB** – Printed Wiring Board: Same meaning as PCB (Printed Circuit Board).

**Quasi-Random Vibration** – Nonperiodic vibration that possesses all frequencies within a band limit, and has continuously varying amplitude and phase that is specified as a probability that it will exceed a given value during a time interval.

**Repetitive Shock Vibration (RS)** – A vibration originating from a repeated shock impulse excitation. Typically created from pneumatic hammers impacting a vibration table to which test UUTs are attached.

**RPN** – Risk Priority Number

**RTV** – Room Temperature Vulcanizing: A sealant or coating composed of a silicone elastomeric polymer that cures/vulcanizes by moisture.

**Service Life** – Minimum time, specified in years, during which failure rates are constant or decreasing and cumulative failures for a single wearout failure mechanism do not exceed 1%.

**Six Degrees of Freedom Vibration (6DOF)** – Vibration that has simultaneous acceleration energies in three translations and three rotations.

**SOA** – Safe Operating Area.

**Standard (Noncustom)** – Product developed and qualified without customer specific requirements.

**Statistical Confidence Limits** – Mathematical bounds on distribution estimates made from a sample.

**Statistical Process Control** – Methods using statistical techniques to assess the stability of processes in order to take appropriate action to reduce defects, and to determine the quality level of components, assemblies and products. Often called SPC and also called SQC (Statistical Quality Control).

**Statistical Quality Control** – See Statistical Process Control.

**STRIFE** – Stress + Life Test: Design test used to improve the robustness/reliability of a product through test-fail-fix process where applied stresses are beyond the specified operating limits (also, see HALT).

**Sub-Tier Supplier** – In this document, applies to a component/subassembly supplier to the PCD supplier.

**Supplier** – In this document, applies to a PCD supplier.

**TC** – Temperature Cycling (this implies that this is not powered).

**Temperature Regulation** – The change in output voltage when the ambient temperature is changed from one specified steady-state value to another, with all other factors held constant.

**THB** – Temperature Humidity Bias.

**Thermally Stable** – A device is considered to be thermally stable (at a constant temperature) when the device temperature does not change after three successive temperature readings that are taken at least 15 minutes apart.

**Thermal Stability Time** – The total time from the first temperature reading of a device to the last reading that incorporates at least 3 successive readings, separated by a minimum of 15 minutes apart from each other and during which there is no difference in the device's recorded temperature.

**Thermocouple** – A temperature sensor that is created when two dissimilar metals are joined i.e., fused together. A thermoelectric current flows and creates a voltage potential proportional to temperature. The two types of thermocouples used during a HALT are Control Thermocouples and UUT Thermocouples.

**Thermocouple, Control** – Thermocouple used to control the thermal portion of the chamber that is providing the environmental stress.

**Thermocouple, UUT** – Thermocouples used to take thermal measurements on the UUT.

**Turn-Off Delay Time** – The time from the removal of input power or negation of an on/off control signal until the output voltage starts to decrease (usually measured at the point where the voltage is at 90% of its initial value).

**Turn-Off Fall Time** – The time required for the output voltage to fall, typically measured from the points where the output voltage is equal to 90% of initial value to 10% of initial value.

**Turn-Off Time** – The time from the removal of input power or negation of an on/off control signal until the output voltage is off. This is typically the sum of the Turn-Off Delay Time and the Turn-Off Fall Time

**Turn-On Delay Time** – The time from the application of input power or assertion of an on/off control signal until the output voltage starts to increase (usually measured at the point where the voltage is at 10% of its final value) (adapted from PSMA Handbook of Terms).

**Turn-On Rise Time** – The time required for the output voltage to rise, typically measured from the points where the output voltage is equal to 10% of final value to 90% of final value.

**Turn-On Time** – The time from the application of input power or assertion of an on/off control signal until the output voltage is in regulation and meets the specification. This is typically the sum of the Turn-On Delay Time and the Turn-On Rise Time (adapted from the PSMA Handbook of Terms).

**UDL** – Upper Destruct Limit, e.g., 150 °C or 40 Grms Vibration (see DL).

**UOL** – Upper Operational Limit, e.g., 100 °C or 30 Grms Vibration (see OL).

**Useful Life** – See Service Life.

**User** – In this document, applies to the customer of the PCD supplier.

**USL** – Upper Specification Limit.

**UUT** – Unit under test.

**UVP** – Undervoltage Protection.

**Vsb** – Standby Voltage: An output voltage available when the PCD has an input voltage  $\geq$  the Turn-on voltage, even when the PCD is turned off.

**Wearout** – The time at which a PCD's average failure rate increases by greater than 50%.

### 3 PRODUCT SPECIFICATION AND DOCUMENTATION REQUIREMENTS

The information presented in Section 3, on specifications and documentation requirements, is to be imposed or held to be in-force only for the technology specific application need as discussed between the user and supplier.

**3.1 Product Classification System** Two general classes of PCDs have been established to reflect progressive increases in sophistication, functional performance requirements and testing inspection frequency. It should be recognized that there may be an overlap of both computer and telecommunications end equipment categories in different classes. The user has the responsibility to specify in the contract or purchase order the performance class required for each PCD, and **shall** indicate any exceptions to specific parameters where appropriate.

**3.1.1 Class I General or Standard PCDs** Includes PCDs for consumer computer, telecommunications products and peripherals. These PCDs are generally designed to operate in controlled environments, with intermittent and interruptible service, and with up to five years of service life.

**3.1.2 Class II Enhanced or Dedicated Service PCDs** Includes PCDs for carrier grade telecommunications equipment and network grade computers, sophisticated business machines and instruments where high performance and extended life is required. These PCDs are generally designed to operate in controlled environments, with limited excursions to uncontrolled levels, and with uninterrupted service, and with no less than five years and up to fifteen years of service life.

**3.1.3 ac to dc and dc to dc PCDs** This document **shall** also, where appropriate, differentiate requirements between ac to dc PCDs and dc to dc PCDs, as these devices tend to have different interface requirements due to the characteristics of the sources and load that connect to each type of PCD.

#### 3.1.4 Three Categories of Product

**Category 1:** dc output power supplies to be embedded in equipment, whether the input power is ac or dc.

**Category 2:** Board mounted dc to dc converters including both isolated and nonisolated converters

**Category 3:** ac to dc power supplies used as adapters and chargers that are external to the equipment being powered.

**3.2 Documentation Requirements** The supplier **shall** be able to supply the user with the following pertinent documentation in a reasonable time frame. This documentation **shall** be provided, AABUS, before the evaluation of engineering first article samples and with appropriate NDA protection executed.

- Theory of operation.
- Applicable schematics.
- Qualification test plan.
- EMC reports.
- Reliability data and calculation.
- Design checklist.
- Sample qualification test report.
- DVT report.
- HALT report.
- SMT Power Module Solder Attachment Reliability report.
- Failure Mode and Effect Analysis (FMEA) - Custom products only.
- BOM.
- Approved supplier list for all components.
- PCB artwork.
- Component drawings, including magnetic.
- Manufacturing drawings.
- Regulatory reports (if applicable).
- Change history.
- Mechanical dimension measurements.
- Derating report.

**3.3 Data Sheet Information - Form, Fit and Function** The supplier **shall** provide complete specifications of form, fit and function, including electrical specifications and whether it **shall** be Class I or Class II. The data sheet **shall** be dated and have revision level marked at the bottom of the sheets. Not all of these elements will necessarily apply to a given PCD. Specific values for these parameters cannot be defined in this section as they will depend on the particular device application and requirements.

### 3.3.1 Input Power Specifications

**3.3.1.1 ac to dc PCD Data Sheet** Data sheet **shall** include the following requirements, as applicable (technology specific):

- Nominal input voltage.
- Input voltage range.
- Universal versus switched input voltage.
- Input frequency range.
- Input impedance.
- Inrush current (primary inrush and subsequent pulses).
- Input current at full load.
- Minimum efficiency at a defined load.
- Power factor.
- Turn-on time.
- Auto-restart specifications.
- Input over-current protection and fuse type.
- ac input receptacle type.
- Limits for harmonic current emissions (EN61000-3-2).
- Isolation voltage.
- ac leakage current.
- Slow line transient performance (sag and surge).
- ac line dropout response.
- Full cycle ride thru frequency.
- Maximum chassis current or Y capacitor value.
- Dielectric withstand voltage.
- Energy Star® (US Environmental Protection Agency) requirements.

**3.3.1.2 dc to dc PCD Data Sheet** Data sheet **shall** include the following requirements, as applicable (technology specific):

- Number of voltage inputs.
- Input voltage range(s).
- Minimum efficiency at a full load (define this full load).
- Input over-current/reverse voltage protection and fuse requirements (inrush current as element of fuse requirements).
- Input filter capacitance requirements.
- Conducted EMI.
- Input current at full load.
- No load input current.
- Switching frequency.
- Under voltage lock-out (UVLO).
- Insulation type (e.g., functional, basic or other types - reference: EN/UL 60950).
- Absolute maximum input voltage.

**3.3.2 Logic, Indicator, and Control Specifications** Data Sheet **shall** include the following requirements, as applicable (technology specific):

- Remote on-off signal requirements.
- Remote on-off absolute maximum input voltage.
- Power good signal specifications.
- Communications bus or other serial port specifications.
- Control logic timing requirements.
- Control and logic signal ripple and noise requirements.
- Fan speed control specifications.
- LED indicator specifications.

The PCD supplier **shall** provide the trim equations and schematics, and a table showing the trim resistor values. Additionally, detailed information and recommendation on Trim Control via external voltage or current source (D/A converter), I<sup>2</sup>C or equivalent communications bus, overvoltage, undervoltage, overcurrent and overtemperature (latching, self-resetting, inhibit, crowbar or other applicable methods) performance **shall** be provided on request.

Where the PCD includes the capability for external control (synchronization) of the switching frequency, the signal requirements and the minimum and the maximum switching frequency (capture range) achievable by external control of the PCD **shall** be included.

### 3.3.3 Output Specifications

**3.3.3.1 ac to dc PCD Data Sheet** Data sheet **shall** include the following requirements, as applicable (technology specific):

- Time when the device is considered to be thermally stable.
- dc output voltages.
- Output current capability.
- Minimum load requirements.
- dc voltage output tolerances.
- Output load regulation.
- Output temperature coefficient (%/C), output ripple and noise.
- Common-mode voltage and common-mode current.
- Output-to-output isolation.
- Voltage adjustment range.
- Output transient response to dynamic loading.
- Capacitive loading capability.
- Turn-on overshoot characteristics.
- Over-current protection.
- Short circuit protection.
- Over-voltage and under-voltage protection.
- Reverse current protection.
- Thermal protection.
- Reset after shutdown conditions (hiccup or latch off).
- Remote sense specifications.
- Current sharing/parallel operation.
- Hot swap requirements.
- Output connector specifications.
- Turn-on monotonicity.
- Turn-on delay (start-up time).

- Multiple output rise-time characteristics.
- Hold-up time and cross-regulation of up to four outputs. (Note: For any PCD with greater than four outputs, a guaranteed output voltage range **shall** be specified for each output for any output-load combination).
- Line regulation (each output).

**3.3.3.2 dc to dc PCD Data Sheet** Data sheet **shall** include the following requirements, as applicable (technology specific):

- Number of outputs.
- Line regulation (each output).
- Output capacitance range noise & ripple.
- I/O isolation voltage.
- Isolation resistance.
- Time when the device is considered to be thermally stable.
- dc output voltages.
- Output current capability.
- Minimum load requirements.
- dc voltage output tolerances.
- Output load regulation.
- Output temperature coefficient (%/C).
- Output ripple and noise.
- Common-mode voltage and common-mode current.
- Output-to-output isolation.
- Voltage adjustment range.
- Output transient response to dynamic loading.
- Capacitive loading capability.
- Turn-on overshoot characteristics.
- Over-current protection.
- Short circuit protection.
- Over-voltage and under-voltage protection.
- Reverse current protection.
- Thermal protection.
- Reset after shutdown conditions (hiccup or latch off).
- Remote sense specifications.
- Current sharing/parallel operation.
- Hot swap requirements.
- Output connector specifications.
- Turn-on monotonicity.
- Turn-on delay (start-up time).
- Multiple output rise-time characteristics.
- Hold-up time and cross-regulation of up to four outputs.
- For any PCD with greater than four outputs, a guaranteed output voltage range **shall** be specified for each output for any output-load combination.
- Isolation capacitance.



**3.3.3.3 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** include the following requirements, as applicable (technology specific):

- Storage temperature.
- Operating temperature.
- Nonoperating humidity.
- Operating humidity.
- Nonoperating altitude.
- Operating altitude.
- Cooling requirements method.
- Cooling requirements versus altitude.
- Output derating versus temperature.
- Shipping/storage vibration.
- Operating vibration.
- Shipping/storage shock and operating shock.
- Acoustic noise.
- Class.
- Type.

### 3.3.4 Reliability

**3.3.4.1 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** include reliability specified as FIT rate at a specified operating condition and service life, as applicable - technology specific.

### 3.3.5 Safety and Regulatory

**3.3.5.1 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** list certifications for safety, EMC compliance, lead-free and restricted materials compliance such as RoHS/WEEE certification, as applicable - technology specific.

### 3.3.6 Physical Dimensions and Electrical Connections

**3.3.6.1 ac to dc and dc to dc PCD Data Sheet** Data sheet **shall** include acoustics measurements and methods, complete dimensions, weight, electrical connector definitions and drawings of PCD and of shipping and packaging configurations, as applicable - technology specific.

**3.4 Material Control and Labeling** The PCD supplier **shall** implement a documented, capable material control system for all incoming, in-process and outgoing material. Documentation of a material control plan **shall** be made available. The material control system **shall** include the following elements:

- A. Material Identification** All material **shall** be properly segregated and/or labeled throughout the testing and manufacturing process.
- B. Discrepant Material** All discrepant material **shall** be reworked or disposed of according to the supplier's material control system requirements. Records of all rework and scrap **shall** be kept and summary reports provided to the user on request.
- C. Labeling** All PCDs **shall** be labeled and each PCD **shall** have the markings of 1 through 8, below. For smaller PCDs, space may not be available for all these items on the PCD. Therefore, items are shown in priority of importance, and **shall** be included from item 1, until space is exhausted. Remaining items **shall** be included on the PCD packaging.
  - 1) Part number, serial number and lot date code in human readable text format (space permitting, otherwise in machine readable format).
  - 2) Appropriate regulatory certification labels and any required cautionary statements in appropriate languages.
  - 3) Model and Manufacturer's name.



- 4) For ac to dc units: Nominal ac input voltages and frequencies. Maximum ac input currents. For dc to dc units: Nominal dc input voltages. Maximum dc input currents.
- 5) Nominal Output Voltages and Maximum Continuous Output Currents.
- 6) Maximum Continuous Output Power.
- 7) Country of Origin [i.e., (Product of XXXX) where XXXX is country of final assembly].
- 8) Date of latest printed circuit board artwork revision and revision level of the schematic.

**3.5 Revision Control** All changes affecting form, fit, function, or regulatory agency requirements **shall** cause a next level revision of the supplier's part numbers, or be correlated to a cut-in date that **shall** be tracked by specific production week code contained in the product serial number. Specific information for change traceability **shall** be provided in the Change Notice as discussed in Section 6. The revision control number and/or production date code **shall** be placed on the ID label away from the PCD part number. The user **shall NOT** ship to its customers, nor accept units for revenue that have not been released to manufacturing at the supplier's facility. The release of units to manufacturing indicates that the PCD is fully agency approved (regulatory and safety), where such agency approval is required.

## 4 DESIGN FOR RELIABILITY

This section describes industry best practices for PCD suppliers to specify, design and document the performance and reliability of a PCD. Exceptions to these methods **shall** be documented and shared with the user.

**4.1 Reliability Prediction (FIT)** With user's operating specifications provided, the supplier **shall** define expected reliability of a PCD and the conditions under which the reliability is specified. The overall Power Supply FIT rate **shall** be supplied and **shall** be calculated using Telcordia Technologies SR-332, *Reliability Prediction Procedure for Electronic Equipment* (Method 1, Case 1: Parts Count). The supplier **shall** specify the quality level used. Caution should be exercised when interpreting FIT rates using any predictive model. Models may not consider actual electrical stresses on the power components or may rely strictly on temperature rise estimation and component count. In addition, individual component FIT rate estimates used in these models may not accurately reflect the actual FIT rates of components used by a given power manufacturer. As a result, predictions are often subjective and may vary significantly from actual reliability. Using these methods for comparing one PCD supplier to another could lead the user to the wrong conclusion with respect to the overall reliability of the design.

**4.2 Component Selection** The PCD supplier **shall** have a documented process in place to select all components for product designs and **shall** provide information on all components and all component suppliers to the PCD user as described below. The component selection process **shall** incorporate the following factors:

- The supplier **shall** assure that electrical, mechanical and thermal specifications for all components meet the requirements of the Derating Guidelines, described in 4.3 and Appendix A, for the operating conditions of the PCD design. Exceptions to derating guidelines are allowable only if documented with data supporting that the violation will not negatively impact reliability or service life.
- For custom products, the supplier **shall** assure that effects of all critical component failure modes have been considered in the DFMEA analysis and that appropriate corrective action has been taken where required. Supplier **shall** upon request, provide a report to the user, as described in 4.4.
- The supplier **shall** develop and implement a quality management system that will define quality and technical requirements to their sub-tier suppliers. Quality and technical requirements are defined as quality programs, software control processes, engineering drawings, specifications and functions to be performed by sub-tier suppliers. The PCD supplier may elect to use a contract, purchase order or other suitable means in defining these requirements, as long as the quality and technical requirements are fully documented and that the sub-tier supplier verify understanding and implementation of such requirements.
- The supplier **shall** perform a quality review of all proposed sub-tier suppliers prior to awarding business to a sub-tier supplier as described in 6.2.
- The supplier **shall** review component reliability requirements with their sub-tier suppliers. The supplier **shall** implement testing as required to verify performance and reliability of components, or **shall** assure that the sub-tier supplier implement and report on such testing. Test reports **shall** be provided on a regular basis AABUS.



**4.3 Metal Corrosion with PCD Electronic Assembly** Corrosion resistance has become an important factor for long-term reliability of power modules due to the increasing deployment of electronic products in more corrosive environments in the current global market place and the implementation of the RoHS directive. This section is intended to provide the best practices for improving the corrosion resistance of power modules for multiple instances of corrosion behavior, including creep corrosion, flaking of corrosion products and corrosion that leads to failure of electronic soldered or connector interfaces.

Assembled modules can be subject to corrosion failure, especially in harsher atmospheric conditions encountered in the installation environments. Design guidelines can help reduce the risk as can the utilization of appropriate corrosion resistant materials. However, both field results and controlled environment testing are better predictors of the demise of power modules, as data gathered speaks volumes.

**4.3.1 Corrosion Testing** Mixed flowing gas (MFG) testing is currently the most commonly used of the controlled environment tests. Similarly, field data can also identify a majority of corrosion-susceptible failures, albeit over a much longer time frame compared to the controlled environment testing. Both sources of data allow the user to much more accurately predict the type of corrosion against which the power module needs protection and the rate of corrosion build-up.

Where controlled environment testing is used, the MFG severity should attempt to match the severity of the deployed environment in which the power module is deployed. However, when the deployed environment is not known or cannot be controlled, then testing should be done for the most severe environment that is likely to be encountered. MFG testing conditions developed by Battelle and Telcordia were intended to simulate North American environmental conditions and are commonly used to identify susceptible materials and design weaknesses. For example, Cu corrosion rates forecasted by Telcordia conditions are considered to correlate to one day of testing to one year of field life in a typical North American outdoor setting. However, new test conditions are being designed to show what is likely to occur in more corrosive environments encountered in the current global market place or in severe industrial situations where the ambient atmosphere may be orders of magnitude more corrosive.

#### **4.3.2 Appropriate Printed Circuit Board Surface Finishes**

**4.3.2.1 Surface Finishes for the Computer Industry** Field failure rates that have been encountered in more highly corrosive environments have shown that one of the highest risks for corrosion failures in typical information technology products is from creep corrosion occurring on printed circuit boards. Field data in non-North American markets or in highly corrosive industrial environments such as paper manufacturing or oil refining have shown creep corrosion-induced electronic interconnect failures occurring in as little as 1 year. However, proper choices of surface finish and flux can reduce or eliminate this creep corrosion.

**4.3.2.2 Surface Finishes for Telecommunication Industry** Long service life products, such as some telecom modules, are also at risk for flaking of corrosion products, leading to shorting. This failure mode can occur with any of the common surface finishes, including OSP, immersion silver, and ENIG finishes. It is strongly recommended that the suitability of any surface finish for longer service life modules should be validated in MFG testing. The end result of this work is that every common surface finish has advantages as well as disadvantages when compared to the others - the user must use caution and discretion when choosing the surface finish for the specific application in the assembled and unassembled product. The user is advised to gather all data available and discuss the choice of surface finish with the supply chain involved.

#### **4.3.3 Surface Finishes for Assembly Parts, ECM as a Failure Mechanism and Conformal Coatings**

**4.3.3.1 Components (Thick Film)** For thick film (TF) resistor corrosion mitigation, the selection of corrosion-resistant designs is key. These include large overlap of metal (nickel) over glass to minimize corrosive gas diffusion to the silver underlayer. Some TF resistor manufacturers reduce the corrosion risk by using Gold in place of Silver for the primary conductor layer. Also note that the use of silver palladium (AgPd) alloys for the conductive layer does not eliminate the sulfur corrosion failure mode. Validate corrosion resistance of components with mixed flowing gas tests (ASTM B827-05), or Flowers-of-Sulfur (ASTM B809-95), as needed.

**4.3.3.2 Connectors** Connector corrosion can be mitigated if these guidelines are followed:

- 1) Use connectors with at least  $\frac{3}{4} \mu$  [30  $\mu$ m] of hard gold on contacts. For telecommunication products, use gold thicknesses as specified in Telcordia GR-78-CORE.
- 2) Do NOT use connectors with flash gold on contacts.

- 3) Avoid using Ag as contact finish except in benign environments.
- 4) Select connectors that have passed EIA-364-65 Mixed Flowing Gas class IIIA testing.
- 5) Select connectors that have passed porosity testing according to EIA-364-53 Nitric Acid Vapor Test for gold plating or EIA-364-60 General Methods for Porosity Testing of Contact Finish for Electrical Connectors for palladium/nickel plating (sulfurous acid). Periodically validate contact plating quality.
- 6) Select connectors that have passed EIA-364-31 Humidity Test Procedure for Electrical Connectors, Method II (40 °C ± 3 °C, 93% ± 5% RH) for a minimum of 14 days with no evidence of corrosion on the connector contact area after completion of the test.
- 7) Avoid designs that will mate different metal contacts, such as gold plated contacts to tin plated contacts, as galvanic corrosion will occur.
- 8) Do not use tin plated contacts in non-gas tight contact for G2 environments and beyond due to the risk of fretting corrosion.

**4.3.3.3 Electrochemical Migration Failures** Surface contamination with flux residues, chemical salt residues, particulates, oils, and other substances can contribute to corrosion and electrochemical migration (ECM) failures in finished assemblies. Contamination has been shown to cause both immediate and latent failures depending on the type and severity of the contamination. To increase ECM resistance and contamination-related corrosion resistance:

Ensure all printed boards conform to the ionic cleanliness requirements in IPC-6012.

- 1) Select fluxes that have been tested according to IPC-TM-650, 2.6.3.7, with results such that all resistance readings stabilizing above 100 MΩ and less than two decades below the control.
- 2) For telecommunication products, fluxes **shall** be conformant to Telcordia GR-78 requirement (Section 13.1).
- 3) Select L0 or L1 fluxes, per IPC J-STD-004 classification.
- 4) Select fluxes with hard rosin residues. Residues that are soft and capable of being penetrated by a test probe (referred to being “probeable”) may not encapsulate ionic species, and may amplify the effect of any ionic contamination found on the PWB and components.
- 5) If probeable fluxes must be used, validate the ECM performance of the flux residues in combination with the particular materials that will be present during the service life, including other fluxes, solder masks, and component terminations. Ensure that the residues will not remain tacky while in service in order to minimize the accumulation of particulates.
- 6) If VOC-free fluxes must be used, minimize flux on the top side, and ensure that the flux is fully activated and the water content is completely dried in the process. This process verification is particularly important when using selective wave soldering due to the tendency of pallets to impede full activation and drying of flux in protected areas.

**4.3.3.4 Conformal Coatings** Conformal coatings are sometimes used to provide environmental protection and to improve the corrosion resistance of electronic assemblies. The term “conformal coatings” can refer to any material whose contact surface conforms or shapes itself to the surface on which it is deposited. Typical coating materials include epoxies, polyurethanes, acrylics, and paraxylene. They are deposited in one or more thin layers, and are applied by either flood or flow coating, spraying, spinning, dipping, brushing, or by vapor deposition.

Conformal coatings for environmental protection and corrosion prevention should have the following properties:

- 1) Low moisture penetration rate and moisture absorption potential.
- 2) Good adhesion.
- 3) Electrically insulating (high dielectric strength and high breakdown voltage).
- 4) Low out-gassing.
- 5) Good heat resistance.
- 6) Low stress (flexible or compliant coatings).
- 7) Close match between CTE of coating and CTE of underlying substrate.
- 8) Propensity to suppress metal migration, especially silver.

This document neither encourages nor discourages the use of conformal coatings. When using conformal coatings to improve corrosion resistance:

- 1) Thoroughly clean and bake modules prior to coating to improve adhesion and avoid trapping contamination.
- 2) Minimize pinholes by applying multiple thin applications of the coating, or by drawing a vacuum on the wet coating after application to remove any entrapped air pockets. Use caution with lower viscosity coatings as they will tend to evolve the trapped gasses more easily and more completely, but will result in thinner coatings.
- 3) Select coatings that can withstand all subsequent process and service temperatures.
- 4) Carefully clean any coating material from leads or SMT connectors that may prevent subsequent soldering. Ensure no additional contaminants are introduced in the cleaning process or chemistry.

## REFERENCES for Corrosion Section

For more information about the relative corrosion resistance of surface finishes and a more detailed discussion of the merits of different surface finishes, see the references below.

1. R. Veale. "Reliability of PCB Alternate Surface Finishes In A Harsh Industrial Environment." SMTA 2005.
2. P. Mazurkiewicz. "Accelerated Corrosion of Printed Circuit Boards due to High Levels of Reduced Sulfur Gasses in Industrial Environments." Proceedings of the 32nd International Symposium for Testing and Failure Analysis, Austin, Texas, 2006.
3. C. Xu, J. Smetana, J. Franey, G. Guerra, D. Fleming, W. Reents, D. Willie, Alfredo Garcia I. and X. Jiang. "Creep Corrosion of PWB Final Finishes: Its Cause and Prevention." APEX 2009.
4. R. Schueller. "Creep Corrosion On Lead-Free Printed Circuit Boards In High Sulfur Environments." SMTA 2007.
5. ISA-S71.04-1985, "Environmental Conditions for Process Measurement and Control Systems: Airborne Contaminants," Instrument Society of America, 1985.
6. Coombs. *Printed Circuits Handbook*. McGraw Hill, New York, 2008.

For more information about electrochemical migration (ECM), surface contaminations, and fluxes, consult the references below.

1. Ellis. *Cleaning and Contamination of Electronic Components and Assemblies*. Electrochemical Publications, Scotland, 1986.
2. Tautscher. *The Contamination of Printed Wiring Boards and Assemblies*. Omega Scientific Services, Bothell, WA, 1976.
3. Hwang. *Solder Paste in Electronics Packaging*. Van Nostrand Reinhold, New York, 1989.

Further references on conformal coatings may be found in IPC-CC-830, *Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies*, IPC-HDBK-830, *Guidelines for Design, Selection and Application of Conformal Coatings* and MIL-I-46058, *Military Specification, Insulating Compound, Electrical (for Coating Printed Circuit Assemblies)*. Some of the testing methods can be found in IPC-TM-650, *Test Methods Manual*.

**4.4 Derating Guidelines** In order to provide a reliable power conversion product the supplier **shall** use the method of component derating specified in Appendix A in all electrical designs and **shall** provide details on the derating methods, conditions and results to the PCD user upon request. Documentation reflecting results of the derating analysis is to be according to the items listed in 4.4.1.

Derating is a technique used to ensure that component ratings are not exceeded, either under steady state or transient conditions. The intent of component derating is to improve reliability of electrical components in electronic products by compensating for many variables inherent in a design. Proper component derating will lower failure rates through reduced stresses, reduce the impact of material, manufacturing, and operational variability, and enable continued circuit operation with long-term part parameter shifts.

**4.4.1 Derating Documentation Requirements** The items listed below **shall** be documented for each derating evaluation. Soft and/or hard copies of each item **shall** be provided upon customer request.

- Applicable schematics.
- Data on component(s) where Derating Guidelines are not met, supporting the stress level to which each PCD component is exposed.



**Documents**

Document Sharing Hub

- Electrolytic Capacitor Life calculation from each supplier.
- Electrical and thermal stress levels (e.g., voltage, temperature, etc.) for each derated component shown by reference designator.
- Component ratings and specifications (upon user's request).
- Derated stress level in percent of specified maximum level.
- BOM.
- Approved supplier list for all components.
- Change history.

**4.5 Design Failure Modes and Effects Analysis (DFMEA)** PCD suppliers **shall** complete a Design Failure Mode and Effects Analysis for each custom PCD design on new topologies/architectures with no previous DFMEA, or in cases where there are new technology components or significant component changes. Supplier **shall** provide results of the analysis and of any corrective actions to the customer upon request. DFMEA is to be performed early in the power supply development cycle.

The DFMEA activities are designed to:

1. Recognize and evaluate the potential failure modes of each component in a product and its effects on the product.
2. Identify actions that could eliminate or reduce the chance of the potential failure occurring.
3. Document the process for improvement of future designs.

Areas to be targeted are those critical to proper power supply operation, safety and areas that are considered to be a higher design risk (i.e., new technology, new topology or new circuitry). The intent is not to cover every aspect of every circuit or sub-circuit. DFMEAs performed on similar products or families can be used providing the supplier can provide evidence of correlation. The processes and definitions used in IEC-60812, Analysis Techniques for system reliability - Procedures for failure modes effects analysis (FMEA), **shall** be used as reference.

A DFMEA is a team-based systematic approach that examines the effects of Single Point Failures (SPF) on overall system performance and mitigates system failure risk by corrective action implementation. Key features of a DFMEA are:

1. DFMEA is a team oriented analysis of a system design. DFMEA elements are the building blocks of related information that comprise an analysis. The team approach is essential in identifying DFMEA elements. Although actual document preparation is often the responsibility of an individual, DFMEA inputs **shall** come from a multi-disciplinary team. These contributors are also the major beneficiaries of the document and the knowledge gained in the DFMEA process.
2. DFMEA is a weakness-oriented, bottoms-up approach. To begin, the lowest levels of the system are outlined; this can be the individual components or the lowest assemblies in the system. For each lowest level element, a list of potential failure modes is generated; their local effects, next high-level effects and/or end effects are then determined. DFMEA focuses on failure mode consequences to the product's end use and assesses risk of each.
3. DFMEA is NOT a design review, but always works on the assumption that the design is nominally correct. It addresses single point failure modes. It does not cover improper usage, incorrect problem diagnosis or any software incompatibilities.

The DFMEA *method* consists of defining the DFMEA scope and the system to be investigated, identifying team members and beginning the DFMEA process itself.

The DFMEA *process* includes assignment of roles and responsibilities for team members, defining the scope of the DFMEA (finalizing DFMEA target areas, subsystem level interrelationships and level and type of the approach), differentiating between Causes, Failure Modes and Effects (being aware that failure modes can drive multiple effects, so that each unique end level effect **shall** be separated and causes for each end level effect **shall** be grouped), and defining severity, occurrence and detection rating scales for the DFMEA at hand.

One common format for a DFMEA worksheet report is shown in Figure 4-1. The supplier may share this detail of analysis with the PCD user, or may provide a summarized report listing all failure modes, effects and severity and corrective actions where effects are unacceptable to the operation of the PCD. Figure 4-2 below shows a table of Severity, Occurrence and Detection Ranking used in a DFMEA process. The ranking numbers are used in calculating the value of RPN, which is the product of the severity, occurrence and detection rank numbers. RPN stands for Risk Priority Number, and provides a relative measure of the importance of each effect. The higher the RPN, the higher the priority of its associated failure mode as needing to be resolved. Note that if the severity of a failure mode is a critical safety hazard (fire, electrical shock, etc.)

| Item/<br>Function     | Potential<br>Failure<br>Mode                                     | Potential<br>Effect(s)<br>of Failure                                                                                                       | Severity         | Class           | Potential<br>Cause(s)/<br>Mechanism(s)<br>of Failure | Occurrence | Current<br>Design<br>Controls | Detection | Recommended<br>Action(s)                                                             | Responsibility<br>and Target<br>Completion<br>Date | Results of<br>Action Taken | RPN                                                       |
|-----------------------|------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----------------|------------------------------------------------------|------------|-------------------------------|-----------|--------------------------------------------------------------------------------------|----------------------------------------------------|----------------------------|-----------------------------------------------------------|
| Control<br>Chip<br>U1 | Pin 1-2 short<br>Pin 2-3 short<br>Pin 3-4 short<br>Pin 4-5 short | No effects,<br>however, need<br>VRM supplier Test<br>Plan to verify if<br>they can detect<br>these shorts                                  | 1<br>1<br>1<br>1 |                 | Bad<br>component,<br>Solder<br>bridge                | 1          |                               |           | Need VRM<br>Supplier<br>Test Plan to<br>verify if they<br>can detect<br>these shorts | DJW -<br>10/20/06                                  |                            | 0<br>0<br>0<br>0                                          |
|                       | Pin 5-6 short                                                    | Shuts down the<br>output                                                                                                                   | 4                | Signif.         | Bad<br>component,<br>solder<br>bridge                | 1          |                               | 5         | Improve<br>solder pro-<br>cess and<br>inspection                                     | LBJ -<br>11/15/06                                  |                            | 20                                                        |
|                       | Pin 6-7 short                                                    | V<5v, goes to<br>some artificial<br>V point                                                                                                | 4                | Signif.         | Bad<br>component,<br>solder<br>bridge                | 1          |                               | 5         | Improve<br>solder pro-<br>cess and<br>inspection                                     | LBJ -<br>11/25/06                                  |                            | 20                                                        |
|                       | Pin 7 to Gnd<br>short                                            | Short to ground, V<br>goes up, output V<br>high, full duty<br>cycle (80%-90% of<br>12v), firing SCR<br>and blowing fuse,<br>possible smoke | 5                | Smoke<br>hazard |                                                      | 2          |                               | 5         | Change Lay-<br>out Mask                                                              | QRT -<br>11/30/06                                  |                            | 50<br>Must<br>address<br>because<br>of<br>Smoke<br>Hazard |

**NOTE:** In Figure 4-1, the final failure mode, pin 7 to ground short, may result in emission of smoke (indicated in the Potential Effects of Failure column and in the Class column), a situation that for this example, and for PCDs in general, is an unacceptable hazard condition. Acceptable and unacceptable effects must be defined for each product type as required by the PCD user.

**Figure 4-1 DFMEA Worksheet Form Used by Many Companies**

| Severity |             |                                                                                                                         | Occurrence |             |                                              | Detection |                         |                                                                                                                   |
|----------|-------------|-------------------------------------------------------------------------------------------------------------------------|------------|-------------|----------------------------------------------|-----------|-------------------------|-------------------------------------------------------------------------------------------------------------------|
| Ranking  | Description | Interpretation                                                                                                          | Ranking    | Description | Interpretation                               | Ranking   | Description             | Interpretation                                                                                                    |
| 5*       | Hazardous   | Safety related cata-<br>strophic failure*                                                                               | 5          | Very High   | Failure is almost<br>inevitable, <1 in<br>3  | 5         | Absolute<br>Uncertainly | Undetectable until cata-<br>strophic failure occurs,<br>or there is no design control                             |
| 4        | High        | Product is totally<br>inoperable                                                                                        | 4          | Frequent    | Repeated failure,<br><1 in 8                 | 4         | Remote                  | Remote chance the Design<br>Control will detect a potential<br>Cause of failure or sub-<br>sequent Failure Mode   |
| 3        | Moderate    | Product is operable,<br>but at a reduced level<br>of performance                                                        | 3          | Moderate    | Occasional fail-<br>ure, <1 in 80            | 3         | Low                     | Low chance the Design Con-<br>trol will detect a potential<br>Cause of failure or sub-<br>sequent Failure Mode    |
| 2        | Low         | Product is operable, but<br>comfort or convenience<br>item(s) are inoperable<br>or at a reduced level<br>of performance | 2          | Infrequent  | Relatively few<br>failures, <1 in<br>150,000 | 2         | Moderate                | Moderate chance the Design<br>Control will detect a potential<br>Cause of failure or sub-<br>sequent Failure Mode |
| 1        | None        | No effect                                                                                                               | 1          | Rare        | Failure is<br>unlikely, <1 in<br>1,500,000   | 1         | High                    | High chance the Design Con-<br>trol will detect a potential<br>Cause of failure or sub-<br>sequent Failure Mode   |

\* When there is a safety hazard as a result of a failure, the failure mode MUST be eliminated

**Figure 4-2 DFMEA Severity, Occurrence and Detection Ranking Chart Used by Many Companies**

or other life threatening issue) the RPN value is overruled by a note in the Class column that the failure mode **shall** be eliminated before a design is released.

**4.6 Voltage Spacing Design Requirements** Recommended voltage-spacing between uninsulated conductors (external PWB layers) in a power assembly is defined in Figure 4-3.

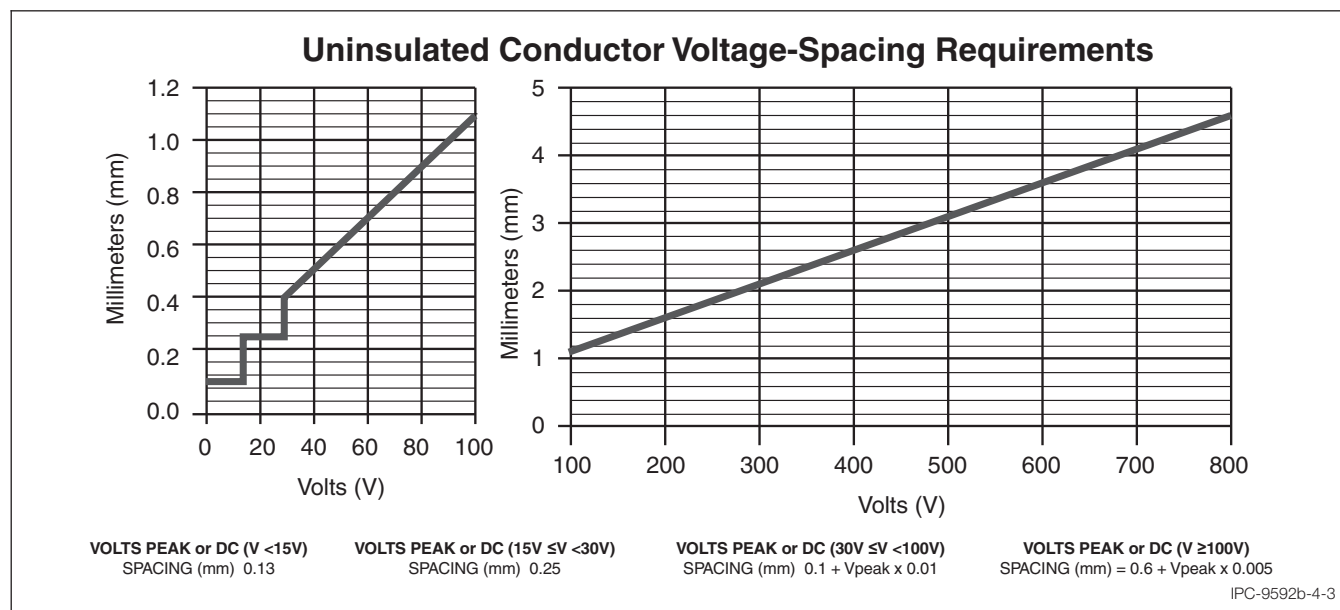


**Figure 4-3 Uninsulated Conductor Voltage-Spacing Requirements**

All uninsulated PC board conductors, component leads, heatsinks and other conductive features **shall** meet the voltage-spacing requirements of Figure 4-3 for ac circuits, switching circuits, or any dc potential above 100V. It is recommended that these voltage-spacing guidelines be followed for dc circuits under 100V as well. Features with spacings not meeting the above voltage-spacing requirements must be insulated; for example by RTV, conformal coating, sleeving or a combination of these methods.

**NOTE:** Engineering exceptions may be taken to the above criteria based on a risk/cost analysis. Careful review of that decision is recommended.

Board-to metal chassis spacings **shall** meet the criteria of Figure 4-3. For these situations, a guard band to the Figure 4-3 criteria is recommended. The guard band **shall** account for reasonable device lead length variability.

**NOTE:** Insulation is highly recommended between the underside of PC mother boards and chassis sheet metal, even if the above voltage-spacing requirement criterion is met.

Whenever the creepage or clearance requirements of IEC 60950 are greater than the requirements defined in Figure 4-3, the IEC 60950 requirements **shall** take precedence over this document.

**4.7 Moisture Sensitivity Level (MSL) Rating of Surface Mount Power Conversion Devices (PCDs)** Electronic components that are Moisture Sensitive may be susceptible to damage when exposed to elevated reflow temperatures. This is especially true for ICs exposed to lead-free reflow commonly exposed to peak temperatures of 260 °C. J-STD-020 and J-STD-033 define moisture sensitivity levels for SMT ICs and how they are to be packaged and handled. J-STD-075 addresses MSL of non-IC components. Bare printed circuit boards do not currently have an MSL rating standard. Historically SMT PCDs have not been moisture sensitive and therefore had not required an MSL rating standard; however, at reflow temperatures of 260 °C, SMT PCDs can be moisture sensitive. The purpose of this section is to establish requirements for classifying and handling moisture sensitive PCDs.

**4.7.1 Application of MSL Guidelines During Assembly of PCDs** Suppliers **shall** have a documented process in place that insures proper packaging and handling of moisture sensitive devices used in the assembly of surfaced mounted components used in all PCDs. These processes should follow applicable standards mentioned above. PWBs do not currently have an MSL rating, users should be aware of the risk of moisture sensitivity of PWBs and take appropriate precautions.

**4.7.2 Applicability of MSL Requirements** All SMT BMPs **shall** be evaluated for MSL sensitivity. SMT PCDs not designed for Lead-free reflow environments are exempt from this requirement. This requirement does not apply to through-hole BMPs, except for pin-in-paste applications.

Definitions of MSL levels and maximum exposure times may be found in Table 4-1. This table also contains standard test exposure conditions referenced in 5.2.2.1. This table is taken from IPC/JEDEC J-STD-020 Table 5.1.

**Table 4-1 MSL Levels per the Table 5.1 in IPC/JEDEC J-STD-020**

| Level | Floor Life |               | Soak Requirements |              |                        |              |
|-------|------------|---------------|-------------------|--------------|------------------------|--------------|
|       |            |               | Standard          |              | Accelerated Equivalent |              |
|       | Time       | Conditions    | Time (hours)      | Conditions   | Time (hours)           | Conditions   |
| 1     | Unlimited  | ≤30 °C/85% RH | 168 +5/-0         | 85 °C/85% RH | N/A                    | N/A          |
| 2     | 1 year     | ≤30 °C/60% RH | 168 +5/-0         | 85 °C/85% RH | N/A                    | N/A          |
| 2a    | 4 weeks    | ≤30 °C/60% RH | 696 +5/-0         | 30 °C/60% RH | 168                    | 60 °C/60% RH |
| 3     | 168 hours  | ≤30 °C/60% RH | 192 +5/-0         | 30 °C/60% RH | 52                     | 60 °C/60% RH |
| 4     | 72 hours   | ≤30 °C/60% RH | 96 +2/-0          | 30 °C/60% RH | 24                     | 60 °C/60% RH |

**4.7.3 Identification of MSL Rating** Nonexempt SMT PCDs **shall** carry an MSL rating equal to the worst case MSL rating of components contained in the product Bill of Materials (BOM). Each component in the BOM **shall** have an MSL rating assigned which represents the worst case (highest MSL numerical value) of all approved suppliers for that component. Component MSL ratings **shall** be determined by the supplier under Lead-free (260 °C) reflow conditions following the appropriate IPC/JEDEC J-STD-020 requirements. For PWBs on the BOM, a default MSL 2a **shall** be assumed.

Documentation of data used to derive PCD MSL ratings **shall** be made available to OEMs upon request.

**4.7.4 Packaging Requirements** All Lead free SMT PCDs **shall** be packaged in a Moisture Barrier Bag (MBB) containing appropriate desiccant and Humidity Indicator Card (HIC) consistent with IPC/JEDEC J-STD-033, Section 3.3.2. BMPs with an MSL 2 or higher rating **shall** also require a package label consistent with requirements of IPC/JEDEC J-STD-033, Section 3.3.3.

**4.7.5 Handling Requirements for BMP Users** Users of PCDs with an MSL2 or higher rating **shall** be responsible for insuring parts are adequately protected after opening the original MBB.

Due to temperature sensitive packaging material typically used for PCDs, baking in the original packaging **is not** recommended. PCD manufacturers will not be responsible for maintaining equipment and processes for baking products returned by OEMs for over-exposure after opening MBBs.

In this circumstance, PCD manufactures may be asked to participate in a risk assessment AABUS. If baking is recommended and is done in original packaging, supplier **shall** recommend a maximum temperature which will not adversely affect packaging integrity. It will be left to the OEM to determine required bake time at the temperature selected. If this procedure is performed, OEMs will also assume risk for damage or degraded performance such as reduced solderability.

**4.7.6 Qualification Testing for MSL** There is currently no standard for testing to confirm SMT PCDs MSL rating. It is not the intention of this document to propose such a method at this time. Section 5.2.2 outlines testing that is intended to provide some relative degree of assurance that assigned MSL rating is appropriate.

## 5 DESIGN AND QUALIFICATION TESTING

The testing described in this section has two main purposes. First, design verification testing and electromagnetic susceptibility testing including EMI and ESD testing, are intended to provide assurance that the device will function according to its specification. Second, environmental stress testing, including HALT, is intended to provide a measure of assurance (not proof) that the device is robust enough to operate in its intended environment without damage or degradation that would affect its operation.

After a PCD has been introduced to the market, any supplier design change requires that the supplier **shall** notify the user, per 6.5.1.3. Any additional testing required as a result of the design change **shall** be a subset of the tests detailed in this design and qualification testing section with the specific tests defined.

It is specifically not a purpose of the testing in this section to provide any measure of the device's reliability (failure rate) or expected service life.



## 5.1 Design Verification Testing (DVT)

**5.1.1 Scope of Testing** All parameters, features and functions listed or described in the device specification **shall** be tested for conformance to the specification. DVT applies to both Classes I and II.

In addition, suppliers **shall** test devices for any parameters, features or functions listed below that are not listed in the device specification.

**5.1.2 Sample Size** A complete DVT **shall** be performed on a minimum of three devices. The same devices **shall** be used for all tests.

If a unit fails during DVT testing and cannot be repaired to a like-new state, then an additional device may be substituted. This substituted device **shall** have all DVT tests performed on it. No credit can be claimed for tests performed on a device that does not complete the DVT.

**5.1.3 Test Methods** Suppliers **shall** use the test methods described in Appendix C for any parameter, feature or function for which a test method is given in Appendix C or in this section.

For parameters, features or functions for which no test method is given in Appendix C or this section, the supplier may use their own test method. This test method **shall** be sufficiently described in the test report so that a user can duplicate the test methods and conditions.

**5.1.4 Test Conditions and Limits** All test limits **shall** be at the minimum and maximum operating limits given in the device's specification.

**5.1.5 DVT Report** A report of the DVT **shall** be prepared. The DVT report **shall**:

- Provide the dates and locations of the design verification testing.
- List the serial numbers, if available, date codes and revision levels (both hardware and firmware) of the devices being tested.
- List the parameter, feature or function being tested.
- Provide a description or reference to the test method.
- Give the limits of the test.
- Provide the results of the test for each device tested. Tests providing parametric data, such as output voltage regulation, **shall** give the actual measured results of the test and not just "Pass/Fail."
- Provide the results of failure mode analysis for all failures in DVT and the corrective action for each DVT failure.
- Provide for each parameter, feature or function tested a statement of "Pass" if all of the tested devices meet the specification or "Fail" if any of the devices did not meet the specification (one device failing any test is counted as a DVT failure).
- Give a statement that the device passed DVT if all tested units meet all specifications or that the device failed DVT if any tested device did not meet specification for any tested parameter, feature or function.

It is left to the supplier's discretion on whether or not to supply all or part of the DVT report to any particular customer.

### 5.1.6 Design Verification Testing - ac Input Parameters

**5.1.6.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.6.2 Parameters to Be Measured** DVT on a device operating from an ac power source **shall**, at a minimum, test all of the following parameters:

- Input current as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Input power as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Inrush current (The peak value and oscillograms of the inrush current from the application of power until the inrush current transient is complete **shall** be recorded. At least one oscillogram **shall** have a time resolution to show no less than one half cycle per division of the oscilloscope display.)



- Input current harmonics and power factor as a function of input voltage and output load.
- Input voltage at which the device becomes operational and the input voltage at which the device turns off.
- Hold-up time.

### 5.1.7 Design Verification Testing - dc Input Parameters

**5.1.7.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.7.2 Parameters to Be Measured** DVT on a device operating from a dc power source **shall**, at a minimum, test all of the following parameters:

- Input current as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Input power as a function of input voltage and output load (including any operation in standby or an equivalent mode).
- Input voltage at which the device becomes operational and the input voltage at which the device turns off.

### 5.1.8 Design Verification Testing - Overall Input to Output Parameters

**5.1.8.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.8.2 Parameters to Be Measured** DVT on all PCDs **shall**, at a minimum, test the following:

- Efficiency as a function of input voltage and output loading.
- Turn on delay time of each output.
- Ability to start and operate with the minimum specified output load.
- Start up at minimum and maximum specified ambient or baseplate temperatures.

### 5.1.9 Design Verification Testing - dc Output Parameters

**5.1.9.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.9.2 Parameters to Be Measured** The following parameters are the minimum that **shall** be tested on each sample:

- Load regulation (each output individually).
- Cross regulation.
- Line regulation.
- Temperature regulation.
- Short term (24 hour) output voltage drift.
- PARD on each output.
- Dynamic output voltage response to output load changes (maximum deflection and recovery time as a function of the magnitude and rate of output current change).
- Voltage rise time on each output.
- For devices with more than one output, the time delay and rise time of all relative to the other outputs.

**5.1.10 Design Verification Testing - Protection Features** Protection features are those features and functions intended to prevent damage, degradation or loss of data. Examples of protection features include circuits that:

- Prevent excessive output voltage (output overvoltage protection).
- Send an alarm or stop power conversion when the output voltage is less than the minimum specified value of the output undervoltage protection (UVP).
- Stop power conversion or disconnect the device from the source when the input voltage exceeds the maximum specified value of the input overvoltage protection (OVP).
- Respond to excessive output current by stopping power conversion or limiting the output current to a specified value of the output overcurrent protection (OCP).

- Stop power conversion when the ambient or internal temperature of the device exceeds limits determined by the supplier of the overtemperature protection (OTP).

**5.1.10.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.10.2 Parameters to Be Measured** For each protection feature or function, the minimum tests **shall** include:

- The voltage, current, temperature, power or other condition that causes the detector circuit to indicate an abnormal condition.
- The device's response to the detection of the abnormal condition.
- If applicable, the voltage, current, temperature, power or other condition that causes the detector circuit to indicate a return to normal operation.
- If applicable, the device's behavior during the change from an abnormal operating condition to normal operation.
- If applicable, the means or method used to reset a device that has shut down in response to an abnormal condition.

#### **5.1.11 Design Verification Testing - Input and Output Signals and Indicators**

**5.1.11.1 Test Conditions** All testing **shall** be performed according to the methods described in Appendix C.

**5.1.11.2 Parameters to Be Measured** For all signals and indicators, all parameters given in the product specification **shall** be verified. This includes, but is not limited to:

- Conditions and criteria that cause a signal or indicator to be asserted, to be negated, or to change state.
- Signal electrical levels.
- Signal and indicator timing.

#### **5.1.12 Design Verification Testing - Other Electrical Parameters, Features and Functions**

**5.1.12.1 Current Sharing** The tests in this section **shall** be applied to all devices whose specifications indicate that the outputs can be connected in parallel.

**5.1.12.2 Test Conditions** Sample units **shall** be connected and configured according to the supplier's instructions for current sharing operation.

At the minimum, the tests below **shall** be performed at all combinations of:

- Minimum, nominal and maximum ambient or baseplate temperature.
- Minimum, nominal and maximum input voltage.

**5.1.12.3 Test Procedure** All testing **shall** be performed according to the methods described in Appendix C. Specifically, for Current Sharing, see Appendix C-4.17.

**5.1.13 Design Verification Testing - Hot Swap** The tests in this section **shall** be applied to all devices whose specifications describe them as suitable for insertion into and removal from an energized system.

**5.1.13.1 Test Conditions** The test fixture is configured to hold at least two devices operating in parallel.

For standard product, the device manufacturer **shall** specify the test fixture used for hot swap testing. For custom devices, the test fixture **shall** utilize the customer end application equipment as much as possible to provide the maximum possible assurance that there is no hot swap problem in the end application.

The input voltage source is set to the nominal value. The ambient temperature is set to  $25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$ .

**5.1.13.2 Test Procedure** All testing **shall** be performed according to the methods described in Appendix C. Specifically, for Hot Swap, see Appendix C-4.18.

**5.1.14 Design Verification Testing - Mechanical Compliance** DVT **shall** include a mechanical compliance test. The supplier **shall** make dimensional measurements on at least three samples of a device.

The test report **shall** include a brief description of each measurement (such as “overall length”), the specified dimension and tolerance from the specification, mechanical design file or drawing, and the results of the measurement, and a statement of whether the measured values are, or are not, within the tolerances allowed on the design file or drawing. All dimensions on all devices **shall** be within tolerance for this test to be passed. One dimension on any sample that is out of tolerance **shall** be considered a failure of this test.

**5.2 Environmental Stress Testing (EST)** This section refers to testing and qualification related to the operating environment, such as temperature and humidity; not to environmental requirements such as RoHS.

**5.2.1 EST Purpose** The purpose of the environmental stress testing is to demonstrate a minimum ability of the product to withstand steady-state and changing temperature, humidity, input power and output loading without damage or degradation.

This testing, by itself, cannot assure a minimum reliability or service life as those calculations require detailed knowledge of the product’s operating conditions. It is up to each user to use the stresses described here and their knowledge of the end use environment to determine whether a product meeting this standard will perform adequately in the end use.

**5.2.2 Test Sequence for EST** Each of the tests in this section is to be considered stand-alone. The tests may be performed in any order convenient to the supplier.

The supplier is permitted, but not required to use different physical samples for each of the environmental stress tests.

**5.2.2.1 Module Preconditioning** The purpose of module preconditioning is to simulate stresses applied to category 2, surface mount, power conversion devices during the OEM’s main printed circuit board solder reflow assembly process. These samples are then used to perform the long duration EST tests: Temperature Humidity Bias, High Temperature Operating Bias, Temperature Cycling, and Power and Temperature Cycling.

This test method establishes a standard preconditioning process for surface mount (SMT) power conversion devices that is representative of a typical OEM multiple solder reflow assembly operation. However, it does not provide proof of any specific MSL level for the PCD.

- 1) Perform electrical functional testing.
- 2) Visual inspection with a 40X microscope to identify any cracks, printed circuit board delamination or other damage prior to preconditioning.
- 3) Humidity soak per the power conversion device MSL classification and Table 4-1. The MSL classification of the BMP converter is defined in 4.7 Moisture Sensitivity Level (MSL) Rating of Surface Mount Power Conversion Devices (PCDs).
- 4) Subject the PCD to two SnPb or Pb-free reflow cycles using thermal profiles per IPC/JEDEC J-STD-020.
- 5) Visual inspection with a 40X microscope to identify any cracks, printed circuit board de-lamination or other damage.
- 6) Perform electrical functional testing.

After preconditioning, the samples will be used for the following EST tests in 5.2:

- a) Temperature Humidity Bias.
- b) High Temperature Operating Bias.
- c) Temperature Cycling.
- d) Power and Temperature Cycling.

**5.2.3 Highly Accelerated Life Test (HALT)** Highly Accelerated Life Test (HALT) is a series of tests performed on a product as part of the design process to aid in improving product robustness. The principal idea of HALT is to find design weaknesses as quickly as possible and then fix them. After improving one weakness, the next design weakness is found and improved and so on until no design weaknesses remain that could result in field failures. During HALT, a product is stressed beyond the product specifications or what the product will encounter in a typical use environment to quickly accelerate and identify design weaknesses. The resulting failures are what is important, not the stress level. HALT is not a pass/fail test. It is a test to explore and improve the operational and destruct limits of the design.

HALT **shall** be performed on completed standard PCDs. Additional information on HALT may be found in Appendix D.

**5.2.3.1 Scope and Purpose** The purpose of HALT is to assure there is adequate margin to specified stress levels and as a means to find weaknesses in designs for corrective action prior to design release. It is specifically not to be used as a

to predict reliability (failure rate) or service life. It is strongly recommended that HALT be performed as early in the design cycle as possible. HALT gives the best results when problems that are found, can be corrected well before the rest of the qualification testing.

### 5.2.3.2 HALT Chamber Equipment Requirements

#### 5.2.3.2.1 Chamber Thermal and Vibration Capability

- HALT chamber(s) capable of generating 6 degrees-of-freedom (3 linear and 3 rotational) multi-axis and pseudo-random repetitive shock vibrations via pneumatic hammers under a table to which the UUT is directly coupled..
- The vibration system should be capable of generating a minimum 75 Grms level in a 5-5,000 Hz spectrum on a bare table, and retain a minimum of 70% capability for any given PSU weight.
- The chamber should have a minimum thermal range of -80 °C to +170 °C. The air thermal rate of change **shall** be  $\geq 60$  °C/min at measured air temperature.

#### 5.2.3.2.2 Chamber Minimum Reporting Requirements

- Chamber maker, model number, serial number, calibration date/frequency and calibrating agency, specification for temperature range and rate of change, and table vibration specification, chamber control software version.
- Pictures of the following items during all test sequences: Chamber setup, unit orientation and mounting configuration, Air ducting configuration, and ATE/cabling configuration.

**5.2.3.3 Vibration and Thermal Monitoring Capability** The collection of thermal and vibration data is required to provide credible evidence that required stresses were applied to the unit, thermal and vibration response of the unit is documented, and profiles were met per the procedure.

#### 5.2.3.3.1 Minimum Requirements for Accelerometers

- Single axis or tri-axes accelerometer(s) for the measurement of product response from vibration. Accelerometers should be low mass type with a frequency response capability of 2 Hz to 10 KHz, and a measurement range of  $\pm 500g$ 's.
- Accelerometers should be small enough to be mounted in the desired location on the UUT, and light enough that their mass does not significantly impact or alter the vibration dynamic characteristics of the sample tested.
- Must have sufficient number of accelerometers to monitor each unit under test.

#### 5.2.3.3.2 Minimum Requirements for Thermocouples

- Thermocouples used for HALT should have sufficient stability characteristics through the temperature range of the chamber (approximately -100 °C to +200 °C). The diameter of the thermocouple wires size should not exceed 22 gauge.
- Sufficient numbers of thermocouples must be present to monitor each unit under test and chamber ambient.

#### 5.2.3.3.3 Minimum Reporting Requirements for Vibration and Thermal Monitoring

- Pictures of thermocouple and accelerometer mounting locations on each unit tested.
- Picture and location of accelerometer monitoring location for table response.
- Picture and location of thermocouple monitoring of ambient temperature.
- Thermocouple type, manufacturer.
- Accelerometer manufacturer, model number, serial number, frequency response, measurement range (g's), sensitivity (mV/g).

### 5.2.3.4 Laboratory Test Equipment

#### 5.2.3.4.1 Source and Loading

- Programmable voltage source that can provide required power and support the minimum and maximum voltage range required for the application.
- Programmable Electronic load that can support the maximum rated current and power for the connected power supply output.



**Documents**

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#### 5.2.3.4.2 Monitoring Capability

- Thermocouple monitoring capability via the use of the available thermocouple monitoring channels of the HALT test system. The use of an external data acquisition instrument capable of multiple channel measurements should also be available. Must have sufficient monitoring capability to monitor each unit under test and chamber ambient.
- Thermocouple measurement data must be able to be electronically stored.
- Monitoring capability for fault condition of power supply during test via the electronic load or external equipment.
- Spectrum Analyzer to monitor the PSD of the table and product response. Need to record the PSD and Grms level for each vibration step sequence.

#### 5.2.3.4.3 Additional Hardware

- ATE and cable harnesses to support functional test of each unit.
- Sufficient mounting equipment (fixtures, crossbars, bolts, nuts, etc.) to support mounting of units during vibration testing.
- Calibrated torque wrench.
- Any additional test hardware to support unique requirements for the PSU being tested.

**5.2.3.4.4 Minimum Reporting Requirements for Laboratory Equipment** For all test equipment used provide the Maker and model number, key specifications related to capability (i.e., Voltage, Amps, number of channels for data recording, etc...), calibration date/frequency and calibrating agency.

**5.2.3.5 Sample Size** The minimum total sample size for HALT tests **shall** be 21 (see Note 1) per Table 5-1. All test samples in each test (low temperature, high temperature, or thermal cycling, etc.) **shall** be tested into failures, until equipment capability limits are reached, or until fundamental limit of the technology (FLT) is reached.

Table 5-1 Minimum Sample Size for HALT Tests

|                                         | Low Temperature Step Test | High Temperature Step Test | Rapid Thermal Cycling Test | 6-DOF Random Vibration Test | Input Voltage Test | Output Load Test | Combined Stresses Test |
|-----------------------------------------|---------------------------|----------------------------|----------------------------|-----------------------------|--------------------|------------------|------------------------|
| All Classes and Categories <sup>1</sup> | 3                         | 3                          | 3                          | 3                           | 3                  | 3                | 3                      |

**Note 1:** For Categories 1 and 3 (Power Supplies /Adapters), users have the option of starting with less than 12 samples and re-using samples which survive a given sequence of testing. Users are cautioned that some HALT failures require extensive repairs after failures during early testing and may not be suited for subsequent testing. Category 2 (BMPM) must begin with 3 new units for each test sequence, except for units which have not failed a HALT test when the equipment capability limits have been reached. These units may be used in the next test rather than replacing them with new units.

**5.2.3.6 Functional Test Requirements** The functional test of the sample under test should provide adequate coverage to determine overall performance of the sample and the occurrence of multiple types of failure modes. The test coverage must include variation in input voltage and output load to ensure equivalent stress on applicable circuits.

**5.2.3.6.1 Pre-Test Verification** Each unit **shall** be submitted to initial verification testing to ensure compliance to product specifications under specified maximum and minimum input voltages and loading conditions per output rail. Testing **shall** be done at nominal ambient environment.

**5.2.3.6.2 Thermal Step Stress/Combined Environment/Rapid Thermal Cycle** Total sum power during dwell time must equal 100% of rated power. Minimum and Maximum input voltage conditions must be tested at each temperature. The supplier is to test one sample at low line, one sample at high line, and the other sample at the worst case of either low or high line.

**5.2.3.6.3 Vibration Step Stress** Each unit **shall** be loaded at 100% of rated power, with nominal input voltage.

**5.2.3.6.4 Monitoring** Real time monitoring or power supply output for fault condition **shall** be implemented as dictated in the equipment section.

**5.2.3.7 Test Reporting and Documentation Requirements** This section defines the minimum documentation requirements to show compliance to the procedures defined in the document.

1. Follow the reporting requirements as dictated in 5.2.3.5 for test equipment and setup.

2. Product specification for voltage and current per output rail.
3. Over Current Protection limit and input voltage specifications.
4. Product operating temperature specifications, including OTP limit range.
5. Product model number/part number, sample revision, product development stage (i.e., EVT, DVT).
6. Test date, Report date/revision, Test location, Test Organization (internal organization or external lab) who tested, Person who tested the unit, person who prepared, reviewed and approved the report.
7. BOM revision for product tested.
8. Component sources/part numbers used in each sample must be made available upon request.
9. Pictures of the following items during all test sequences: Chamber setup, unit orientation and mounting configuration, Air ducting configuration, and ATE/Cabling configuration.
10. Grms and PSD at the table for each vibration sequence/each level.
11. Items provided below **shall** be provided per Serial number for step stress testing:
  - Test conditions (input voltage, output loading condition (voltage/current) for each test sequence and increment (i.e., 30 Grms, 40 Grms, etc...). Loading condition must clearly show loading per output rail.
  - Test result for each test sequence/increment (measured voltage/note any fault condition).
  - Upper and lower operating and destruct limits per serial number tested.
  - Combined thermocouple measurement graph and temperature log file of chamber ambient vs. product thermal response for all temperature sequences. Axes must be time and temperature. Must clearly identify thermocouple in the legend (i.e., Chamber Ambient).
  - Product vibration response, including PSD and Grms for each vibration sequence/each level.
12. Items provided below **shall** be provided per Serial number for the input voltage and output load test (as applicable):
  - Upper and Lower current limit.
  - Upper and lower input voltage limit.
  - Program settings/overall test profile (per Table 5-6) used for input voltage test. Must contain voltage step size, Ton/Toff during each step (Table 5-7), output load, temperature, and test result for each input voltage step (showing input voltage/result). Must clearly state if temperature protection is disabled during this test.
  - Program settings/overall test profile (per Table 5-8) used for Output current test. Must contain step size for output load (in terms of current, not %), individual test profile per step (Table 5-9), temperature, and test result for each output load condition (showing output current/result). Loading condition must clearly show loading per output rail.
  - Must clearly state if output current limit and temperature protection is disabled during test.
13. For combined testing, must provide the following information by serial number:
  - Upper and Lower current limit.
  - Upper and lower input voltage limit.
  - Program settings for each combined profile, including temperature, vibration, input voltage, dwell times, and loading per output rail.
  - Must clearly state if output current limit and temperature protection is disabled during test.
14. Failure summary and CLCA report for all failures.
15. For product that is repaired and used in additional testing, provide a list of all repairs made by serial number/test sequence.
16. Deviations taken from the procedures defined in this document on any test or tests.

**5.2.3.8 Root Cause Analysis and Corrective Actions** Root Cause Analysis (RCA) is an integral part of the HALT process to determine the root cause of the failures identified from the test. All failures found during HALT tests **shall** be analyzed to their root causes.

- The root cause analysis process must be documented with the failure mode, the exact cause of the failure or the suspected cause if uncertain. This should include the results of a failure analysis lab, if used, with pictures of damage at the flawed site.

- The suppliers **shall** have failure analysis capability, or may utilize an external/independent facility to perform this responsibility.

Following the understanding of the failure mode through the root cause analysis process a corrective action plan may be incorporated.

- The suppliers **shall** be responsible to document, report, and as necessary, implement corrective action for all design and process defects identified during the HALT.
- The corrective action “fixes” **shall** be summarized with a cause and effect report for review by PSU users.
- If suppliers decide not to fix a failure found during HALT, detailed report of reasoning **shall** be provided to and approved by PSU users.

## 5.2.4 Temperature, Humidity and Bias (THB)

**5.2.4.1 Purpose** The THB test is used to test for moisture induced failures such as conductive anodic filaments (CAF), corrosion and dendrites.

**5.2.4.2 Applicability** This test is applicable to Class I and Class II products.

**5.2.4.3 Sample Size** The minimum sample size for this test **shall** be as per Table 5-2.

Table 5-2 Minimum Sample Size for THB Tests

|          | Category 1 (Power Supplies) | Category 2 (BMPMs) | Category 3 (Adapters/Chargers) |
|----------|-----------------------------|--------------------|--------------------------------|
| Class I  | 3                           | 5                  | 3                              |
| Class II | 6                           | 30                 | 6                              |

**5.2.4.4 Test Procedure** The THB test starts with a pre-conditioning soak of all units for 72 hours under the following conditions:

- Unpowered.
- Ambient temperature: 85 °C.
- Relative humidity: 85%.

The THB testing is performed for 500 hours for Class I and 1000 hours for Class II under the following conditions:

- Input voltage: Rated maximum continuous input voltage.
- Output loading (all outputs): Minimum rated.
- Ambient temperature: The maximum rated ambient temperature or 85 °C, whichever is less.
- Relative Humidity: 85%.

For BPM, natural convection is preferred, but the minimum forced air cooling is allowed if necessary to prevent the device’s specified baseplate or hot spot temperature exceeding rated maximum temperature. If forced air is used, then the device’s baseplate or hotspot temperature **shall** be as close to the maximum rating, as possible.

During the testing, the units **shall** be monitored for proper functioning. The monitoring may either be continuous or sampled at a rate no less frequently than once a minute.

**5.2.4.5 Pass Criteria** At the conclusion of the test time, all tested units **shall** be visually inspected and **shall** be free of solder joint cracking, corrosion, dendrites, or other defects.

All tested units **shall** pass a functional test within 24 hours after completion of the test.

It is permitted to remove the units from the test and visually inspect and functionally test them at times less than the minimum 500 hours for Class I or minimum 1000 hours for Class II. If failures are detected, then corrective action **shall** be implemented and the test restarted from the beginning. No credit is given for any completed unit-hours. Fresh units may be used for the restarted test.

## 5.2.5 High Temperature Operating Bias (HTOB)

**5.2.5.1 Purpose** This test is to find weaknesses that appear only after long operation times (not infant mortality). This test is not intended to test or prove service life.

