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User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance and Other Internal Electrochemical Migration Testing

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User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance and Other Internal Electrochemical Migration Testing

Developed by the Electrochemical Migration Task Group (5-32e) of the
Cleaning and Coating Committee (5-30) of IPC

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Users of this publication are encouraged to participate in the
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1 SCOPE

This document is the product of the IPC Electrochemical Migration (ECM) Task Group. It was drafted to provide guidance regarding implementation of the User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance and Other Internal Electrochemical Migration Testing to evaluate the effects of mechanical stress, laminate material fracturing, ionic contamination, moisture content prior to press lamination, and other material processing characteristics on formation of conductive paths within laminate material such as conductive anodic filaments (CAF), one specific type of ECM failure mode. This internal ECM test method provides a proven standard for determining the risk of through-hole bias and other internal conductor orientations that result in significant reduction of insulation resistance internally, rather than on the surface of printed boards.

2 BACKGROUND

In recent years, internal electrochemical migration (ECM) liability concerns in the industry have increased as board designs have advanced in terms of decreasing clearances, dimensions and/or higher voltages. ECM failures describe any phenomena that causes internal drop in insulation resistance, including conductive anodic filament (CAF) formation, weak polymer resin bond, hollow fibers, poor wetting of glass reinforcement fibers with resin, foreign material or contamination, rough hole walls, and excessive copper wicking within plated through holes. Temperature, humidity and bias testing of insulation resistance using test coupons is the methodology used to check for these defects. The user of this document is encouraged to become familiar with IPC-9201, *Surface Insulation Resistance Handbook* to distinguish between internal ECM failures and possible confounding Surface Insulation Resistance (SIR) failures.

3 PURPOSE

This user guide addresses test issues regarding determining pass/fail criteria based on knowledge of three product goals:

- What are the long term reliability requirements?
- What is the closest spacing required for a given voltage?
- Evaluate the internal ECM Failure risk.

4 INTRODUCTION

Internal ECM, including conductive filament growth occurs within a printed board and may or may not be visible under a microscope. It is often associated with adjacent laminate material fracturing or defect (i.e., “pathway”) that contributed to its formation. Examples of visible filament growth shown in Figures 4-1, 4-2, 4-3 and 4-4 would fail the temperature, humidity, and bias conditions selected to determine multilayer board reliability between internal features.

The high magnification photo, Figure 4-1 below, shows a printed board with layer 1 (top layer) removed, revealing a near shorting condition between the plated through hole and layer 2 ground plane.

Poor press lamination and/or defective prepreg material may contribute to entrapped contaminants and the formation of conductive pathways which results in early test failure if the resin/reinforcement bonding strength and resistance to mechanical stress is reduced.

Failure analysis, as seen in two perspectives in Figure 4-2, show a near-shorting condition from the hole barrel to the plane on layer 3.

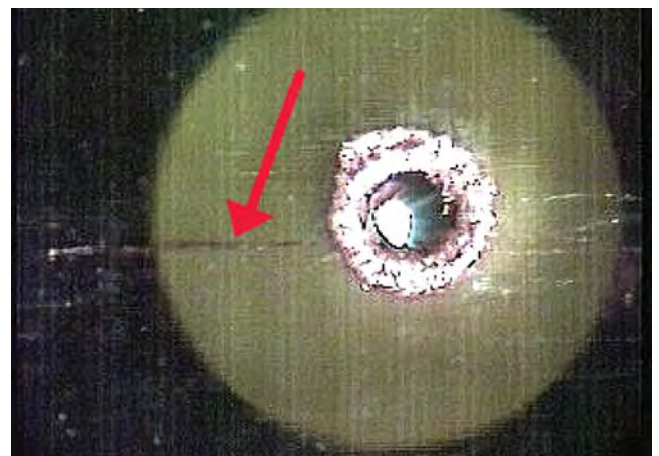


Figure 4-1 Example of an Internal Conductive Filament
[Photo courtesy of Matsushita]

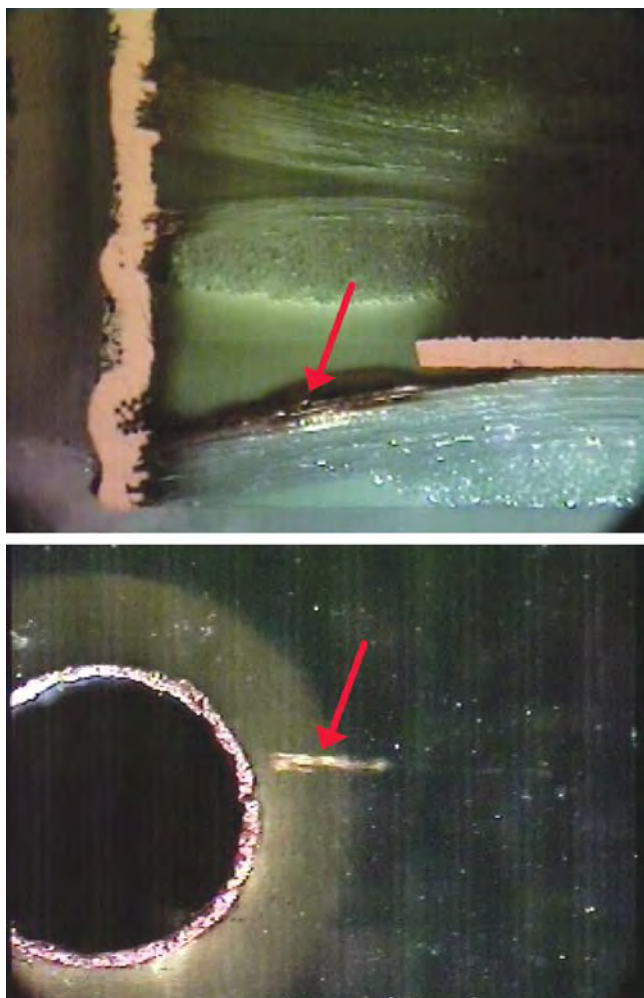


Figure 4-2 Two Perspectives of the Same Conductive Path

[Photographs courtesy of Matsushita]

During internal ECM testing, the use of no more than 5 volts per 0.001 inches bias voltage and at least 1.0 megohm current limiting resistor can facilitate, with sufficient time, formation of the larger scale conductive growths possibly detectable by microscopic examination. If the power goes out on an Auto-SIR all data can be lost, so it is recommended to use an uninterruptible power source (UPS) to mitigate the effects of any short disruption in power.

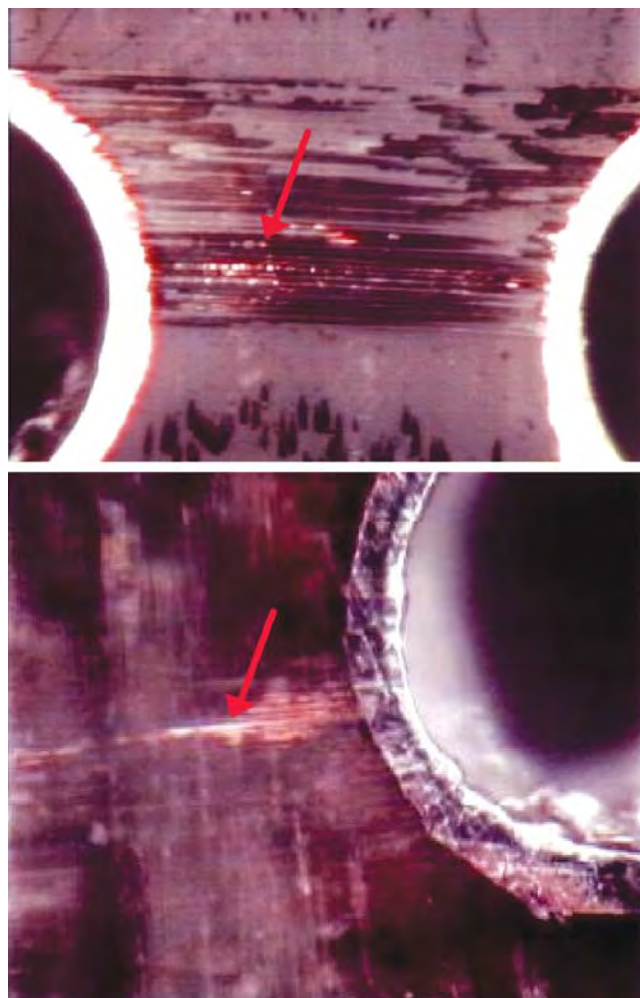


Figure 4-3 Two Photos Showing Failure Between Plated Through Holes

[Photographs courtesy of Arlon Co.]

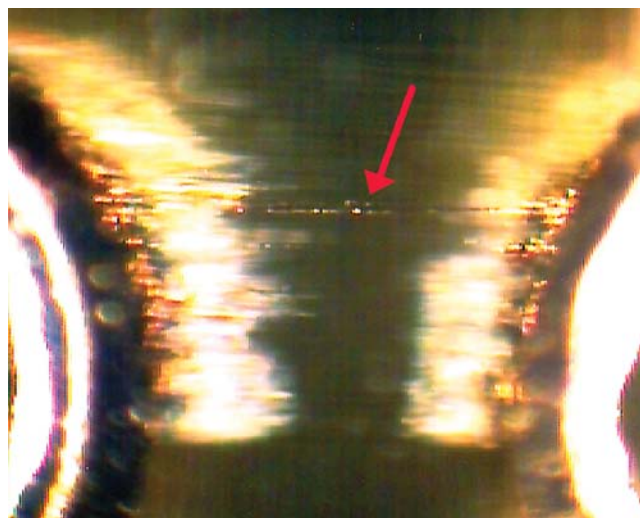


Figure 4-4 Failure Analysis Photo Showing Suspected CAF Failure Between Very Closely-Spaced Plated Through Holes

[Photograph courtesy of Park-Nelco]

5 WHAT IS CONDUCTIVE ANODIC FILAMENT GROWTH?

Conductive Anodic Filament (CAF) growth is a conductive copper-containing salt, atacamite, that grows electrochemically from the anode toward the cathode along a pathway, often at the resin-glass interface. The formation of atacamite as a conductive filament was first reported on a board surface in 1971 (Raffolovich), but it was not reported as a type of electrochemical migration failure until 1979 [1]. The mechanism for CAF is the transfer of copper (Cu) ions and the deposition of Cu salts in the presence of moisture and voltage bias, and is influenced by concentration and pH gradients associated with hydrolysis. The conductive path is the growth from the anode by a salt, as compared to dendrite formation on the surface of the board where metal ions deposit on the cathode [2].

Historically, true CAF is associated with mechanically drilled holes where drilling disrupts the glass-to-resin interface, permitting the absorption of subsequent processing chemistry. CALCE uses the term conductive filament formation which they define as an electrochemical process that involves the transport (usually ionic) of a metal through or across a non-metallic medium under the influence of an applied electric field. This definition is not specific to CAF but can include surface dendrites, CAF, and copper plating within hollow glass fibers.

The emphasis of this guide is ECM growth within the printed board.

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6 OTHER INTERNAL ECM MODES

Hollow Fibers in Printed Board Laminate Material Introduction

In the manufacture of laminates used for the electronic industry, glass fibers are used for reinforcement. Laminates are composed of several plies of glass fabrics encapsulated with a polymeric resin. The most common fabric fiber material used today in laminate manufacture is E-glass, a continuous filament glass yarn with a chemical composition by weight of mostly SiO_2 , but also containing various amounts of CaO , Al_2O_3 , B_2O_3 and other materials. A homogeneous melt composition with negligible impurities is necessary for the successful manufacture of glass fibers. Solid inclusions of even submicron dimensions will act as stress concentrators that reduce the fiber strength. Furthermore, the decomposition of raw materials during glass melting can cause trapped gases. In the raw materials, water, carbonates (such as XCO_3), sulfates and other organic materials will decompose with heat to form gases. Depending on the viscosity of the glass mixture and various manufacturing processes, these gases can get trapped as bubbles, called seeds. The process of fining, removes these seeds by adding fining agents - which create nucleation sites for bubbles to coalesce and escape the melt.

If the molten glass contains a sufficient level of decomposition gas, bubbles may become trapped inside the fibers while being drawn through the bushing. These bubbles, unless very large, do not cause fiber breakage but end up as capillaries in the glass fibers, otherwise known as hollow fibers. Hollow fibers can span the entire length of a laminate. A cross-section of a laminate containing hollow fibers is shown in Figure 6-1. A cross-section of a single hollow glass fiber is shown in Figure 6-2.

Conductive Filament Failure (CFF) Due to Hollow Fiber

The presence of hollow fibers makes the CFF a one step process, effectively removing the first step - the need for path formation. Therefore, laminates composed of hollow fibers pose a threat to the reliability of electronic systems by providing a convenient open path for CFF. The most apparent solution of hollow fibers is to improve glass fiber manufacturing processes and controls.

Section 6 Hollow Fibers References

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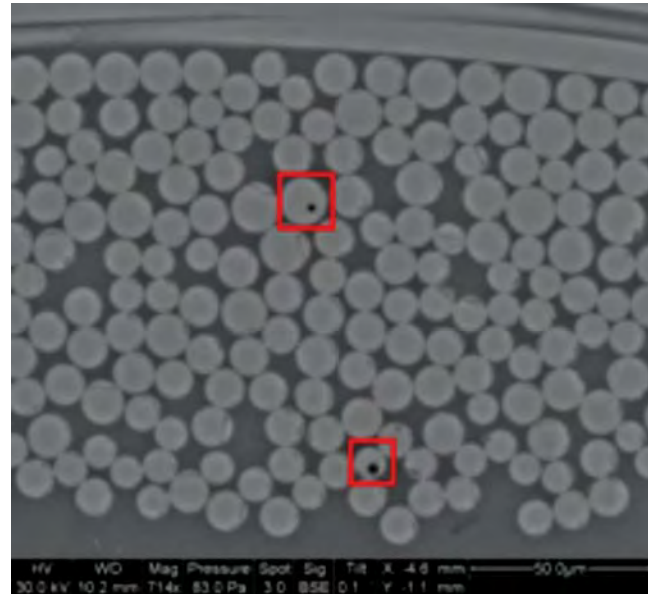


Figure 6-1 Cross-section SEM micrograph of a laminate material. The hollow glass fibers are highlighted.
[Courtesy: CALCE Center, University of Maryland]

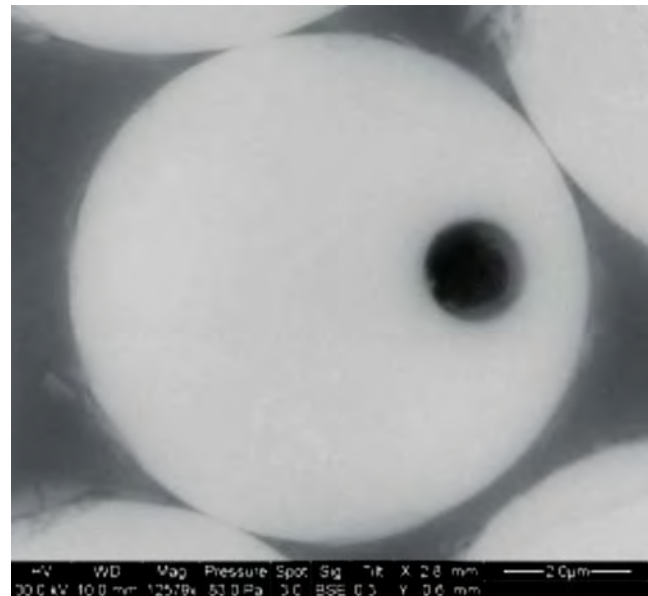


Figure 6-2 A cross-section of a hollow fiber can be seen in the middle fiber in this SEM micrograph. Hollow fibers of smaller diameter may be potentially more damaging as they tend to fill faster with conductive medium.
[Courtesy: CALCE Center, University of Maryland]

- [5] A. Shukla, M. Pecht, J. Jordan, K. Rogers, and D. Jennings, "Hollow Fibres in PCB, MCM-L and PBGA Laminates May Induce Reliability Degradation," Circuit World, Vol. 23, No. 2, pp. 5-6, 1997

Poor Wetting of Resin to Glass Fibers

Poor wetting of glass reinforcement fibers with resin can occur within closely bound fiber bundles, such as at tri-point locations (Figure 18-4) and other areas where resin has not completely encapsulated fibers during the prepreg manufacturing process. Incomplete or inadequate glass fiber surface treatments can also result in poor wetting and bonding with resin, facilitating electrochemical migration after subsequent processing along these fibers.

Foreign Material

Foreign material or contamination such as insect or plant material, cosmetics, salt, ionic contamination can compromise bonding within the laminate material resulting in cracks or voids within the material. During subsequent printed board Fab manufacturing processing these can become pockets where ionic residues and contamination remain trapped, potentially contributing to longer term electrochemical migration failures. For example, in some space applications the laminate material maximum allowable size and length criteria for foreign inclusions listed in IPC-4101, 3.8.3, are not considered adequate.

7 INCREASING INTERNAL ECM RISK TRENDS

Internal ECM failure mechanism models show increasing risk with decreasing through-hole pin pitch, decreasing BGA, LGA, or other close escape via grid/pitch arrangements, and with increasing voltage differential between adjacent holes. Table 7-1 shows design trends at one major OEM (year shown is actual or estimated first production release for the indicated technology level).

**Table 7-1 Plated Through Hole Wall-to-Wall Spacing Trends
(IPC PCB Technology Roadmap Hole-Wall-to-Hole-Wall Spacing):**

Mechanical Hole Formation (1.5 mm Laminate Standard)

Attribute	2013-2014		2015-2016		2017-2018		2019-2023	
	RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Via Size Min (µm)	225	125	212	125	200	125	200	125
Aspect Ratio	7:1	12:1	8:1	12:1	9:1	12:1	10:1	12:1
Via Pitch (µm)	400	225	400	200	400	200	350	200

Mechanical Hole Formation (3.0 mm Laminate Standard)

Attribute	2013-2014		2015-2016		2017-2018		2019-2023	
	RCG	SoA	RCG	SoA	RCG	SoA	RCG	SoA
Via Size Min (µm)	225	150	200	137	175	125	200	100
Aspect Ratio	14:1	20:1	15:1	20:1	15:1	20:1	15:1	20:1
Via Pitch (µm)	350	200	300	175	275	175	250	175

RCG: Revenue Center of Gravity

SoA: State of the Art

Reference: Table 7-1: 2013 IPC Technology Roadmap

The Bell Labs CAF model uses a general formula where the values of many factors and constants were selected for best fit to the available data. Using this model and the above design trend data between 1995 and 2006, an approximate 8x increase in CAF risk was calculated.

The CALCE CAF model uses a chemical diffusion controlled reaction rate for the second step in CAF formation (more closely matches the physical dynamics of the CAF failure mechanism). The adjusted CALCE CAF model was developed based upon early CAF testing at Sun Microsystems to account for the existence of a fast failure region immediately adjacent to plated-through holes (PTHs) resulting from drilling and other mechanical stresses that occur during printed circuit board manufacturing. Using the adjusted CAF model and the above design trend data between 1995 and 2006, it also shows an approximate 8x increase in CAF risk. This result shows good agreement between the adjusted CALCE and Bell Labs CAF models.

8 ADJUSTED CALCE CAF FAILURE MODEL

$$t(f) = ((\rho a R T (L - 2D)^2) / (2n F M C H V)) * e^{E/RT}$$

t(f)	time to failure
ρ	density of copper
a	volume fraction of filament in the region between electrodes
R	gas constant
T	absolute temperature (degrees K)
L	initial distance between electrodes
D	extent of fast failure region immediately adjacent to PTH
n	number of valence electrons (n-2 for copper)
F	Faraday constant (charge of one mole of electrons)
M	ion mobility constant (dependent upon laminate material)
C	copper ion concentration in a water solution
H	relative humidity
V	voltage differential (bias)
E	activation energy

The CALCE model for CAF failure risk shows that when there is the same failure risk for voltage #1 (e.g., 10V) and spacing #1 versus voltage #2 (e.g., 100V) and spacing #2 and where L is large and all other conditions are the same so that $D_1 = D_2$, then the “easily conductive region” D can be determined.

$$[(L_1 - 2D_1)^2 / V_1] = [(L_2 - 2D_2)^2 / V_2]$$

At close hole spacings, the laminate material is less supported during drilling which causes more mechanical damage and higher D. The Figure 8-1 SEM photograph of a plated-through hole (PTH) cross-section shows the typical extent of copper wicking in the perpendicular direction out from the PTH. The microfracturing portion of the D parameter extends further out from the hole wall and is less visible. The white bar at the top left corner of the photo is 0.1 mm in length.

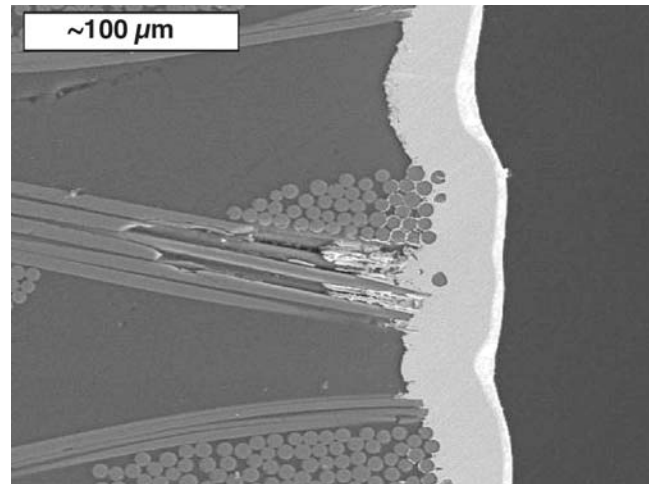


Figure 8-1 Typical Copper Wicking in a Plated Through Hole

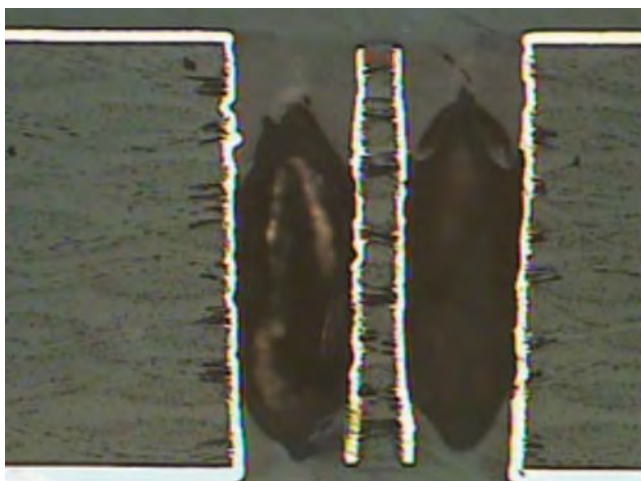


Figure 8-2a Internal Separation

[Courtesy: A. Caputo, “Conductive Anodic Filament (CAF) Formation,” Ph.D., Materials Science and Engineering, University of Toronto, Toronto Canada, 2010]



Figure 8-2b Damage Due to Hole Drilling and Wicking

[Courtesy: A. Caputo, “Conductive Anodic Filament (CAF) Formation,” Ph.D., Materials Science and Engineering, University of Toronto, Toronto Canada, 2010]

9 INTERNAL ECM TEST VEHICLE DESIGN

A number of internal ECM test board designs have been developed by various OEMs and others in the industry.

Generally, the key objective of all such Internal ECM test coupons is to optimize the number of potential failure opportunities within the printed boards by utilizing different drill patterns and internal conductor constructions (e.g., hole-to-hole, hole-to-plane, hole-to-trace and trace-to-trace). Some designs vary the hole-to-hole pitch of test patterns, while others vary the drill size on constant-pitch patterns to obtain different spacing between vias, thereby yielding results that are specific to a given drill bit diameter.

A well-designed ECM test coupon should allow objective comparison of internal ECM performance of key target parameters, including (1) different laminate materials, (2) different prepreg glass styles and/or (3) different printed board suppliers and their process capabilities. In all cases, it is important for the evaluation of internal ECM test results to know for each test board design the number of opportunities for failure per daisy chain net and the number of daisy chain nets per test board for each test board feature geometry and set of conditions. It is also important to know the number of test boards run for each condition tested (for example, samples with and without solder mask, samples with different board finishes, etc.).

Finally, other differences in test failure criteria, such as time to failure on one or a few samples versus percent failure during X hours of testing multiple samples, may not allow meaningful comparison of internal ECM test results. These differences in test methodology and test sample preparation should be kept to a minimum. The printed board manufacturing process used should be according the specific requirements of each laminate material tested, which also helps ensure that at least 24 out of each set of 25 test samples will have consistent 96-hour resistance levels that are within a decade of the mean. The basis for determining the subsequent decade drop in resistance failure criteria is the mean resistance of all good samples measured after 96 hours of temperature and humidity conditioning without bias. Internal ECM test reports for alternative test board designs should include all the above information.

IPC CAF Test Vehicle

There are four different IPC internal ECM test coupons: IPC-9253, IPC-9254, IPC-9255 and IPC-9256. Each offers slightly different test parameters. For example, IPC-9256, 6.0 in x 0.75 in, can be incorporated into a supplier's working panel and used as an off-board internal ECM test coupon. IPC-9253 and IPC-9254 form the basis of Test Method 2.6.25 and are further described below.

9.1 Printed Board Thickness and Stackup The IPC-9253 and IPC-9254 coupons are each 10-layer, single-ply constructions with default thickness of 1.5 mm. Overall board thickness and the number of plies used in a stack-up can affect the test results. Layer count can be reduced as desired by the user, but for comparative studies the board construction and final thickness should be held constant among all samples being tested.

Glass style can be a significant contributor to internal ECM performance. Generally, the risk from internal ECM increases with higher-glass content prepregs, such as 7628, which are more susceptible to drill damage and poor resin wet-out compared with lower-glass content materials, such as 1080. Table 9-1 summarizes typical resin-glass content for several common prepreg styles. But there are other factors that influence internal ECM performance of a given glass style, including glass spread, cleanliness of glass fiber before silane treatment, silane finish and resin impregnation process parameters (e.g., temperature, flow rate, etc.) (SOURCE: "Conductive Anodic Filament Formation in PCBs," DfR Solutions, 2012). [Glass styles 2113 and 2313 are reported to be most sensitive to drilling parameters].

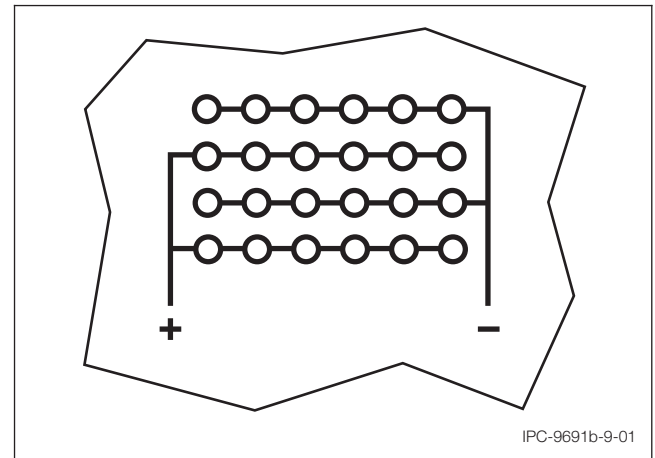


Figure 9-1 IPC-9253 Test Coupon Region A: Plated Through Holes in Alignment with X, Y

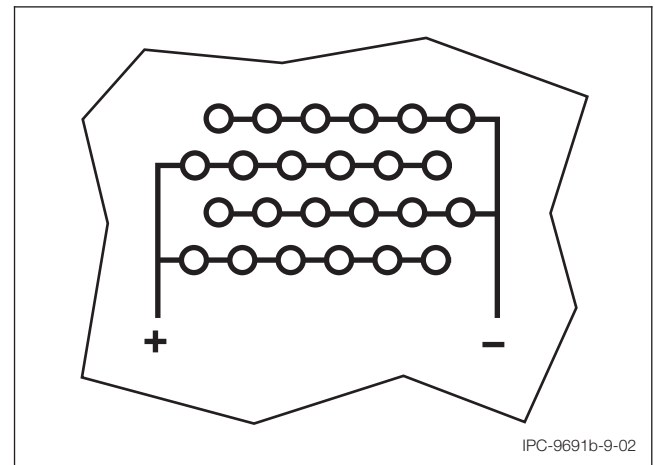


Figure 9-2 Region B Via Test Pattern. The Anode Vias are Staggered Diagonally to the Cathode Vias