

IPC-A-600

Revision K – July 2020
Supersedes Revision J
May 2016

Acceptability of Printed Boards

Developed by



BUILD ELECTRONICS BETTER

Full document details: IPC A-600K-2020



The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2809.

Thank you for your continued support.



IPC-A-600K

Acceptability of Printed Boards

If a conflict occurs between the English and translated versions of this document, the English version will take precedence.

Developed by the IPC-A-600 Task Group (7-31a) of the Product Assurance Committee (7-30) of IPC

Supersedes:

IPC-A-600J - May 2016
IPC-A-600H - April 2010
IPC-A-600G - July 2004
IPC-A-600F - November 1999

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 105N
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

This Page Intentionally Left Blank

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources across many continents. While the principal members of the A-600 Task Group (7-31a) of the Product Assurance Committee (7-30) are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of IPC extend their gratitude. Special thanks goes to the members of the Rigid Printed Board Committee (D-30) for their efforts in establishing acceptance criteria for printed boards.

Product Assurance Committee

Chair
Robert Cooke
NASA Johnson Space Center
Vice-Chair
Debbie Wade
Advanced Rework Technology-A.R.T

IPC-A-600 Task Group

Co-Chair
Scott Bowles
Lockheed Martin Space
Systems Company
Co-Chair
Denise Charest
Amphenol Printed Circuits, Inc.

Technical Liaison of the IPC Board of Directors

Bob Neves
Microtek (Changzhou) Laboratories

IPC-A-600 Task Group

Elizabeth Allison, NTS - Baltimore
David Anderson, Raytheon Company
Norman Armendariz, Raytheon Company
Lance Auer, Conductor Analysis
Technologies, Inc.
Jimmy Baccam, Lockheed Martin Missiles
& Fire Control
John Bauer, Collins Aerospace
Phil Befus, Honeywell Aerospace
James Blanche, NASA Marshall Space
Flight Center
Steven Bowles, DuPont SVTC
Mark Buechner, BAE Systems
Michael Chang, Northrop Grumman
Corporation
Thomas Clark, Lockheed Martin Missiles
& Fire Control
Michael Collier, Teledyne Leeman Labs
Robert Cooke, NASA Johnson Space
Center
Cesar De Luna, NTS - Anaheim
Francesco Di Maio, GESTLABS S.r.l.
Don Dupriest, Lockheed Martin Missiles &
Fire Control
Julie Ellis, TTM Technologies
Richard Etchells, Electronic Technology
Resource Partners
Gary Ferrari, FTG Circuits
William Fox, Lockheed Martin Missile &
Fire Control
Mahendra Gandhi, Northrop Grumman
Space Systems
Gonzalo J Garcia Leypon, Cirexx
International, Inc.

Herb Girtz, Holaday Circuits Inc.
Constantino Gonzalez, ACME Training &
Consulting
Pierre-Emmanuel Goutorbe, Airbus
Defence & Space
Vicka Hammill, Honeywell Inc. Air
Transport Systems
Hardeep Heer, FTG Circuits
Philip Henault, Raytheon
Joshua Huang, Nvidia Corporation
Emma Hudson, Emma Hudson Technical
Consultancy Ltd
Frank Huijsmans, PIEK International
Education Centre
Henrik Jensen, Gaasdal Bygningsindustri
A/S
Joseph Kane, BAE Systems
Allen Keeney, Johns Hopkins University
Maan Kokash, BAE Systems
Nick Koop, TTM Technologies
Kelly Kovalovsky, BAE Systems
Kevin Kusiak, Lockheed Martin
Corporation
Meredith LaBeau, Calumet Electronics
Corp.
Jeremy Lakoskey, Honeywell International
Leo Lambert, EPTAC Corporation
Christina Landon, NSWC Crane
David Lee, BMK Professional Electronics
Gmb
Minsu Lee, Korea Printed Circuit
Association
Peggy LeGrand, TTM Technologies
Andrew Leslie, BAE Systems

Jeff Lewis, Holaday Circuits Inc.
Peter Lindhardt, TTM Technologies -
Logan Division
Dan Loew, L3Harris
Jennifer Ly, BAE Systems
Todd MacFadden, Bose Park Place
Manufacturing
Chris Mahanna, Robisan Laboratory Inc.
Tabishur Malik, TTM Technologies
Tim McKliget, Holaday Circuits Inc.
Melissa Meagher, Raytheon Missile
Systems
Michael Miller, NSWC Crane
James Monarchio, TTM Technologies
Steven Murray, Northrop Grumman
Corporation
Robert Neves, Microtek Laboratories
China
Thi V. Nguyen, Lockheed Martin Missile &
Fire Control
Jamie Noland, Blackfox Training Institute
Gerard O'Brien, Solderability Testing &
Solutions, Inc.
Gianluca Parodi, IIS Progress SRL
Gerry Partida, Summit Interconnect -
Anaheim
Helena Pasquito, EPTAC Corporation
Yogen Patel, Candor Industries Inc.
Jan Pedersen, Elmatica AS
Stephen Pierce, SGP Ventures, Inc.
John Potenza, Lockheed Martin Mission
Systems & Training
Randy Reed, R. Reed Consultancy LLC

Acknowledgment (cont.)

Owen Reid, Lockheed Martin Missiles & Fire Control
Curtis Ricotta, Lockheed Martin Space Systems Company
Jose Rios, Raytheon
Nef Rios, Summit Interconnect - Anaheim
Kris Roberson, Bandjwet Enterprises, Inc. D/B/A BEST
Thomas Romont, IFTEC
Christina Rutherford, Honeywell Aerospace
Gilbert Shelby, Raytheon Systems Company
Russell Shepherd, NTS - Anaheim

Hans Shin, Pacific Testing Laboratories, Inc.
Patrick Smith, Cirexx International, Inc.
David Sommervold, Henkel US Operations Corp.
Brian Stevens, Collins Aerospace
Marshall Stolstrom, TTM Technologies, Inc.
Stephanie Stork, L3Harris Communications
Ingrid Swenson, TTM Technologies, Inc.
Audra Thurston, Calumet Electronics Corp.

Bradley Toone, L3Harris Communications
Paul Van Dang, Innovative Circuits
Crystal Vanderpan, UL LLC
Pietro Vergine, Advanced Rework Technology-A.R.T
Adeodato Vigano, Compunetics Inc.
Jennet Volden, Collins Aerospace
Debbie Wade, Advanced Rework Technology-A.R.T
Rob Walls, PIEK International Education Centre (I.E.C.) BV

A special note of thanks goes to Curtis Ricotta of Lockheed Martin Space Systems Company and Denise Charest of Amphenol Printed Circuits, Inc. for supplying a significant amount of new photographs for this revision.

Table of Contents

Acknowledgment	iii	2.6 Holes – Unsupported	42
1 Introduction	1	2.6.1 Haloing	42
1.1 Scope	1	2.7 Edge Board Contacts	43
1.2 Purpose	1	2.7.1 Surface Plating – Printed Board Edge Connector Lands	43
1.3 Approach To This Document	1	2.7.1.1 Surface Plating – Edge Connector Lands (Gap/Overlap Area)	45
1.4 Classification	1	2.7.2 Burrs on Edge-Board Contacts	46
1.5 Acceptance Criteria	2	2.7.3 Adhesion of Overplate	47
1.6 Applicable Documents	3	2.8 Marking	49
1.6.1 IPC	3	2.8.1 Etched Marking	50
1.6.2 American Society of Mechanical Engineers	4	2.8.2 Ink Marking	52
1.7 Dimensions and Tolerances	4	2.9 Solder Mask	54
1.8 Terms and Definitions	4	2.9.1 Coverage Over Conductors (Skip Coverage)	55
1.9 Revision Level Changes	4	2.9.2 Registration to Holes (All Finishes) ...	56
1.10 Workmanship	4	2.9.3 Registration to Rectangular Surface Mount Lands	57
2 Externally Observable Characteristics	5	2.9.3.1 Registration to Round Surface Mount Lands (BGA) – Solder Mask-Defined Lands	58
2.1 Printed Board Edges	5	2.9.3.2 Registration to Round Surface Mount Lands (BGA) – Copper- Defined Lands	59
2.1.1 Burrs	5	2.9.3.3 Registration to Round Surface Mount Lands (BGA) – (Solder Dam)	60
2.1.1.1 Nonmetallic Burrs	6	2.9.4 Blisters/Delamination	61
2.1.1.2 Metallic Burrs	7	2.9.5 Adhesion (Flaking or Peeling)	63
2.1.2 Nicks	8	2.9.6 Waves/Wrinkles/Ripples	64
2.1.3 Haloing	9	2.9.7 Tenting (Via Holes)	65
2.2 Base Material Surface	10	2.9.8 Soda Strawing	66
2.2.1 Weave Exposure	11	2.10 Pattern Definition – Dimensional	68
2.2.2 Weave Texture	12	2.10.1 Conductor Width and Spacing	68
2.2.3 Mechanically Induced Disrupted Fibers	13	2.10.1.1 Conductor Width	69
2.2.4 Surface Voids	14	2.10.1.2 Conductor Spacing	70
2.3 Base Material Subsurface	15	2.10.2 External Annular Ring – Measurement	71
2.3.1 Measling	20	2.10.3 External Annular Ring – Supported Holes and Microvia Capture Land ...	72
2.3.2 Crazeing	22	2.10.4 External Annular Ring – Unsupported Holes	74
2.3.3 Delamination/Blister	25	2.10.5 Surface Plating – Rectangular Surface Mount Lands	75
2.3.4 Foreign Inclusions	28	2.10.6 Surface Plating – Round Surface Mount Lands (BGA)	77
2.4 Solder Coatings and Fused Tin Lead	30	2.10.7 Surface Plating – Wire Bond Pads ..	79
2.4.1 Nonwetting	30	2.11 Flatness	81
2.4.2 Dewetting	31		
2.5 Holes – Plated-Through – General	33		
2.5.1 Nodules/Rough Plating	33		
2.5.2 Pink Ring	34		
2.5.3 Voids – Copper Plating	35		
2.5.4 Voids – Finished Coating	36		
2.5.5 Lifted Lands – (Visual)	37		
2.5.6 Cap Plating of Filled Holes – (Visual)	38		
2.5.7 Back-Drilled Holes – (Visual)	40		

Table of Contents (cont.)

3	Internally Observable Characteristics	83		
3.1	Dielectric Materials	84		
3.1.1	Laminate Voids/Cracks (Outside Thermal Zone)	84		
3.1.2	Registration/Conductor to Holes	87		
3.1.3	Clearance Hole, Unsupported, to Power/Ground Planes	88		
3.1.4	Dielectric Material, Clearance, Metal Plane for Supported Holes	89		
3.1.5	Delamination/Blister	90		
3.1.6	Dielectric Removal	91		
3.1.6.1	Etchback	93		
3.1.6.2	Smear Removal	95		
3.1.6.3	Negative Etchback	97		
3.1.7	Layer-to-Layer Spacing	99		
3.1.8	Resin Recession	101		
3.1.9	Hole Wall Dielectric/Plated Barrel Separation (Hole Wall Pullaway)	102		
3.2	Conductive Patterns – General	103		
3.2.1	Etching Characteristics	105		
3.2.2	Print and Etch	107		
3.2.2.1	Overhang	108		
3.2.3	External Conductor Thickness (Foil Plus Plating)	109		
3.2.4	Non-Plated Layer Copper Foil Thickness	110		
3.2.5	Solder Mask Thickness	111		
3.3	Plated-Through Holes – General	112		
3.3.1	Copper Plating Voids	114		
3.3.2	Plating Nodules	115		
3.3.3	Plating Folds/Inclusions	116		
3.3.4	Wicking	118		
3.3.4.1	Wicking, Clearance Holes	119		
3.3.5	Innerlayer Inclusions	120		
3.3.6	Innerlayer Separation – Vertical (Axial) Microsection	121		
3.3.7	Innerlayer Separation – Horizontal (Transverse) Microsection	123		
3.3.8	Plating Separation	124		
3.3.9	Foil Crack – (Internal Foil) “C” Crack	126		
3.3.10	Foil Crack (External Foil) “A,” “B,” “D” Cracks	127		
3.3.11	Plating Crack (Barrel) “E” Crack	128		
3.3.12	Plating Crack – (Corner) “F” Crack	129		
3.3.13	Plating Microanomalies	130		
3.3.14	Annular Ring – Internal Layers	131		
3.3.15	Annular Ring – Microvia to Target Land	134		
3.3.16	Microvia Target Land Contact Dimension	136		
3.3.17	Microvia Target Land Piercing	139		
3.3.18	Lifted Lands – (Cross-Sections)	140		
3.3.19	Copper Plating Thickness – Hole Wall	141		
3.3.20	Copper Wrap Plating	142		
3.3.21	Copper Cap Plating of Filled Holes	145		
3.3.22	Plated Copper Filled Vias (Through, Blind, Buried and Microvia)	147		
3.3.23	Material Fill of Through, Blind, Buried and Microvia Structures (Other than Copper Plating)	149		
3.3.24	Back-Drilled Holes (Microsection Evaluation)	151		
3.3.25	Solder Coating Thickness (Only When Specified)	152		
3.4	Plated-Through Holes – Drilled	153		
3.4.1	Burrs	154		
3.4.2	Nailheading	155		
3.5	Plated-Through Holes – Punched	156		
3.5.1	Roughness and Nodules	157		
3.5.2	Flare	158		
4	Miscellaneous	159		
4.1	Flexible and Rigid-Flex Printed Boards	159		
4.1.1	Coverlay Coverage – Coverfilm Separations	160		
4.1.2	Coverlay/Covercoat Coverage – Adhesives	162		
4.1.2.1	Adhesive Squeeze-Out – Land Area	162		
4.1.2.2	Adhesive Squeeze-Out – Foil Surface	163		
4.1.3	Access Hole Registration for Coverlay and Stiffeners	164		
4.1.4	Plating Anomalies	165		
4.1.5	Stiffener Bonding	166		
4.1.6	Transition Zone, Rigid Area to Flexible Area	167		
4.1.7	Solder Wicking/Plating Penetration Under Coverlay	168		
4.1.8	Laminate Integrity	169		
4.1.8.1	Laminate Integrity – Flexible Printed Board	170		

Table of Contents (cont.)

4.1.8.2	Laminate Integrity – Rigid-Flex Printed Board	171
4.1.9	Etchback (Type 3 and Type 4 Only)	172
4.1.10	Smear Removal (Type 3 and 4 Only)	173
4.1.11	Trimmed Edges/Edge Delamination	174
4.1.12	Silver Film Integrity	176
4.2	Metal Core Printed Boards	178
4.2.1	Type Classifications	179
4.2.2	Spacing Laminated Type	180
4.2.3	Insulation Thickness, Insulated Metal Substrate	181
4.2.4	Insulation Material Fill, Laminated Type Metal Core	182
4.2.5	Cracks in Insulation Material Fill, Laminated Type	183
4.2.6	Core Bond to Plated-Through Hole Wall	184
4.3	Flush Printed Boards	185
4.3.1	Flushness of Surface Conductor	185
5	Cleanliness Testing	186
5.1	Solderability Testing	187
5.1.1	Plated-Through Holes (Applicable to Solder Float Test)	188
5.2	Electrical Integrity	190

This Page Intentionally Left Blank

1 INTRODUCTION

Introduction

1.1 SCOPE

This document describes the target, acceptable, and nonconforming conditions that are either externally or internally observable on printed boards. It represents the visual interpretation of minimum requirements set forth in various printed board specifications, e.g.; IPC-6010 series, J-STD-003, etc.

1.2 PURPOSE

The visual illustrations in this document portray specific criteria of the requirements of current IPC specifications. In order to properly apply and use the content of this document, the printed board should comply with the design requirements of the applicable IPC-2220 series document and the performance requirements of the applicable IPC-6010 series document. In the event the printed board does not comply with these or equivalent requirements, then the acceptance criteria should be as agreed between user and supplier (AABUS).

1.3 APPROACH TO THIS DOCUMENT

Characteristics are divided into two general groups:

- Externally Observable (section 2)
- Internally Observable (section 3)

“Externally observable” conditions are those features or imperfections which can be seen and evaluated on or from the exterior surface of the board. In some cases, such as voids or blisters, the actual condition is an internal phenomenon and is detectable from the exterior.

“Internally observable” conditions are those features or imperfections that require microsectioning of the specimen or other forms of conditioning for detection and evaluation. In some cases, these features may be visible from the exterior and require microsectioning in order to assess acceptability requirements.

Specimens should be illuminated during evaluation to the extent needed for effective examination. The illumination should be such that no shadow falls on the area of interest except those shadows caused by the specimen itself. It is recommended that polarization and/or dark field illumination be employed to prevent glare during the examination of highly reflective materials.

The illustrations in this document portray specific criteria relating to the heading and subheading of each page, with brief descriptions of the acceptable and nonconforming conditions for each product class. (See 1.4.) The visual quality acceptance criteria are intended to provide proper tools for the evaluation of visual anomalies. The illustrations and photographs in each situation are related to specific requirements. The characteristics addressed are those that can be evaluated by visual observation and/or measurement of visually observable features.

Supported by appropriate user requirements, this document should provide effective visual criteria to quality assurance and manufacturing personnel.

This document cannot cover all of the reliability concerns encountered in the printed board industry; therefore, attributes not addressed in this issue **shall** be AABUS. The value of this document lies in its use as a baseline document that may be modified by expansions, exceptions, and variations which may be appropriate for specific applications.

When making accept and/or reject decisions, the awareness of documentation precedence must be maintained.

This document is a tool for observing how a product may deviate due to variation in processes. Refer to IPC-9191.

IPC-A-600 provides a useful tool for understanding and interpreting Automated Inspection Technology (AIT) results. AIT may be applicable to the evaluation of many of the dimensional characteristics illustrated in this document.

IPC-9121 is a useful troubleshooting guideline for problems, causes and possible corrective actions related to printed board manufacturing processes.

1.4 CLASSIFICATION

This standard recognizes that electrical and electronic products are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in producibility, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of product between classes.

1 INTRODUCTION

Introduction (cont.)

Process Indicator imperfections are permitted and are deliverable.

The user is responsible for defining the product class. The procurement documentation package **shall** state the product class and any exceptions to specific parameters, where appropriate.

Criteria defined in this document reflect three classes, which are as follows:

Class 1 General Electronic Products – Includes limited life products suitable for applications where the requirement is function of the completed product.

Class 2 Dedicated Service Electronic Products – Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical.

Class 3 High Performance/Harsh Environment Electronic Products – Includes products where continued high performance or performance-on-demand is critical, product downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the product must function when required.

Acceptability criteria in this document have been separated so that printed board product may be evaluated to any one of the three classes. The use of one class for a specific characteristic does not mean that all other characteristics must meet the same class. Selection should be based on minimum need. The customer has the ultimate responsibility for identifying the class to which the product is evaluated. Thus, accept and/or reject decisions must be based on applicable documentation such as contracts, procurement documentation, specifications, standards and reference documents.

1.5 ACCEPTANCE CRITERIA

Most of the illustrations and photographs included in this document represent three levels of quality for each specific characteristic; i.e., Target Condition, Acceptable and Nonconforming. The text included with each level establishes the “Acceptance Criteria” for each class of product.

Target Condition in many cases is close to perfect. While this is the desired condition it is not always achievable and may not be necessary to ensure the reliability of the printed board in its service environment.

Acceptable indicates that the condition depicted, while not necessarily perfect, will maintain the integrity and reliability of the printed board in its service environment. The acceptable condition is considered acceptable for at least one or more classes but may not be acceptable for all classes, as specified by the associated acceptance criteria.

Nonconforming indicates that the condition depicted may be insufficient to ensure the reliability of the printed board in its service environment. The nonconforming condition is considered unacceptable for at least one or more classes of product but may be acceptable for other classes as specified by the associated acceptance criteria.

Process Indicator Condition A condition (not a defect) that identifies a characteristic that does not affect the form, fit or function of a product.

- Such condition is a result of material, design and/or operator/machine related causes that create a condition that neither fully meets the acceptance criteria nor is a defect.
- Process indicators should be monitored as part of the process control system. When the number of process indicators indicate abnormal variation in the process or identify an undesirable trend, then the process should be analyzed. This may result in action to reduce the variation and improve yields.
- Disposition of individual process indicators is not required and affected product should be used as is.

The target, acceptable and nonconforming conditions depicted herein and the associated acceptance criteria are intended to represent typical industrial practices. Requirements of individual product designs may deviate from these criteria.

The examples shown in the photographs and/or illustrations are sometimes exaggerated to make the referenced imperfection more apparent. The relationship between the text and the examples is not always parallel; it would be difficult to find many cases so specific that they would always match the acceptance criteria. When photographs or illustrations contained in this standard are not consistent with discussion in the written text, the written text takes precedence and should be followed.

It should also be noted that some of the photographs used may have more than one type of condition on the same example. It is necessary that the users of this document pay particular attention to the subject of each section to avoid misinterpretation.

1 INTRODUCTION

Introduction (cont.)

It should be understood that the first inference to nonconformance given implies that all other conditions of lesser magnitude are acceptable. Thus, a criteria which states a nonconformance condition as 50% of the surface is pitted, for example, implies that anything less than 50% of the surface being pitted is acceptable for that characteristic in that class. Obviously, nonconformance in Class 1 implies nonconformance in Class 2 and Class 3; and likewise, nonconformance for Class 2 implies nonconformance in Class 3.

An inspector **shall not** make the selection as to which class the part under inspection belongs. When making accept and/or non-conformance decisions, the awareness of precedence of documentation must be maintained.

In all cases, documentation should be available to the inspector defining to which class the part submitted for inspection belongs.

Procedures and requirements for conducting visual inspections related to this document **shall** be in accordance with the requirements of the applicable performance specification.

In the event of conflict, the following order of precedence **shall** apply:

1. Purchase Order (including exceptions to the master drawing, if any)
2. Procurement documentation reflecting the customers detailed requirements (such as master drawing)
3. Other documents to the extent specified by the customer
4. The end item performance specification such as the IPC-6010 series when invoked by the customer
5. This acceptability document. Printed boards should be of uniform quality and **shall** conform to the IPC-6010 series.

IPC-6010 series establishes the minimum acceptability requirements for printed boards. This document, IPC-A-600, is a companion and complementary document, providing pictorial interpretation of these requirements. It is not intended to be used as a performance specification for printed board manufacture or procurement.

IPC-A-600 can be used as a support document for inspection. It does not specify frequency of in-process inspection or frequency of end product inspection. Nor is the allowable number of nonconforming process indicators or the number of allowable repair/rework of defects specified.

Visual examination for applicable attributes **shall** be conducted at 3 diopters (approx. 1.75X). Visual examination of microvias features for applicable dimensional or workmanship attributes **shall** be conducted at 30X minimum. If confirmation of a suspected nonconformance cannot be made at 3 diopters, it should be verified at progressively higher magnifications (up to the maximum referee magnification power of 40X) to confirm conformance. Dimensional requirements such as spacing or conductor width measurements may require other magnifications and devices with reticles or scales in the instrument, which allow accurate measurements of the specified dimensions. Contract or specification may require other magnifications.

Microsection evaluation of PTHs, including buried and blind vias, **shall** be examined for foil and plating integrity at a magnification of 100X $\pm$ 5%. Referee examinations **shall** be accomplished at a magnification of 200X $\pm$ 5%. Each side of the hole **shall** be examined independently.

Microsection evaluation of microvias **shall** be examined for plating integrity and interconnection integrity at a magnification of 200X $\pm$ 5%. Referee examinations **shall** be accomplished at a magnification of 400 - 500X. Each side of the hole **shall be examined independently**.

AIT results may be applicable to the evaluation of many of the dimensional characteristics illustrated in this document.

1.6 APPLICABLE DOCUMENTS

The following specifications of the revision in effect at the time of order form a part of this document to the extent specified herein. If a conflict of requirements exists between this specification and the listed applicable documents, this specification **shall** take precedence.

1.6.1 IPC¹

J-STD-003 Solderability Tests for Printed Boards

J-STD-609 Marking and Labeling of Components, PCBs and PCBA's to Identify Lead (Pb), Lead-Free (Pb-Free) and Other Attributes

1. www.ipc.org

1 INTRODUCTION

Introduction (cont.)

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-TM-650 Test Methods Manual²

- 2.1.1 Microsectioning, Manual and Semi or Automatic Method
- 2.2.2 Optical Dimensional Verification
- 2.2.7 Hole Size Measurement, Plated
- 2.2.13.1 Thickness, Plating in Holes, Microhm Method
- 2.3.25 Detection and Measurement of Ionizable Surface Contaminants
- 2.4.1 Adhesion, Tape Testing
- 2.4.15 Surface Finish, Metal Foil
- 2.4.22 Bow and Twist
- 2.4.28.1 Adhesion, Solder Resist (Mask), Tape Test Method
- 2.6.25 Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing)

IPC-SM-840 Qualification and Performance of Permanent Solder Mask

IPC-2220-FAM Family of Design Documents

IPC-4562 Metal Foil for Printed Wiring Applications

IPC-4781 Qualification and Performance Specification of Permanent, Semi-Permanent and Temporary Legend and/or Marking Inks

IPC-6012 Qualification and Performance Specification for Rigid Printed Boards

IPC-6013 Qualification and Performance Specification for Flexible Printed Boards

IPC-9121 Troubleshooting for PCB Fabrication Processes

IPC-9191 General Requirements for Implementation of Statistical Process Control

IPC-9252 Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-9691 User Guide for the IPC-TM-650, Method 2.6.25, Conductive Anodic Filament (CAF) Resistance Test (Electrochemical Migration Testing)

1.6.2 American Society of Mechanical Engineers³

ASME B46.1 Surface Texture (Surface Roughness, Waviness and Lay)

1.7 DIMENSIONS AND TOLERANCES

All dimensions and tolerances specified herein are applicable only to the end product. Dimensions are expressed in hard SI (metric) units and parenthetical soft imperial [inch] units.

Reference information is shown in parentheses ().

1.8 TERMS AND DEFINITIONS

Terms and definitions **shall** be in accordance with IPC-T-50.

1.9 Revision Level Changes Changes made to this revision of the IPC-A-600 are indicated throughout by gray-shading of the relevant subsection(s). Changes to a figure or table are indicated by gray-shading of the figure or table header.

1.10 WORKMANSHIP

Printed boards fabricated to the requirements of this document **shall** be processed in such a manner as to be uniform in quality and to preclude the introduction of dirt, foreign matter, oil, fingerprints, flux residues, or other contaminants that may affect the life or serviceability of the product. Printed boards **shall** be free of defects in excess of those allowed by this document. Acceptance of imperfections not specifically covered by this document **shall** be AABUS.

2. www.ipc.org/test-methods.aspx

3. www.asme.org

2 EXTERNALLY OBSERVABLE CHARACTERISTICS

Introduction

This section addresses those characteristics which are observable from the surface. This includes those characteristics that are external and internal in the printed board but visible from the surface as follows:

- **Surface Imperfections** such as burrs, nicks, scratches, gouges, cut fibers, weave exposure and voids.
- **Subsurface Imperfections** such as foreign inclusions, measling/crazing, delamination, pink ring and laminate voids.
- **Imperfections in Conductive Pattern** such as loss of adhesion, reduction of conductor width or thickness due to nicks, pin-holes, scratches, surface plating or coating anomalies.
- **Hole Characteristics** such as diameter, misregistration, foreign material, plating or coating anomalies and scratches.
- **Marking Anomalies** including location, size, readability, and accuracy.
- **Solder Mask Surface Coating Imperfections** such as misregistration, blisters, bubbles, delamination, adhesion, physical damage and thickness.
- **Dimensional Characteristics** including printed board size and thickness, hole size and pattern accuracy, conductor width and spacing, registration and annular ring.

2.1 Printed Board Edges

Imperfections such as burrs, nicks or haloing along the edge of the printed board are acceptable provided they do not exceed the limits below.

2.1.1 Burrs

Burrs are characterized by small lumps or masses with an irregular shape, convex to a surface, and are a result of a machine process, such as drilling or gouging.

2.1 PRINTED BOARD EDGES

2.1.1.1 Nonmetallic Burrs



Figure 2111a

Target Condition – Class 1, 2, 3

- Edge conditions – smooth, no burrs.



Figure 2111b

Acceptable – Class 1, 2, 3

- Edge conditions – rough but not frayed.
- Edge conditions – loose burrs do not affect fit and function.

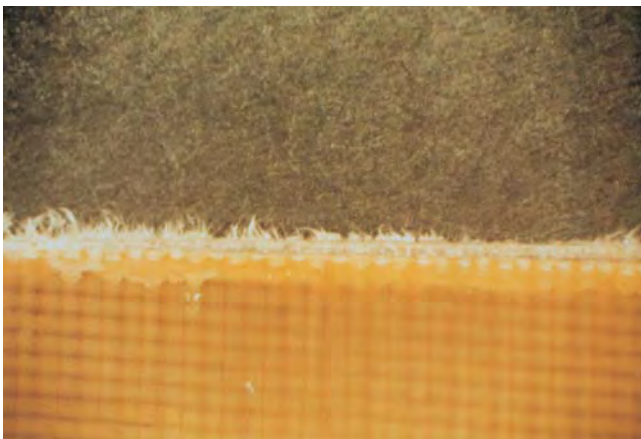


Figure 2111c

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.1 PRINTED BOARD EDGES

2.1.1.2 Metallic Burrs

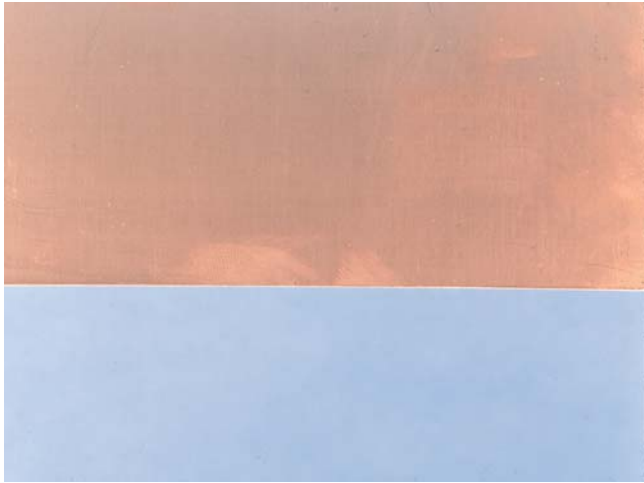


Figure 2112a

Target Condition/Acceptable – Class 1, 2, 3

- Edges **shall** be clean cut and without metallic burrs.



Figure 2112b

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.1 PRINTED BOARD EDGES

2.1.2 Nicks

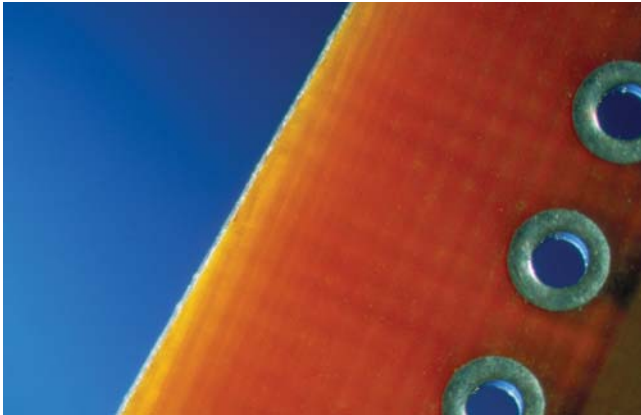


Figure 212a

Target Condition – Class 1, 2, 3

- Edge condition – smooth, no nicks.

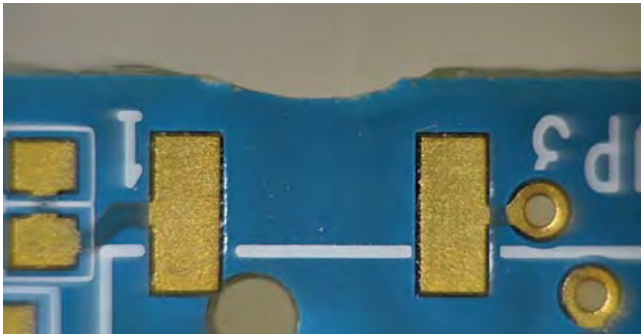


Figure 212b

Acceptable – Class 1, 2, 3

- Edges are rough but not frayed.
- Nicks do not exceed the specified minimum distance between printed board edge and conductive pattern, when edge spacing is designed in accordance with IPC-2222.
- Nicks do not exceed 50% of the distance from the printed board edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less, when no edge spacing requirement is specified and when edge spacing is designed in accordance with IPC-2222.
- Penetration of nicks from the edge of the printed board to the nearest conductor are AABUS when edge spacing is not designed in accordance with IPC-2222.

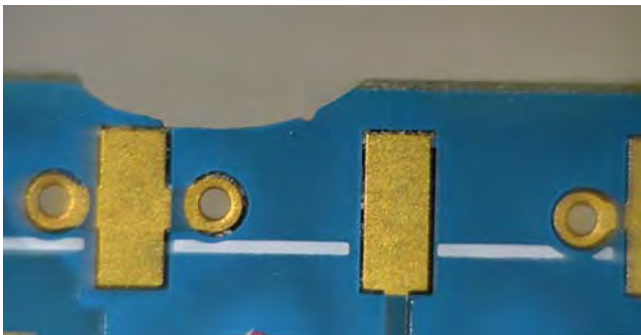


Figure 212c

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.1 PRINTED BOARD EDGES

2.1.3 Haloing

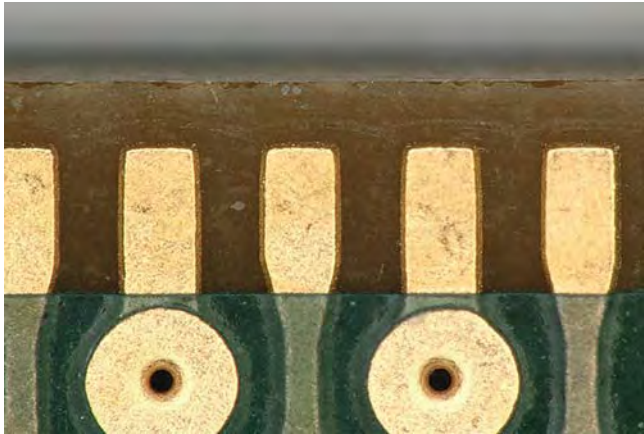


Figure 213a

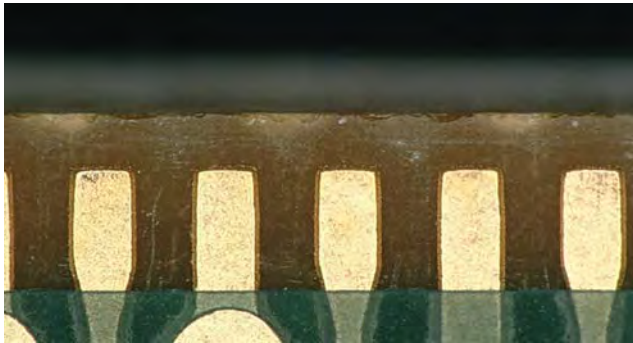


Figure 213b



Figure 213c

Target Condition – Class 1, 2, 3

- No haloing.

Acceptable – Class 1, 2, 3

- Distance between the haloing penetration and the nearest conductive feature is not less than the minimum lateral conductor spacing, or 100 μm [3,937 μin] if not specified, when edge spacing is designed in accordance with IPC-2222.
- Distance between the haloing penetration and the nearest conductive feature is AABUS when edge spacing is not designed in accordance with IPC-2222.

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

Introduction

Identification of Imperfections

Nondestructive visual criteria have been established to aid in the identification and disposition of laminate anomalies. Refer to the following sections where definitions, illustrations and photographs have been provided which precisely define and identify the following conditions:

Surface 2.2

- weave exposure 2.2.1
- weave texture 2.2.2
- exposed/disrupted fibers 2.2.3
- pits and voids 2.2.4

Subsurface 2.3

- measling 2.3.1
- crazing 2.3.2
- delamination/blister 2.3.3
- foreign inclusions 2.3.4

It is important to note that laminate anomalous conditions may exist when the fabricator receives the material from the laminator, or may become apparent during the fabrication of the printed board. Some anomalies may be induced during processing.

2.2 BASE MATERIAL SURFACE

2.2.1 Weave Exposure

Weave Exposure: A surface condition of base material in which the unbroken fibers of woven cloth are not completely covered by resin.

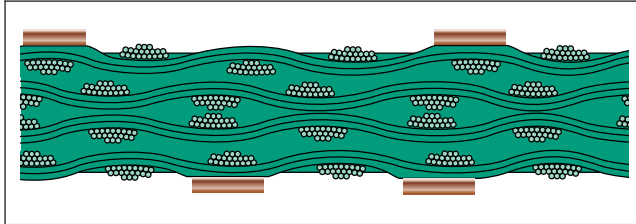


Figure 221a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

Acceptable – Class 3

- No weave exposure.

Acceptable – Class 1, 2

- Excluding the area(s) with weave exposure, the remaining space between conductors meets the minimum conductor spacing requirement.

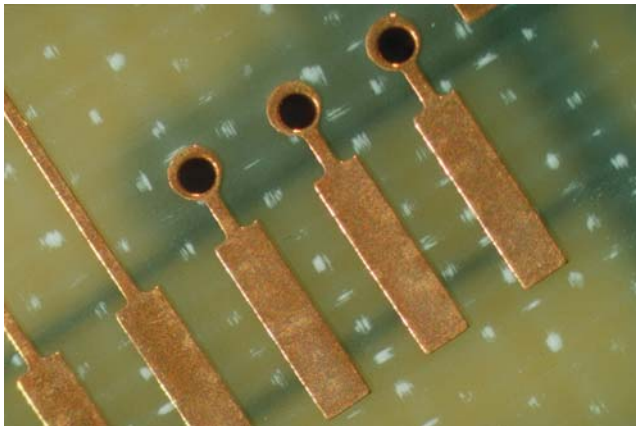


Figure 221b

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.2 BASE MATERIAL SURFACE

2.2.2 Weave Texture

Weave Texture: A surface condition of base material in which a weave pattern of cloth is apparent although the unbroken fibers of woven cloth are completely covered with resin.

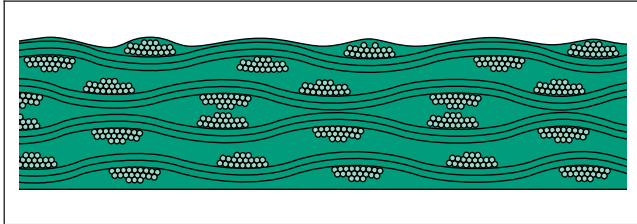


Figure 222a

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

Acceptable – Class 1, 2, 3

- Weave texture is an acceptable condition in all classes but is sometimes confused with weave exposure because of similar appearances.

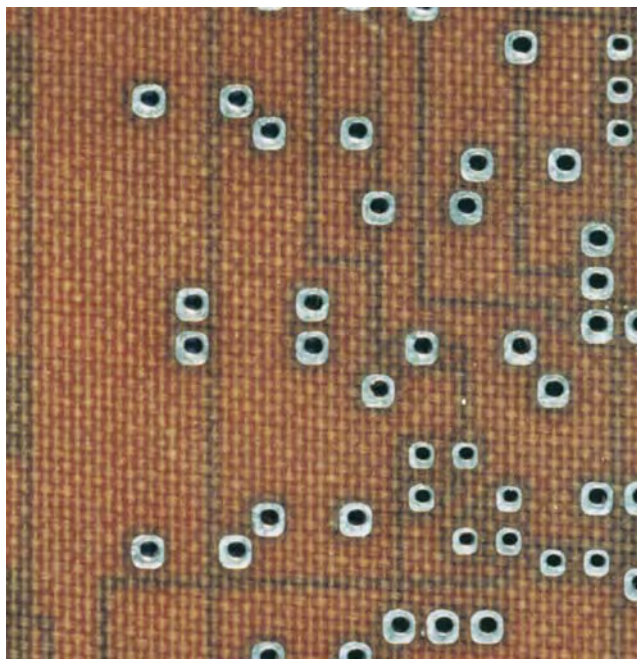


Figure 222b

Figure 222b is an example of a surface condition that could be either weave exposure or weave texture. The difference cannot be determined from this view. The difference can be discerned using nondestructive tests (oblique illumination with microscope) or microsection.

2.2 BASE MATERIAL SURFACE

2.2.3 Mechanically Induced Disrupted Fibers

Disrupted Fibers: Localized separation of glass fibers from the resin, induced by mechanical damage or stress to the printed board.

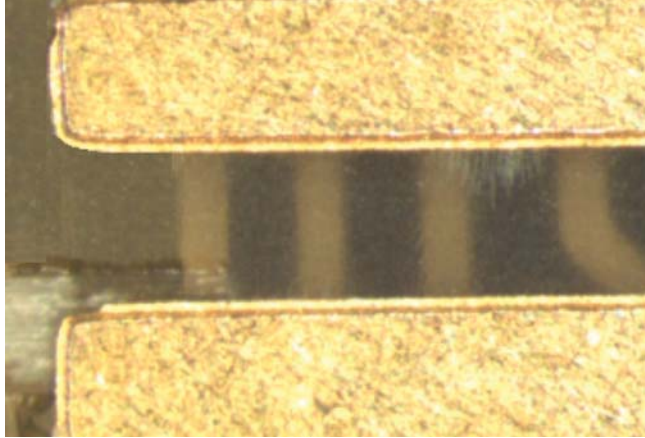


Figure 223a

Acceptable – Class 1, 2, 3

- Exposure of disrupted fibers due to mechanical damage does not bridge conductors and does not reduce the remaining lateral conductor spacing below the minimum requirements.

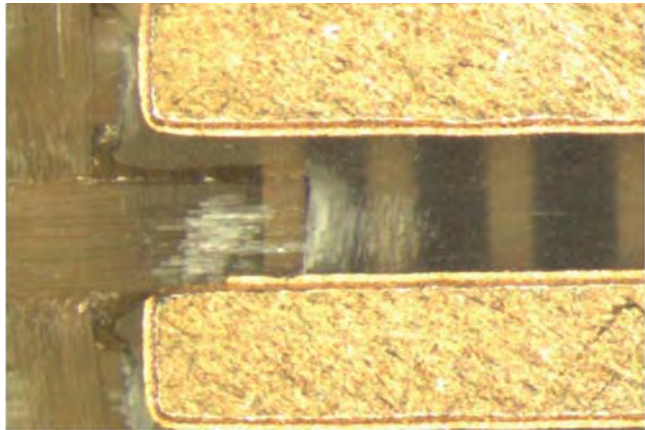


Figure 223b

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.2 BASE MATERIAL SURFACE

2.2.4 Surface Voids



Figure 224a

Target Condition – Class 1, 2, 3

- No pits or voids.

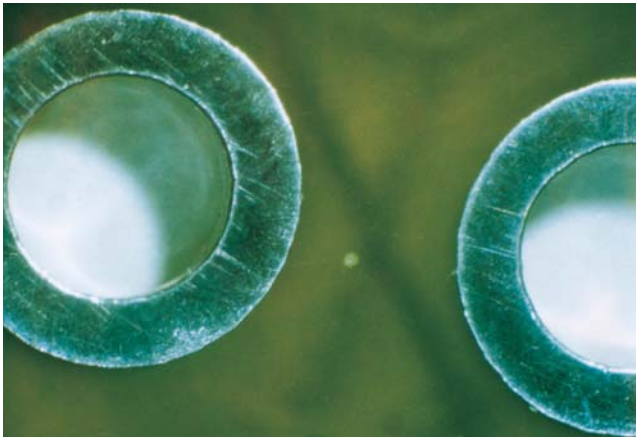


Figure 224b

Acceptable – Class 1, 2, 3

- Surface voids do not exceed 0.8 mm [0.031 in] in the longest dimension.
- Surface voids do not exceed more than 5% of the total printed board area per side.
- Surface voids do not bridge conductors.

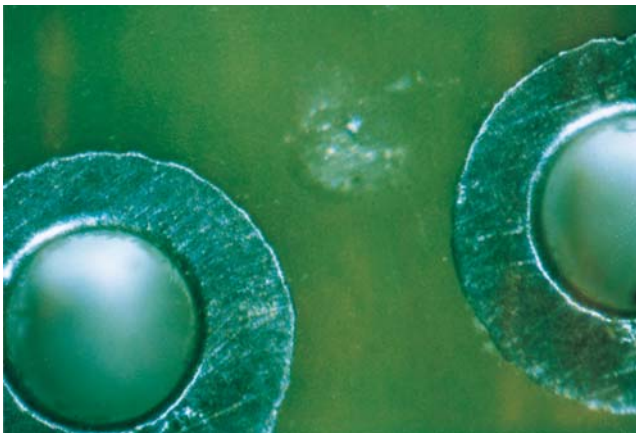


Figure 224c

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.3 BASE MATERIAL SUBSURFACE

Introduction

This section is focused on those subsurface conditions of laminated base materials that are externally observable through the base material itself and some solder mask coatings. The most frequent subsurface base material conditions are termed measling, crazing, delamination, blistering and foreign materials. These conditions may be observed throughout the printed board manufacturing and inspection process; such as:

- During incoming metal-clad base material evaluations after being manufactured by the laminator,
- By the printed board manufacturer after having removed (etched) the metal cladding in the preparation of “innerlayer” details for multilayer printed boards,
- After etching the “outer” layers of printed board to form the required arrangement of conductive patterns and markings,
- After baking operations (such as solder mask or component legends),
- After thermal shock, as in solder fusing/coating or solderability testing processes.

Base material subsurface conditions have been the subject of considerable discussion within the printed board industry for several decades. Of the several subsurface conditions, measling and crazing continue to cause the most concerns. Measles and crazing have been the primary focus of three IPC “Blue Ribbon Committees” of experts. The following are brief summaries and additional comments from the IPC Blue Ribbon Committees:

Brief summary of the First IPC Blue Ribbon Committee on Measles

This first committee conducted a wide overview of printed board base material surface and subsurface conditions with a major focus on measles. IPC’s “Measles in Printed Wiring Boards, Information Document” was published in 1973 as a result of this effort. The committee was to collect as much data as was available on measles and other surface/subsurface conditions; and to standardize the terms, definitions (descriptions), photographs, and illustrations of surface and subsurface conditions. It was felt that sufficient research had been done by industry and that a position on “measles” could be prepared by the committee. The committee’s recommendation was as follows, “comprehensive review of available literature and available research and test data, that while measles may be objectionable cosmetically, their effect on functional characteristics of finished products, are at worst minimal, and in most cases insignificant.”

Comments: Despite the committee’s recommendation and industry data, there was still a strong reluctance by most government and industry personnel to accept that measles are a cosmetic condition with no functional effect in most applications. Most companies continued to retain “no measling” requirements in their specifications. But when measles or other nonconforming surface/subsurface conditions had severe impact on their production schedules, the customer (or acceptance agency) would produce a document that established acceptance guidelines for measles (and frequently other surface and subsurface conditions). The new guidelines were based on size, percent reduction in conductor spacing, and amount of affected area. They also varied from customer-to-customer. As technology evolved, in particular reductions in conductor spacing, the effect of measling and other surface/subsurface conditions once again became a serious industry wide concern. As a result, a second IPC Blue Ribbon Committee on Measles was formed.

Introduction (cont.)

Brief summary of the Second IPC Blue Ribbon Committee on Measles

This second committee was formed in late 1978. This committee reviewed the findings of the first committee, solicited the industry for additional data, and reviewed the proprietary acceptance criteria provided by IPC members. The Second Blue Ribbon Committee came to the same conclusion. Measles are a cosmetic process indicator and had almost no reported effects on a product's functional performance in most applications. The major exception was high voltage applications. There was still reluctance by some government organizations and a few industrial companies to categorically accept measles. As such, this committee established a set of measling/crazing requirements that obtained consensus from all IPC members. The result was a matrix of acceptance limitations for the three major phases of the printed board electronic assembly process: laminated material, printed board final inspection, and after printed board assembly. These requirements included percent reductions in conductor spacing (not exceeding minimum conductor spacing), and various amounts of measled area for each side of the printed board (or assembly) based on the Class of product. These requirements were added as an amendment to the first printing of the IPC-A-600, Revision C, and were included in later printings of the C revision and, in a different format, the IPC-A-600, Revision D.

Comments: The primary concerns expressed by the reluctant individuals are summarized in the following list (with comments):

- Electrical Insulation Resistance, both volume and surface – several reports and available test data indicates that insulation resistance is not significantly affected by measling or crazing.
- Contamination – the concern was that ionic materials could diffuse or be “pumped” (by alternating atmospheric pressure) into measles or crazing and would result in lower insulation resistance or conductive anodic filament (CAF) growths, shorts. Salt spray tests indicated this was not a valid premise, and most ionic materials (such as salts) will not diffuse into the base material.
- Applied Voltages – high voltage applications are a concern (in particular where there is the possibility of “corona” in the measling or crazing) the dielectric strength is reduced by 20-50% in comparison to a similar non-measled/crazed area, in particular at altitudes greater than 20 km [12.43 miles].
- Environmental – most measling/crazing did not appear to increase in size or occurrence due to environmental testing.

IPC-A-600, Revision E, was the first revision to reflect the needs for surface mounted component technology. As such, the acceptance requirements for measling and crazing were separated. For measles, the acceptance requirements allowed bridging under surface conductor spacing. This was done based on the definition of measles, test data, and industry experience of measles having never been documented to cause a functional failure. Crazing is much less controlled separation in the base material forming “interconnections” between measles and possibly adjacent conductive patterns; therefore, the acceptance requirements for crazing were set the same as the similar conditions of delamination and blistering.

Over a period of time, governing specifications have become excessively heavy regarding the presence of measles. In addition, cosmetic appearance has become a major acceptance criterion. In actual fact, no failure has ever been attributed to measling, based on all military and industry testing to date. IPC, industry and various military agencies have conducted extensive testing in severely measled assemblies under extreme environmental conditions for long periods of time with no evidence of growth, spreading or any detriment to the function of the assembly. Measles should not be the cause for rejection.

2.3 BASE MATERIAL SUBSURFACE

Introduction (cont.)

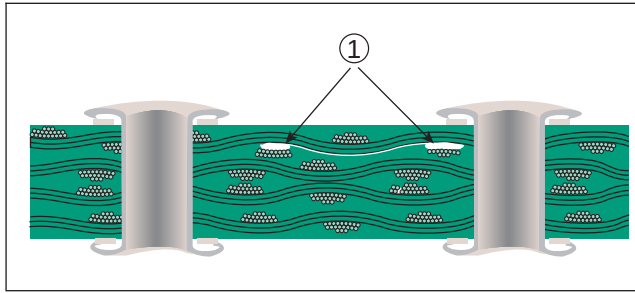


Figure 23a Example of Crazing

Note 1: Irregularly shaped white spots in non-woven material.

Note 2: This graphic is for illustrative purposes only and does not require a microsection evaluation.

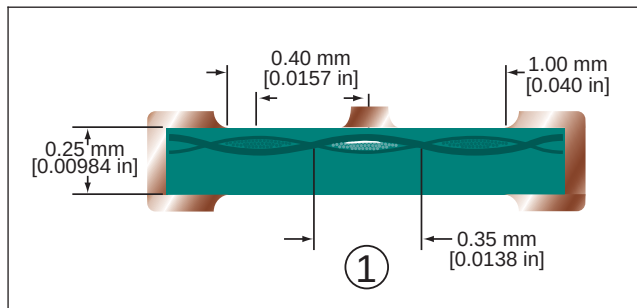


Figure 23b Example of Measling

Note 1: Measle centered between two PTHs

Note 2: This graphic is for illustrative purposes only and does not require a microsection evaluation.

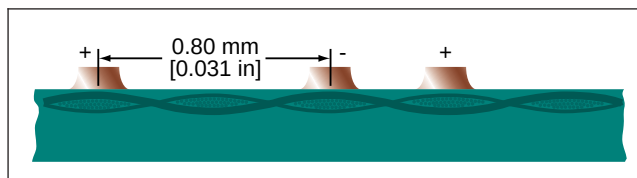


Figure 23c Example of Potential Failure Mechanism Between Two Surface Conductors

Note: This graphic is for illustrative purposes only and does not require a microsection evaluation.

Measling is an internal condition occurring in the woven fiber reinforced laminated base material in which the bundles are separated at the weave intersection. The term “crazing” is sometimes used to describe an array of measles which appear from the surface to be interconnected. When the measles look to be interconnected, this condition called “crazing” is a form of delamination in that there are separations along the length of the fiber/yarns and the resin. For non-woven material, this condition resembles a measle but is randomly located and has an irregular shape (see Figure 23a).

In a case study done, the prime cause of the observed measles was a combination of moisture, which diffuses readily into epoxy-glass, and component soldering temperatures. The application of local high temperatures for component mounting caused entrapped moisture to vaporize and break the epoxy-glass bond at the “knuckle” (intersection of the warp and fill of the e-glass cloth). From previous experience, it is known that epoxy-glass absorbs atmospheric moisture, and when moisture content exceeds 0.3 wt%, it can give rise to measling during solder dip/level and/or assembly soldering operations.

There are other factors that can contribute to measles/crazing such as: resin composition, method of making laminates, coupling agents, T_g , etc. In the past, reports were compiled which revealed that measles and crazing with over 50% spacing violation were not adverse to the reliability of the hardware. Why, if all test reports showed no problems with measles and no reported field failures, are we so concerned about measles and crazing? Because it appears feasible, in theory, that if measles with 100% conductor spacing violation combines with moisture or some other contaminant, copper migration (IR failures) should be experienced between conductors.

2.3 BASE MATERIAL SUBSURFACE

Introduction (cont.)

Even when the potential failure mechanism mentioned above is analyzed, it is almost impossible to experience such (IR/ migration) failure. First, a measle(s) gapping conductive patterns is needed. Secondly, moisture in the printed board/ assembly, along with a conductive or ionic contaminant such as chlorides, is necessary.

In this instance, a typical industry example, the measle is at the center between two plated through holes (see Figure 23b). The measle is 0.4 mm [0.0157 in] wide. In order to get possible copper migration, the measle had to gap the two plated through holes. This of course would be most unlikely. The second example (see Figure 23c) illustrates what is required for a potential failure mechanism between two surface conductors. A (+) conductor directly over a knuckle is required and a (-) conductor is also required directly over a knuckle. For an electrical short to occur between these conductors through the base material, there would need to be a conductive path from one conductive pattern, through the remaining dielectric materials (resin and yarn) to the separation (measle), along the separation in the direction of the other conductive pattern, once again through the remaining dielectric materials (resin and yarn), and to the second conductive pattern. In order to induce a failure all of the above mentioned ingredients are required along with a voltage potential between two adjacent conductors. This occurrence is highly unlikely and is most likely why the industry has not experienced any adverse reliability problems due to measles.

When making acceptance calls on electronic hardware, consider all the possible concerns mentioned above. Measles should not be considered a nonconforming condition. It should instead be considered a process indicator, telling you that the process is on the verge of going out of control. Correct the problem, but do not scrap the product, taking into account all of the above mentioned variables.

Brief summary of the Third IPC Blue Ribbon Committee on Measles

In 2004, the issue of printed board laminate degradation caused by internal Conductive Anodic Filament (CAF) growth came to the forefront of discussions among the IPC printed board assembly standards groups (including the 7-31b IPC-A-610 and 5-22a National Standard for Soldering task groups.) It was observed that circuit density, operating speed, band pass and reduced operating voltage had impacted the ability of circuits to operate under conditions supporting dendrite or CAF development.

With the proliferation of finer line conductors and reduced spacing in current designs, discussions within the assembly standards groups questioned the role of measles within printed board laminate materials as a potential catalyst for CAF growth.

2.3 BASE MATERIAL SUBSURFACE

Introduction (cont.)

For years, IPC standards for electronic production contained no restrictions for the occurrence of measles in printed boards and/or assemblies. Theoretically, measles could be continuous between conductors and could exist throughout the printed board. It was noted that this allowance was based on studies conducted nearly 30 years earlier based on circuit designs from that time period. It was recognized that a need existed to reconsider the measles requirements for today's production designs and product environment.

In the interim, as a means to call attention to this potential problem, IPC assembly documents were changed to include pass/fail (defect) criteria for Class 3 assemblies that exhibited the visual appearance of measles.

The new measles criteria created in the assembly documents defined requirements that were stricter than those given in the printed board documents unless the additional IPC-6012 space and military avionics addendum requirements were considered. The IPC-6012 space and military avionics addendum does not allow measles in bare boards for these industry segments, however Class 3 printed boards produced in accordance with IPC-6012, which exhibited measles, were no longer acceptable for use in the assembly documents for Class 3 in general. This requirement conflict was brought to the attention of the IPC Technical Activities Executive Committee (TAEC) and that body directed both groups to work together to come to some resolution, based on test data that would bring the documents into agreement on the acceptance criteria.

The leadership of the printed board standards committees formed a new Blue Ribbon Committee on Measles and designed and performed testing to determine if measles contributed to CAF failures in actual end product. This test protocol was completed in late 2006 and presented to the printed board standards committees at IPC Printed Circuits Expo/APEX 2007. There was conclusive evidence within the test that measles did not contribute to CAF growth; nor did the presence of measles promote CAF failures in the end product that exhibited CAF.

This presentation was then given to the assembly standards groups for their consideration. The request was made that the requirements in the bare printed board and assembly documents be changed to track with each other.

The leadership of the assembly standards groups concurred that the industry now had test data that addressed their original concerns regarding the potential of measles to promote CAF failures. They also agreed that the documents should be amended to eliminate the conflicting measles requirements. The groups jointly drafted the words, comments, and instructions for all documents regarding measles and these were presented to the committee membership at the 2007 IPC Midwest Conference. Copies of the test protocol summary are available through the IPC.

2.3 BASE MATERIAL SUBSURFACE

2.3.1 Measling

Measling: Measling manifests itself in the form of discrete white squares or “crosses” below the surface of the base material, and is usually related to thermally induced stress. Measles are subsurface phenomena that have been found in new laminated materials and in every board type made from woven fiber reinforced laminates at one time or another. Since measles are strictly subsurface phenomena and occur as a separation of fiber bundles at fiber bundle intersections, their apparent positions relative to surface conductors have no significance.



Figure 231a

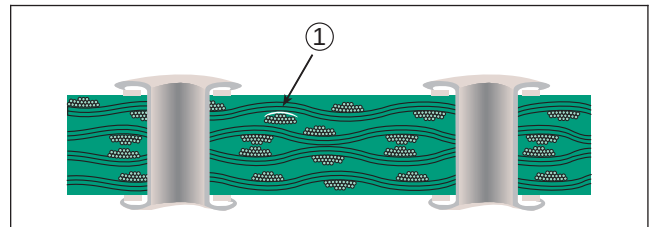


Figure 231b

Note 1: Measling

Note 2: This graphic is for illustrative purposes only and does not require a microsection evaluation.



Figure 231c

Note: Measles are observed from the surface. Cross-sections are for illustration purposes only.

2.3 BASE MATERIAL SUBSURFACE

2.3.1 Measling (cont.)

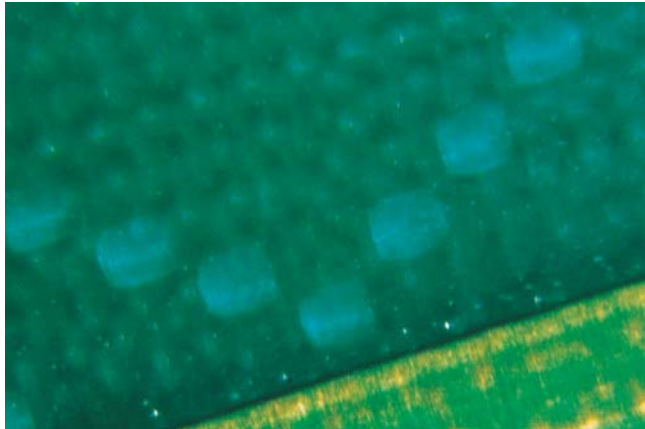


Figure 231d

Target – Class 1, 2, 3

- No evidence of measling.

Acceptable – Class 1, 2

- The criteria for measling is that the printed board is functional.

Process Indicator – Class 3

- Measled areas in laminate substrates exceed 50% of the physical spacing between noncommon conductors.

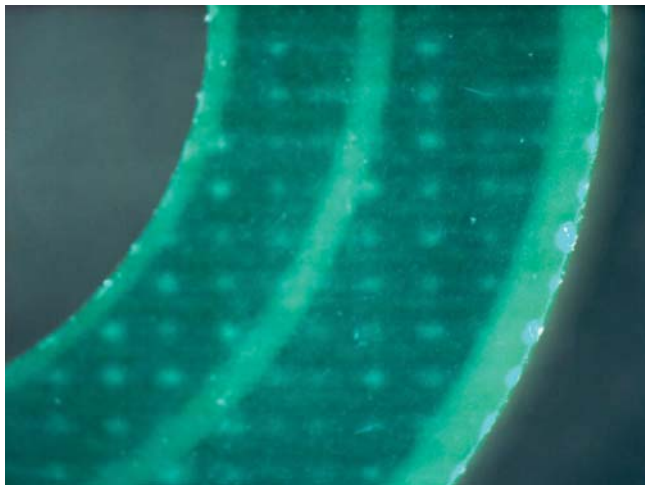


Figure 231e

Note: Measling is an internal condition which does not propagate as a result of thermal testing that replicates future assembly processes and has not been conclusively shown to be a catalyst for CAF growth. Delamination is an internal condition which may propagate under thermal stress and may be a catalyst for CAF growth. The IPC-9691 user's guide for CAF resistance testing and IPC-TM-650, Method 2.6.25, provide additional information for determining laminate performance regarding CAF growth. Users who wish to incorporate additional criteria for measle conditions may consider invoking the IPC-6012 space and military avionics addendum requirements which does not allow the presence of measles.

Note: Measles are observed from the surface. Cross-sections are for illustration purposes only.

2.3 BASE MATERIAL SUBSURFACE

2.3.2 Crazing

Crazing: An internal condition occurring in the laminated base material in which the fibers within the yarn are separated. This can occur at the weave intersections or along the length of the yarn. This condition manifests itself in the form of connected white spots or “crosses” below the surface of the base material, and is usually related to mechanically induced stress. When the crosses are connected the condition is evaluated as follows:



Figure 232a

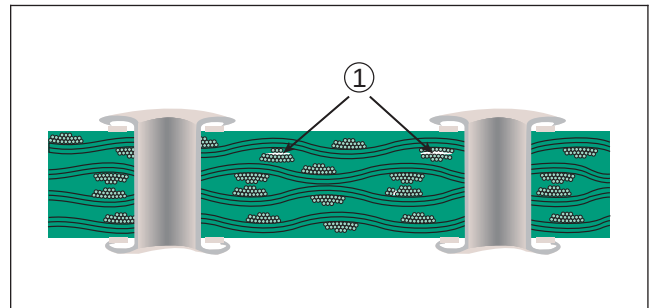


Figure 232b

Note 1: Crazing

Note 2: This graphic is for illustrative purposes only and does not require a microsection evaluation.



Figure 232c

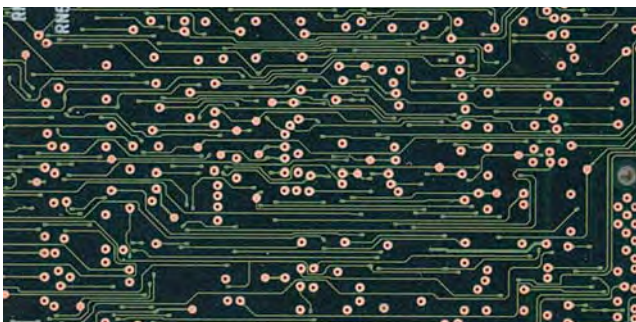


Figure 232d

Target Condition – Class 1, 2, 3

- No evidence of crazing.

Note: Crazing is observed from the surface. Cross-sections are for illustration purposes only.

2.3 BASE MATERIAL SUBSURFACE

2.3.2 Crazing (cont.)

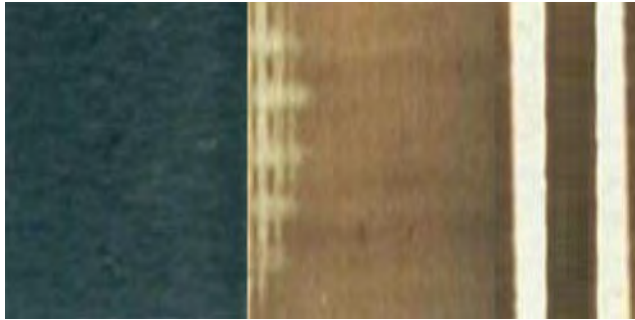


Figure 232e

Acceptable – Class 2, 3

- The imperfection does not reduce the conductor spacing below the minimum.
- The distance of crazing does not span more than 50% of the distance between adjacent conductors.
- No propagation of the imperfection as a result of thermal testing that replicates the manufacturing process.
- Crazing does not exceed the specified minimum distance between printed board edge and conductive pattern when edge spacing is designed in accordance with IPC-2222.
- Crazing does not exceed 50% of the distance from the printed board edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less, when no edge spacing requirement is specified and when edge spacing is designed in accordance with IPC-2222.
- Penetration of crazing from the edge of the printed board to the nearest conductor are AABUS when edge spacing is not designed in accordance with IPC-2222.

Acceptable – Class 1

- The imperfection does not reduce the conductor spacing below the minimum.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- Crazing does not exceed the specified minimum distance between printed board edge and conductive pattern when edge spacing is designed in accordance with IPC-2222.
- Crazing does not exceed 50% of the distance from the printed board edge to the nearest conductor or 2.5 mm [0.0984 in], whichever is less, when no edge spacing requirement is specified and when edge spacing is designed in accordance with IPC-2222.
- Penetration of crazing from the edge of the printed board to the nearest conductor are AABUS when edge spacing is not designed in accordance with IPC-2222.

Note: Crazing is observed from the surface. Cross-sections are for illustration purposes only.

2.3 BASE MATERIAL SUBSURFACE

2.3.2 Crazing (cont.)

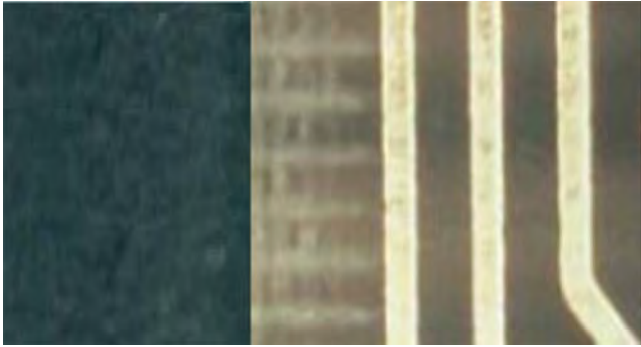


Figure 232f

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

Note: Crazing is observed from the surface. Cross-sections are for illustration purposes only.

2.3 BASE MATERIAL SUBSURFACE

2.3.3 Delamination/Blister

Delamination: A separation between plies within a base material, between a material and conductive foil, or any other planar separations within a printed board.

Blister: Delamination in the form of a localized swelling and separation between any of the layers of a lamination base material, or between base material and conductive foil or protective coating.

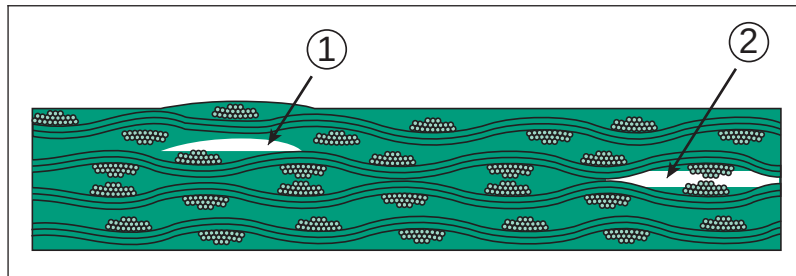


Figure 233a

Note 1: Blistering

Note 2: Delamination

Note 3: This graphic is for illustrative purposes only and does not require a microsection evaluation.

2.3 BASE MATERIAL SUBSURFACE

2.3.3 Delamination/Blister (cont.)

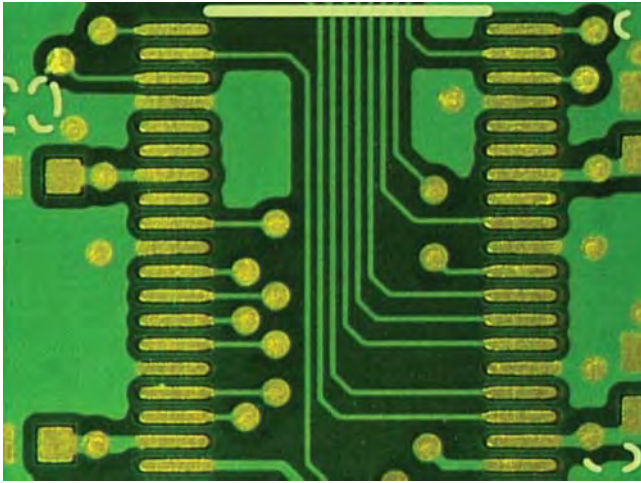


Figure 233b

Target Condition – Class 1, 2, 3

- No blistering or delamination.

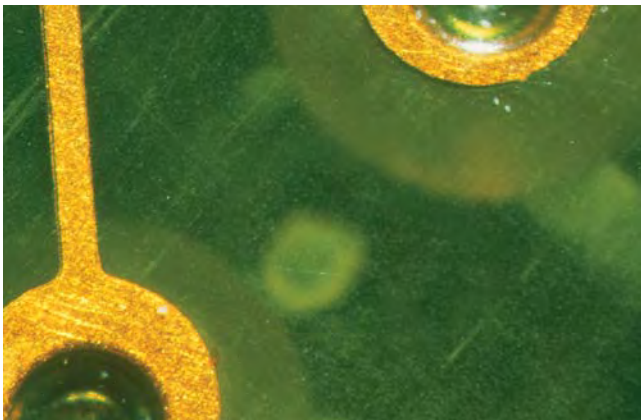


Figure 233c

Acceptable – Class 2, 3

- The area affected by imperfections does not exceed 1% of the printed board area on each side.
- The imperfection does not reduce the distance between conductive patterns below the minimum conductor spacing.
- The blister or delamination does not exceed more than 25% of the distance between adjacent conductive patterns.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- The imperfection does not exceed the specified minimum distance between printed board edge and conductive pattern. If no edge spacing requirement is specified, any base material edge delamination does not exceed 2.5 mm [0.0984 in].

2.3 BASE MATERIAL SUBSURFACE

2.3.3 Delamination/Blister (cont.)



Figure 233d

Acceptable – Class 1

- The area affected by imperfections does not exceed 1% of the printed board area on each side.
- The blister or delamination spans more than 25% of the distance between conductors, but does not reduce the space between conductor patterns below the minimum conductor spacing.
- No propagation as a result of thermal testing that replicates the manufacturing process.
- The imperfection does not exceed the specified minimum distance between printed board edge and conductive pattern. If no edge spacing requirement is specified, any base material edge delamination does not exceed 2.5 mm [0.0984 in].



Figure 233e

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

Note: The area affected is determined by combining the area of each imperfection and dividing by the total area of the printed board. A separate determination is made for each side.

2.3 BASE MATERIAL SUBSURFACE

2.3.4 Foreign Inclusions

Foreign Particles: Metallic or nonmetallic, which may be entrapped or embedded in an insulating material.

Foreign material may be detected in raw laminate, B stage, or processed multilayer printed boards. The foreign objects may be conductive or nonconductive, and both types may be nonconforming depending on size and location.

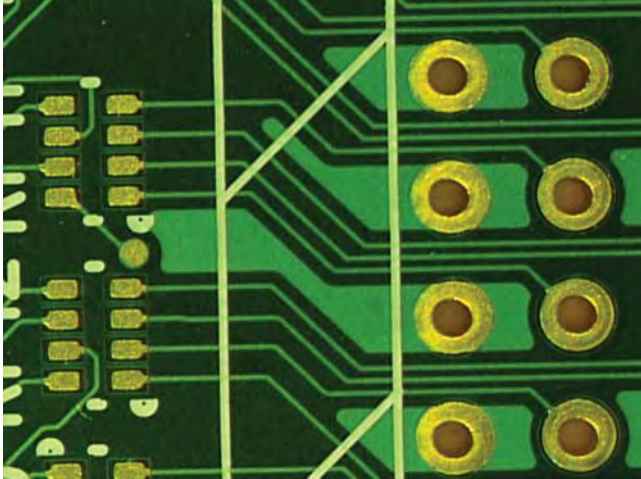


Figure 234a

Target Condition – Class 1, 2, 3

- No foreign inclusions.



Figure 234b

Acceptable – Class 1, 2, 3

- Translucent particles trapped within the printed board.
- Opaque particles trapped within the printed board do not reduce the spacing between adjacent conductors to below the minimum spacing specified.

2.3 BASE MATERIAL SUBSURFACE

2.3.4 Foreign Inclusions (cont.)



Figure 234c

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.4 SOLDER COATINGS AND FUSED TIN LEAD

2.4.1 Nonwetting

Nonwetting: The inability of molten solder to form a metallic bond with the basis metal.

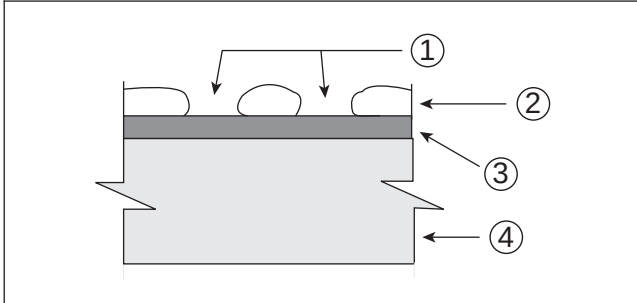


Figure 241a

Note 1: Nonwetting

Note 2: Solder

Note 3: Basis Metal

Note 4: Base Material

Note 5: This graphic is for illustrative purposes only and does not require a microsection evaluation.

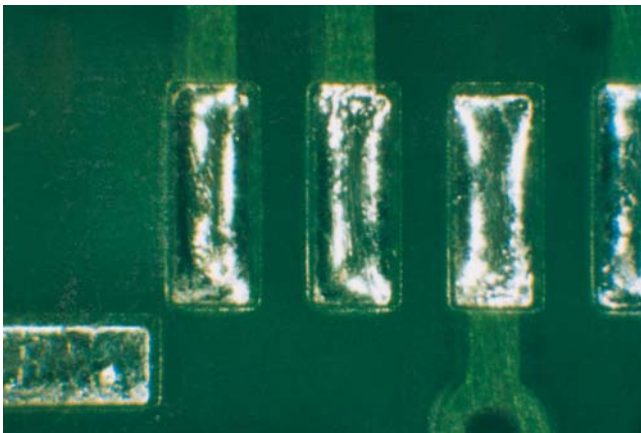


Figure 241b

Target Condition – Class 1, 2, 3

- No nonwetting.

Acceptable – Class 1, 2, 3

- Complete wetting on all conductive surfaces where a solder connection will be required. Vertical sides (conductor and land) areas may not be covered.

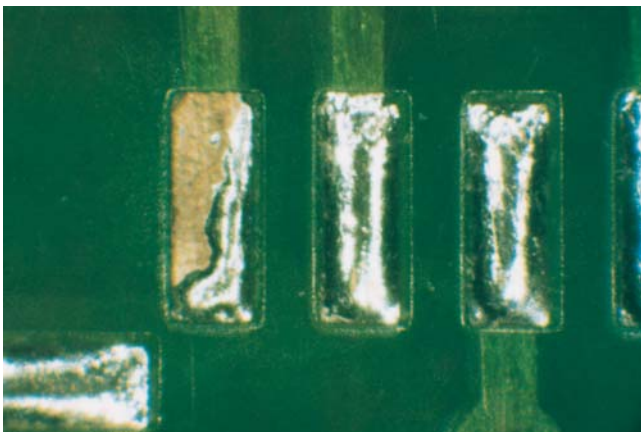


Figure 241c

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.4 SOLDER COATINGS AND FUSED TIN LEAD

2.4.2 Dewetting

Dewetting: A condition that results when molten solder coats a surface and then recedes to leave irregularly-shaped mounds of solder that are separated by areas that are covered with a thin film of solder and with the basis metal not exposed.

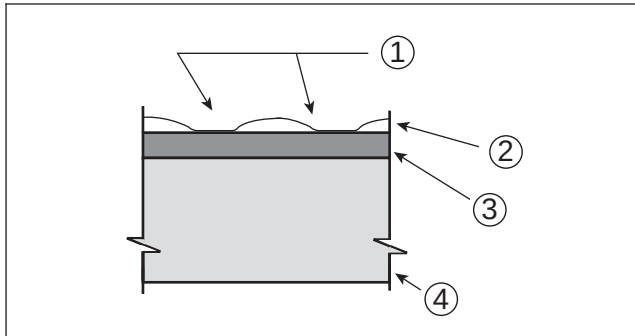


Figure 242a

Note 1: Nonwetting

Note 2: Solder

Note 3: Basis Metal

Note 4: Base Material

Note 5: This graphic is for illustrative purposes only and does not require a microsection evaluation.

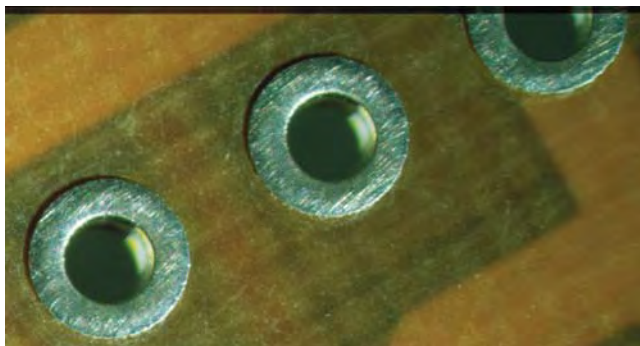


Figure 242b

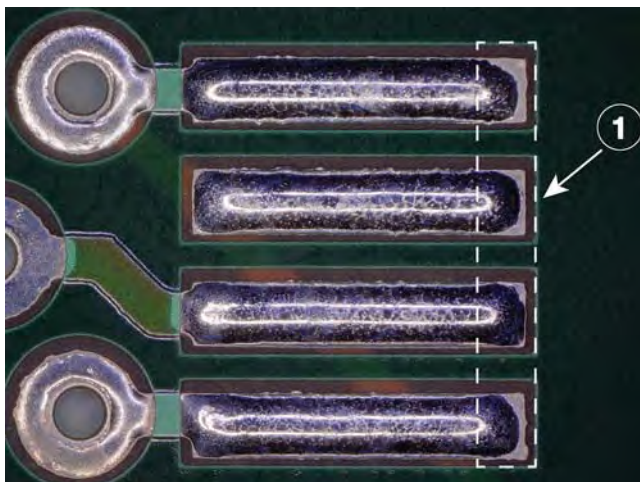


Figure 242c

Note 1. Area of dewetting.

Target Condition – Class 1, 2, 3

- No dewetting.

Acceptable – Class 2, 3

- On conductors and ground or voltage planes.
- On 5% or less of each land area for solder connection.

Acceptable – Class 1

- On conductors and ground or voltage planes.
- On 15% or less of each land area for solder connection.

2.4 SOLDER COATINGS AND FUSED TIN LEAD

2.4.2 Dewetting (cont.)

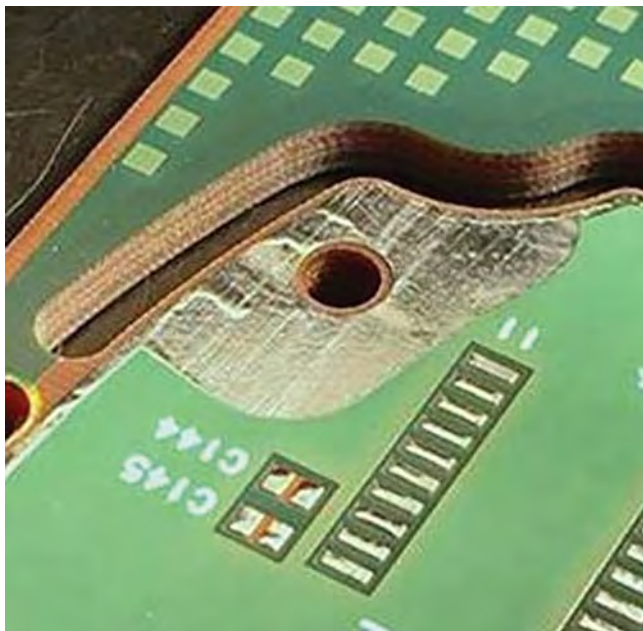


Figure 242d

Note: Thickness variation is a natural part of the HASL process and is not considered receding or dewetting solder. The high-low solder is due to solder movement from the air knife and not a reflection of surface preparation and can be confirmed through solderability testing to IPC-J-STD-003.

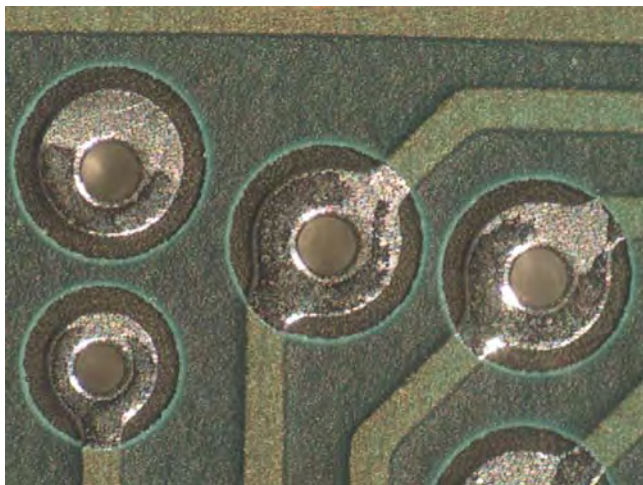


Figure 242e

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.1 Nodules/Rough Plating

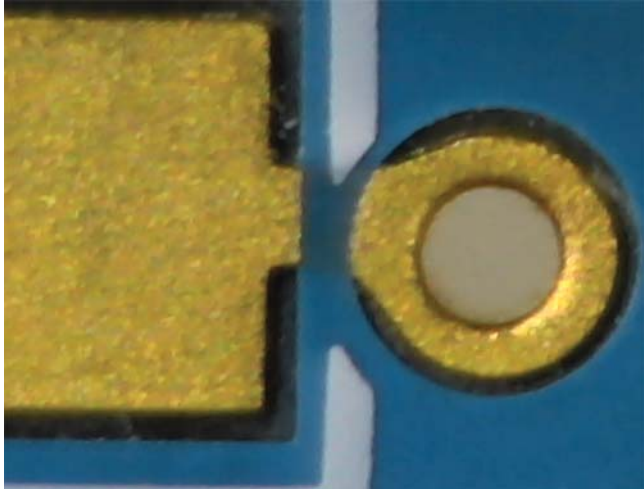


Figure 251a

Target Condition – Class 1, 2, 3

- No evidence of nodules or rough plating.

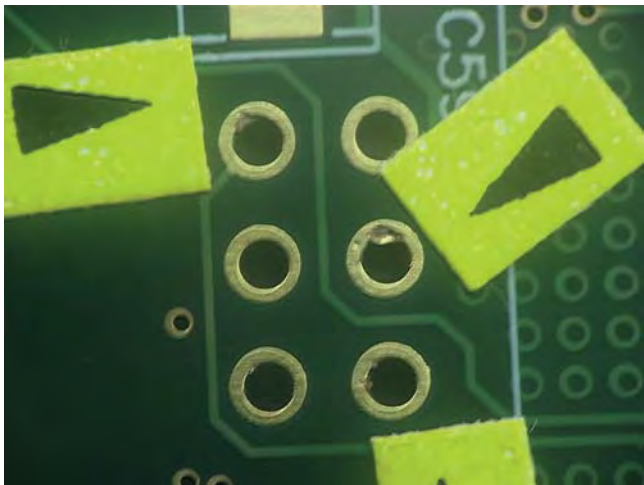


Figure 251b

Acceptable – Class 1, 2, 3

- Nodules or rough plating that do not reduce the hole diameter below the minimum limits defined in the procurement documentation.



Figure 251c

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.2 Pink Ring

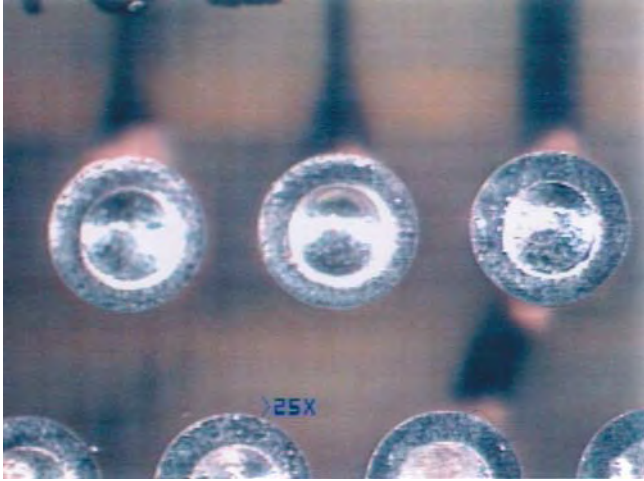


Figure 252a

Acceptable – Class 1, 2, 3

- No evidence exists that pink ring affects functionality. The presence of pink ring may be considered a process indicator but is not nonconforming. The focus of concern should be the quality of the lamination bond and hole cleaning and conditioning processes.

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.3 Voids – Copper Plating

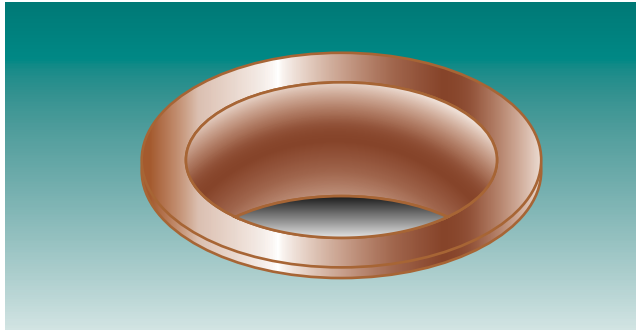


Figure 253a

Target Condition – Class 1, 2, 3

- No voids.

Acceptable – Class 3

- No evidence of voids in the hole.

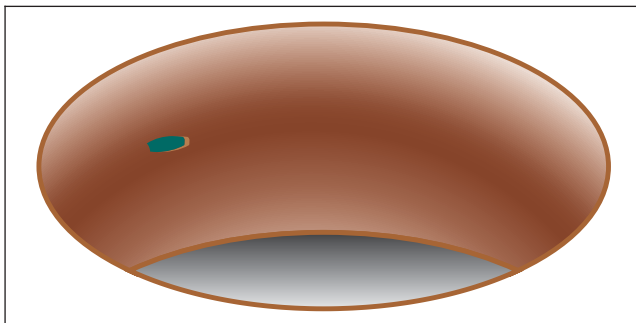


Figure 253b

Acceptable – Class 2

- No more than one void in any hole.
- Not more than 5% of the holes have voids.
- Any void is not more than 5% of the hole length.
- The void is less than 90° of the circumference.

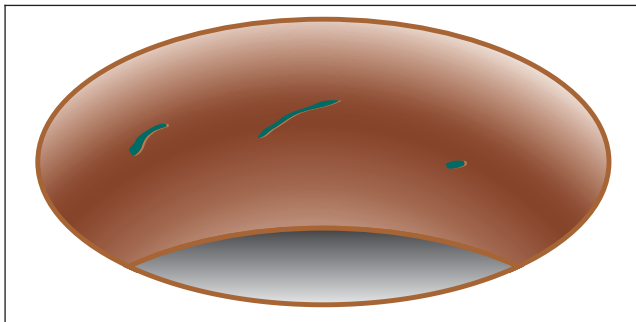


Figure 253c

Acceptable – Class 1

- No more than three voids in any hole.
- Not more than 10% of the holes have voids.
- Any void is not more than 10% of the hole length.
- All voids are less than 90° of the circumference.

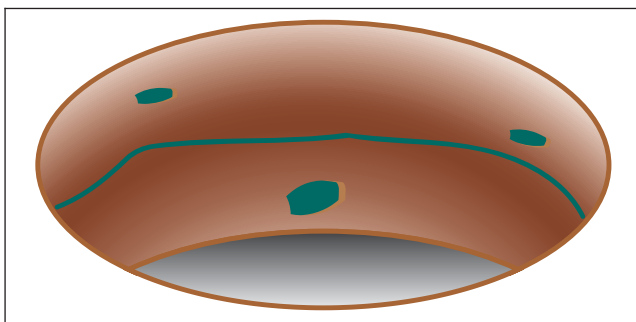


Figure 253d

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.4 Voids – Finished Coating

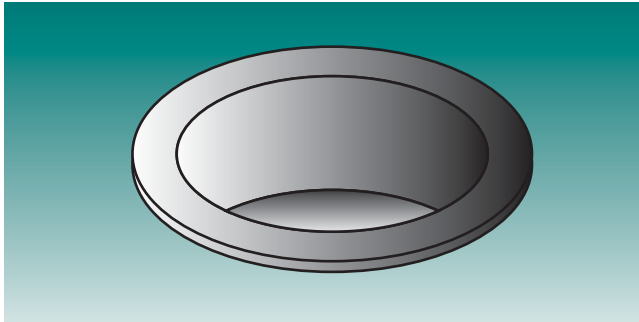


Figure 254a

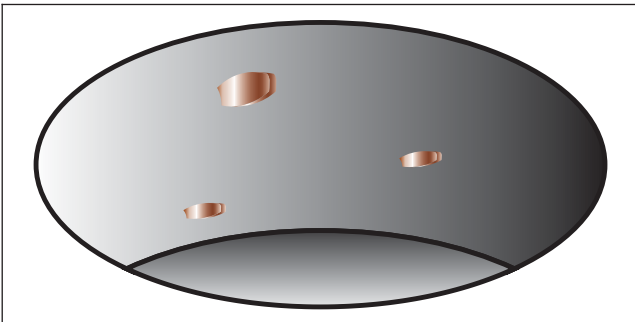


Figure 254b

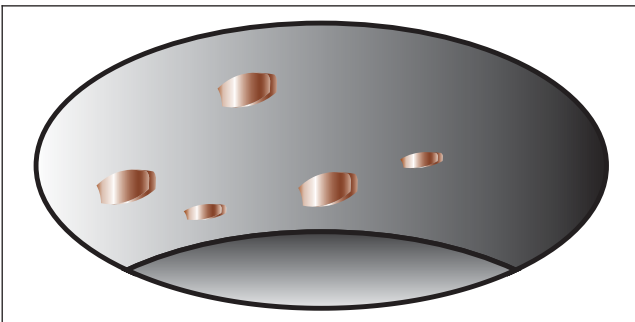


Figure 254c

Target Condition – Class 1, 2, 3

- No voids.

Acceptable – Class 3

- No more than one void in any hole.
- Not more than 5% of the holes have voids.
- The void is not more than 5% of the hole length.
- The void is less than 90° of the circumference.

Acceptable – Class 2

- No more than three voids in any hole.
- Not more than 5% of the holes have voids.
- Any void is not more than 5% of the hole length.
- All voids are less than 90° of the circumference.

Acceptable – Class 1

- No more than five voids in any hole.
- Not more than 15% of the holes have voids.
- Any void is not more than 10% of the hole length.
- All voids are less than 90° of the circumference.

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.5 Lifted Lands – (Visual)



Figure 255a

Target Condition/Acceptable – Class 1, 2, 3

- No lifting of lands.

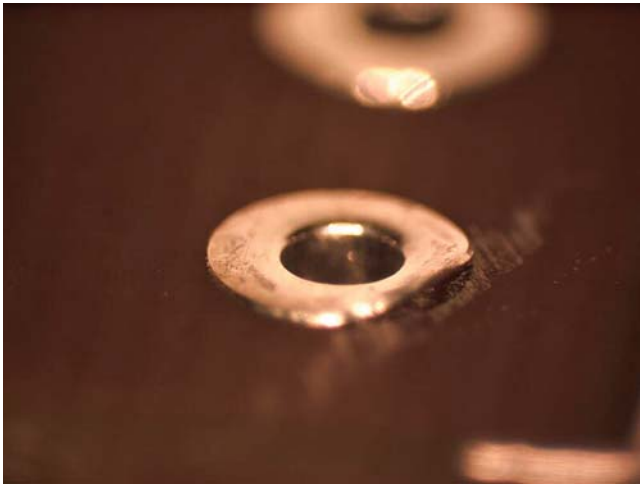


Figure 255b

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

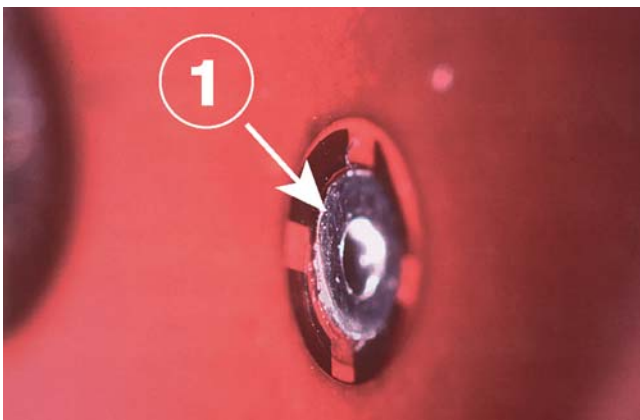


Figure 255c

Note 1: Lifted Land

2.5.6 Cap Plating of Filled Holes – (Visual)

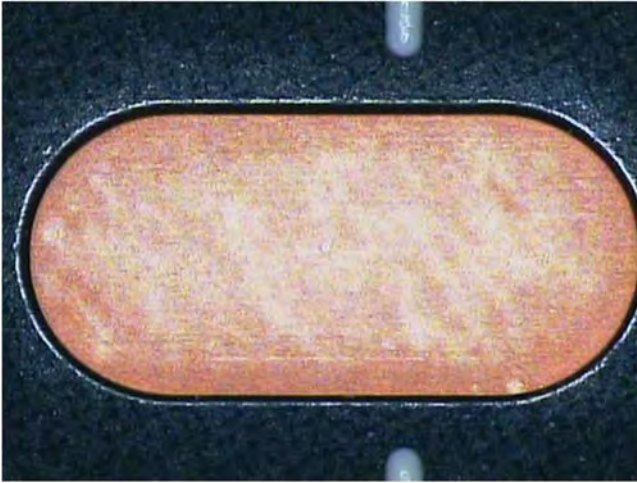


Figure 256a



Figure 256b

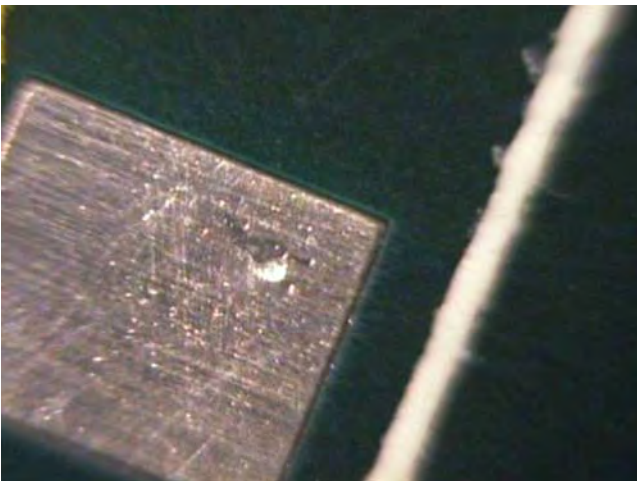


Figure 256c

Target Condition – Class 1, 2, 3

- Copper surface is planar with no indication of cap plating.

Acceptable – Class 1, 2, 3

- When cap plating of the filled via is specified on the procurement documentation, the requirements of 2.10.5, 2.10.6, 2.10.7 and the requirements of the applicable performance specification for rectangular and round surface mount pads **shall** apply.
- No plating voids exposing the resin fill area, unless covered by solder mask.
- Visually discernable protrusions (bumps) and/or depressions (dimples) that meet the integrity requirements of the applicable performance specification.

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.6 Cap Plating of Filled Holes – (Visual) (cont.)

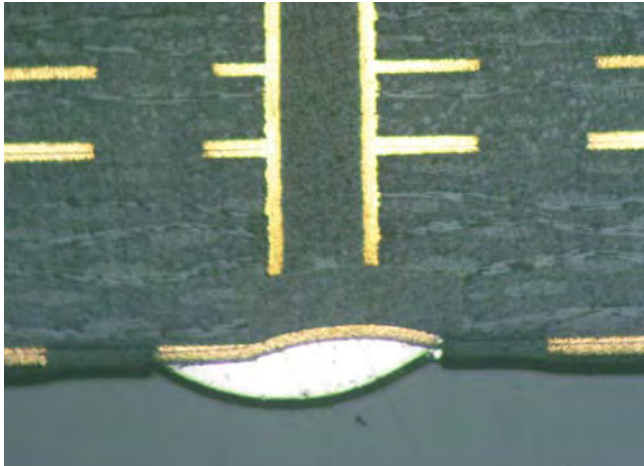


Figure 256d

Note 1: This graphic is for illustrative purposes only and does not require a microsection evaluation. See 3.3.23 for microsection evaluation requirements.

Acceptable – 1, 2, 3

- Unless otherwise specified, the back-drilled portion of the filled, overplated via is exempt from the cap plating requirement

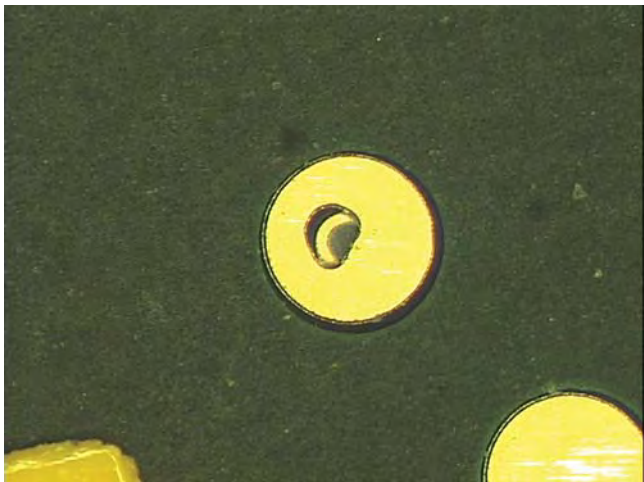


Figure 256e

Nonconforming – Class 1, 2, 3

- Observed conditions either do not meet or exceed above criteria.

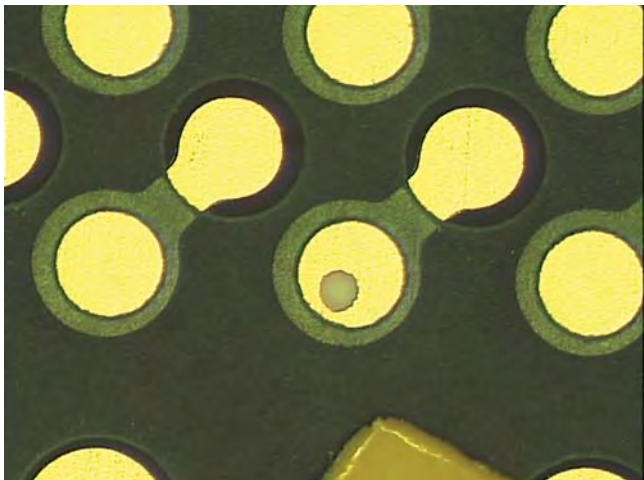


Figure 256f

2.5 HOLES – PLATED-THROUGH – GENERAL

2.5.7 Back-Drilled Holes – (Visual)

Back-Drilling A method of reducing the overall length of any plated hole by drilling out a portion of the plated hole from either side to a predetermined depth, for purposes of signal integrity or circuit isolation (see Figure 257a).

Back-drilled holes are excluded from the printed board edge spacing requirements of 2.1 in the visual assessment.

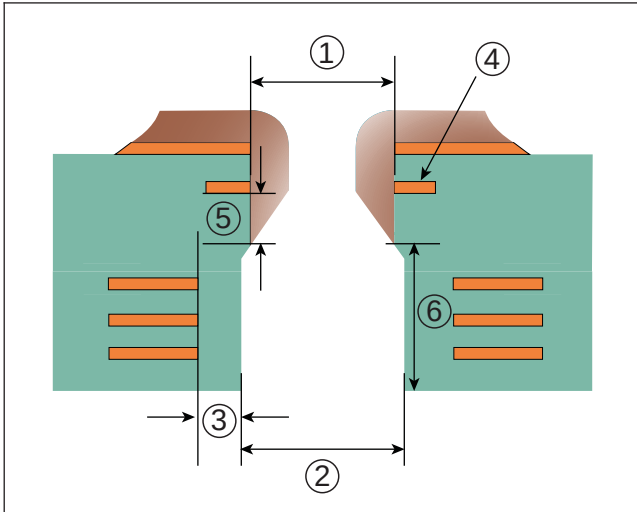


Figure 257a (Illustration Not to Scale)

Note 1: Primary drilled hole diameter.

Note 2: Back-drill hole diameter.

Note 3: Distance between nearest conductive feature and back-drill hole.

Note 4: Target Layer (e.g., Must Not Cut Layer).

Note 5: Stub length (excluding target layer copper thickness).

Note 6: Back-drill depth.

Note 7: This graphic is for illustrative purposes only and does not require a microsection evaluation. See 3.3.24 for microsection evaluation requirements.

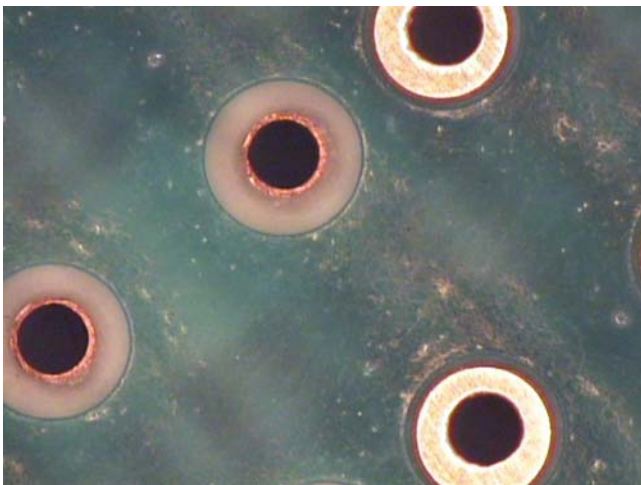


Figure 257b

Target Condition/Acceptable – Class 1, 2, 3

- No plating slivers or loose debris (conductive or non-conductive).
- No evidence of external land remnant in the barrel or on the outer surface.
- Finished hole size tolerances meet the requirements of IPC-6010 series for hole size, hole pattern accuracy and pattern feature accuracy.