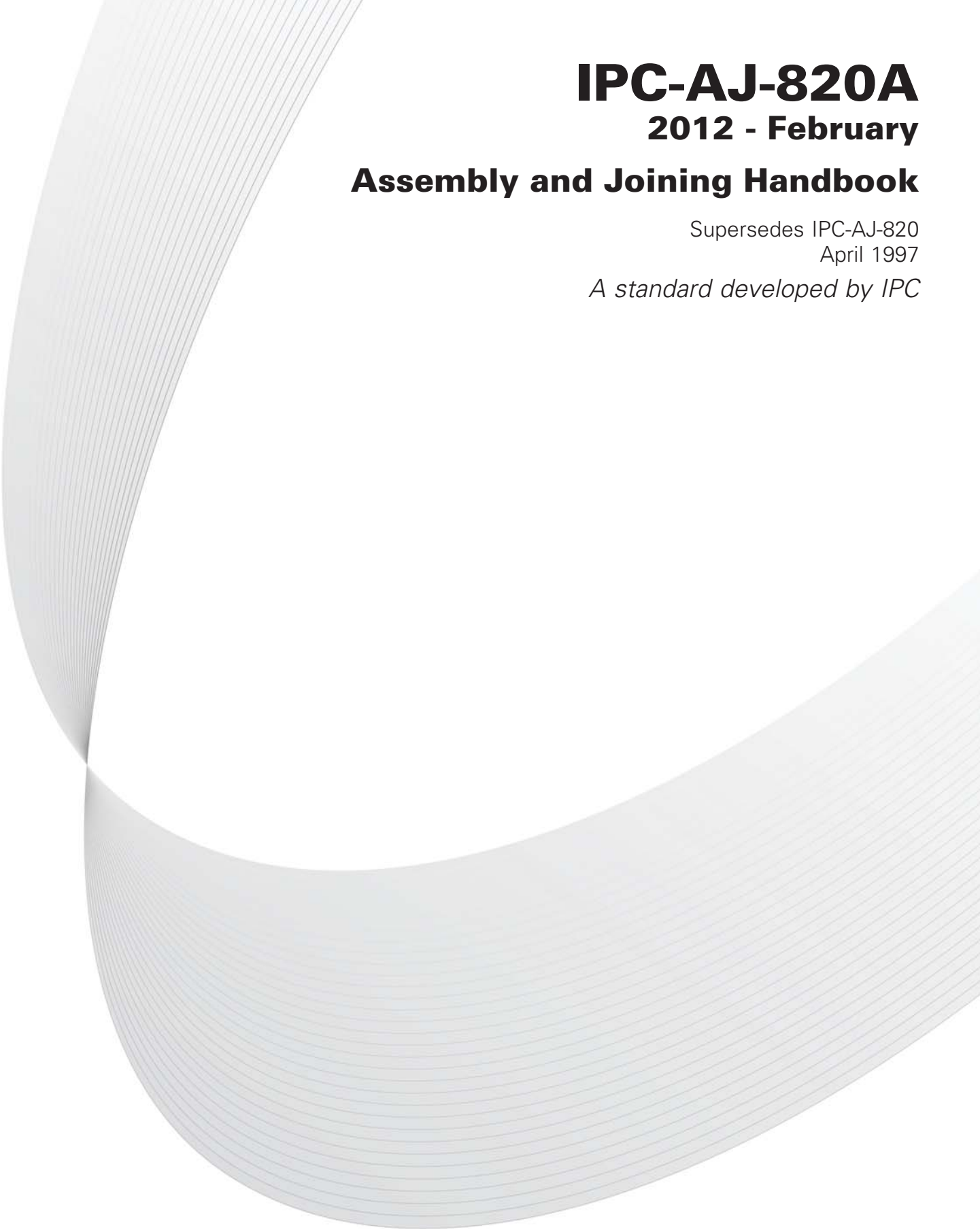




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April 1997

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Association Connecting Electronics Industries



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Assembly and Joining Handbook

Developed by the Assembly and Joining Subcommittee (7-35) of the
Product Assurance Committee (7-30) of IPC

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Users of this publication are encouraged to participate in the
development of future revisions.

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Assembly and Joining Handbook

IPC-AJ-820 OUTLINE

The purpose of this Assembly and Joining Handbook is to provide practical and useful information regarding various approaches and techniques for the interconnection of electronic components. The table of contents is an indication of the variety of data included in this document.

Chapter 1	Introduction
Chapter 2	Handling Electronic Assemblies
Chapter 3	Design Considerations
Chapter 4	Printed Boards
Chapter 5	Electronic Circuit Components
Chapter 6	Solderability
Chapter 7	Assembly and Joining Materials
Chapter 8	Component Mounting
Chapter 9	Solder Techniques and Connections
Chapter 10	Other Assembly and Joining Methods
Chapter 11	Cleaning and Cleanliness
Chapter 12	Conformal Coating (HDBK-830)
Chapter 13	Encapsulation and Potting
Chapter 14	Rework and Repair

1 SCOPE

This document provides guidelines and supporting information for manufacturing electronic assemblies. The intent is to explain the “how-to” and “why” information, and fundamentals for these processes.

Additional detailed information can be found in documents referenced within each individual section. Users are encouraged to use those referenced documents to better understand the applicable subject areas.

The words “shall,” “must,” etc., are used in various places within this handbook. However, nothing within this handbook is considered mandatory unless otherwise specified in the design or contract documentation. In event of a conflict between the content of this handbook and the requirements invoked by the design or contract documentation, the requirements of the design or contract documentation shall take precedence.

1.1 Assembly and Joining Technology Selection of appropriate assembly and joining techniques for electronic circuits should consider the requirements of the end product equipment and subassembly, including form, fit, function, cost effectiveness, performance, and marketability. Other factors include packaging density, assembly profile height, development time, development cost, circuit element factors, manufacturing costs, thermal considerations, reliability, and specific implementation details.

The assembly process steps differ according to the type of product being assembled, i.e., through-hole, surface mount, or mixed technology. They also vary according to manufacturer expertise, experience, and preference.

The selection of a particular method for mounting and terminating a component will also depend on the type of component (size, weight and shape), the equipment available for mounting and interconnecting, the connection method (e.g., soldering, welding, or crimping), the reliability and maintainability (ease of replacement) required, and of course, cost.

1.2 Through-Hole Technology The most significant advantage of through-hole mounting is compatibility with conventional mass soldering techniques, such as dip and wave soldering. One of the significant disadvantages is space. Through-hole parts usually take up a much larger footprint on the PWA than a similar surface mount component. They also require space on both sides of the board, as the leads protrude through to the opposite side.

1.3 Surface Mount Technology The most obvious benefits of surface mount technology (SMT) compared to older through-hole (THT) technology are increased circuit density and improved electrical performance. Less obvious benefits include lower process costs, higher product quality, reduced handling costs, and higher reliability.

Some SMT package types also facilitate assembly automation, rework, and repair. Because of the complexity and density of some assemblies (e.g., intermixed THT and SMT components on both sides of a printed board), proper design and process control are necessary to control process costs and reduce rework and repair.

Improved electrical performance may include higher operating speed and frequency. SMT lowers the parasitic lead and trace inductance, while improving capacitance, resistance, and other performance characteristics.

Increasing device complexity has been a primary driving factor for SMT. In order to keep component package size down, typical lead spacing was initially decreased to 1.27mm [0.050 in]. Further increases in active elements in very-large-scale integration (VLSI) required devices with more than 100 terminals and closer lead spacings of 0.64 and 0.50 mm [0.025 and 0.020 in]. Today, spacings of 0.38 and 0.25 mm [0.015 and 0.010 in] are becoming a reality. Packages with lead pitches of 0.65 millimeter or less are known as fine-pitch technology (FPT) packages. Because of the design flexibility of gate arrays and standard cells, small companies can now do their own custom integrated circuit design around these technologies without a heavy investment in personnel and equipment. The basic integrated circuit (IC) cell has already been designed for them.

As the complexity of ICs continues to drive the adoption of SMT, the printed board will also change. With more of the circuit customization going into silicon, and with the component package size decreasing, the printed board may also get smaller. However, the higher I/O demand will require multilayer designs with interconnection wiring for closely spaced devices. Both sides of the printed board will be needed to place all the components. In many cases, power dissipation per printed board will also increase.

1.4 Related Documents This section describes documents that are related to the subject matter included in this handbook. The information here is for reference only.

1.4.1 Joint Industry Standards¹ IPC-Association Connecting Electronics Industries develops standards and other publications that are designed to serve the public interest through the elimination of misunderstandings between manufacturers and purchasers, to facilitate the interchangeability and improvement of products, and to assist the buyers in selecting and obtaining the products that satisfy their needs.

IPC documents are sometimes developed unilaterally. However, when it best serves the interests of the Electronics Industry, IPC jointly develops standards and specifications with other organizations. Sometimes these documents are identified with a “J-STD” prefix. The following documents of this type are related to this handbook.

1.4.1.1 J-STD-001

Title: Requirements for Soldered Electrical and Electronic Assemblies

Department of Defense (DoD) Adoption: Yes

Abstract: The requirements of this document were written with the intention of superseding IPC-S-815 and MIL-STD-2000. This standard defines the requirements for soldering electrical and electronic assemblies. It also defines the materials, methods, and verification criteria for producing quality soldered interconnections and assemblies, including cleaning, coating, encapsulation, rework/repair, and verification.

It is not the intent of J-STD-001 to exclude any acceptable procedure for placing components, or for applying flux and solder used to make electrical connections. However, the methods used must produce solder connections conforming to the acceptability requirements in the standard.

Additional Associated documents:

1.4.1.1.1 J-STD-001 Space Addendum

Title: Space Applications Electronic Hardware Addendum to J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

Abstract: This addendum provides additional requirements over those published in IPC J-STD-001 to ensure the reliability of soldered electrical and electronic assemblies that must survive the vibration and thermal cyclic environments getting to and operating in space. When required by procurement documentation/drawings, this Addendum supplements or replaces specifically identified requirements of J-STD-001, Revision D of February 2005.

1. www.ipc.org

1.4.1.2 J-STD-002

Title: Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

Department of Defense (DoD) Adoption: Yes

Abstract: The requirements of this document were written to supersede IPC-S-805 and EIA-IS-49A. This standard prescribes recommended test methods, defect definitions, acceptance criteria, and illustrations for assessing the solderability of electronic component leads, terminations, solid wire, lugs, and tabs.

1.4.1.3 J-STD-003

Title: Solderability Tests for Printed Boards

Department of Defense (DoD) Adoption: Yes

Abstract: The requirements of this document were written to supersede IPC-S-804. This standard prescribes the recommended test methods, defect definitions, and illustrations for assessing the solderability of printed board surface conductors, attachment lands, and plated-through holes.

1.4.1.4 J-STD-004

Title: Requirements for Soldering Fluxes

Department of Defense (DoD) Adoption: Yes

Abstract: This document is one of a set of three Joint Industry Standards that also includes J-STD-005 and J-STD-006. The set of standards prescribes general requirements and test methods for soldering materials used in the Electronics Industry, and are a replacement for Mil-F-14256 and QQ-S-571. J-STD-004 covers classification and testing of soldering fluxes.

1.4.1.5 J-STD-005

Title: Requirements for Soldering Pastes

Department of Defense (DoD) Adoption: Yes

Abstract: This document is one of a set of three Joint Industry Standards for soldering materials that also includes J-STD-004 and J-STD-006. J-STD-005 prescribes general requirements for the characterization and testing of solder pastes used to make high quality interconnections. It is a quality control document and is not intended to relate directly to the material's performance in the manufacturing process.

1.4.1.6 J-STD-006

Title: Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

Department of Defense (DoD) Adoption: Yes

Abstract: This document is one of a set of three Joint Industry Standards for soldering materials that also includes J-STD-004 and J-STD-005. J-STD-006 prescribes the nomenclature, requirements, and test methods for electronic grade solder alloys, for fluxed and non-fluxed bar, ribbon, and powder solders, and for "special" electronic grade solders. This is a quality control standard and is not intended to relate directly to the material's performance in the manufacturing process.

1.4.1.7 J-STD-012

Title: Implementation of Flip Chip and Chip Scale Technology

Abstract: This document describes the implementation of flip chip and related chip scale semiconductor packaging technologies. The areas discussed include design considerations, assembly processes, technology choices, application, and reliability data. Chip scale packaging variations include flip chip, High Density Interconnect (HDI), Micro Ball Grid Array, Micro Surface Mount Technology (MSMT) and Slightly Larger than Integrated Circuit Carrier (SLICC).

J-STD-012 provides general information on implementing flip chip and chip scale technologies for creating single chip or multichip modules (MCM), IC cards, memory cards, and very dense surface mount assemblies.

1.4.1.8 J-STD-020

Title: Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

Abstract: This standard may be used to determine what classification/preconditioning level should be used for SMD package qualification. Passing the criteria in this test method is not sufficient by itself to provide assurance of long-term reliability

1.4.1.9 J-STD-033

Title: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

Abstract: The purpose of this document is to provide SMD manufacturers and users with standardized methods for handling, packing, shipping, and use of moisture/reflow sensitive SMD packages that have been classified to the levels defined in J-STD-020. These methods are provided to avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. By using these procedures, safe and damage-free reflow can be achieved, with the dry packing process, providing a minimum shelf life capability in sealed dry-bags of 12 months from the seal date.

1.4.1.10 J-STD-075

Title: Classification of Non-IC Electronic Components for Assembly Processes

Abstract: The purpose of this specification is to establish an agreed set of worst case solder process limits (SnPb and Pb-free) which can safely be used for assembling non-semiconductor electronic components on common substrates, e.g., FR4, ceramic, polyimide, etc., along with documenting unique commodity specific exceptions.

1.4.1.11 JESD22-B111

Title: Board Level Drop Test Method of Components for Handheld Electronic Products

Abstract: This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure.

1.4.1.12 JESD201

Title: Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes

Abstract: This standard was generated under the auspices of the JEDEC JC14.3 Subcommittee on Silicon Device Reliability Qualification and Monitoring and the iNEMI Tin Whisker User Group. It is intended to provide a uniform environmental acceptance testing and reporting methodology for tin whisker susceptibility of tin and tin alloy surface finishes used in the Electronics Industry.

1.4.1.13 J-STD-609

Title: Marking and Labeling of Components, PCBs and PCBA's to Identify Lead (Pb), Lead-Free (Pb-Free) and Other Attributes

Abstract: This standard applies to components and assemblies that contain Pb-free and Pb-containing solders and finishes. This standard describes the marking of components and the labeling of their shipping containers to identify their 2nd level terminal finish or material, and applies to components that are intended to be attached to boards or assemblies with solder or mechanical clamping or are press fit. This standard also applies to 2nd level terminal materials for bumped die that are used for direct board attach.

1.4.2 IPC - Association Connecting Electronics Industries Documents² The IPC develops and publishes specifications, standards, and guideline documents to help establish common terminology and promote best practices for printed boards and related products and assemblies.

1.4.2.1 IPC-DRM-18

Title: Component Identification Training and Reference Guide

2. www.ipc.org

Abstract: The Component Identification Training & Reference Guide is a valuable tool for employee training and quick reference. This comprehensive component identification resource for electronics assembly operators and inspectors contains color photographs, computer graphics, schematic symbols and detailed descriptions of more than 50 common through-hole and surface mount components used in electronics assembly today.

1.4.2.2 IPC-T-50

Title: Terms and Definitions for Interconnecting and Packaging Electronic Circuits

Department of Defense (DoD) Adoption: Yes

Abstract: This document includes definitions of common industry terms developed by the IPC Committee on Terms and Definitions. The Committee meets regularly to add new terms and definitions.

1.4.2.3 IPC-CH-65

Title: Guidelines for Cleaning on Printed Boards and Assemblies

Abstract: The purpose of this document is to collect and update all the pertinent information on printed wiring assembly (PWA) cleaning in a single, easy to revise/updated document.

1.4.2.4 IPC-FA-251

Title: Assembly Guidelines for Single-Sided and Double-Sided Flexible Printed Circuits

Abstract: This document provides information for design and manufacturing engineers on flexible printed circuit assembly techniques. These guidelines include the types of parts available, techniques and processes for their proper use, advantages, disadvantages, problems, implementation, and where to find additional information.

1.4.2.5 IPC-D-279

Title: Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

Abstract: This document establishes design concepts, guidelines, and procedures to promote “Design for Reliability” (DfR) of printed wiring assemblies (PWAs). The focus is directed toward PWAs with surface mount (SMT) components, alone or intermixed with through-hole components, mounted on one or both sides of the board.

1.4.2.6 IPC-D-355

Title: Printed Board Assembly Description in Digital Form

Abstract: This standard is used to describe the relationship between components (electronic, electro-mechanical, and mechanical) and the printed boards used as the major form of interconnection. Included in these descriptions are the physical characteristics of components and boards required as input to an automated assembly system.

The physical characteristics used in the electronic design process are described in digital form to enable data exchange and archiving between systems that support design, fabrication, assembly, and testing.

This structure provides the capability to describe all elements in their final form after completion of manufacturing. It may be used for component preparation (sequencing, lead bonding, etc.), component insertion, adhesive application, or component placement.

1.4.2.7 IPC-C-406

Title: Design and Application Guidelines for Surface Mount Connectors

Abstract: The growing popularity of surface mount technology has fostered a need for surface mount connectors to provide a common packaging approach. This document provides guidelines for the design, selection, and application of soldered surface mount connectors for all types of printed boards including rigid, rigidflex, and backplanes. It does not cover solderless interconnections, such as those that employ conductive elastomers.

1.4.2.8 IPC-D-422

Title: Design Guide for Press Fit Rigid Printed Board Backplanes

Abstract: This design guide assumes that the user possesses basic knowledge of the various types of interconnection systems, including electrical and mechanical properties.

The purpose of this document is to enlarge upon the user's analysis, and approach the design from the fabricator's and assembler's perspective with respect to design optimization. This design optimization can dramatically improve life cycle cost of the equipment. Major topics include:

- Design and Documentation
- Fabrication, Assembly and Repair
- Inspection, Testing and Shipping

1.4.2.9 IPC-DW-426

Title: Specification for Assembly of Discrete Wiring

Abstract: This specification covers the acceptance and test requirements of conformally coated and non-coated discrete wiring assemblies consisting of discrete wiring boards manufactured in accordance with IPC-DW-425 on which separately manufactured electrical and/or mechanical components are mounted.

1.4.2.10 IPC-A-610

Title: Acceptability of Electronic Assemblies

Department of Defense (DoD) Adoption: Yes

Abstract: This standard is a collection of visual quality acceptability requirements for electronic assemblies. It presents acceptance requirements for the manufacture of electrical and electronic assemblies. The criteria in this standard are not intended to define processes to accomplish assembly operations, nor are they intended to authorize repair/modification or changes to the design.

1.4.2.11 IPC-OI-645

Title: Standard for Visual Optical Inspection Aids

Abstract: This standard establishes the requirements, definitions, and certification provisions for optical inspection aids, and defines inspection grades for inspection using magnification.

1.4.2.12 IPC-TM-650

Title: Test Methods Manual

Abstract: This manual contains information on various test methods for printed boards, hybrid circuits, discrete wiring, and flat cable. These methods can be utilized by test laboratories, manufacturers, and users of these products.

This document also provides an organized reference source of test methods that can be utilized by the Technical Committees of the IPC as they develop new standards and specifications. The following test methods are referenced in this document.

- 2.3.25 Detection and Measurement of Ionizable Surface Contaminants by Resistivity of Solvent Extract
- 2.3.25.1 Ionic Cleanliness Testing of Bare PWBs
- 2.3.26 Ionizable Detection of Surface Contaminants (Dynamic Method)
- 2.3.26.1 Ionizable Detection of Surface Contaminants (Static Method)
- 2.3.27 Cleanliness Test - Residual Rosin
- 2.3.27.1 Rosin Flux Residue Analysis-HPLC Method
- 2.3.28 Ionic Analysis of Circuit Boards, Ion Chromatography Method
- 2.3.38 Surface Organic Contaminant Detection Test
- 2.3.39 Surface Organic Contaminant Identification Test (Infrared Analytical Method)
- 2.4.37.2 Evaluation of Hand Soldering Tools on Heavy Thermal Loads
- 2.6.1.1 Fungus Resistance - Encapsulation
- 2.6.3 Moisture and Insulation Resistance, Printed Boards
- 2.6.3.1 Moisture and Insulation Resistance-Polymeric Solder Masks and Encapsulation
- 2.6.7.1 Thermal Shock - Encapsulation
- 2.6.9.1 Test to Determine Sensitivity of Electronic Assemblies to Ultrasonic Energy
- 2.6.9.2 Test to Determine Sensitivity of Electronic Components to Ultrasonic Energy
- 2.6.11.1 Hydrolytic Stability - Encapsulation

1.4.2.13 IPC-CM-770

Title: Guidelines for Printed Board Component Mounting

Abstract: This document contains a review of some pertinent design criteria, impacts, and issues, covers preparation of components for assembly to printed boards, techniques of general interest for assembly (both manual and machines), and discusses considerations of, and impacts upon, subsequent soldering, cleaning, and coating processes. The information in the document consists of compiled data representing commercial and industrial applications.

1.4.2.14 IPC-SM-780

Title: Component Packaging and Interconnecting with Emphasis on Surface Mounting

Abstract: This document provides guidelines for the surface mounting of electronic parts on printed boards and for the intermixing of surface mount and through-the-board components. It includes types of materials, interconnection substrates, land pattern designs, solder-joint configurations, rework, and repair. The intent is to aid in designing a producible product by providing information on processing and on various types of substrates and joining materials. The substrate's physical and electrical characteristics and their compatibility for surface mounting are discussed.

1.4.2.15 IPC-SM-784

Title: Guidelines for Chip-on-Board Technology Implementation

Abstract: This document provides guidelines for the use of Chip-on-Board (COB) Technology including:

- Design Guidelines
- Manufacturing Information
- Assembly Guidelines
- Testing Guidelines
- Bibliographic References

1.4.2.16 IPC-SM-785

Title: Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

Abstract: This document provides guidelines for the accelerated reliability testing of surface mount solder joint attachments. Particular attention is given to evaluating and extrapolating the results of these tests towards actual use environments for electronic assemblies. The intent is to:

- Allow comparison of results from different test programs.
- Provide technical understanding of design for adequate reliability.
- Permit analytic predictions of reliability based on the use of a generic database and associated technical understanding.
- Reduce cost and avoid time-consuming testing of every design iteration.
- Establish practical alternatives to long duration tests for products that are subject to severe use environments or with low failure tolerances.

1.4.2.17 IPC-S-816

Title: SMT Process Guidelines and Checklist

Abstract: This document provides guidelines and troubleshooting for surface mount attachment of components. Each section includes a list of common problems observed during a specific part of the surface mount assembly process. The list of observed symptoms is matched by a description of possible causes and suggestions for corrective action. These suggestions may be related to the equipment, materials, or design so some may not be applicable to the shop floor.

1.4.2.18 IPC-SM-817

Title: General Requirements for Dielectric Surface Mounting Adhesives

Abstract: This document defines dielectric surface mount adhesives through the specification of test methods and inspection criteria. Particular attention is given to adhesives that are applied by pin transfer, syringe, or screening/stenciling. Curing methods covered include ultraviolet (UV) light, visible light, heat, or ambient conditions.

1.4.2.19 IPC-CC-830

Title: Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

Abstract: This standard establishes qualification and conformance requirements for conformal coatings. It has been designed to provide maximum confidence in the materials with minimum test redundancy and covers:

- The qualification and qualification retention of the conformal coating material.
- The quality conformance of conformal coating material properties.

1.4.2.20 IPC-HDBK-830

Title: Guidelines for Design, Selection and Application of Conformal Coatings

Abstract: The purpose of this handbook is to assist the individuals who either make choices regarding conformal coating or who work in coating operations.

1.4.2.21 IPC-SM-839

Title: Pre and Post Solder Mask Application Cleaning Guidelines

Abstract: This document covers all aspects of cleaning processes associated with the application of a permanent polymer coating (solder mask) to printed boards. This includes maintaining cleanliness of coated boards during the storage and handling prior to component assembly and during the coating application and cure processes. It also covers cleanliness that is consistent with the end-product application.

1.4.2.22 IPC-SM-840

Title: Qualification and Performance of Permanent Polymer Solder Mask

Department of Defense (DoD) Adoption: Yes

Abstract: This standard is intended to provide the user with the maximum information about and confidence in the solder mask material under evaluation with the minimum of test redundancy. It covers:

- The evaluation and conformance of permanent polymer coatings (solder masks) and material properties.
- The qualification of the solder mask with the standard IPC-B-25 test board.
- The qualification assessment of the solder mask/production board system.
- The quality conformance of the solder mask/production board system.

1.4.2.23 IPC-1601

Title: Printed Board Handling and Storage Guidelines

Abstract: This document provides suggestions for proper handling, packaging materials and methods, environmental conditions, and storage for printed boards. These guidelines are intended to protect printed boards from contamination, physical damage, solderability degradation, electrostatic discharge (ESD) (when necessary), and moisture uptake.

1.4.2.24 IPC-2221

Title: Generic Standard on Printed Board Design

Department of Defense (DoD) Adoption: Yes

Abstract: This standard covers generic requirements for printed board design. All aspects and details of the design requirements are addressed, to the extent that they can be applied to the broad spectrum of designs, including organic or inorganic board materials in combination with inorganic metal, glass, ceramic, etc. The decision on the choice of product type should be made as early as possible. Once a component mounting and interconnecting technology has been selected, the user should obtain the sectional document (described below) that provides the specific focus on the chosen technology.

1.4.2.25 IPC-2222

Title: Sectional Design Standard for Rigid Organic Printed Boards

Department of Defense (DoD) Adoption: Yes

Abstract: This standard establishes the specific requirements for the design of rigid organic printed boards and other forms of component mounting and interconnecting structures. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials. The interconnections may be single, double, or multilayered.

1.4.2.26 IPC-2223

Title: Sectional Design Standard for Flexible Printed Boards

Department of Defense (DoD) Adoption: Yes

Abstract: This standard establishes the specific requirements for the design of flexible printed circuit applications, including forms of component mounting and interconnecting structures. The flexible materials used in these structures include insulating films (reinforced or non-reinforced dielectric) in combination with metallic layers. These interconnecting boards may contain single, double, multilayer, or multiple conductive layers and can be composed wholly of flex or a combination of flex and rigid.

1.4.2.27 IPC-6012

Title: Qualification and Performance Specification for Rigid Printed Boards

Abstract: This specification establishes and defines the qualification and performance requirements for the fabrication of rigid printed boards.

1.4.2.28 IPC-7093

Title: Design and Assembly Process Implementation for Bottom Termination Components

Abstract: This document describes the design and assembly challenges for implementing bottom termination surface mount components (BTCs), whose external connections consist of metallized terminations that are an integral part of the component body. These include components designated in industry as DFN (Dual Flat No-lead), QFN (Quad Flat No-Lead package), LGA (Land Grid Array), SON (Small Outline No-Lead - leads on two sides), PQFN (Plastic Quad Flat No-Lead), MLFP (Micro Leadframe Plastic Package), and MLP (Micro Leadframe Package) which utilize surface-to-surface interconnections without solder balls. The focus is on critical design, assembly, inspection, repair, and reliability issues associated with BTCs.

1.4.2.29 IPC-7094

Title: Design and Assembly Process Implementation For Flip Chip and Die Size Components

Abstract: This document describes the design and assembly challenges for implementing flip chip technology in a direct chip attach (DCA) assembly. The effect of bare die or die size components in a flip chip format has an impact on current component characteristics and dictates the appropriate assembly methodology. The focus is on design, assembly methodology, critical inspection, repair, and reliability issues associated with flip chip and die size package technologies (including wafer level BGA).

1.4.2.30 IPC-7095

Title: Design and Assembly Process Implementation for BGAs

Abstract: This document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology. The effect of BGA and FBGA on current technology and component types are addressed, as is the move to lead-free assembly processes. The focus is on critical inspection, repair, and reliability issues associated with BGAs.

1.4.2.31 IPC-7711/7721

Title: Rework of Electronic Assemblies/Repair and Modification of Printed Boards and Electronic Assemblies

Abstract: This document prescribes the procedural requirements, tools, materials and methods to be used in the modification, rework, repair, overhaul or restoration of electronic products. Although this document is based in large part on the Product Class definitions used in IPC documents such as J-STD-001 or IPC-A-610, this document should be considered applicable to any type of electronic equipment.

IPC has identified the most common equipment and process in order to make a specific repair or rework. It is possible that alternate equipment and processes can be used to make the same repair. If alternate equipment is used, it is up to the user to determine that the resultant assembly is good and undamaged.

1.4.2.32 IPC-9191

Title: General Guidelines for Implementation of Statistical Process Control (SPC)

Abstract: This document describes the general requirements for the implementation of Statistical Process Control (SPC). It is intended for use by individuals in electronics and other industries that are involved in the planning, implementation, and evaluation of an SPC system. It outlines SPC philosophy and different implementation strategies, tools, and techniques that may be applied depending on end-product requirements.

1.4.3 United States Government Documents³ The United States Government develops design, fabrication, assembly and testing standards and specifications for a wide range of electrical and electronic products and materials. These consist basically of Department of Defense (Military) and Federal documents.

Military documents are identified by a “MIL-” or “DOD-” prefix. The “DOD” prefix usually indicates that the document primarily uses metric units. Federal documents are identified by a multiple letter prefix, e.g., “QQ-.”

If the document is a specification, the prefix is followed by a letter that is representative of the subject of the document, e.g., “C-” for a “Connector” specification. The prefix is followed by “STD-” if the document is a standard.

1.4.3.1 MIL-STD-202

Title: Test Method Standard Electronic and Electrical Component Parts

Abstract: This standard establishes uniform methods for testing electronic and electrical component parts and assemblies, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military operations, and physical and electrical tests. For the purpose of this standard, the term “component parts” includes such items as capacitors, resistors, switches, relays, transformers, and jacks.

This standard is intended to apply only to small parts, such as transformers and inductors, weighing up to 300 pounds, or having a root mean square test voltage up to 50,000 volts, unless otherwise specifically invoked.

1.4.3.2 AMS-QQ-N-290

Title: Nickel Plating (Electrodeposited)

Abstract: This specification covers the requirements for electrodeposited nickel plating on steel, copper and copper alloys, and zinc and zinc alloys, but usage is not limited to such applications. It covers 2 classes:

Class 1 - Corrosion protective plating

Class 2 - Engineering plating

The Class 1 plating can be further classified into plating thicknesses that range from 0.0002 inches to 0.0016 inches.

1.4.3.3 MIL-HDBK-454

Title: General Guidelines for Electronic Equipment

Abstract: This handbook is the technical baseline for the design and construction of electronic equipment for the Department of Defense. It captures in one document, under suitable subject headings, fundamental design guidelines for multiple general electronic specifications.

The opportunity to focus on a single document, afforded to contractors, results in substantial savings to the Government. This handbook was prepared by and is regularly updated through the cooperative efforts of Government and industry.

1.4.3.4 MIL-A-1130

Title: Connections, Electrical, Solderless, Wrapped

3. <https://assist.daps.dla.mil/quicksearch/>

Abstract: This standard establishes the requirements to produce mechanically and electrically stable, solderless wrapped, electrical connections made with single, solid, round wire and appropriately designed wrap posts (terminals).

1.4.3.5 MIL-STD-1686

Title: Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment

Abstract: This standard covers the requirements for an Electrostatic Discharge (ESD) control program for electrical and electronic parts, assemblies, and equipment containing these parts, excluding electrically-initiated explosive devices. “Parts,” as used herein, applies to electrical and electronic parts. “Assemblies,” as used in the document, applies to subassemblies and all higher assemblies up to but not including the equipment level.

This standard covers ESD sensitive (ESDS) items, design criteria, protected work areas, handling procedures, training, marking of documentation and hardware, intra-plant protective covering, packaging for delivery, installations, quality assurance provisions, audits and reviews.

1.4.3.6 MIL-A-28870

Title: Assemblies, Electrical Backplane, Printed Wiring, General Specification for

Abstract: This specification covers the general requirements for printed wiring electrical backplane assemblies consisting of rigid printed wiring boards on which separately manufactured component parts have been added.

1.4.4 American Society of Mechanical Engineers⁴ ASME codes and standards, publications, conferences, continuing education and professional development programs provide a foundation for advancing technical knowledge.

1.4.4.1 ASME Y14.5-2009

Title: Dimensioning and Tolerance Standard

Department of Defense (DoD) Adoption: Yes

Abstract: This standard covers dimensioning, tolerancing, and related practices for use on engineering drawings and in related documents. It also establishes uniform practices for stating and interpreting these requirements.

1.4.5 ASTM International⁵ ASTM International, formerly known as the American Society for Testing and Materials (ASTM), is a globally recognized leader in the development and delivery of international voluntary consensus standards. Today, some 12,000 ASTM standards are used around the world to improve product quality, enhance safety, facilitate market access and trade, and build consumer confidence.

The following ASTMs are referenced in this document:

1875-00	D-1458
B193-02	D-2196
B-488	D-2214
B-579	D-2240
C-408	D-2556
D-149	D-3359
D-150	D-3418
D-257	D-3482
D-570	D-3833
D-571	D-4065
D-595	E92-82(2003)e2
D-635	E-96
D-638	E-595
D-709	E794-06
D-751	E831-06
D-1002	F1249

4. www.asme.org

5. www.astm.org

1.4.6 SAE International⁶ SAE International is a global association of more than 128,000 engineers and related technical experts in the aerospace, automotive and commercial-vehicle industries. SAE International's core competencies are life-long learning and voluntary consensus standards development. SAE International's charitable arm is the SAE Foundation, which supports many programs, including A World in Motion and the Collegiate Design Series.

1.4.6.1 SAE AS5553

Title: Counterfeit Electronic Parts; Avoidance, Detection, Mitigation, and Disposition

Abstract: This document is intended for use in aviation, space, defense, and other high performance/reliability electronic equipment applications. This standard is recommended for use by all contracting organizations that procure electronic parts, whether such parts are procured directly or integrated into electronic assemblies or equipment. The requirements of this standard are generic and intended to be applied/flowed down to all organizations that procure electronic parts, regardless of type, size, and product provided.

1.4.6.2 SAE AS6174

Title: Counterfeit Materiel; Detection, Mitigation, and Disposition

Abstract: This SAE Standard standardizes practices to: a) maximize availability of authentic materiel (made from the proper materials using the proper processes with required testing), b) procure materiel from reliable sources, c) assure authenticity and conformance of procured materiel, d) control materiel identified as counterfeit and e) report counterfeit materiel to other potential users and government investigative authorities.

1.4.7 Federal Aviation Regulations (FARs)⁷

1.4.7.1 FAR §25.853 and Appendix F

Title: Flammability Requirements for Seat Cushions

1.4.8 Underwriters Laboratories⁸

1.4.8.1 UL94 Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

1.4.8.2 UL746C Polymeric Materials - Use in Electrical Equipment Evaluations

1.4.9 IEC Standards⁹

1.4.9.1 IEC 60664

Title: Insulation coordination for equipment within low-voltage systems

Abstract: This standard applies to assemblies protected against pollution by the use of coating, potting or molding, thus allowing a reduction of clearance and creepage distances as described in Part 1 or Part 5.

1.4.9.2 IEC 61086

Title: Coatings for loaded Printed Wire boards (Conformal Coatings)

Abstract: Gives the definitions, classification and general requirements for electrical insulating materials suitable for application as coatings for loaded printed wire boards (conformal coatings).

1.4.10 Independent Distributors of Electronics Association (IDEA)¹⁰

1.4.10.1 IDEA-QMS-9090

Title: Quality Management System

6. www.sae.org
7. www.faa.gov
8. www.ul.com
9. www.iec.ch
10. www.idofea.org

Abstract: This document layers on top of ISO 9001, AS9120 and ANSI/ESD S20.20 certification, with specific components talking about supplier selection, inventory posting, customer provision and the inspection protocol.

1.4.11 Electrostatic Discharge Association¹¹ ESD Association standards and specifications provide the guidance companies need to get their ESD Control Programs off and running.

1.4.11.1 ANSI/ESD S20.20

Title: Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)

Abstract: This standard provides administrative and technical requirements for establishing, implementing, and maintaining an ESD Control Program to protect electrical or electronic parts, assemblies, and equipment susceptible to ESD damage from Human Body Model (HBM) discharges greater than or equal to 100 volts.

2 HANDLING ELECTRONIC ASSEMBLIES

It is important that electronic assemblies are properly handled during all operations from incoming inspection of component parts to final delivery of product.

Proper handling is required to prevent damage due to:

1. Electrostatic discharge
2. High temperatures experienced during reflow
3. To non-hermetically sealed components that are not maintained in a moisture free environment or otherwise baked prior to reflow soldering.

Improper handling can also introduce contamination that may prevent formation of acceptable solder connections. This section addresses the more common issues pertaining to handling of electronic assemblies.

The following topics are addressed in this section of the handbook:

2.1 Definitions

2.1.1 Electrostatic Discharge (ESD) Electrostatic Discharge (ESD) is the rapid discharge of electrical energy that was created from static sources.

When the electrical energy is allowed to come in contact with or even close to a sensitive component it can cause damage to the component.

2.1.2 Electrostatic Discharge Sensitive Components (ESDS) Electrostatic Discharge Sensitive (ESDS) components are those components that are affected by high energy surges. The relative sensitivity of a component to ESD is dependent upon its construction and materials. As components become smaller and operate faster, the sensitivity increases.

2.1.3 Electrical Overstress (EOS) Electrical Overstress (EOS) is the internal result of an unwanted application of electrical energy that results in damaged components. This damage can be from many different sources, such as electrically powered process equipment or ESD occurring during handling or processing.

2.2 Handling of ESDS Items (Components and/or Assemblies) When components or boards are removed from their protective wrappings, handle them with great care. Touch only the edges away from any edge connector tabs. Where a firm grip on the board is required due to any mechanical assembly procedure, gloves should be worn. Any gloves used should meet EOS/ESD requirements. These principles are especially critical when no-clean processes are employed.

ESDS components can fail to operate or change in value as a result of improper handling or processing. These failures can be immediate or latent. The result of immediate failure can be additional testing and rework or scrap. However the consequences of latent failure are the most serious. Even though the product may have passed inspection and functional test, it may fail after it has been delivered to the customer.

11. www.esda.org

Even if no ESDS markings are on an assembly, it still should be handled as if it were an ESDS assembly. Normally, ESDS components and electronic assemblies are identified by suitable EOS/ESD labels or marking. Some components may be marked with one or more triangles to designate the level of sensitivity to EOS. Many sensitive assemblies will also be marked on the assembly itself.

To prevent ESD and EOS damage to sensitive components all handling, unpacking, assembly and testing is performed at a static controlled work station. The manufacturer should implement and maintain an ESD Control Program to a recognized methodology such as ANSI/ESD S20.20. (This document is also invoked in J-STD-001.)

It's important to build protection for ESDS components into circuit designs and packaging. However, in the manufacturing and assembly areas, we often work with unprotected electronic assemblies that are attached to the ESDS components. The following paragraphs are dedicated to safe handling of these unprotected electronic assemblies.

2.2.1 Electrical Overstress (EOS) Damage Prevention Electrical components can be damaged by unwanted electrical energy from many different sources. This unwanted electrical energy can be the result of ESD potentials or the result of electrical spikes caused by the tools we work with, such as soldering irons, soldering extractors, testing instruments, or other electrically operated process equipment. Some devices are more sensitive than others. The degree of sensitivity is a function of the design of the device. Generally speaking higher speed and smaller devices are more susceptible than their slower, larger predecessors. The purpose or family of the device also plays an important part in component sensitivity. This is because the design of the component can allow it to react to smaller electrical sources or wider frequency ranges. With today's products in mind, we can see that EOS is a more serious problem than it was even a few years ago. It will be even more critical in the future.

When considering the susceptibility of the product we should keep in mind the susceptibility of the most sensitive component in the assembly. Applied unwanted electrical energy can be processed or conducted just as an applied signal would be during circuit performance.

Before handling or processing sensitive components, tools and equipment should be tested to ensure that they do not generate damaging energy including spike voltages. Current research indicates that voltages and spikes less than 0.5 volts are acceptable. However, an increasing number of extremely sensitive components require that soldering irons, solder extractors, test instruments, and other equipment not generate spikes greater than 0.3 volts.

Periodic testing may be warranted to preclude damage as equipment performance may degrade with use over time (See ANSI/ESD S20.20). Maintenance programs should be established for process equipment to ensure the continued ability to not cause EOS damage. EOS damage is certainly similar in nature to ESD damage, since damage is the result of undesirable electrical energy.

2.2.2 Electrostatic Discharge (ESD) Damage Prevention The best ESD damage prevention is a combination of preventing static charges and eliminating static charges if they do occur. All ESD protection techniques and products address one or both of the two issues.

ESD damage is the result of electrical energy that was generated from static sources either being applied or in close proximity to ESDS devices. Static sources are all around us. The degree of static generated is relative to the characteristics of the source. To generate energy relative motion is required. This could be contacting, separation, or rubbing of the material.

Most of the serious offenders are insulators since they concentrate energy where it was generated or applied rather than allowing it to spread across the surface of the material.

Common materials such as plastic bags or Styrofoam containers are serious static generators and should not be allowed in processing areas especially static safe areas. Peeling adhesive tape from a roll can generate 20,000 volts. Even compressed air nozzles which move air over insulating surfaces generate charges.

Table 2-1 identifies typical static charge sources.

Destructive static charges are often induced on nearby conductors, such as human skin, and discharged into conductors. This can happen when a printed board assembly is touched by a person having a static charge potential. The electronic assembly can be damaged as the discharge passes through the conductive pattern to a static sensitive component. Static discharges may be too low to be felt by humans (less than 3500 volts), and still damage ESDS components. Typical static voltage generation is included in Table 2-2.

Table 2-1 Typical Static Charge Sources

Work surfaces	Waxed, painted or varnished surfaces; untreated vinyl and plastics; glass
Floors	Sealed concrete; waxed or finished wood; floor tile and carpeting
Clothes and personnel	Non-ESD smocks; synthetic materials; non-ESD shoes; hair
Chairs	Finished wood; vinyl fiberglass; non-conductive wheels
Packaging and handling materials	Plastic bags, wraps, envelopes; bubble-wrap, foam; Styrofoam; non-ESD totes, trays, boxes, parts bins
Assembly tools and materials	Pressure sprays; compressed air; synthetic brushes; heat guns, blowers; copiers, printers

Table 2-2 Typical Static Voltage Generation

Source	10-20% Humidity	65-90% Humidity
Walking on carpet	35,000 volts	1,500 volts
Walking on vinyl flooring	12,000 volts	250 volts
Worker at a bench	6,000 volts	100 volts
Vinyl envelopes (Work Instructions)	7,000 volts	600 volts
Plastic bag picked up from the bench	20,000 volts	1,200 volts
Work chair with foam pad	18,000 volts	1,500 volts

2.3 Physical Handling Care should be taken during all operations (e.g., manufacturing, inspection, testing) to ensure product integrity at all times. Table 2-3 provides general guidance. Improper handling can readily damage components and assemblies (e.g., cracked, chipped, or broken components and connectors, bent or broken terminals, badly scratched board surfaces, and conductor lands). Physical damage of this type can ruin the entire assembly or attached components.

Table 2-3 General Rules for Handling Electronic Assemblies

1	Keep work stations clean and neat. There should not be any eating, drinking, or use of tobacco products in the work area.
2	Minimize the handling of electronic assemblies and components to prevent damage.
3	When gloves are used, they should be changed as frequently as necessary to prevent contamination from dirty gloves.
4	Solderable surfaces should not be handled with bare hands or fingers. Body oils and salts reduce solderability, promote corrosion and dendritic growth. They can also cause poor adhesion of subsequent coatings or encapsulates.
5	Hand creams or lotions containing silicone should be avoided since they can cause solderability and conformal coating adhesion problems.
6	Never stack electronic assemblies on each other or physical damage may occur. Special racks should be provided in assembly areas for temporary storage.
7	Always assume the items are ESDS even if they are not marked.
8	Personnel should be trained and follow appropriate ESD practices and procedures.
9	Never transport ESDS devices unless proper packaging is applied.

2.3.1 Handling after Soldering After soldering and cleaning operations, the handling of electronic assemblies still requires great care. Finger prints are extremely hard to remove and will often show up in conformally coated boards after humidity or environmental testing. Gloves or other protective handling devices should be used to prevent such contamination. Use mechanical racking or baskets with full ESD protection when handling during cleaning operations.

2.4 Contamination Contamination by handling with bare hands or fingers without some form of protection causes soldering and coating problems; body salts and oils, and unauthorized hand creams are typical contaminants. Body oils and acids reduce solderability and promote corrosion and dendritic growth. They can also cause poor adhesion of subsequent coatings or encapsulates. Normal cleaning procedures will not always remove such contaminants. Lotion formulated specifically for use in solder assembly areas is available. The best solution is to prevent contamination.

2.5 Processing Moisture Sensitive Components The acronym MSD stands for moisture sensitive devices. These devices include everything from the bare PCB to the components placed on them.

Some PCB laminates and many plastic bodied components absorb moisture. This absorption of moisture can create defects during the solder reflow process. In the reflow process, when heat is applied to the board and components, pressure from the entrapped moisture builds up. This pressure can cause damage to the bare PCB in the form of delamination. For parts that are sealed, it can cause delamination to the packaging materials of the part or delamination of the lead frame from the

internal die substrate. It can also cause internal cracks that do not extend to the outside of the package, bond damage, wire necking, bond lifting, die lifting, thin film cracking, and/or cratering beneath the bonds.

To prevent damage from moisture exposure bare PCBs should not be left to sit in the open ambient air for an extended amount of time. They should be placed in a nitrogen environment/dry cabinet or used within a limited period of time after being removed from a vacuum bag. If the level of moisture is unknown, bare PCB cards should be slowly baked to remove any moisture from them. Polyimide laminate boards are particularly susceptible to moisture absorption. For more recommendations on baking of substrates refer to IPC-1601 - Printed Board Handling and Storage Guidelines.

Plastic components are in the same situation. J-STD-020 discusses the Moisture/Reflow sensitivity classification for Non-hermetic solid state devices and the process of baking. J-STD-033 discusses the handling, packing, and shipping of moisture sensitive SMD parts. Moisture sensitive components (as classified by IPC/JEDEC J-STD-020 or other documented classification procedure) should be handled in a manner consistent with IPC/JEDEC J-STD-033 or other documented procedure to prevent this component damage.

Certain new technology components such as “flip-chip” field programmable gate arrays (FPGA) with Ball Grid Array (BGA) terminations may have been manufactured with built-in vents. The purpose of these vents is to allow for escape of gasses or moisture during the FPGA manufacturing process. However, these vents can also allow the entry of cleaning solvents and/or de-ionized water during the post reflow soldering process.

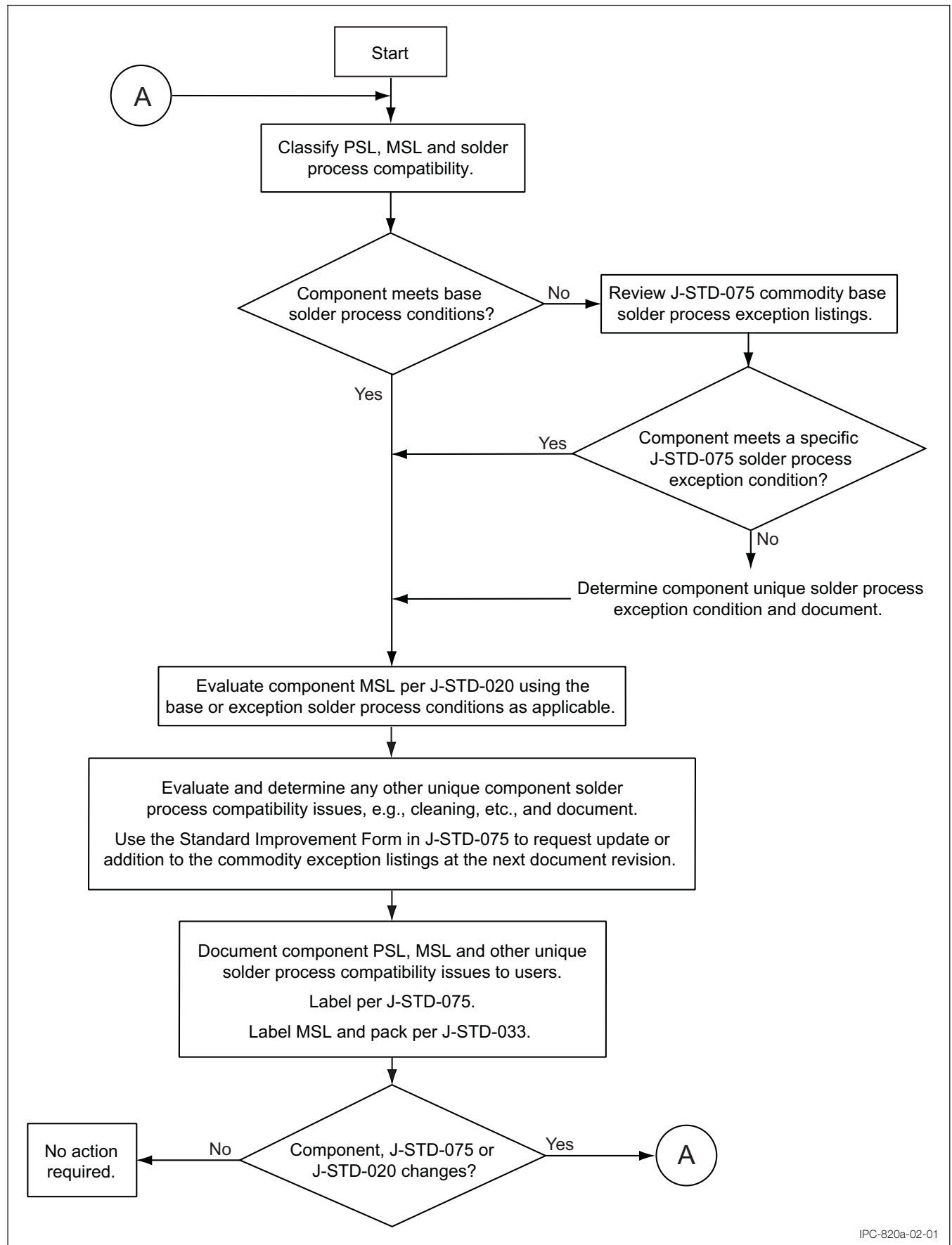
Lessons learned have shown that the entrapped cleaning solvents and/or DI water have resulted in corrosion of components within the FPGA (e.g., by-pass capacitor). This corrosion has caused open or short circuits of the by-pass capacitor and depending on the failure mode, it may cause operational failure of the FPGA.

The assembly manufacturer should take appropriate precautions for any “vented” component to ensure the cleaning process does not cause damage to the component.

2.6 Classification of Non-IC Electronic Components for Assembly Processes (ECA/IPC/JEDEC J-STD-075) Paragraph 2.5 above addressed process controls for dealing with moisture sensitive semiconductors. However, there are other types of components such as, but not limited to, capacitors that can be damaged when subjected to the higher temperatures that occur during soldering processes. The J-STD-075 document outlines a process to classify and label a non-semiconductor component's Process Sensitivity Level (PSL) and Moisture Sensitivity Level (MSL) consistent with the semiconductor industry's classification levels (See 2.5). The specification does not establish re-work conditions.

The purpose of J-STD-075 is to establish an agreed set of worst case solder process limits (SnPb and Pb-free) which can safely be used for assembling non-semiconductor electronic components on common substrates (e.g., FR4, ceramic, polyimide, etc.) along with documenting unique community specific exceptions. The document process conditions are used to evaluate a non-semiconductor component's PSL and MSL. It is important for all users of J-STD-075 to be highly familiar with the document's information and processes to insure optimal product quality and reliability.

Figure 2-1 describes the J-STD-075 process for classifying non-semiconductor devices.



IPC-820a-02-01

Figure 2-1 J-STD-075 Process Flow Diagram

Table 2-4 describes the J-STD-075 Wave Solder PSL Classification.

Table 2-4 Wave Solder PSL Classification

PSL Classification	Is the component process sensitive?	Classification Temp (T _c)
W0	No	–
W1	Yes ¹	275 °C (User maximum and Supplier Minimum)
W2	Yes ¹	270 °C
W3	Yes ¹	265 °C
W4	Yes ¹	260 °C
W5	Yes ¹	255 °C
W6	Yes ¹	250 °C
W7	Yes ¹	245 °C
W8	Yes ¹	240 °C
W9	Yes ^{1,2}	–

Note 1: See Table 5-3 (J-STD-075) if a 3rd PSL character is specified.

Note 2: The component has been determined to be process sensitive but this standard does not specify the process sensitivity exceptions. The Supplier should be contacted for recommended solder process conditions.

Table 2-5 describes the J-STD-075 Reflow Solder PSL Classification.

Table 2-5 Reflow Solder PSL Classification

PSL Classification	Is the component process sensitive?	Classification Temp (T _c)
R0	No	–
R1	Yes ¹	N/A
R2	Yes ¹	N/A
R3	Yes ¹	N/A
R4	Yes ¹	260 °C (User maximum and Supplier Minimum)
R5	Yes ¹	255 °C
R6	Yes ¹	250 °C
R7	Yes ¹	245 °C
R8	Yes ¹	240 °C
R9	Yes ^{1,2}	–

Note 1: See Table 5-3 (J-STD-075) if a 3rd PSL character is specified.

Note 2: The component has been determined to be process sensitive but this standard does not specify the process sensitivity exceptions. The Supplier should be contacted for recommended solder process conditions.

Table 2-6 defines the limitations indicated by the optional PSL 3rd character. There are also several other process limitations that are important to certain types of components such as preheat limitation, thermal spike limitation, time in wave limitation, ramp down rate limitation, etc. These are described using the 3rd character of the PSL description as noted in Table 2-6.

The standard also includes various tables that describe the recommended process parameters for soldering specific types of non-semiconductor components.

Table 2-6 PSL 3rd Character

PSL 3rd Character	Definition
(Blank)	Component has no additional process limitations beyond the Classification Temperatures listed in Tables 5-1 or 5-2.
A	Component has a Thermal Spike limitation.
C	Component has a Preheat limitation.
E	Component has a Time in Wave limitation.
F	Component has a Time (t_L) Above 217 °C liquidus temperature (TL) limitation.
G	Component has a Time Within 5 °C of T_c limitation.
H	Component has a Ramp Down Rate limitation.
J	Component has a Number of Passes / Reflows limitation.
K	Component has a Flux limitation.
M	Component has a Cleaning limitation.
N	Component has limitations: C; F; G and J.
P	Component has limitations: C; F; G and H.
R	Component has limitations C; F and G.
Y	Component has additional limitations but the combination has not been assigned a code. Details of these unique limitations will need to be obtained from the Supplier.

3 DESIGN CONSIDERATIONS

This Section of the Assembly and Joining Handbook provides general assembly and joining information that pertains to the design of printed circuit assemblies (PCA).

3.1 Background and Theory In most of today's companies there is no coordination in the advancement of technology throughout the different disciplines and departments. Even the most sophisticated automated soldering system available cannot cope with PCAs that have been designed without an input from a manufacturing engineer on how to best utilize the system.

Design of an efficient and integrated design team will give all disciplines the visibility needed to best utilize the equipment and talents available within a company. A typical team will involve the Project Manager, Design Engineering, Components Engineering, Process Engineering, Reliability, Manufacturing Engineering, Tooling Design, Quality, and Material.

3.2 Basic Considerations The mounting, attachment of components, and the assembly materials (e.g., adhesives, fluxes, solder alloys) play important roles in the design of a PCA. These factors also affect component density and conductor routing which further impact assembly, solder joint integrity, reparability, and testing. Therefore, it is important that the design reflect appropriate tradeoffs that recognize these and other manufacturing considerations.

The variety of components available and the complexity of the components demand that proper component layout and placement procedures are followed to ensure economical designs for PCA production.

Parts to be mounted should meet the storage and operating conditions specified for the equipment. Parts should also maintain their integrity after having been subjected to the rigors of assembly processing, forming, placement, insertion, heating, cooling, and cleaning.

As a minimum, component mounting and attachment should be based on the guidelines presented in IPC-CM-770, IPC-222x series of Design Standards and J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies.

3.2.1 End-Product Usage The success or failure of a board design depends on many interrelated considerations. As a minimum, the impact of design on the following parameters should be considered:

- Equipment environmental conditions, such as ambient temperature, heat generated by the components, and ventilation.
- Maintenance philosophy during the service life of the equipment, especially with respect to component placement that affects component accessibility.
- Spacing between boards that might limit lead protrusions and affect the placement of brackets and hardware.

- d. Testing/fault location requirements that might affect component placement, conductor routing, connector contact allocations, etc.
- e. If an assembly is designated as repairable, consideration should be given to component/circuit density and the selection of board/conformal coating materials. In general, rework and repair criteria should be in accordance with the guidelines of IPC-7711/7721.

3.2.2 Performance and Reliability A circuit design is measured by three factors. The first of these three factors is the ability of the circuit to perform the functions required of it. While a great deal of evaluation can be done at the circuit level, the ability to meet system and operational specifications is the true proof of performance acceptability. Second is the ability of the circuit to perform without interruption for the operational life of the system. The circuit reliability is measured at the system level as Mean-Time-Between-Failures (MTBF).

Third is producibility, which is impossible to assess independent of the other two factors. Producibility is too often given a low priority, resulting in a system which is difficult or expensive to produce. Specific manufacturing processes may further complicate the problem of designing a producible system.

System reliability is critical. The system should be designed to meet the end item requirements, including life cycle, environment (e.g., shock, vibration, temperature) and function. The most crucial reliability problems are plated through hole (PTH) cracking and solder joint fatigue. Both failures can be caused by the cyclic temperature strains, induced warpage of the printed board/package, and interconnecting (P&I) structure and the attached components. For components with leads, the cyclic strains are accommodated to some degree by the compliancy for the component leads so solder joint reliability is normally a less important issue.

Leadless components, on the other hand, are fully subjected to these cyclic strains and the reliability of their solder joints should be carefully considered in conjunction with the other design requirements. Solder joint reliability is complicated. While the effects of some parameters are fairly well modeled, other influences are poorly understood and so solder joint reliability remains difficult to predict.

3.2.3 Designing for Producibility Risk management and obsolescence management of materials are areas that should also be implemented during the design process. These can be managed using a value engineering and manufacturing affordability approach that ensures the producibility and maintenance philosophy during the service life of the equipment.

Developmental and operational testing needs should also be identified early in the design activity. The earlier these test processes are applied, the larger the realized benefit in terms of cost, schedule, and information gained.

3.2.3.1 Soldering and Cleaning When considering soldering and cleaning, the part materials and finishes will be driven by the choice of soldering method and the use of lead or lead free solder. The board and component chemical resistance and temperature ratings make these choices more critical than before. The choice of flux that is compatible with the solder method and solder will itself determine the cleaning methods used. Final cleanliness will be determined by the end environment and in some cases the contract requirements.

When design restrictions mandate mounting components incapable of withstanding soldering temperatures, such components should be mounted and hand soldered to the assembly as a separate operation or should be processed using localized reflow technology.

Some components (e.g., Flip Chip Ball-Grid-Arrays, etc.) may have built-in vent holes into which cleaning solvents (e.g., deionized water and saponifier) can enter and cause internal capacitors in the component to corrode and ultimately fail. The cleaning process needs to address the use of such parts. It may be necessary to mask the vent holes prior to cleaning, or eliminate the use of a saponifier, if possible, since the saponifier can lower the surface tension of the water, as compared to DI water alone such that the saponifier can enter the vent holes and may not be removed by the cleaning process. See Section 11 for cleaning considerations.

3.2.3.2 Printed Circuit Board (PCB) The design of the printed circuit board is of prime consideration and has the most effect on producibility. The type and grouping of the components will drive the soldering and placement methods. For wave soldered assemblies the direction of the components will also affect the producibility. Board finish, e.g., tin fuse, solder fuse, nickel plate, Organic Surface Preservative (OSP), has an effect on the way solder will wet the board. Finish will influence solder joint appearance, the type of solder used, and long term joint reliability.

In multilayer board design, the use of heavy ground and voltage planes can often severely hinder the soldering process by affecting the heat dispersion throughout the board. Additionally, location of holes and vias in or near mounting lands are a great concern. For example a via placed in a land intended to receive a Surface Mount Technology (SMT) component may generate process results that do not conform to the requirements of IPC-A-610, and J-STD-001. Design guidelines for proper P&I Structures can be found in the IPC-2221 series documents. Failure to consider process requirements may complicate assembly or result in defect conditions when IPC-A-610 or J-STD-001 requirements are applied. The IPC-6010 series (e.g., IPC-6011, 6012, and 6013) standards and IPC-A-600 provide accept and reject criteria for unpopulated PCBs. Additionally, MIL-PRF-31032 (with applicable detail slash sheets) may be specified by the customer, in lieu of use of the IPC documents.

As a final step in manufacturing of a PCB, solder masking is used to mitigate the amount of solder that gets placed on a board, as well as to provide additional dielectric insulation between components and the board conductor paths. Selection and use of solder mask is addressed in IPC-SM-840.

3.2.3.3 Component Selection The material properties and mounting method of each component should be evaluated for compatibility with the manufacturing process. The lead finish, initial soldering process, subsequent hand soldering operations, plus exposure to cleaning chemicals constitute a major portion of the selection process after electrical consideration.

The sensitivity of parts to the environment to which they will be exposed should be considered during the manufacturing process.

3.2.3.4 Design for Rework and Test Given the problems inherent in the manufacture and assembly of PCBs, care should be taken in designing a PCB that may be repaired and tested without resulting damage. It is possible to design an assembly that can be fabricated but not successfully reworked.

3.3 Packaged-Component Assembly Considerations The selection of an appropriate packaged-component assembly technique should initially include the requirements of the end product equipment and subassemblies from the viewpoint of form, fit, and function with respect to cost effectiveness, performance, and marketability issues. After characterizing the assembly in this manner, an implementation technique should be selected and should be based on specific electrical and mechanical functions.

Determining factors will include packaging density, assembly profile height, development time, development cost, circuit element factors, manufacturing costs, thermal considerations, reliability, etc., and specific related implementation details, Table 3-1.

3.3.1 Component Orientation Another consideration for manufacturing is alignment of components on a PCB. Similar types of components should be aligned in the same orientation for ease of component placement, inspection, and soldering.

In wave soldering, proper alignment is necessary to prevent solder skips or bridging. On any printed circuit assembly where the secondary side is wave soldered, the preferred orientation of devices on that side should be such as to optimize the resulting solder joint quality as the assembly exits the solder wave.

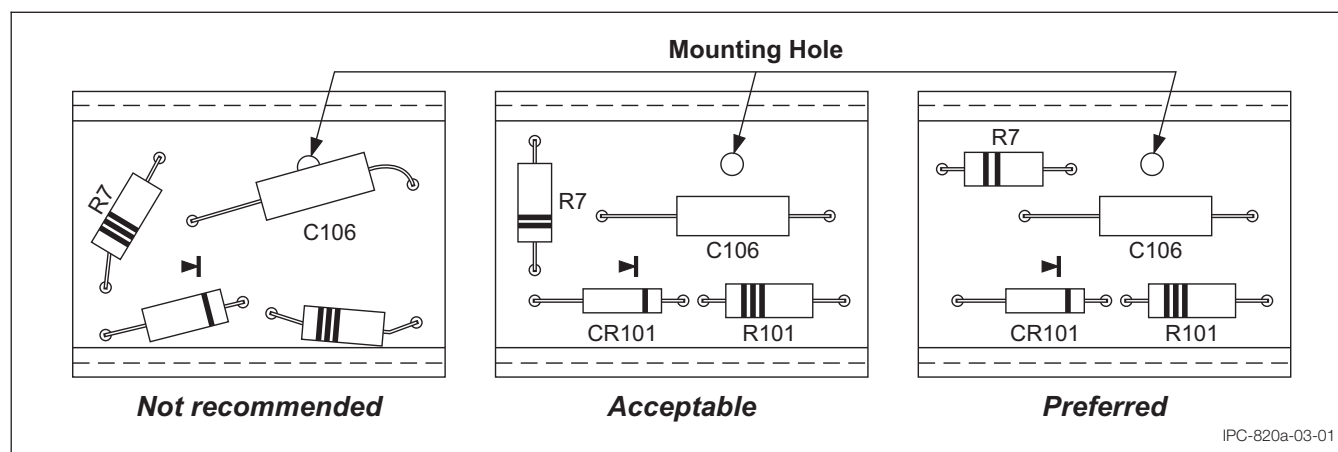
Thus:

- a. Components should be mounted parallel to the edges of the printed board.
- b. All passive components should be mounted parallel or perpendicular to one another as shown in Figure 3-1.
- c. The longer axis of SOICs and of passive components should be perpendicular to each other.
- d. The long axis of passive components should be perpendicular to the direction of travel of the printed board along the conveyor of the wave soldering machine.
- e. When appropriate, the component should be mounted in such a manner as to optimize the flow of cooling air.
- f. When selective wave soldering, components should be mounted with 2.54 mm [0.1 in] between Through Hole and SMT components for fixture wall.

In addition, orienting similar components in the same direction is very desirable for automated assembly equipment because not all machines have head rotational capability. Uniform orientation is also desirable for visual inspection. More detailed information is available in IPC-CM-770.

Table 3-1 Integrated Circuit Packaging Technology Comparison

Characteristics	Through Hole	Leaded Surface Mount	Leadless Perimeter Packages	Area Array Packages	Direct Deposit	Bare Chip
Packaging Density	low	moderate	good	high	good	high
Standardization	very good	good	good	good	good	limited
Thermal Performance	moderate	good	very good	good	good	fair
Substrate Choices	very good	very good	good	good	fair	limited
Fab Investment	low	low	moderate	moderate	moderate	high
Assembly Investment	high	low	moderate	moderate	moderate	high
Support Investment	low	moderate	moderate	moderate	high	high
External Assembly Services	very high	high	high	moderate	moderate	limited
Maintenance Skills	low	moderate	moderate	moderate	high	high
Change Risk	very low	low	low	moderate	moderate	high
Assembly Test	very easy	easy	moderate	complex	moderate	complex
Documentation	easy	easy	moderate	moderate	complex	complex
Logistics Support	field change	field change	field change	factory only	field change	factory only
Component Burn-In	easy	easy	easy	easy	easy	impractical
Pretest	very easy	very easy	easy	easy	easy	impractical
Change & Repair	easy	easy	depends	easy	easy	difficult
Chip Availability	excellent	very good	good	good	good	limited
Multiple Sourcing	excellent	very good	good	good	good	limited
Footprint Commonality	excellent	very good	good	good	good	poor
Profile	high	high	moderate	moderate	low	low

**Figure 3-1 Component Orientation with Respect to Boundaries and Mounting Accessibility**

3.3.2 Accessibility Electronic components should be located and spaced so that the lands for each component are not obscured by any other component, or by any other permanently installed parts. Each component should be capable of being removed from the assembly without having to remove any other component. These guidelines do not apply to non-repairable assemblies or to the use of bus bars.

3.3.3 Design Envelope The projection of the component, other than connectors on the board should not extend over the edge of the printed board or interfere with board mounting. Preferably there should be a minimum of 1.5 mm [0.06 in] from the edge of the printed board and board guide or mounting hardware. This clearance from the board edges is also recommended to allow for machine conveyors and soldering and test fixtures, as shown in Figure 3-1.

Unless otherwise detailed on the assembly drawing, the board edge should be regarded as the extreme perimeter of the assembly, beyond which no portion of the component, other than a connector, is allowed to extend. The designer should prescribe the perimeter with regard for maximum part body dimensions and the mounting provisions dictated by the board and assembly documentation.

3.3.4 Clearances Spacing between noncommon conductors should not violate specified minimum electrical clearance (3). This is shown in Figure 3-2 as the distances between (1) & (2) and (1) & (5). In general, uncoated conducting areas should provide for a clearance of approximately 0.75 mm [0.03 in] as shown in Figure 3-2, but not less than the minimum allowable electrical conductor spacing.

The minimum electrical spacing should be determined based of the worst case circuit voltage/ampere rating, and the ambient environment (e.g., closed versus open construction). This dimension should be referenced on the manufacturing drawings.

3.3.5 Physical Support Dependent upon weight and heat generation characteristics, components weighing less than 5 grams [0.18 ounces] per lead, that dissipate less than one watt, and are not clamped or otherwise supported, should be mounted with the component body as close to the printed board as is practical unless otherwise specified.

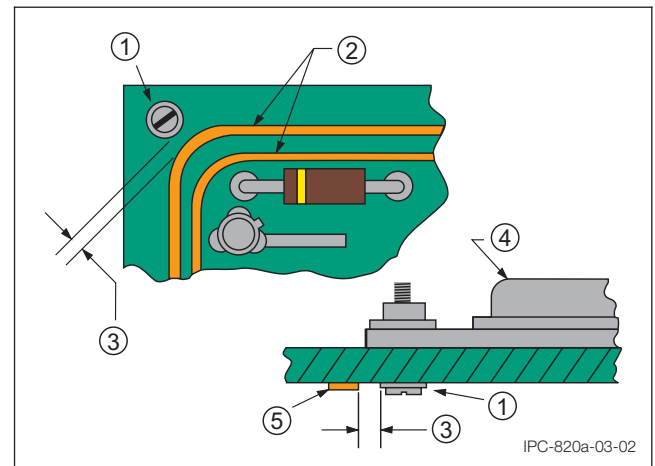


Figure 3-2 Uncoated Printed Board Clearance

1. Metallic hardware
2. Conductive pattern
3. Specified minimum electrical clearance
4. Mounted component
5. Conductor

3.4 Design for Automated Assembly With few exceptions, automated techniques and equipment are now available for most component types and assemblies. This equipment ranges from dedicated devices for specific component types (radial leaded, axial leaded, chip carriers, discrete chips, sockets, etc.) to flexible “robotic” equipment programmed to handle a range of parts.

Clearance for tooling “footprints (fiducial marks)” should be provided. Hole tolerances for through hole components and land size tolerances for surface mounted components are important and are generally smaller than those necessary with manual techniques. Sequence of component assembly is of more concern with automated techniques as is clearance from substrate edges. Layout of traces to prevent bridging as a result of clinching should be considered.

When automatic component insertion and attachment is employed, the following printed board design parameters should be taken into consideration. These parameters are not applicable when manual assembly techniques are used.

3.4.1 Fiducial Marks A fiducial mark is a printed artwork feature that is created in the same process as the circuit artwork for optical recognition systems. The fiducial and a circuit pattern artwork are etched in the same step. The fiducial marks provide common datum points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of fiducial marks, Global and Local.

Global fiducial marks are used to locate the position of all circuit features on an individual board, and Local fiducial marks are used to locate the position of an individual component requiring more precise placement. Common industry practice is to use local fiducial marks for any components with <0.635 mm [<25 mil] pitch.

For additional guidance on fiducials, see IPC-2614 and IPC-7351.

3.4.2 Automated Through Hole Assembly For automatic assembly of printed boards with components whose leads pass through the printed board, specific consideration should be given to providing allowable clearances for the insertion and clinching of the component leads.

3.4.3 Automated Surface Mount Assembly Automatic assembly considerations for surface mounted components include pick-and-place machines used to place or position chip components, discrete chip carriers, small outline packages, and flat packs. Design restrictions should maintain appropriate clearances for the automatic pick-and-place equipment to position the parts in their proper orientation and allow sufficient clearances for the placement heads.

Special orientation symbols should be incorporated into the design to allow for ease of inspection of the assembled surface mounted part. Techniques may include special symbols, or special land configurations to identify such characteristics as a lead of an integrated circuit package.

3.4.4 Automated Mixed-Technology Assembly The automatic processing of assemblies that use both through hole and surface mounted components require special design considerations in order that the components assembled during the first phase of the process do not interfere with component placement heads during the second phase. Such component placement should also consider the stresses that are put on the printed board with assembly equipment, by isolating parts wherever possible to specific areas so that the second phase component placement stresses do not impact previously soldered connections.

3.5 Through Hole Assembly Through hole assembly technology is based on the use of packaged components such as dual-inline packages (DIPs), single-inline packages (SIPs), and other leaded device configurations. As the name implies, through hole mounted components are assembled with their leads through holes in the printed board.

Advantages – As compared to the other processing technologies, the advantages of using through hole mounting technologies include:

- The technology is very mature.
- There is excellent component availability.
- Computer-aided tools are available to support design, fabrication, assembly, and testing operations.
- End-product reliability is well established.
- Electrical test needs are well understood.
- There are existing assembly test procedures.
- Rework capabilities exist.

Disadvantages – Disadvantages pertain specifically to:

- Component mounting density is minimal.
- End-product weight is increased.
- Component lead count is limited (except with pin-grid array packages).
- Component mounting holes minimize inter-connecting conductor routing density.

3.5.1 Lead Configuration The objectives of lead termination are to form the lead and electrically connect it to the conductors in such a manner that the required circuit continuity is provided through the life of the equipment regardless of the environments to which the assembly may be subjected. See Figure 3-3 for the most frequently used methods.

Leads should be attached to unsupported printed board lands by clinching. Leads should be terminated in such a manner that they do not exert a lifting force on the copper foil land or conductor. The attachment should be completed by soldering. Requirements are described in IPC-A-610. The main purpose of lead clinching is to secure the components during subsequent processing.

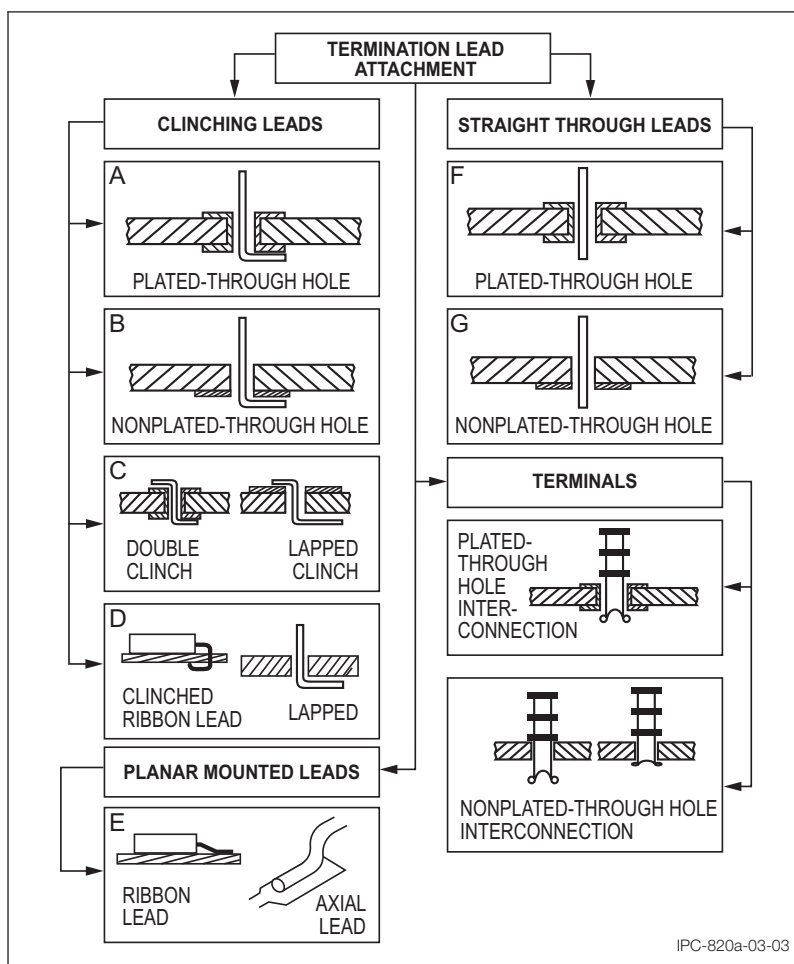


Figure 3-3 Lead Terminations

Component attachment to printed boards should have the lead or terminal pass through the printed board and be soldered to the conductor pattern on the opposite side of the printed board. Though heat maybe applied simultaneously to both sides of the assembly, solder should be applied to only one side of the board, unless the application is Pin-in-Paste.

Each functional lead should have an associated land. There should be no more than one lead in any lead mounting hole.

3.5.1.1 Straight-Through Leads The most direct method for mounting components to the printed board is the straight through method with un-clinched leads.

The use of straight through leads requires minimal device handling, including a straightening of the component leads and cutting the leads to length before or after insertion.

Disadvantages – Associated with this approach are:

- a. The device is subject to movement both before and during the soldering operation. This makes it difficult to control the component height off the mounting surface. This movement can be a source of solder joint problems.
- b. It is difficult to maintain a suitable clearance between the body of the component and the printed board surface for flux removal and, when applicable, conformal coating of the assembly. This is greatly minimized when multiple lead cans with integral standoffs are used creating a component seating plane below the surface of the can from which the leads emerge.
- c. Supported holes are preferred in the printed board for the component lead holes to enhance the mechanical strength of the solder joint. Otherwise the clearance between the component lead, the hole, and the circumscribing land must consider the lead-to-hole ratio and the hole-to-land difference that would allow sufficient remaining conductor to promote solderability.
- d. The automatic insertion of the device leads in limited space can present problems.

The mounting of multi-lead component cans with plastic spacers has been used to overcome some of the disadvantages for the more conventional straight-through lead mounting techniques. Spacers with protrusions on one side should be mounted with the protrusions against the printed board.

Advantages – In addition to the considerations common to the straight-through mounting techniques, the mounting of component with spacers has the advantages of:

- a. A suitable-clearance between the component body and the printed board can be maintained to facilitate soldering flux removal and conformal coating and can preclude damage to the component due to heat from the wave soldering process.
- b. A bearing surface for the body is provided if the component leads are to be clinched.
- c. The extension of un-clinched leads beyond the printed board surface can be more accurately controlled.
- d. The height of the component body above the printed board surface can be more accurately controlled; this is especially important when the printed board assemblies are closely spaced.
- e. The spacer helps to reduce the magnitude of mechanical stresses that are transmitted to the lead/body interface seal.

3.5.1.2 Full-Clinched Leads Clinching of leads prior to soldering is commonplace, either as part of machine insertion or following hand insertion. The substrate land configuration and spacing to adjacent lands should be considered. Clinching in line with traces and trimming of leads before clinching is recommended where clinch direction may cause shorting to adjacent lands. It is preferred not to clinch all leads of a multi-leaded device, The lead is passed through-the-board and is clinched to make contact with the land or conductor and is then soldered. The lead or terminal should make contact with the conductor pattern before soldering.

Leads should not extend beyond the edge of their lands, however, if overlap does occur, the lead should not violate electrical spacing requirements. The lead termination hole may be supported by eyelets or plated-through holes or it may be unsupported.

Advantages – In addition to the considerations common to all straight-through mounting methods, this method has the following advantages:

- a. A reinforced mounting hole is not required; tear drop and offset lands can be used.

Disadvantages – This method has some of the disadvantages mentioned for un-clinched straight-through mounting, in addition:

- a. Care must be taken when cutting the lead to length and forming the clinch to assure that minimum conductor clearances are provided when the clinched lead overhangs the land.

b. The lead clinching operation, if not controlled properly, can unduly stress the component lead-to-can body seal.

Clinched leads should be bent between 75 and 90 degrees from a vertical line perpendicular to the printed board. When maximum mechanical retention of a lead or terminal is required by design, the lead or terminal should be clinched. The component holes may be supported holes (plated through holes), unsupported holes (non-plated through holes), or eyeleted holes.

Clinching requirements should be defined on the assembly drawing. The lead end should not extend beyond the edge of its land or beyond its electrically connected conductor pattern, in violation of the minimum spacing requirements. Partial clinching of leads for part retention should be considered under the requirements for partially-clinched lead termination.

Full-clinched lead clinching is not applicable to leads of dual-in-line packages (DIPs) or pins, other type modules, tempered pins, or leads over 1.3 mm [0.05 in].

For printed boards with non-plated-through holes, leads should be clinched.

3.5.1.3 Partially-Clinched Leads Partially-clinched leads should be bent between 15 to 75 degrees as measured from a vertical line perpendicular to the printed board surface. Lead length should be 1.0 ± 0.5 mm [0.04 ± 0.02 in] as measured from the conductor surface for the plated-through hole. See Figure 3-4.

Do not clinch leads which are tempered, or are over 1.3 mm [0.05 in] in diameter.

Dual-inline package (DIP) component leads may be bent, rather than clinched, toward the termination area to retain parts during soldering operations. It is preferred to bend only one lead outward on opposite corners of the device unless required by the customer and/or equipment class. However, such bent leads should conform to all requirements applicable to un-clinched straight-through leads.

Bends should be limited to 30 degrees maximum outward from the axis of the hole; see Figure 3-5, and to a maximum of four leads per component, with not more than two leads on one side.

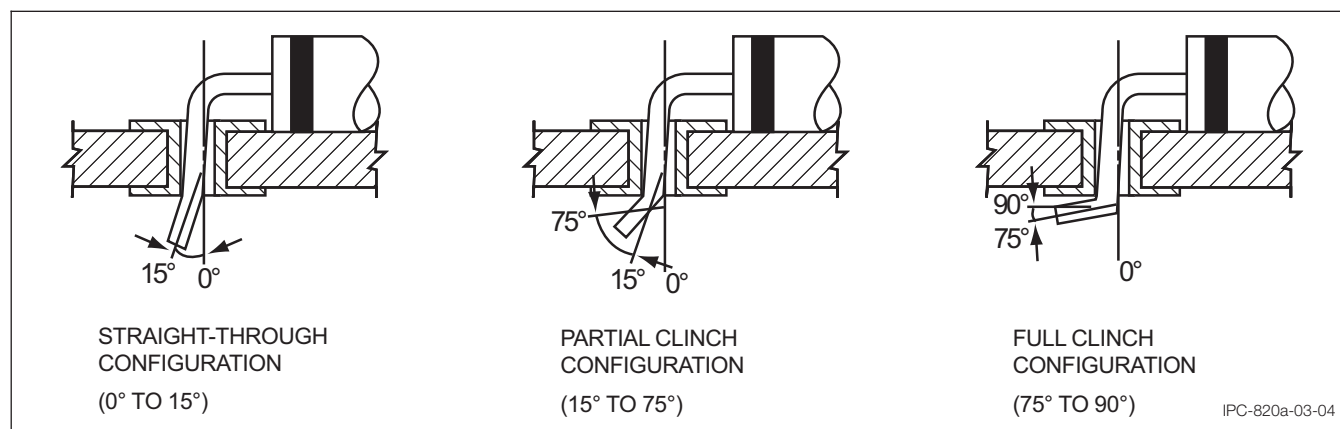


Figure 3-4 Clinched Through Hole Leads

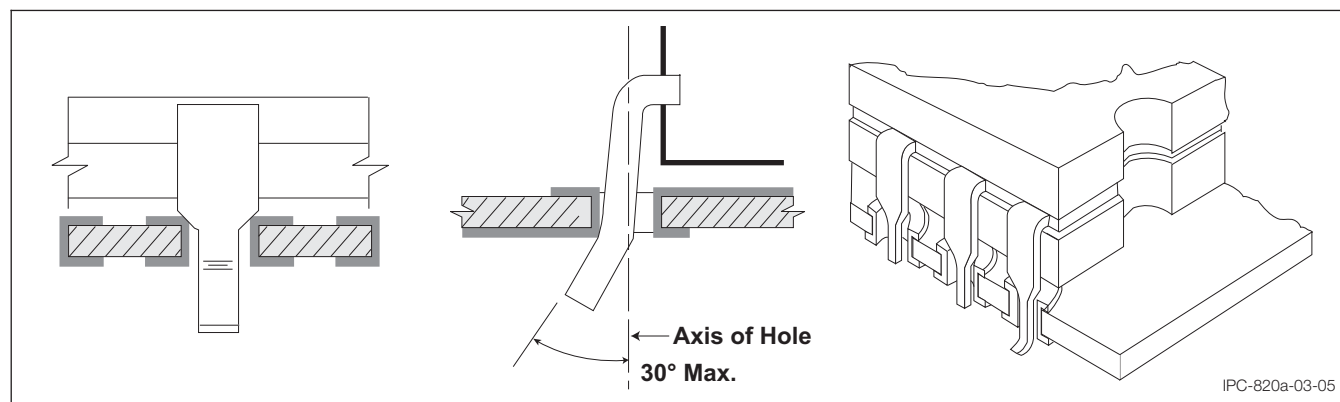


Figure 3-5 Dual-Inline Package (DIP) Lead Bends

3.5.1.4 Lead Bends and Stress Relief Lands and terminals should be located by design so that components can be mounted or provided with stress relief bends in such a manner that the leads cannot over stress the part lead interface when subjected to the anticipated environments of temperature, vibration, and shock. Where the lead bend radius cannot be in accordance with Figure 3-6 in order to achieve design goals, the bends should be detailed on the assembly drawing.

The leads of components mounted horizontally with their bodies in direct contact with the printed board should be mounted with a method that ensures that stress relief is not reduced or negated by solder in the lead bends. Leads should not be bent at the body of the component or between the body of the component and any lead weld. The lead should extend straight from the component body seal or lead weld before starting the bend radius as shown in Figure 3-6.

Typical stress relief bends are shown in Figure 3-7. The criteria of Figures 3-6 and 3-7 should be fully implemented to prevent possible component package damage, particularly glass-bodied parts.

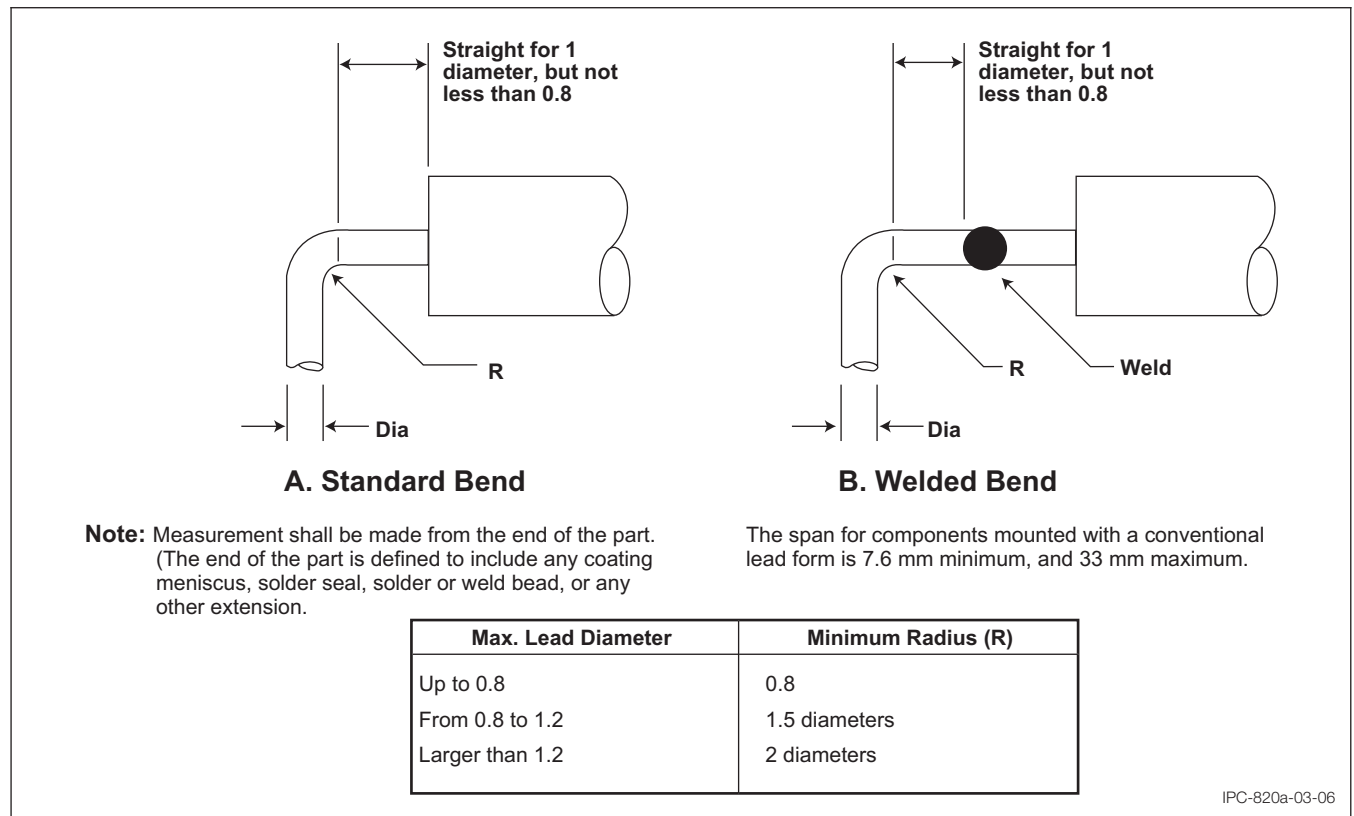


Figure 3-6 Lead Forming and Stress Relief Lead Bends

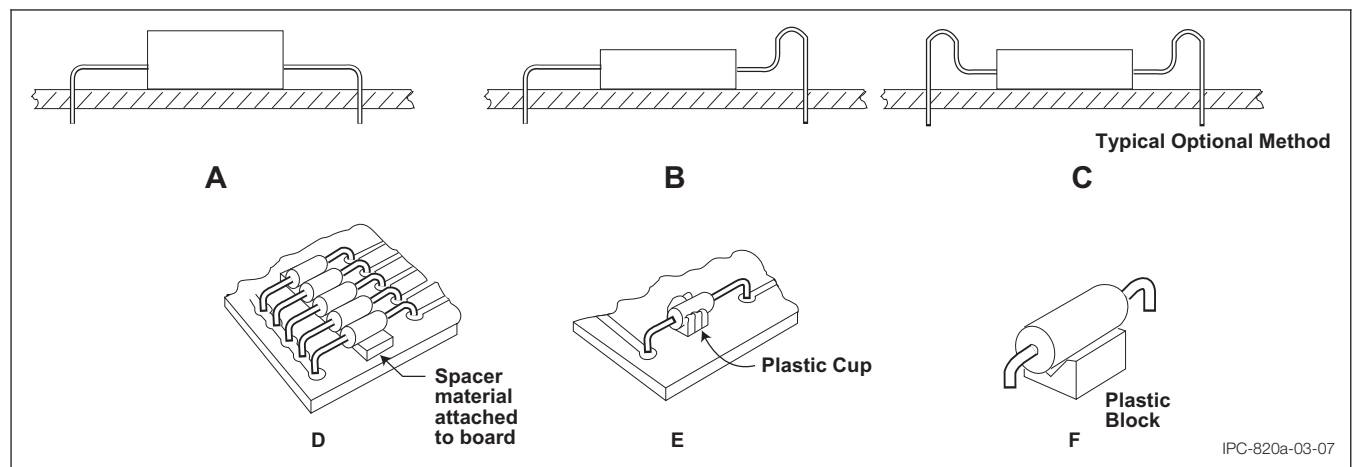


Figure 3-7 Component Mounting Configurations

3.5.2 Lead/Hole Relationships The lead to hole clearance should be such as to provide for good soldering conditions. Generally 0.25 to 0.5 mm [0.010 to 0.020 in] clearance in diameter is used. If the clearance is too small or too large, adequate wicking of solder does not result. A minimum protrusion through the substrate is often specified. The maximum is dependent on specific later process equipment used and end product design clearances. For rectangular leads the dimension across the diagonal should be considered as being the lead diameter.

3.5.2.1 Unsupported Holes In determining the difference between the diameter of an unsupported hole and that of the lead to be placed in the hole, the hole should be from 0.25 to 0.5 mm [0.010 to 0.020 in] larger than the lead diameter.

3.5.2.2 Supported Holes In determining the difference between the diameter of a supported hole and that of the lead to be placed in the hole, the hole should be from 0.25 to 0.7 mm [0.010 to 0.028 in] larger than the lead diameter.

3.5.2.3 Leads in Holes Component leads, jumper wires, and other leads should be mounted such that there is only one lead in any one hole, except when bus bars are used. The preferred method for component leads in unsupported holes are that they are clinched, but if installed straight through they should be required to extend a minimum of 0.5 mm [0.02 in] and a maximum of 1.5 mm [0.06 in] from the surface of the printed board plating or foil. Component leads in plated-through holes should be required to extend a minimum of being flush to a maximum of 1.5 mm [0.06 in] from the surface of the printed board plating.

The straight-through leads on connectors or other devices with tempered leads should extend from 0.25 mm [0.01 in] to 2.0 mm [0.08 in], provided there is no electrical or mechanical interference.

3.5.3 Through Hole Land Patterns Land patterns for through hole mounted components should consider minimum/maximum lead spacing requirements. Standard land spacing patterns should be established for the purpose of uniformity of assemblies and the practical use of assembly tools and equipment. Spacing(s) should be located to accommodate automatic assembly, “bed-of-nails” type or “Flying Probe” types of testing equipment, usually in 2.5 mm [0.100 in] increments, e.g., 7.5, 10, 12.5 mm [0.300, 0.400, 0.500 in], etc.

Land patterns for unsupported holes should have more solderable area than supported holes for a stronger joint after soldering. The optimum dimension is dependent on the device and its mounting characteristics.

The most common geometry is the round land with a centered hole. Square lands with centered holes are sometimes used to indicate polarity for polarized components.

3.5.3.1 Axial-Lead Component Mounting Centers The leads of axial-lead components should extend approximately one lead diameter or thickness, but not less than 0.8 mm, straight out from the body of the component. The end of the body in this application is defined to include any coating meniscus, solder seal, solder or weld bead, or any other extension.

Thus, the minimum component center-to-center printed board lead spacing, can be represented by the equation below.

$$L = B_{\max} + 3D^* + 2FA$$

For lead diameters up to 0.7 mm [0.027 in]; 4D for lead diameters between 0.7 mm [0.027 in] and 1.2 mm [0.048 in]; and 5D for lead diameters over 1.2 mm [0.048 in].

L = Center-to-center lead spacing

B = Body length

D = Nominal lead diameter

FA = Forming allowance (lead should not be disturbed within this distance from the body)

The value of “L” is usually adjusted upward to coincide with the grid used. The total length of both leads should not exceed 25 mm [1 in] in length unless this component is mechanically supported to the mounting base.

Properly formed leads on axial leaded components normally afford adequate stress relief when formed as shown in Figure 3-6. Mechanically sensitive components, such as glass diodes, may require additional stress relief and have one or more leads formed with a stress relief loop. Whenever the possibility exists of solder wicking into the stress relief bend, usually as a result of a small diameter component, stress relief loops or spacers should be provided as the stiffened lead defeats the purpose of the stress relief.

3.5.3.2 Flat-Pack Components When flat pack components are through hole mounted they are usually terminated in a staggered grid of plated-through holes, Figure 3-8. In these instances, proper forming of the leads is required to prevent stressing the lead interface with the component body. An off-board clearance of 0.25 mm [0.01 in] minimum is generally required for cleaning purposes.

The body of the flat pack should not cover vias unless the vias have a protective coating. The leads should extend from the base of the component body a minimum of one lead diameter/thickness, but not less than 0.8 mm [0.03 in] before the bend begins.

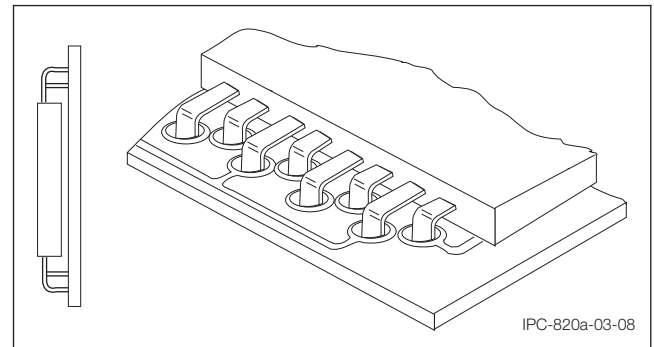


Figure 3-8 Through Hole Flat-Pack Mounting with Staggered Plated Through Holes

3.6 Surface Mount Assembly Surface mount technology (SMT) presents distinct advantages to the manufacturer who needs to reduce the size of the product or to increase the functionality of the product. However, without adhering to proper design rules, this advantage is quickly lost in assembly, rework, quality assurance, and testing. Thus, the printed board designer should work closely with engineering, manufacturing, purchasing, testing, and quality assurance. Together this team, with a good foundation in surface-mount technology design and manufacturing techniques, can eliminate most assembly problems including tomb stoning, component shifting, or component cracking during the reflow process.

3.6.1 Basic Printed Board Features In general, the basic printed board features for surface mount design are smaller than those for through hole technology. Additionally, more vias are often used to connect layers. These vias also are smaller than the holes used to hold component leads. Thus, for surface-mount technology the use of smaller conductors, spaces and vias complicate the design and printed board fabrication process.

The selection of the design and positioning of the land geometry, in relation to the part, may significantly impact the solder joint. The possibility of “heat thieving” is reduced by necking down the conductor near the soldering area. Thus, the printed board designer should understand the capabilities and limitations of the manufacturing and assembly operation (see IPC-7351).

3.6.2 Manufacturing Allowances The design of all land patterns should consider the manufacturing allowances; specifically those relating to conductor width and spacing. In order to have land patterns that are commensurate with reliable solder joint formation, only IPC-222x series Productivity Level B and C conductor width tolerances should be used on the end product conductor configuration.

3.6.2.1 Design for Testability It is recommended that chip carrier sites be located on a fixed grid for optimized testing. This grid should be compatible with assembly and testing equipment, so as to minimize the amount of specialized and complex equipment. In Figure 3-9 land extensions are designed such that the PCB can be electrically tested with a general purpose 2.54 mm [0.100 in] grid bed-of-nails fixture.

For designs where fan-out patterns are not on 2.54 mm [0.100 in] grids, Figure 3-10, a specialized fixture would be required for electrical testing.

Testing on the primary side of an assembly is only recommended for unpopulated PCAs. Thus, designing a chip carrier site for primary side testing does not require dedicated through vias and permits more efficient routing. This is usually only used with designs using blind or buried vias or where the secondary side is not accessible. Testing on a 2.54 mm [0.100 in] grid is suitable on an “IL,” modified “IL,” or staggered fan-out pattern, Figure 3-10.

Any crystals and clocks included in the assembly may need to be disabled to improve the overall testability of the assembly.

3.6.3 SMT Land Pattern Details The IPC-7351 provides generic requirements on land pattern geometries used for the surface attachment of electronic components, as well as surface mount design recommendations for achieving the best possible solder joints to the devices assembled. The intent of the information it presents is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet and to also allow for inspection and testing of those solder joints. In many instances, the land pattern geometries can be slightly different based on the type of soldering used to attach the electronic part.

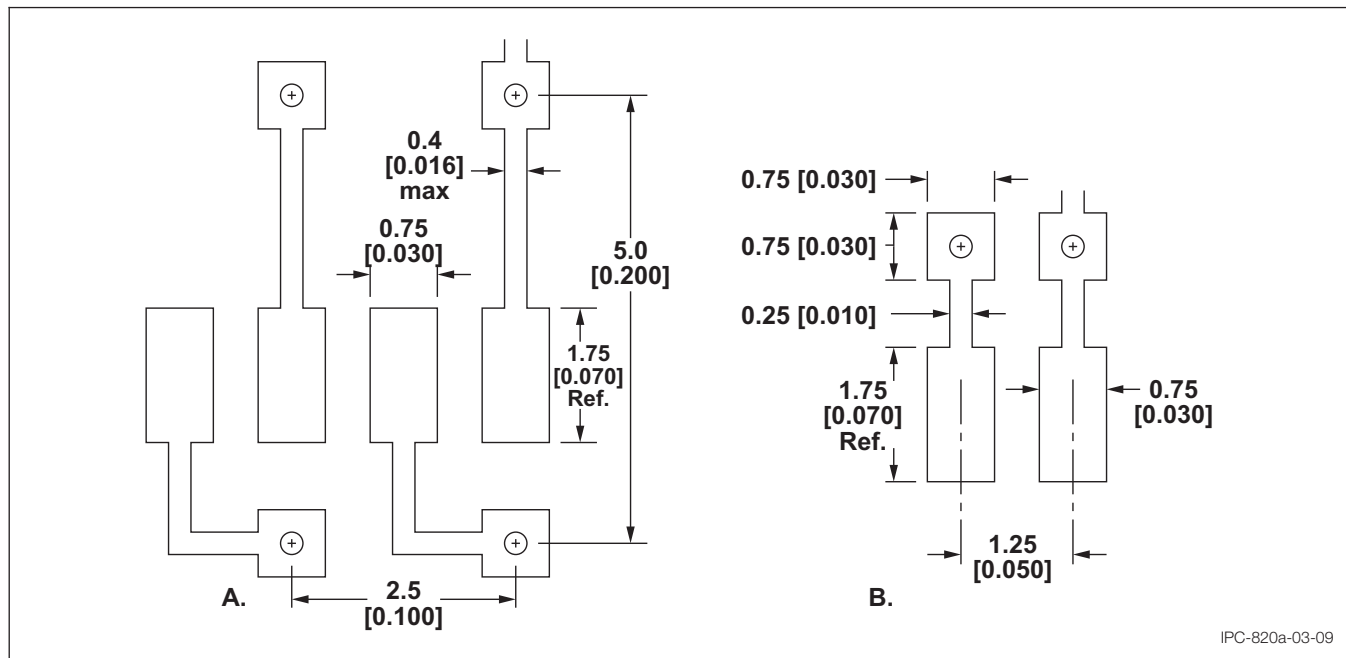


Figure 3-9 Modified Fan-Out Lands, mm [in]

Designers should be able to use the information contained therein to establish standard configurations not only for manual designs but also for computer-aided design systems. Whether parts are mounted on one or both sides of the printed board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

3.6.4 SMT Assembly Processing There are several different ways to process surface mount assemblies. Basically, the differences pertain to the use of SMT components on one (single-sided) or both (double-sided) sides of the assembly, whether there is a mixed SMT/through hole configuration, and whether or not special components must be mounted and/or soldered manually.

3.6.4.1 SMT Substrate Preparation The use of a solder paste (cream) is an important part of surface mount substrate preparation prior to reflow soldering. The solder paste acts partially as an adhesive before reflow and its surface tension can help to align skewed parts during soldering. It contains the flux, solvent, suspending agent, and solder alloy that is traditionally supplied by the wave soldering machine. Therefore, the selection of a particular solder paste involves optimizing its rheology characteristics such as viscosity, flow and spread. Susceptibility to solder ball formation and wetting characteristics must also be considered.

The solder paste is generally applied on the lands of the substrate by screening, stenciling, or syringe dispensing. The use of stencils is preferred for high-volume applications because they are more durable, easier to align, and can be used to apply a thicker layer of solder than the screening process. However, because they are usually more expensive than screens, the use of stencils may not be suitable for low-volume production runs. See IPC-7525 for additional information on stencils.

Solder pre-forms (doughnuts) are sometimes used for the through hole components in mixed-technology applications to facilitate reflow soldering (intrusive soldering, Pin-in-Paste) instead of wave soldering for these applications. The use of preforms and reflow soldering is particularly suitable for assemblies that consist predominantly of surface mount components. In addition, modified stencil apertures can be used to facilitate intrusive/Pin-in-Paste soldering.

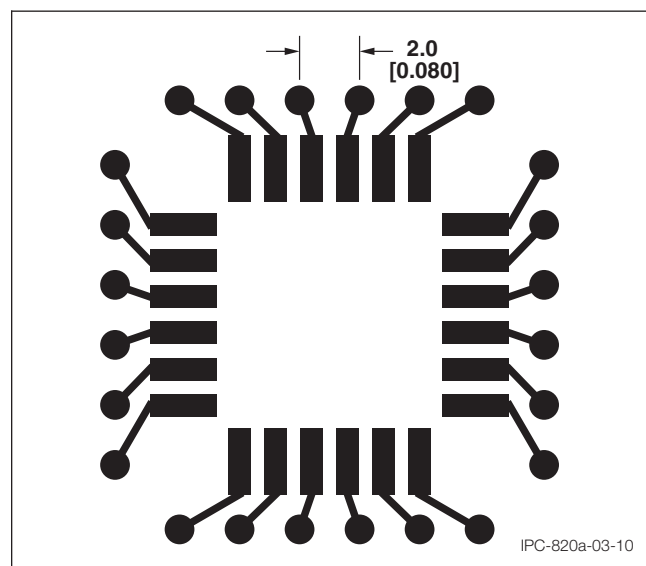


Figure 3-10 Custom-Grid Fan-out Land Pattern

3.6.4.2 Component Preparation The requirements and considerations for mounting components over conductive patterns apply to the surface mounting of components which have leads. Lead forming is a major design consideration and should be described on the assembly drawing. Formed leads should provide stress relief, ensure fit to the land pattern, allow under-body clearance for cleaning, and provide any designed-in provisions for thermal transfer (see Figure 3-11 and J-STD-001).

When flat packs are planar mounted (Figure 3-11) the leads of the flat pack should be configured as shown in Figure 3-12. An off-board clearance of 0.27 mm [0.010 in] minimum should be maintained for cleaning purposes.

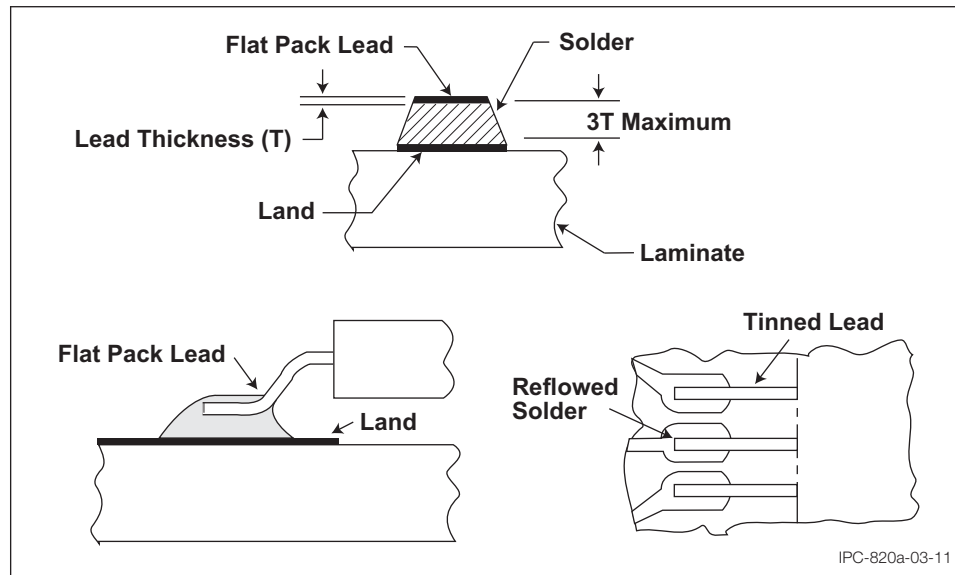


Figure 3-11 Gull Wing Flat Pack Surface Mounting

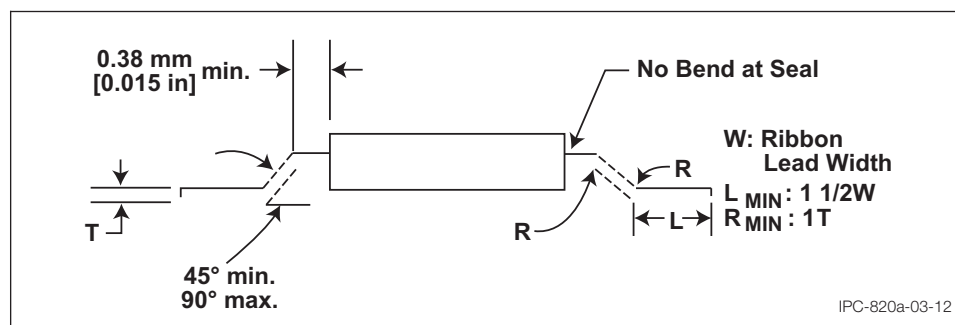


Figure 3-12 Flat-Pack Lead Forming for (Planar) Surface Mounting

Flat-wire ribbon leads may be attached to lands on the printed board, see Figure 3-13. Connections made in this manner may include the deposition of an adhesive under the body of the component when wave soldering is used to make the solder connection.

One of the most significant departures from through hole technology is the need for a solder-deposition process for soldering only. In some instances, components with round leads may be attached to the surface lands without first passing through a hole. The lands should be designed with the proper shape and spacing to be compatible with the surface-mount soldering termination techniques. Axial-leaded components with round leads may have their leads coined or otherwise flattened to provide a positive mounting surface, see Figure 3-14.

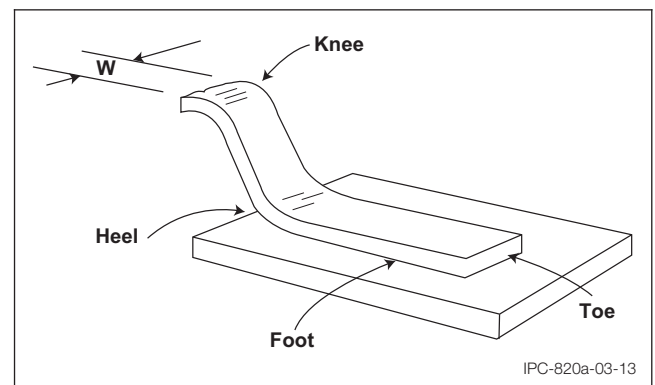


Figure 3-13 Surface-Mount Flat Ribbon Lead Features

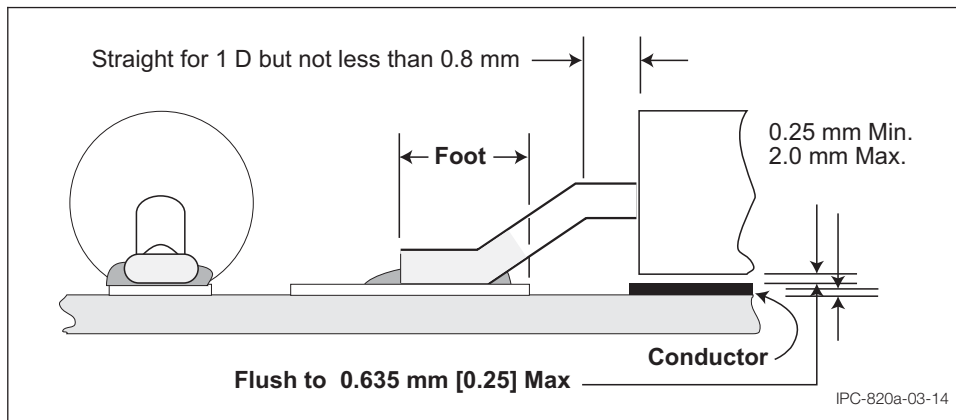


Figure 3-14 Coined Round Leads

3.6.4.3 Component Placement The component placement accuracy requirements for surface mounting, especially with fine-pitch component packages, often necessitates the use of automated assembly machines that are often referred to as “pick-and-place” equipment.

The selection of these machines is generally based on the rate at which components are most cost-effectively assembled and their suitability for use with the appropriate variety of surface mount component package delivery formats such as tape, stick, belt, matrix tray, and cassette feeders.

3.6.4.4 Soldering The selection of a soldering process depends upon the type of components being assembled and, as previously mentioned, whether or not a mixed technology or all surface mount assembly is being manufactured. Depending on the component mix, the candidate technologies are wave soldering and a variety of reflow soldering techniques. Each process has a corresponding set of manufacturing parameters for which it is best suited. Another consideration is for the use of a low-volume batch processing unit or a high-volume inline machine.

3.6.4.5 Cleaning The cleaning of surface mount assemblies is harder to perform than the cleaning of through hole technology assemblies because of the higher density nature of the assembly; especially with respect to removing flux that has been entrapped under the component packages.

Flux entrapment may cause potential reliability problems if the assembly is not properly cleaned. However, new solder paste formulations are being developed that might result in the use of “no-clean,” “no flux,” or low-solids flux soldering technologies in order to minimize these problems.

3.6.4.6 Repairing/Reworking The repair or rework of surface mount assemblies is generally easier than with through hole assemblies due to the absence of component mounting holes. However, because of the high-density nature of the assembly, special tools are used for this purpose that carefully direct the reflow soldering energy so as to minimize the amount of heat applied to the assembly during this operation.

The manual component removal/replacement tools include the use of fork-like soldering iron tips and resistance-heated tweezers. Various types of hot-air devices are also available for this purpose.

For additional information see chapter 14.

4 PRINTED CIRCUIT BOARDS

This Section of the Assembly and Joining Handbook provides general information that pertains to all types of Printed Circuit Boards (PCB), i.e., single, double and multi-layer rigid and flexible structures that are used as the basic substrates of electronic assemblies.

4.1 General Considerations The basic function of printed boards is to provide support for circuit components and to interconnect them electrically. To achieve this, numerous PCB structure types varying in base dielectric material, conductor type, number of conductor planes, rigidity, etc., have been developed.

Familiarity with these variations will allow assembly and joining process engineers and support staff to participate in optimizing the system being developed.