



*The Institute for
Interconnecting
and Packaging
Electronic Circuits*

IPC-D-279

Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-279

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The material in this standard was developed by the IPC SMT Design Reliability Task Group (6-10b) of the Product Reliability Committee (6-10) of the Institute for Interconnecting and Packaging Electronic Circuits.





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Users of this standard are encouraged to participate in the
development of future revisions.

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Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

1.0 SCOPE

This document establishes design concepts, guidelines, and procedures intended to promote appropriate 'Design for Reliability (DfR)' procedures and to ensure reliable printed wiring assembly (PWA) characteristics. The major focus of the information presented is directed toward those PWAs that have surface mount (SM) components, either totally, or intermixed with through-hole components, mounted on one or both sides of the mounting structure.

1.1 Purpose The definition of reliability in this document is:

Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels.

This document addresses reliability-related aspects of product design, process design, as well as material/component selection and qualification. This document identifies appropriate existing IPC documents for basic detailed information.

The effort of this document is directed at SMT; the interconnect structure and the solder joint will receive most of our attention.

1.2 Design Philosophy Before the product design effort can begin, the designers of the product and assembly process need to know the customer's reliability requirements for the product. These requirements should be defined and ranked by a concurrent engineering or cross-functional team through a process such as Quality Function Deployment (QFD), used to capture the voice of the customer.

1.2.1 Establishing the Design Team The design team can include but is not limited to the members who participate in at least the design activities identified in Table 1-1. In this table, DfA/M stands for Design for Assembly/Manufacturability, DfT for Design for Testability, DfR for Design for Reliability.

The design team can consider the general design guidelines and issues presented in the body of this document as a methodology for achieving its reliability goals. Figure 1-1 illustrates the general design steps and process flow using concurrent engineering. Figure 1-2 illustrates the interactive nature of the design for reliability process.

1.2.2 Defining Reliability Requirements The basic reliability requirements to be defined include:

Table 1-1 The Design Team

Design/Engineering Function		Team Improvement Area		
Product	(QFD)	(DfA/M)	(DfT)	(DfR)
Circuit	(QFD)	(DfA/M)	(DfT)	
Printed board		(DfA/M)	(DfT)	(DfR)
Thermal	(QFD)			(DfR)
EMC, EMI, ESD	(QFD)		(DfT)	(DfR)
Mechanical	(QFD)	(DfA/M)	(DfT)	(DfR)
Software	(QFD)		(DfT)	
Marketing	(QFD)			
Process/manufacturing	(QFD)	(DfA/M)		
Test	(QFD)		(DfT)	(DfR)
Package/component		DfA/M	(DfT)	
Field Service	(QFD)		(DfT)	
Purchasing		(DfA/M)		
Material	(QFD)	(DfA/M)	(DfT)	(DfR)
Reliability	(QFD)	(DfA/M)	(DfT)	(DfR)
Regulations	(QFD)		(DfT)	
Upper management	(QFD)	Conceptual Design and Cultural Change		

- years of service
- acceptable failure rate(s)/probability(ies) as a function of time
- repair/replacement/upgrade/service/maintenance/warranty strategy
- life cycle environment(s)
- definition of acceptable performance
- criticality of function(s)
- available test equipment

1.2.3 Understanding the Product Life Cycle The life cycle begins at the component level (including the printed board) and continues through the assembly level; the life cycle includes exposure to the following environments:

- assembly/process
- testing
- storage
- transportation
- operating



Test, storage and transportation need to be considered at both component and assembly levels as well as before, during, and after the assembly process.

1.2.4 Defining the Product Environment For each environment, in 1.2.3, it is critical to identify, characterize and quantify the parameters listed below:

- Temperature Range
- Time at Temperature
- Temperature Rate of Change
- Kind and number of temperature cycles
- Duty Cycle
- Humidity (moisture) exposure
- Atmospheric pressure conditions (earth, space, both)
- Vibration and shock
- ESD, EOS, EMC, EMI and high voltage exposures and requirements
- Chemical exposures (flux, solvents, salt spray, NBC, decontamination, etc.)
- Radiation (Ionizing, light, UV)
- Contamination (dust, oil, paper)
- Pressure conditions

When the life environments have been identified and defined, the engineering team is prepared to analyze and select the materials, components, assembly processes, thermal management and test strategies required.

1.3 Document Organization This document has been organized to provide the reader with consistent information on the various aspects of surface mount technology printed board assemblies and identifies the parameters that need to be addressed. Each section serves a specific function in the SMT design process. The body of this document addresses general design guidelines specific to SMT. The appendices contain detailed information of SMT design or common design considerations between SMT and through hole processes.

1.3.1 Applicable Documents Section 2.0 lists only those documents related to surface mount technology and reliability which are mentioned in the text. The design engineers need to know about the primary documents which underlie the text. The bibliography, Section 9, lists documents by interest area and some entries are duplicated; there are many more documents of use and available to the designer. This lists only those documents used day to day.

1.3.2 Design for Reliability of SM Assemblies Section 3.0, together with Sections 4.0 and 5.0, considers the broad range of environmental stresses to which the printed wiring assembly (PWA) must be robust during its life cycle (life

cycle environment) and some specific mitigation techniques that may be used. A separate Appendix D for SM thermal design augments Appendix A for the DfR of solder attachments and Appendix B for DfR of plated-through vias (PTVs). Appendix C provides DfR information for insulation resistance aspects. Appendix E provides DfR information for insulation resistance aspects Appendix E relates environmental stresses and the corresponding PWA and component responses. Appendix G provides material CTE data. Appendix I describes solvent related stresses on plastics and metals. Appendix L deals with corrosion. Appendix M discusses solder joint variability. Appendix N deals with adhesives, solder masks and conformal coatings. Appendix O covers the special requirements for high altitude and aerospace applications.

1.3.3 Substrates Section 4.0 covers rigid and flexible substrates and their impact on SM assembly reliability. Data on material parameters and tradeoffs is provided. Substrate related issues such as thermal expansion mismatch, moisture absorption, and PTH-via thermal stress are covered. Related materials CTE data is provided in Appendix G. Appendix N deals with adhesives, solder masks and conformal coatings. A detailed DfR treatment for PTVs is provided in Appendix B.

1.3.4 Components Section 5.0 covers components, component-related design issues, and component-process interactions of concern to the designer as well as to the process engineer. Appendix E relates environmental stresses and the corresponding PWA and component responses. Appendix F provides a ready reference to surface mount plastic package cracking during SM reflow and to methods for mitigating those effects. Appendix H provides a ready reference to the electrostatic discharge susceptibility groupings of various component families.

1.3.5 Attachment Materials and Coatings Section 6.0 addresses attachment materials and polymer coatings. The attachment materials include solder, electrically conductive adhesives, thermally conductive adhesives and structural adhesives. The polymer coatings include solder mask conformal coating.

1.3.6 Assembly Processes and DfM Section 7.0 provides an overview of the assembly processes used in surface mount assemblies and highlights the specific reliability issues associated with each of the individual processes, including design for manufacturability (DfM) considerations. The surface mount processing conditions may be the most severe that the assembly ever sees during its life cycle, not only in terms of temperature but shock and flexure as well. A DfM checklist is provided listed in Appendix K together with pointers to DfM assessment tools in software. A detailed list of solvent/plastic/metal compatibilities is provided in Appendix I.

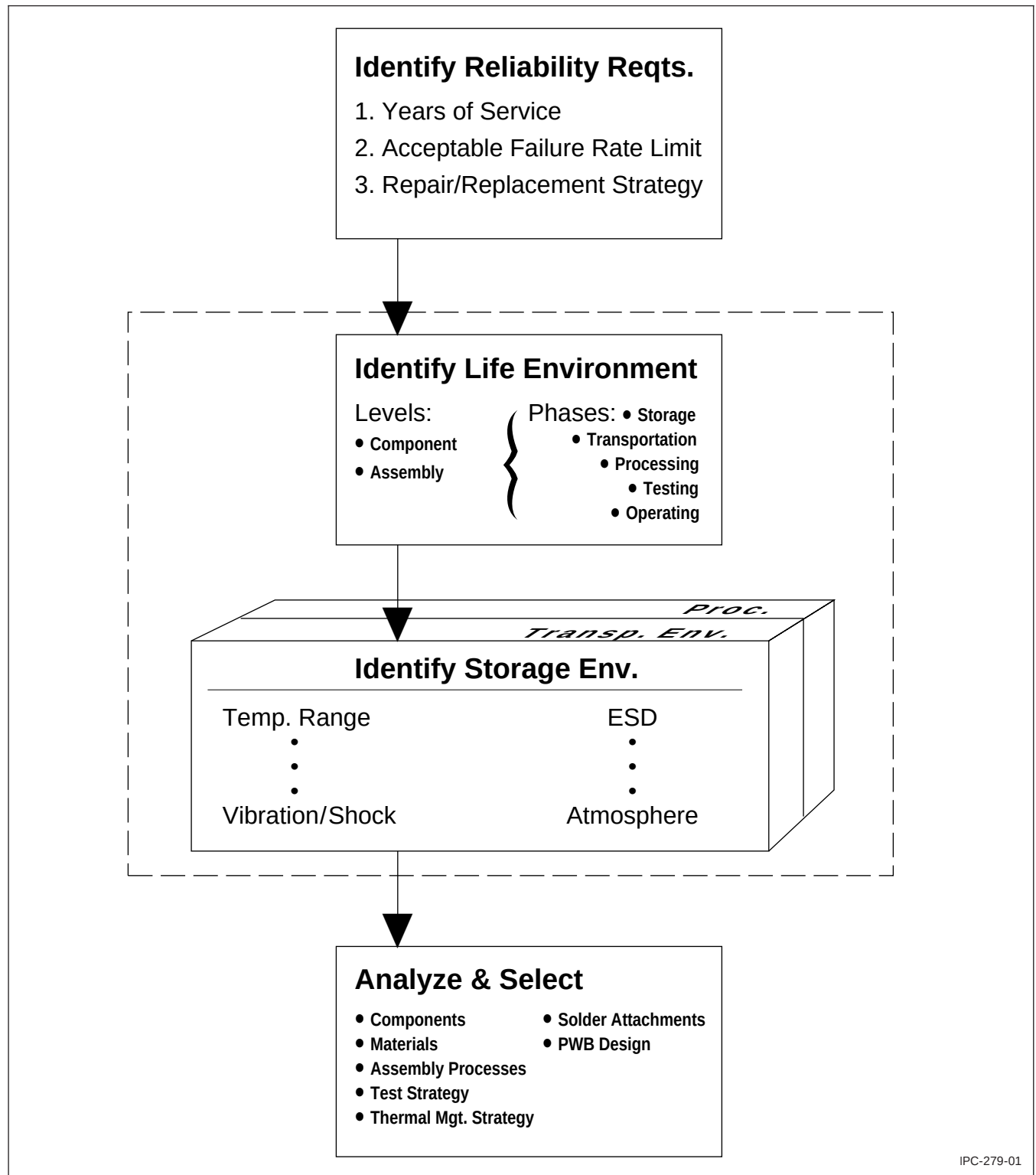


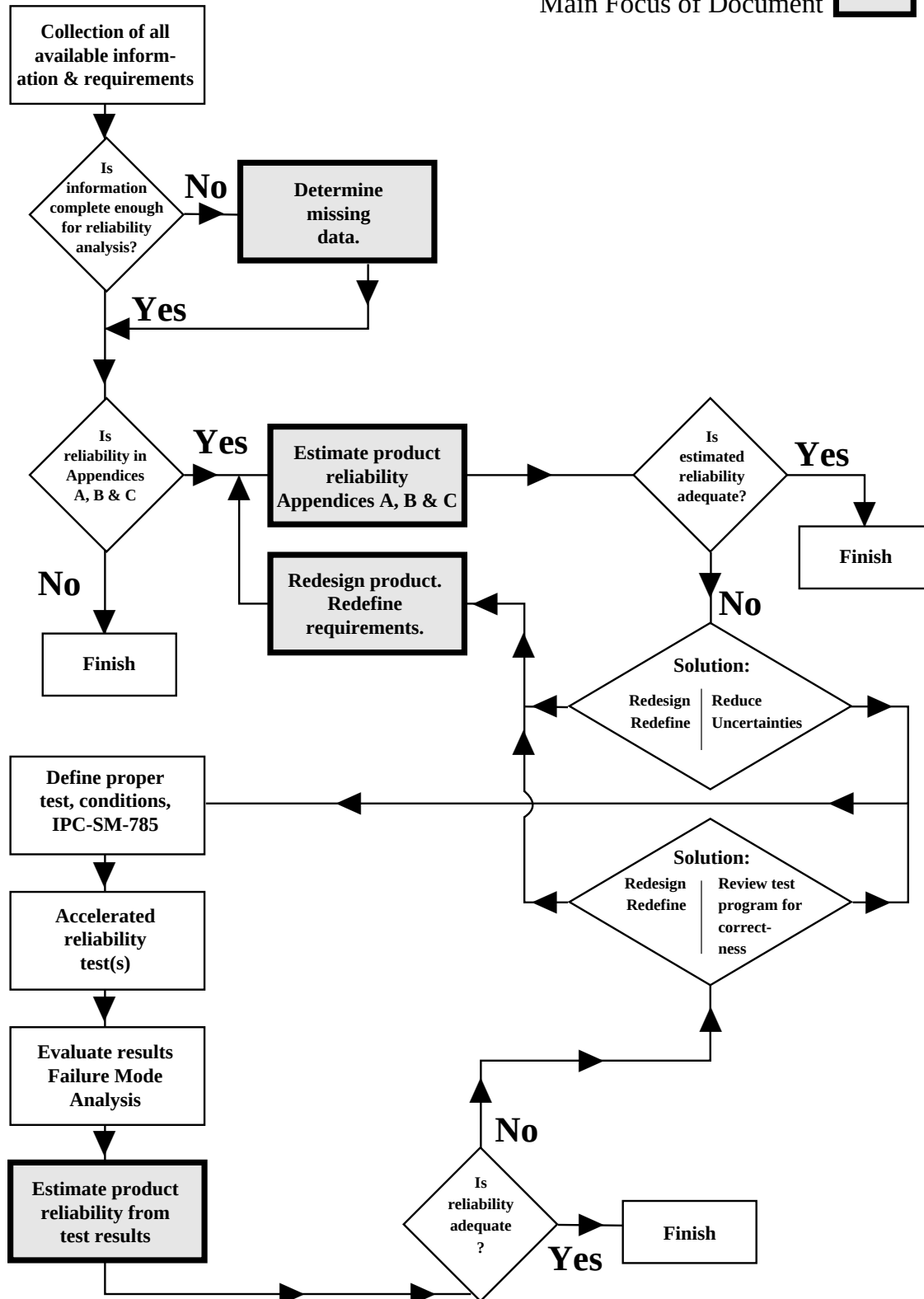
Figure 1-1 General Design Steps

1.3.7 Testing Section 8.0 details the various testing strategies, their purposes and their impact on reliability. Also discussed are design for testability considerations. Checklists for DfT from various sources are provided in Appendix J.

1.4 Terms and Definitions Terms and definitions used here are in accordance with IPC-T-50, and IPC-SM-785 except as otherwise specified.

Flow Chart for Reliability Assurance Processes

Main Focus of Document



IPC-279-02

Figure 1-2 Flow Chart for Reliability Assurance Processes

2.0 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the date of issuance of this specification, form a part of this specification to the extent specified herein. Subsequent issues of, or amendments to, these documents may become a part of this specification.

2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-275 Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies

IPC-TR-476 How to Prevent Electrically Induced Failures (Electromigration) in Printed Wiring Board Assemblies

IPC-TM-650 Test Methods Manual

2.6.20 Assessment of Plastic Surface Mount Components for Susceptibility to Moisture Induced Damage

IPC-ET-652 Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards

IPC-PE-740 Troubleshooting guide for Printed Board Manufacture and Assembly

IPC-SM-782 Surface Mount Design and Land Pattern Standard

IPC-SM-785 Guidelines for Accelerated Surface Mount Solder Attachment Reliability Testing

IPC-SM-786 Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs

IPC-SM-816 SMT Process Guideline and Checklist

2.2 Electronic Industries Association²

EIA-541 Packaging Material Standards for ESD Sensitive Items

EIA-583 Packaging Material Standards for Moisture Sensitive Items

EIA-625 Requirements for Handling Electrostatic Discharge Sensitive (ESD) Devices

JESD 22-A112 Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices

JESD 22-A113 Preconditioning Procedures of Plastic Surface Mount Devices Prior to Reliability Testing

JESD 42 Requirements for Handling Electrostatic-Discharge Sensitive (ESDS) Devices

JEP113 Symbol and Labels for Moisture Sensitive Devices

2.3 Joint Industry Standards

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-004 Requirements for Soldering Fluxes

3.0 DESIGN FOR RELIABILITY FOR SURFACE MOUNT ASSEMBLIES

During the initial design stages of any project, a full knowledge of the product requirements must be understood. These requirements include the life cycle environment, printed board design constraints, thermal effects, serviceability, and all aspects of reliability. This section reviews these considerations and the effects caused by each. The design details for DfR are discussed in Appendices A, B, and C.

3.1 Life Cycle Environment The environmental influences that determine the reliability of surface mount assemblies have to include all environments from manufacture to the end of the design life. These life cycle environments include manufacturing processes, burn-in and/or ESS procedures, transport, storage and use conditions.

Depending upon the product application, any of the life cycle environment periods may have an overwhelming effect on the product reliability. The effects of all these life cycle environment periods can accumulate and need to be summed together using the Palmgren-Miner's rule. (See Equations #9 through #11 in Appendix A)

3.1.1 Manufacturing Processes Many manufacturing processes used in Surface Mount Assembly require changes in temperature. The most severe of these are processes requiring the melting of solder. These processes can affect PTH and PTVs, solder attachments, components and printed boards. Other processes include bake-out of printed boards, curing of adhesives, and curing of polymeric coatings.

3.1.2 Processing Temperature Excursions During processing and assembly of electronic assemblies, temperature excursions, particularly during solder reflow and repair, cleaning, or imposed thermal cyclic testing, take place that are damaging to some parts of the assemblies and consume part of the available life. These thermal excursions can cause fractures in the PTVs of the multilayer printed board.

1. IPC, 2215 Sanders Road, Northbrook, IL 60062-6135.

2. Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.

Table 3-1 Realistic Representative⁽¹⁾ Use Environments, Service Lives, and Acceptable Failure Probabilities for Surface Mounted Electronics Attachments by Use Categories

Worst-Case Environment							
Use Category	Tmin °C	Tmax °C	$\Delta T^{(2)}$ °C	Dwell Time t_D hrs	Cycles/Year	Typical Years of Service	Accept. Failure Risk ⁽³⁾ , %
Consumer	0	+60	35	12	365	1-3	~1
Computers	+15	+60	20	2	1460	~5	~0.1
Telecom	-40	+85	35	12	365	7-20	~0.01
Commercial Aircraft	-55	+95	20	12	365	~20	~0.001
Industrial and Automotive Passenger Compartment	-55	+96	20	12	185	~10	~0.1
			&40	12	100		
			&60	12	60		
			&80	12	20		
Military Grounds and Ship	-55	+95	40	12	100	~10	~0.1
			&60	12	265		
Space leo geo	-55	+95	3 to 100	1	8760	5-30	~0.001
				12	365		
Military Avionics c Maintenance	-55	+95	40	2	365	~10	~0.01
			60	2	365		
			80	2	365		
			&20	1	365		
Automotive under hood	-55	+125	60	1	1000	~5	~0.1
			&100	1	300		
			&140	2	40		

& = in addition

1 Does not cover all possible use environments, but only most common.

2 ΔT represents the maximum temperature swing, but does not include power dissipation effects for components; for reliability estimations the actual local temperature swings for components and substrate, including power dissipation should be used.

3 The 'Acceptable Failure Risk' is the percentage of product in the field that has failed, due to wearout mechanisms, at the end of the 'Typical Years of Service.'

This damage should be minimized by keeping the number of excursions to a minimum; and the damage needs to be considered in the overall reliability estimates for the assemblies. See IPC-PE-740 for trouble-shooting information.

3.1.3 Burn-In and Environmental Stress Screening (ESS) Burn-in tests and ESS have the potential of identifying latent defects that may cause early failures in product, but they also have a negative impact on the good assemblies. The degree of the detrimental impact on reliability depends on the severity of the burn-in and/or ESS procedures.

Burn-in testing generally should be a complete environmental test involving perhaps worst case but still realistic operational environments.

ESS should never be employed routinely. ESS needs to be specifically designed to cause the failure of "weak" elements in the assemblies for which a strong suspicion of processing defects exists.

The assembly elements that are typically most affected by these procedures are the surface mount solder attachments. The effect of extended solder joint temperature cycling can use up a significant amount of solder joint life.

3.1.4 Transport While transport conditions like vibra-

tion, mechanical shock and moisture are routinely considered and accommodated, little is done about the thermal conditions. Electronic product can sit on loading docks or in warehouses, or be in cargo holds of ships, airplanes and/or trucks, in temperatures ranging from -40 to +70°C.

For some applications, e.g. medical implants, these transport conditions would be significantly more severe than the operational environments.

3.1.5 Storage For some product applications, the environmental conditions during storage become significant in the total life cycle environment. In particular, military applications, such as munitions (proximity fuses, etc.), and space applications can require long storage periods, frequently in uncontrolled environments, before final use.

The user should consult with the vendor to determine the shelf life and special storage conditions.

3.1.6 Use Environments The use environments are highly dependent upon the product application. In Table 3-1, typical worst case use environments for 9 product categories are given. These use environments should be regarded as guidelines only; the actual use environment as well as the environmental conditions of the SM assembly being designed may be significantly different.

3.1.7 Environmental Stresses The operating life of a surface mounted assembly is dependent upon a number of factors which include intended usage, usage environments, strength of the materials and components to withstand the stresses imposed by the usage and the environments, material (variables), etc. In a surface mounted assembly, the most critical element from the life cycle viewpoint are the solder joints and PTVs. Cyclic (or fatigue) displacements experienced during various phases of the product's life cycle are responsible for consumption of useful life of material elements.

One of the major contributors to the cyclic loading is thermal cycling due to the internal power cycling and external environmental changes. Another important contributor is vibration during the operational use, transportation, handling, etc. An estimate of the fatigue life of the solder assembly that will be consumed by these fatigue cycles during the product's life cycle can be obtained by performing a cumulative damage analysis.

It should be noted that the cumulative damage analysis requires the knowledge of fatigue characteristics of the materials involved. Also, a thorough understanding of how the product will be used, handled and maintained, by the user and under what environments, is necessary. See Appendix E.

3.1.8 Temperature/Thermal Temperature is one of the most important parameters in the use environment that must be considered in the SM PWA design process. Temperature history is the most significant parameter affecting the reliability of SM solder joints. For some product applications, the use environment consumes the most significant portions of the required fatigue life; this is typically the case where the product development cycle includes producing a prototype prior to the "final build."

Therefore, DfR depends to a large extent on the thermal design for the assembly, as well as the external thermal environment. Temperature is also important, since many materials in electronic assemblies have properties which change significantly with temperature.

3.1.9 Cyclic Temperature Swings Cyclic thermal excursions, ΔT , cause thermal expansion mismatches due to different parts of the assemblies having materials with different CTEs and/or being at different temperatures. Thus, the size of the cyclic temperature swing is proportional to the resulting loading. The larger the ΔT , the larger the threat to reliability.

During cyclic temperature excursions, these cycles can have different profiles, e.g., sinusoidal, trapezoidal, sawtooth, square-wave, etc. These differences are important in understanding time-dependent and rate-dependent processes. The transient parts of the profile give the ramping

rates of the temperature change which can cause transient temperature gradients and over-stress conditions. The steady-state, or near steady-state, parts of the profile determine the duration of the temperature dwells which are important for time-dependent processes like creep and stress relaxation.

3.1.10 Thermal Shock In thermal shock, the extremely rapid temperature changes ($\sim 30^\circ\text{C}/\text{minute}$ and above) result in warping of the surface mount assembly. The warpage is caused by large transient thermal gradients induced by the rapid temperature change when the boards are plunged into a new thermal environment. The warpages result in tensile and shear stresses where the tensile loading dominates over the steady state expansion mismatch. Thus, even assemblies with matched coefficients of thermal expansion will exhibit solder joint failures when subjected to thermal shock. The thermal shock loading mechanism is summarized in Figure 3-1.

Thermal shock conditions can arise from several sources. Examples of these are:

- 1) Rapid changes in external environment, e.g., sun-to-shade in space, missile launch, wing-mounted avionics, automobile start-up from very cold.
- 2) Rapid changes in power dissipation.
- 3) Various manufacturing/repair processes, e.g., reflow, vapor degrease, rework, etc.

The distinction between thermal shock and thermal cycling is not always addressed in designing reliability experiments. There is a fundamental difference between thermal shock and thermal cycling. The primary differences arise from the mechanism of loading. Thermal shock tends to result in multiaxial states of stress dominated by tensile overstresses and tensile fatigue. On the other hand, as previously discussed, thermal cycling results in shear loads and failure occurs from an interaction of shear fatigue and stress relaxation.

Thermal shock is usually performed in dual chamber arrangements or with liquid nitrogen injection whereas thermal cycling is performed in single chamber cycling equipment. Dual chamber arrangements will produce temperature transition rates in excess of $50^\circ\text{C}/\text{minute}$.

Single chambers generally do not produce transition rates even close to $30^\circ\text{C}/\text{minute}$ which is the rate necessary to induce thermal shock. The results of these two types of testing are generally incompatible. Finally, thermal shock testing for purposes of evaluating surface mount solder joint reliability is only appropriate if thermal shock is indeed a field condition encountered by the product.

In some specifications, the definitions of thermal cycling and thermal shock are not fully differentiated; the rates of change are more closely associated with what we are calling thermal shock.



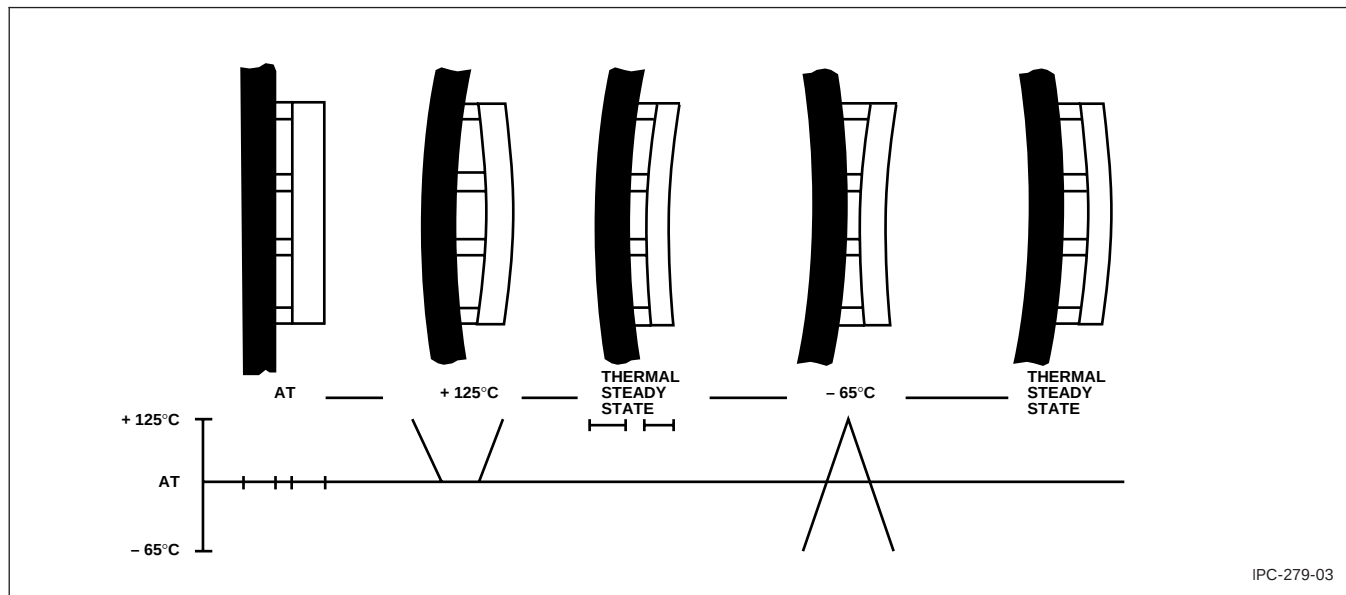


Figure 3-1 SMT Assembly Response to Thermal Shock

3.1.11 Electrical

3.1.11.1 ESD Susceptibility and Damage Prevention

All electronic components containing thin conducting or insulating films are susceptible to electrostatic discharge (ESD) damage. These components include those fabricated in high speed technologies (MOS, bipolar, GaAs), thin film technologies (resistors, integrated circuits, magnetic heads, MOS capacitors), and in future, wafer scale integration and multichip modules.

3.1.12 EMC/EMI The electromagnetic spectrum is usually divided into categories ranging from the long-wavelength radiation from power lines through radio, infrared, visible, ultraviolet, and x-rays, to gamma rays at the short-wave end. All electromagnetic waves consist of an electric field and a magnetic field. The relative magnitude of these fields depend on the emitter (EM source), wave propagation medium, and the proximity of the emitter to the subject assembly.

Many electronic circuits are susceptible to electromagnetic radiation and must be shielded to ensure proper operation. One of the most important effects of the electromagnetic radiation in the environment is electromagnetic interference (EMI). EMI is the electro-magnetic disturbances that impair the desired signal. In practice, EMI is often divided into two categories: conducted EMI and radiated EMI. Conducted EMI is an interfering signal resulting from an undesirable voltage or current coupled into a signal or other pertinent conductor. Radiated EMI is an interfering signal resulting from an electric and/or magnetic field amplitude and frequency spectra intentionally or unintentionally radiated by an electrical source. Examples of radiated emission sources are radio and TV transmitters, light-

ning, digital system noise from electronic control systems, etc. In military applications, an important effect is the interaction of electromagnetic radiation with electroexplosive devices used as detonators. Improper EMI could accidentally initiate the explosion.

EMC is the ability of electronic systems to operate in the intended electromagnetic environment at designed levels of performance and efficiency. The most direct approach to protection is, in most cases, to avoid the limited region in which high radiation levels are found. When exposure cannot be avoided, shielding is the important protective measure. The material selected for shielding can be an important factor. Ideal materials include steel, copper and nickel coating. In the design process, apertures for cooling ventilation and cable connections on the shielding box should be properly designed so that the EMI will have no influence inside the shielded space.

3.1.13 Mechanical Shock and Vibration Shock and vibration are common accelerators of failure in electronic packaging. The most frequent vibration-induced failures in surface mount are:

1. Flexing of leads and interconnects.
2. Dislodging or damaging of parts and structures.

Methods have been developed to counter the destructive effects of shock and vibration. Generally, isolation of a printed board against the effects of shock and vibration requires that the natural frequency of the printed board be substantially lower than the undesired frequency of vibration to avoid the resonance.

The basic system level isolators available are:

1. Natural or synthetic rubber, used to damp the vibration.



2. Metallic isolators including springs, metal meshes or wire rope; the latter provide smooth friction damping.

There are also other isolators such as viscous dampers which are velocity-sensitive. For high-frequency vibration, viscous dampers tend to become ineffective.

There are two approaches that may be taken when shock and vibration are present: either isolate the printed board or design it to withstand the shock and vibration. Studies have shown that the ideal goal is to design equipment to be resistant to shock and vibration, rather than to isolate it from these forces.

Because the surface mount components are generally smaller compared to the through-hole counterparts, they are more vibration resistant due to the lower inertia. As the PWA vibrates, the components mounted on the board are subject to stress from two different effects. First, the mass of the components is subjected to an acceleration that produces a force. The body of the component is kept in equilibrium with reactive forces developed in the leads. Second, the printed board flexes, which tends to bend the leads back and forth at their joints with the board. Because of the shorter lead lengths in SMT, the mechanical stress induced by shock and vibration in leads is considerably smaller compared to that in through-hole leads.

To detect/precipitate the flaws, stress screening with random vibration should be performed. Usually, stress screening should be designed so that it causes minimal damage to properly designed printed boards. This requires careful determination of the screening intensity.

Depending upon the applications, the frequency ranges are very different. For instance, the range for submarine electronic equipment is about 4-34 Hz, but for avionics the range is 15-2000 Hz.

The following considerations must be included in the analysis design for shock and vibration:

1. The location of the surface mount components relative to the supporting structure (i.e., edge, corner, or center of the supporting structure).
2. The orientation of the components with respect to the anticipated direction of the shock or vibration forces.
3. The maximum deflection of the printed board.

Mechanical shock to, and flexure of, a SM Printed Wiring Assembly can occur during its life cycle. Each incident could be characterized by the energy to be absorbed by the assembly, the shock peak amplitude, duration and time rate of change for correlation to sample shock testing:

- PWA struck by tooling during assembly (component insertion or placement, riveting, testing, test fixtures, probing, or depanelling)
- PWA installed into a card carrier or motherboard
- PWA dropped on a hard bench or floor

- Assembly dropped on a hard bench or floor
- Boxed product bounced and jolted during transportation
- Boxed product dropped on a hard bench, floor, truck bed
- Product (in use) dropped on a hard work surface or floor
- Product (in use) struck by passing equipment
- Product stored in racks, PWA fixtures, or rework station grips.
- PWA subjected to combined environmental stress in field use.

The assessment of the potential quality/reliability degradation of a printed wiring assembly (PWA) resulting from exposure to the use environment cannot always be determined by considering each environmental stress in isolation. For instance, consider the non-linear combined effects of severe thermal and vibration stress application. A given magnitude of random vibration at elevated temperature (near or above T_g) may produce increased PWA flexure because of increased board softness or flexibility. Simultaneously, solder joint pull strength is decreased at the elevated temperature. The result may be overload, that is, a PWA configuration for either the elevated temperature or the vibration applied at room ambient temperatures may fail prematurely in service when exposed to the two factors together. Board stiffness and damping as discussed in section 4.0 are key factors to be considered. The adequacy of a proposed design may require combined-environment stress testing of prototypes prior to full-scale production. See also the references by Steinberg and Engel regarding vibration, shock and thermomechanical effects on PWA, section 9.16.

3.1.14 Insulation Resistance

The emerging advanced technologies are characterized by denser packaging resulting in ever finer conductor line widths and spacings. Without changes in the material and the operating environment, which for economic and practical reasons are not likely, finer lines and spacings result in reduced insulation resistance and increased threat of CAF (conductive anodic filament) formation. The DfR principles listed in Appendix C need to be kept in mind in the design and application of these emerging technologies.

The damage mechanisms work generally in two distinct regions: at the surface and in the bulk of the electronic assemblies, particularly the printed board. The measured insulation resistance will depend upon the nature of the laminate, solder mask and/or conformal coating under investigation. It will also depend upon the degree of cure of the polymers and for printed boards on the quality of the drilling process for the plated-through holes (PTHs) and vias (PTVs), and will be affected by the curing process.

residues if they dissolve into the polymeric material during the soldering and/or cleaning processes.

3.1.15 Solvent Compatibility Surface Mount printed wiring Assemblies (PWA) are subjected to solvents (including water) and chemicals during manufacture, rework, repair and service. These agents include those used in soldering (alcohols, glycols and other solvents in flux vehicles at temperatures approaching 150°C), in cleaning the assembly after solder (saponifiers, neutralizers, hot water, terpene, mixtures, hydrochlorofluorocarbon (HCFC) mixtures and other halogenated solvents and blends at moderate process temperatures), during removal of conformal coatings with various chemicals, and during service (hydraulic and cooling fluids and fuels in military applications; alcohols and halogenated hydrocarbons during cleanup). These solvents and chemicals can adversely affect the solder mask (SM), printed wiring board, conformal coating, printed board or component legends and markings as well as degrade thin or mechanically stressed sections of plastic components. See Appendix I.

3.1.16 Corrosion The result of corrosion is material loss of the metallic conductors, permanent or intermittent continuity loss due to build up of non-conductive corrosion residues (particularly between contacts) and permanent or intermittent shorts due to build up of conductive corrosion residues and conductive metal dendrites. Corrosion accelerates the failure of components under cyclic fatigue conditions.

The oxides of tin, nickel and copper are not good conductors. Low interfacial pressure contacts to these metals can become resistive or intermittent. See Appendix L for details.

3.1.17 External Radiation External radiation typically includes X-Rays, β -particles and cosmic rays. It affects the semi-conductor material through the generation of hole-electron pairs in the bulk of the device. The purpose of understanding the radiation effects is to enable the development of radiation-hardened devices.

External radiation affects the different semiconductor devices in different ways. For instance in bipolar types, radiation causes an increase in low-frequency noise, high leakage current across the p-n junctions, and a reduction in current gain; in MOS types, a threshold voltage shift, a reduction in transconductance and an activation of parasitic elements are observed. See Appendix E.

3.1.18 Space Environment The space environment presents an unusual set of conditions which requires careful evaluation (low air pressure, low gravity, low temperature and radiation). See Appendix O.

3.2 Thermal Design The primary thermal parameter

which the designer must address is the temperature of the junction or active film of the component; both the absolute maximum or peak temperature and the steady state operating temperature limits imposed by the component manufacturer (as modified by derating protocols) must be observed. The secondary thermal parameter is the solder joint temperature since long service times at high temperatures will result in grain growth in the solder, growth of the intermetallic compound layers; and large temperature swings in service will subject the joint to conditions leading to cyclic fatigue. See Appendix D for details.

Variation of the external (outside of the equipment enclosure) ambient temperature is one of the multitude of factors that will determine the actual temperature cycle a specific surface mounted device will see in operation. Very simple equipment, powered continuously at constant power will see the same temperature swings as the external ambient. In some cases, the system designer introduces built-in means of reducing the temperature swing inside the cabinet, such as fans activated when the inlet air temperature exceeds certain limits or inlet air heaters which are activated when inlet air temperature drops below certain limits.

In many applications, the variation of the temperature inside the electronic enclosure is generated by variations of the power dissipated by the electronics itself. Examples of this type of behavior are on/off periods for the systems, and fluctuations in the power dissipation as in telecommunication equipment due to variations in the number of simultaneous calls passing through the system.

It follows that different devices inside the same system might be subjected to very different temperature cycles. In order to assess the reliability of the solder joints, the designer must perform a complete thermal analysis at the device level.

In most applications, the temperature variations at a particular component in a system result from a combination of system-external and system-internal temperature variations combined with power dissipation fluctuations within the component.

3.3 Printed Board Design and Layout The printed board design and layout task, particularly for surface mount technology (SMT), has become more difficult and complex.

The difficulty of SMT designs has increased with the increase in conductor density as a result of decreases in termination pitch, conductor width and conductor spacing. The complexity of SMT designs has increased with the need to consider:

- a) thermo-mechanical effects such as solder joint reliability (see section 3.4, 3.6 and Appendix A)
- b) testability and inspectability (see section 3.5 and Appendix B)

- Appendix J) to reduce evaluation time and cost
- c) corrosion avoidance - pertinent cleaning, component clearance and conductor spacing issues (see Appendices E, L and N and section 7.5, 7.8)
 - d) control of electrical transients which become more severe with the increased speeds and power density of SMT designs. (See section 3.1 and Appendix E and the issues of increase in "ground bounce" and signal reflection noise.)
 - e) thermal design and control of the critical junction and solder joint temperatures (see section 3.2 and Appendices A, B, D and E)
 - f) manufacturability for high yield/quality assemblies (see section 7.8 and Appendix K) including orientation, solder thieves
 - g) ESD susceptibility mitigation of components through a combination of layout and software. (See Appendix H)
 - h) Component placement and orientation for enhanced robustness to flexing, vibration and shock during the assembly process as well as in the use environment. (See Appendix E) The significant IPC document for this section is IPC-SM-782
 - i) the impact of the limited heat transfer available from solder joint to internal heat "sinks."

3.3.1 Thermal Design and Layout Where there are thermally sensitive components, heat dissipaters should generally be "downstream" in the air flow. Under certain conditions of PWA geometry, component orientation and relative component heights, turbulence may result in "recirculation cells" conveying heat "upstream."

3.3.2 Thermal Design and Conformal Coating Reduced heat extraction from the PWA (and increased junction temperatures) may result if conformal coating covers heat conduction surfaces on the PWA edge or margin which mate with heat sinks such as card-edge clamps and cold plates. (See Appendix D)

3.3.3 Land Patterns Surface land patterns define the sites where the components are to be soldered to the printed wiring board. The design of land patterns is very critical because it is the land pattern that not only determines the solder joint strength and hence the reliability of solder joints but also impacts the solder defects, cleanability, testability, and repair/rework. The very producibility or the success of the printed board is dependent upon the land pattern design.

There are certain general guidelines that one should develop to cope with the variations in tolerances of components. The selected vendor's components must pass all package qualification requirements. Standardization of

parts reduces the tolerances that the land pattern design will have to support.

A second desirable requirement is that the land pattern design be transparent to the soldering process to be used in manufacturing. This will not only reduce the number of land sizes in the CAD library but it will also be less confusing for the CAD designer.

3.3.4 Balance About Neutral Axis Balanced conductor plane distribution about the neutral axis results in a SM printed board which does not "potato-chip" during the high temperature exposures and results in reduced mechanical stress on component bodies and on solder joints.

3.3.5 Vias Via holes are used to connect surface mounted component lands to conductor layers. They may also be used as test targets for bed-of-nails type probes and/or rework ports. Via holes may be tented if they are not required for node testing or rework. When a via is used as a test point it is required that the location of a test land be found to match the standard grid of the test fixture.

Buried Via A plated-through hole connected to neither the primary side nor the secondary side of a multilayer packaging and interconnecting structure; i.e., it connects only internal layers.

Blind Via A plated-through hole connected to either the primary side or the secondary side and one or more internal layers of a multilayer packaging and interconnecting structure.

IPC-TR-579 noted possible reliability problems for PTVs with small diameters and/or large printed board thicknesses. Copper plating quality in the barrel was found to be a significant parameter; nickel over plating in the barrel increases the robustness of the PTV to temperature cycling.

Use of blind and buried vias can result in effective aspect ratios (AR) much lower than the AR of PTVs in the same substrate with the same diameter. See section 3.6.

Open or untented PTVs (no solder mask on either side of the printed board) can allow liquid flux to be trapped with potential for corrosion, reducing SIR, contaminating test fixtures and causing electrochemical corrosion. (See IPC-D-275) If solder mask is intended to plug or tent these holes, it must do it consistently. Another method to prevent flux from being trapped in these vias is to plug them with solder (which wave soldering does automatically).

3.3.6 Printed Board Trace Widths and Spaces Minimum trace widths should be reviewed keeping in mind the influence of etching tolerances, undercutting, "Mouse-bites," and plated grain size as well as the possibility for electromigration due to current density. The design of

subsequent conductor temperature rise.

Minimum trace spacings should be reviewed keeping in mind the influences of DC voltage and possible electrochemical migration, AC voltage and possible corona leakage currents, high humidity and possible electrochemical migration, low air pressure and possible corona leakage currents/premature voltage breakdown, and conductive or corrosive contamination from the ambient. See IPC-D-275, IPC-SM-782, and IPC-TR-476 and IEC 664.

3.3.7 PTH and PTV Thermal Isolation/Relief Large conductor areas such as ground planes, power planes and thermal planes “heatsink” PTH and PTVs to which they connect. During the soldering or reflow process, the reduction in local temperature can result in “cold” solder joints, bridging or icicling and may require increased time at temperature to affect a proper and reliable solder joint. Thermal relief inner lands such as those depicted in Figure 3-2 provide a measure of thermal resistance between the external soldered lands and the heatsinking plane. The results are lower required reflow temperatures, less printed board stress, and more consistent solder joints.

exercised due to test equipment limitations or lack of available test time; Built-in-Test-Equipment, Built-in-Test, Built-in-Self-Test (BITE, BIT or BIST) capabilities could be invaluable in these circumstances or may be the only alternatives. See section 8 and Appendix J.

Solder mask overlap or residue on test pads (whether by design or by loss of process control) reduces test reliability. (See IPC-D-275, and IPC-SM-782)

Provide adequate margin between the land and solder mask.

Conformal coating on test pads results in diminished test accessibility; testability buss methodologies and structures may be required to permit effective and efficient fault coverage. (See IPC-SM-782)

3.3.9 Spacing Between Parts The designer should provide for manufacturability, inspectability, testability and repairability of SMT assemblies. A minimum interpackage spacing is required to satisfy all these manufacturing requirements. Some designs require that surface mount components be positioned as tightly as possible (brick-

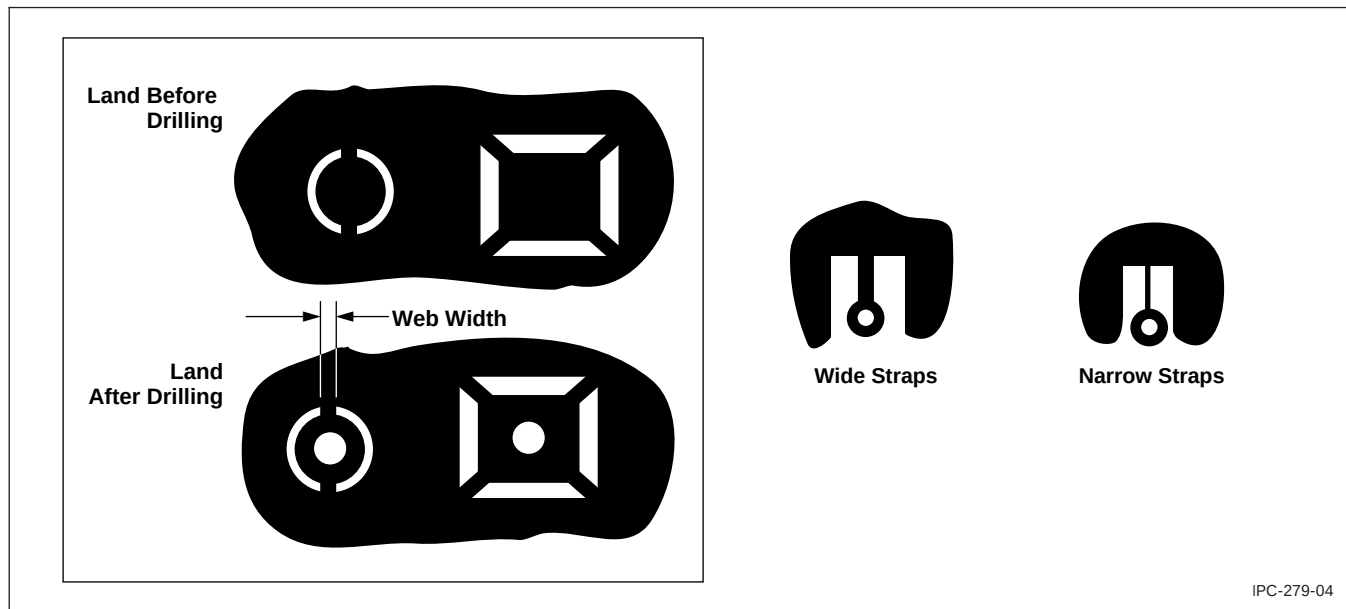


Figure 3-2 Thermal Relief in Ground Planes

3.3.8 Test Pads Test pads are required for bare-board test; see also IPC-ET-652. Previous techniques used to implement digital PWA testability such as massive addition of test nodes, become less feasible with the smaller dimensions of SMT PWAs and the number of test nodes required for components with 100-400 terminations; the mechanical force exerted by test pins is sufficient to flex and break components and solder joints.

Testability is a particular issue for field repair activities where the full capabilities of the SM PWA may not be

walled); these designs do not allow solder joint inspection. See figure 3-3 and section 8.0.

3.3.10 “Pads-Only” Design For this reason, many multilayer military and space applications utilize a “pads-only” outer layer design. By submerging all conductors and power planes in the inner-layers, only the land areas are exposed on the board surface. Connection to the sub-layers is then accomplished by small plated and filled vias

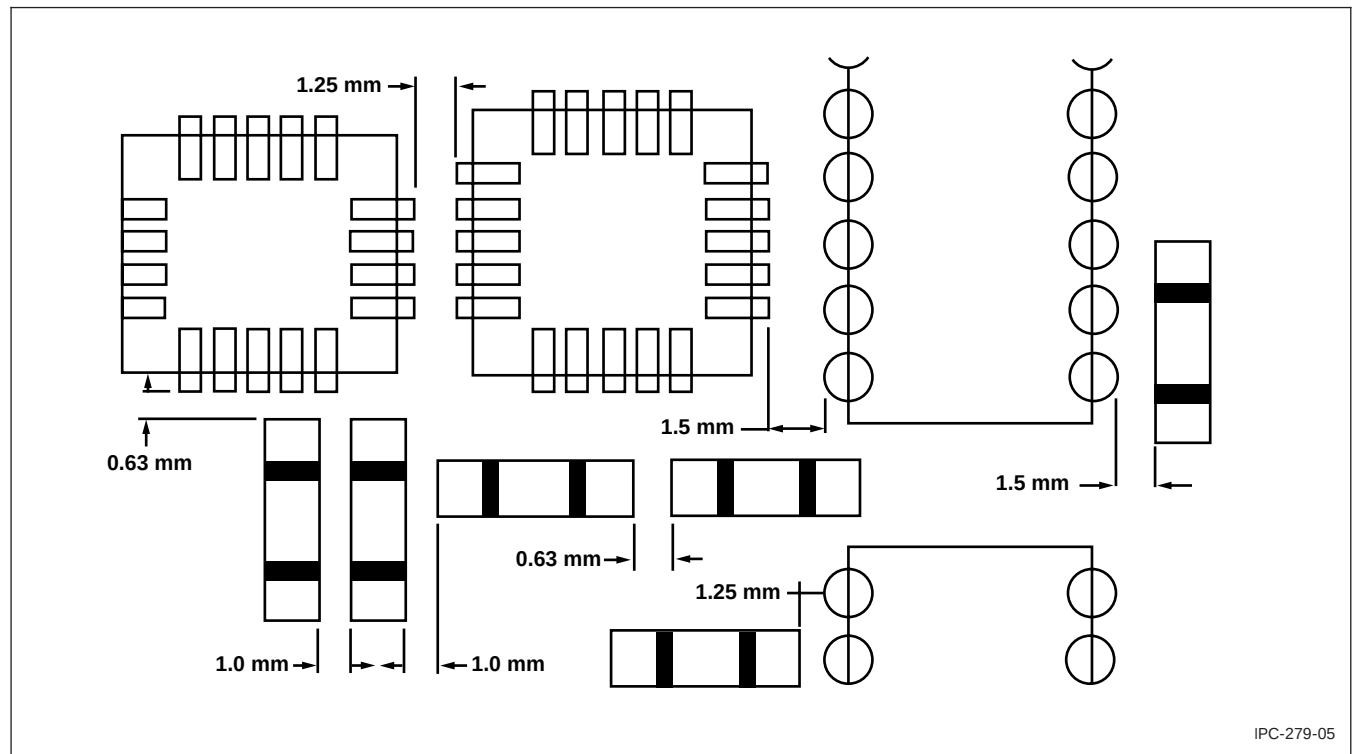


Figure 3-3 Spacing Between Parts

inside the land area. If a “pads-only” approach is not feasible, then it is crucial that solder mask be applied for surface mount designs to act as a dam to solder migration.

The “pads-only” approach has several advantages worth noting:

- the construction is compatible with soldering processes, conformal coatings and common cleaning solvents.
- The electrical and dielectric performance is no different than the remainder of the P/I structure. Stenciling of solder paste is improved.
- Application of solder mask to flexible and flex-rigid P/I structures may be difficult.
- Resolution of this approach is the same as the resolution of copper etching.

3.3.11 Components with Reduced Clearances (Traces Under) Excessively thick solder mask, particularly dry film over traces under components with small clearance, can contribute to the formation of crevices which entrap flux. In the case where the solder mask touches the bottom of the component, if insufficient solder paste is used, it may result in chip component draw-bridging (tombstoning), insufficient solder fillet or lack of solder joint. (See IPC-SM-782 and IPC-D-275.)

3.3.12 Components with Reduced Clearance and Open Vias Components with reduced clearance should not be over open vias, particularly if wave soldering is used. The

vias allow flux up under the component to be entrapped in the reduced clearance space.

Heat dissipaters should generally be “upstream” of tall components to avoid recirculation cells.

Where lower junction temperature T_j is required, consider the following avenues particularly applicable to SMT: thermal vias, thermally conductive adhesives from component to printed board, and power and ground planes included in the thermal design. In addition, consider the following moves: sensitive components “upstream” of power dissipaters, power dissipaters further apart to reduce power density, power dissipaters closer to cold wall (edge of card if card clamps are used), and power dissipaters “upstream” of tall components.

Long, tall components such as connectors are ideally placed parallel to the airflow. Placement of these components perpendicular to the airflow results in the generation of recirculation cells which reduce the heat transfer from heat dissipaters or which increase heat transfer to heat sensitive components.

3.4 Coefficient of Thermal Expansion (CTE) and CTE-Mismatch Electronic assemblies consist of a multitude of elements of different materials. These materials have different coefficients of thermal expansion (CTE), of which some are listed in Appendix G. Some CTEs also vary with temperature. Because of external temperature variations and internal heat generation and different thermal expansion

different locations within an electronic assembly are typically at different temperatures.

Matching the CTEs at a joint is no guarantee of freedom from the problem because electronic components are their own heat sources and because there is a temperature difference between component and substrate. The problem is directly related to the size of the component, the thickness of the solder joint and the compliance of the lead. The major problem arises from thermally induced cyclic stress in the solder joint of the leadless ceramic chip carrier (LLCCC) components. Some components are very easy to assemble, test and repair; others are not. The availability of a component, its performance data, its degree of testability, its reliability and its compatibility with manufacturing and assembly processes and equipment influences component selection.

3.5 Solder Joint Reliability The reliability of the surface mount solder attachment of components to the printed circuit boards depends on a number of different parameters. Some of these parameters are under the direct control of the designer, some can be influenced by the designer, and some are beyond the control of the designer.

Also, some of these parameters have a very strong influence on reliability. Relatively small changes or inaccuracies in these primary parameters have a large impact on the reliability. The impact of these parameters can be seen from the reliability prediction Equations A-3 and A-4 in Appendix A, Solder Joint Reliability.

3.5.1 Primary Design Parameters The following are design parameters that have been identified as having a primary (order of magnitude) influence on SM solder attachment fatigue reliability.

3.5.1.1 Component Size The physical size of the component determines the amount of displacement a solder joint experiences during thermal expansion/contraction of the component and the substrate to which it is soldered. Larger components are larger threats to reliability. The component size is determined by the number of I/Os and the pitch.

3.5.1.2 Attachment Type The choice of attachment type (leadless or leaded) determines the maximum stress level that can be experienced in a solder joint during thermal cycling. The stiff leadless attachments typically stress the solder beyond the yield strength, whereas compliant leaded attachments typically do not. This choice determines the reliability model that needs to be applied and affects the statistical failure distribution (Weibull slope). Leaded attachments provide larger reliability margins, which increase with decreasing lead stiffness. It needs to be noted that lead compliance can vary greatly depending on the

lead geometry. Lead stiffnesses as high as 1100 N/mm for SM connector header leads and as low as 1.5 N/mm for fine-pitch S-leads have been determined.

3.5.1.3 Solder Joint Height The solder joint height determines the strain level experienced in the solder joint for a given component/substrate displacement. It results from the solder-filled gap between the component metallization or component lead and the substrate pad. Higher solder columns reduce the strains in the solder joints and increase reliability. Solder joint height is not the height of the fillet. For leaded attachments the solder joint height is not a measurable quantity; it has been defined in terms of the solder paste stencil thickness.

3.5.1.4 Solder Joint Area Solder joint area determines the stresses in a solder joint resulting from a given component/substrate displacement. It is of importance primarily for compliant leaded attachments. Larger solder joint areas reduce the applied stresses and increase reliability; however, the possible range of effective increase in area is very limited.

3.5.1.5 Lead Stiffness The lead stiffness determines the forces resulting from a given component/substrate displacement. Because the corner solder joints experience the largest displacements and the displacements are in the direction of the component center (neutral point), it is the diagonal lead stiffness which is of primary importance. Lower lead stiffness results in increased reliability.

3.5.1.6 Coefficient of Thermal Expansion The linear coefficient of thermal expansion (CTE or α) represents the change in linear dimension of a material due to a change in its temperature. Components and substrates consist typically of a variety of materials all having different CTEs; the effective CTEs are a combination of the individual material CTEs and typically are different in different directions of components and substrates. CTEs need to be measured to avoid possible large errors in the reliability predictions. See Appendix G for CTE values of different materials.

3.5.1.7 CTE - Mismatch The CTE-mismatch (ΔCTE or $\Delta\alpha$) is the difference between the coefficients of thermal expansion (CTE) of two materials or parts joined together; in most instances it is the CTE-mismatch between component and substrate, the global expansion mismatch, that is most important, while the CTE-mismatch between the solder and the materials to which it is bonded (ceramic, alloy 42, Kovar), the local expansion mismatch, plays a smaller, but not negligible role. In some designs (ceramic component on ceramic or silicone substrate), this local CTE-mismatch assumes primary importance. Large CTE mismatches pose large reliability threats; the effect of power dissipation within the component makes CTE-mismatching

the optimum solution (see A-2.3 and A-3.6 for explanations).

3.5.1.8 Cyclic Temperature Swing The cyclic temperature swing (ΔT) of components and substrate is the difference in the maximum and minimum steady-state temperatures experienced during either externally (daily) imposed temperature variations or operationally (on/off, load fluctuations) imposed variations. It needs to be realized that the temperature swing of the components is typically not the same as the temperature swing of the substrate due to the power dissipated in active devices. Smaller ΔT s result in improved reliability. It needs to be noted that for some applications the temperature swings during transport and storage prior to operation can be more severe and a bigger threat to reliability than the operating conditions.

3.5.1.9 Cyclic Expansion Mismatch The cyclic expansion mismatch, $\Delta(\alpha\Delta T)$ results from the difference in the thermal expansion of components and substrate which are determined by the respective thermal expansion coefficients (CTE) and cyclic temperature swings (ΔT). Smaller expansion mismatches result in improved reliability.

3.5.2 Secondary Design Parameters While the effects of secondary design parameters are, by themselves, of second-order importance, their additional contribution to the effects of the first-order parameters can be significant.

The effect of some of these second-order parameters might be different in accelerated testing and actual operational use. The effect of these secondary parameters is indirectly included in the reliability predictions of Equations A-3 and A-4 in Appendix A, Solder Joint Reliability, is the “non-ideal” factor, F. This F-factor is empirically determined.

Design parameters having second-order effects on solder joint reliability are as follows:

3.5.2.1 Solder/Base-Material CTE-Mismatch The large CTE-mismatch ($\Delta\alpha$) between the solder and some base materials (ceramic, Alloy 42, Kovar, silicon) can make substantial contributions to the cyclic fatigue damage (see A-2.3 and A-3.6).

3.5.2.2 Solder Joint Shape/Fillet/Volume Experimental evidence indicates that solder joint shape/fillet/volume have only secondary importance for reliability. In some highly accelerated tests cyclic life improvements of about a factor of two have been achieved, but it is not clear whether even these small benefits would result for the slower conditions prevalent in most product operations. The improvements result from the time necessary for crack propagation through the fillet.

Stress concentrations, e.g. from solder-mask-defined soldering lands for ball grid arrays (BGAs), can reduce the

solder joint fatigue life by as much as a factor of three depending upon the severity of the loading conditions.

3.5.2.3 Solder Joint Uniformity Some experiments in which solder joints were loaded primarily in a stress-driven mode (high cyclic frequencies, no hold times, very large temperature swings with fast transitions) showed the need for extreme uniformity of all the solder joints of a component to avoid unequal stressing; accelerated tests utilizing test conditions more closely resembling product use conditions did not reveal a need for extraordinary solder joint uniformity.

3.5.2.4 Initial Solder Joint Grain Structure A fine initial grain structure in solder joints results in cyclic life improvements of about a factor of two in highly accelerated tests. The grain structure of solder is inherently unstable and will grow with time. Higher temperatures and cyclic loading accelerate the grain growth. Thus, for most product applications a fine initial grain structure will not result in a significant improvement of fatigue life; the solder joints of accelerated test vehicles should be artificially aged to start the tests with more product-related grain structures.

3.5.2.5 Conformal Coating Conformal coating can have different effects on solder joint life during thermal cycling depending on the type of material, thickness, and location. The advantage of conformal coating is that it slows the absorption of water and oxygen into surface cracks. The presence of oxides on the cracked surfaces may accelerate the crack propagation. Oxidation layers prevent “re-welding” of the solder during crack closure.

On the negative side, conformal coating may add another material with a very high thermal coefficient of expansion which may influence reliability. This addition can be significant especially if the coating wicks under components, filling the gap between the printed board and component. In addition, conformal coating can become rigid below the glass transition temperature. This condition can exert considerable stress on the components and solder joints during the thermal cycles.

Because of the large variation in conformal coating material properties, thickness applied, methods of application, etc., the effect of conformal coating, in general, needs to be evaluated empirically for each application.

3.5.2.6 Compliant Substrate Surface Layers Compliant layers at substrate surfaces can provide additional reliability margins, but by themselves are not adequate to counteract the effects of large expansion mismatches.

3.5.2.7 Solder Composition The most widely used solder compositions are eutectic (63/37) and 60/40 tin-lead solder. Solder compositions other than these are used in

somewhat higher or lower fatigue reliability and are, on the whole, significantly less well characterized from a reliability point of view.

3.6 Plated-Through Hole and Via Reliability In surface mounting the plated-through holes (PTHs) have been reduced to the single function of providing electrical connections through the circuit board. Because the PTH-vias (PTVs) no longer need to be able to accept component leads, there is no need for the traditional large PTH diameters. The drive towards higher circuit board densities also has put pressure on designers to reduce PTV diameters. At the same time, the number of layers and, thus, the circuit board thicknesses have been increasing. Therefore, the PTV aspect ratio (the ratio of circuit board thickness and drilled PTV diameter) has been increasing. The results of an IPC round robin study (IPC-TR-579, Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in PWBs) show that for PTVs with aspect ratios (AR) > 3 , special care is necessary to produce high quality PTVs. Copper plating quality in the barrel was found to be a significant parameter; nickel plating in the barrel increases the robustness of the PTV to temperature cycling.

The PTVs are most stressed during temperature excursions into the solder reflow range. For high quality PTVs five (5) excursions to solder reflow temperatures consume about 1/6 of the available fatigue life of the PTH-via copper barrels; for low quality PTH-vias the solder reflow operations can cause PTH-via barrel fracture during manufacture. For high quality PTH-vias the 1/6 loss of available life is not significant; however, for applications with more severe use conditions (see Table 3-1) this 1/6 loss of life could be a sizeable portion of the design life.

The most important aspect of high quality PTVs is the quality of the copper deposit in the via barrels. As the PTV's aspect ratio increases, it becomes more difficult to plate high quality, uniform copper deposits inside the holes. Special electrolytic plating formulations or electroless plating may be required.

3.7 DfR of SM Solder Attachments The material in Appendix A gives a detailed treatment of DfR of solder attachments.

3.8 DfR of Insulation Resistance The material in Appendix C gives a detailed treatment of DfR with regard to Insulation Resistance.

4.0 SUBSTRATES

This section addresses the materials related issues of substrates. For printed board design and layout, see section 3.3 above.

See also IPC-D-275 for more details on rigid boards.

4.1 General Substrate Categories Interconnect substrate technologies can be divided into the following categories:

1. Organic based printed wiring board
2. Discrete wiring printed board
3. Ceramic based printed circuit board (thick film, co-fired)
4. Ceramic based printed circuit board (thin film)

Categories 1-3 above can be further classified:

- Type 1—Single sided
- Type 2—Double sided
- Type 3—Multilayer with blind or buried vias
- Type 4—Multilayer with blind and/or buried vias
- Type 5—Multilayer metal-core board without blind or buried vias
- Type 6—Multilayer metal-core with blind and/or buried vias
- Type 7—Rigid-flex multilayer without blind or buried vias (organic only)
- Type 8—Rigid-flex multilayer with blind and/or buried vias (organic only)

See Table 4-1 for the advantages and disadvantages of common substrates.

Surface mount components are held on these substrates with solder. The components normally have a different CTE than the substrate; consequently, there will be mechanical stresses on solder joints as the ambient temperature changes. The cycling stress is a potential reliability problem. To minimize this problem, packages can use compliant leads and have the CTE matched to that of the substrate. Substrates are also used for removal of heat. Selected substrates must maintain their function in adverse environmental conditions and be manufactured/assembled at reasonable cost.

Substrates for surface mount technologies include the most commonly used fiber glass reinforced epoxy system with flame retardant, FR-4. The next commonly used material is polyimide glass because of its higher temperature. Each of the materials has its own particular characteristics and properties and behaves differently under varying conditions of temperature, humidity, and other stresses.

4.2 Substrates and Their Functions:

- a. Power distribution;
- b. Signal distribution, interconnecting lands to each other and to the next level with acceptable signal integrity;
- c. Structural, providing a stable platform with a CTE close enough to that of the components that sufficient reliability under use conditions is obtained.

For the assembly to function properly, the electrical, mechanical, and thermal requirements of each material used in the substrate must be considered for the operating conditions and use environments.

Table 4-1 provides guidance in the material choices. See IPC-D-275 for other material discussions.

4.3 Moisture and its Effects on Polymer Substrates

Polymers commonly used in SMT printed boards absorb and adsorb water when exposed to moist atmospheres (high relative humidity) for durations ranging from several days to several weeks; the equilibration time depends upon the thickness of the laminates and the geometry of the conductor pattern. The relative permittivity of water is 80 and that of common substrates ranges from 3 to 5; the absorption of 1-3% by weight of water can significantly (but reversibly) increase the dielectric constant between conductors and hence the capacitive coupling between conductors, over time. The absorption and adsorption of water also decreases the insulation resistance between conductors at the surface (SIR). Together with ionizable contaminants and DC bias, condensed moisture can lead to electrochemical corrosion and dendrites on the surface of the substrates; conductive anodic filament (CAF) formation at the glass fiber-resin interface; and electrochemical corrosion and dendrites at delaminations and voids such as occur between conductors on inner layers and between barrels of PTVs and PTHs. Moisture effects are more significant in SM printed boards because the spaces between conductors and the interbarrel distances are much less than the corresponding dimensions in through hole printed boards; in addition, solder masks may not be easily applied between land patterns in the fine and extra fine pitch SM patterns. See Appendix C for DfR information on SIR. See also IPC-TR-476.

Some materials with higher glass transition temperatures (T_g) such as bismaleimides and polyimides, appear to absorb more water than the lower T_g materials, such as the epoxies. Drying of the higher T_g materials (as well as thicker buildups of the epoxy systems) prior to SM reflow exposure or rework/repair is recommended to minimize delamination or separation, for instance, of the conductor from the resin or the glass fiber from the resin.

The laminate surface is porous when treated by etching to enhance adhesion of conductors; this surface porosity can retain hydrolyzable and ionizable contaminants and water, as well as hydrophilic materials such as polyglycols which are used in the formulation of some water soluble SM solder pastes. Solder mask and conformal coating materials cover and seal the porous surface and help to retain SIR values and reduce the risk of corrosion.

Common solder masks (and conformal coatings) are permeable to water vapor; the presence of water soluble contaminants between solder mask or conformal coating and

the underlying surface can result in vesication or mealing and in electrochemical corrosion/migration.

Chemisorption of water into polymers appears to reduce the T_g slightly, reduces the adhesion of the polymer to other materials and reduces the strength of the polymer. See also the bibliography of IPC-SM-786.

4.4 Coefficient of Thermal Expansion (CTE) of Polymer Systems Polymer systems expand with increasing temperature, demonstrating a glassy phase response below T_g with a CTE or α_1 and a rubbery phase response above T_g with a much higher α_2 , typically 3 times α_1 . The transition from glassy phase to rubbery phase is gradual, but for most polymer substrates may be characterized by T_g , the glass transition temperature.

Glass fiber reinforced substrates exhibit significantly different CTE in the z (out of plane) axis compared to the CTE in the x and y axes; for example, below its T_g , Quartz/Bismaleimide material with 35% resin by weight exhibits a CTE(x-y) of 6 ppm/°C and a CTE(z) of 41. Woven glass fiber reinforcement exhibits an additional difference between x and y axes on the order of 1-5 ppm/°C; this difference may be significant where the CTE of a large SM component package is to be matched to the CTE of the substrate to enhance cyclic life of the solder attachments.

The CTE(z) is particularly significant in determining the cyclic life of PTH and PTVs in SM PWAs because the aspect ratio (ratio of substrate thickness to finished hole diameter) is generally much larger than the corresponding aspect ratio achieved in printed boards manufactured for through hole technologies. Higher CTE(z) values result in higher cyclic tensile stress in the barrel of the PTH or PTV during temperature excursion during SM reflow, or SM component removal/rework/repair as well as during printed board fabrication, solder dipping, hot air leveling, or wave solder. See IPC-TR-579 and IPC-SM-782.

The thermal cycle reliability, vibration robustness, and the thermal management of high performance Surface Mount (SM) products are heavily dependent upon the constraining core such as copper-molybdenum-copper (CMC), copper-Invar-copper (CIC) and molybdenum-graphite-molybdenum (MGM) composite material systems.

The ratios of the various materials in those composite systems can be adjusted to tailor the effective CTE to the optimum value. The tradeoffs include weight and cost. See IPC-MC-324.

4.5 Constraining Cores in Substrates A constraining core is an internal supporting plane in a packaging and interconnecting structure, used to alter the coefficient of thermal expansion of printed boards.

Table 4-1 Advantages and Disadvantages of Various Types of Substrates

TYPE	MAJOR ADVANTAGES	MAJOR DISADVANTAGES	COMMENTS
ORGANIC BASE SUBSTRATE			
Epoxy fiberglass	Substrate size, weight; reworkable; dielectric properties; conventional board processing, availability, cost/performance value.	Thermal conductivity	x, y, and z axis CTE a concern for high density applications.
Polyimide fiberglass	Same as epoxy fiberglass plus high temperature z axis CTE; substrate size; weight; reworkable, dielectric properties.	Thermal conductivity; moisture absorption.	Same as epoxy fiberglass; x, y, and z axis CTE a concern for high density applications.
Epoxy aramid fiber	Same as epoxy fiberglass; x-y axis CTE; substrate size; lightest weight; reworkable; dielectric properties.	Thermal conductivity; resin microcracking; z axis CTE; water absorption; cost; resin adherence.	Volume fraction of fiber can be controlled to tailor x-y CTE. Resin selection critical to reducing resin microcracks.
Polyimide aramid fiber	Same as epoxy aramid fiber; z axis CTE; substrate size; weight; reworkable; dielectric properties.	Thermal conductivity; resin microcracking; water absorption; cost; resin adherence.	Same as epoxy aramid fiber.
Polyimide quartz (fused silica)	Same as polyimide aramid fiber; x, y, z axis CTE; substrate size; weight; reworkable; dielectric properties.	Thermal conductivity; drilling; availability; cost; low resin content required.	Volume fraction of fiber can be controlled to tailor x-y CTE. Drill wearout higher than with fiberglass.
Fiberglass/Teflon laminates	Dielectric constant; high temperature stability; thermal conductivity; x and y axis CTE.	Same as epoxy fiberglass; low temperature stability; thermal conductivity; x and y axis CTE; difficult processing.	Suitable for high speed logic and high frequency applications. Same as epoxy fiberglass.
Flexible dielectric	Lightweight; minimal concern to CTE; configuration flexibility.	Size	Rigid-flexible boards offer tradeoff compromises.
Thermoplastic	3-D configurations; low high-volume cost.	High injection molding setup costs; additive processing.	Very limited applications.
Bismaleimide/triazine glass	Improved dielectric properties; multiple thermal shock; minimum cost penalty for upgrade.	Thermal conductivity; x, y, and z axis CTE.	Applicable to MCM-L technology.
Composite CEM-1 and CEM-3	Punchable at room temperature; cost; stiff enough for SMD.	x and y axis CTE; thermal conductivity.	Substrate of choice for consumer products with SMDs.
Paper-based phenolic	Punchable with heat; lowest cost.	Single-sided only; stiffness; availability; x and y axis CTE.	Majority of world market is paper-based.
NONORGANIC BASE			
Alumina (ceramic)	CTE; thermal conductivity; conventional thick film or thin film processing; integrated resistors.	Substrate size; rework limitations; weight; constant; brittle; dielectric constant.	Most widely used for hybrid circuit technology.
SUPPORTING PLANE			
Printed board bonded to plane support (metal or nonmetal)	Substrate size; reworkability; dielectric properties; conventional board processing x-y axis CTE; stiffness; shielding; cooling.	Weight	The thickness/CTE of the metal core can be varied along with the board thickness, to tailor the overall CTE of the composite.
Sequential processed board with supporting plane core	Same as board bonded to supporting plane.	Weight	Same as board bonded to supporting plane.
Discrete wire	High speed interconnections; good thermal and electrical features.	Licensed process; requires special equipment; cost; availability.	Same as board bonded to low expansion metal support plane.
CONSTRAINING CORE			
Printed board bonded with constraining metal core	x and y axis CTE; uses FR-4 or polyimide/glass materials.	Weight; internal layer registration; delamination; via hole cracking, z axis CTE.	Can be used as power/ground planes.
Printed board bonded to low expansion graphite fiber core	Same as board bonded to low expansion metal cores; stiffness, thermal conductivity; low weight.	Cost; microcracking; z axis CTE.	The thickness of the graphite and board can be varied to tailor the overall CTE of the composite.
Compliant layer structures	Substrate size; dielectric properties; x-y axis CTE.	z axis CTE; thermal conductivity.	Compliant layer absorbs difference in CTE between ceramic package and substrate.

As with printed boards with supporting planes, one or more supporting metallic or non-metallic planes can serve as a stiffener, heatsink, and/or CTE constraint in constraining core printed boards.

The results of “accelerated” life tests which incorporate temperatures which approach or exceed the T_g of the substrate should not be extrapolated to predict service life; these tests may be used to discriminate between alternatives.

4.5.1 Printed Board Stiffness and Damping Constrained core systems with skins of high modulus material form boards which in comparison with standard base materials are stiffer and have higher damping frequencies. These characteristics may be beneficial, depending upon the environmental vibration and noise spectrum.

4.6 Flexible Printed Board with Metal Support Plane Another arrangement for a printed board with leadless components involves conventional fine-line polyimide flexible printed wiring. These assemblies can be constructed in multilayer form while retaining the low-modulus feature that reduces residual strain at the solder joints. Furthermore, lasers can drill very fine holes in the thin, printed wiring laminate. These holes can be plated-through or filled with solid copper as required.

To retain inherent flexibility while dissipating heat from the solder joint, cutouts in the flexible circuit accommodate pillars from the metal heatsink support plane. Although this appears to be heavy and cumbersome, if the heatsink baseplates are made from thin sheets of aluminum, the resulting density of the combined circuit/heatsink assembly might actually be less than other constructions.

4.7 Discrete Wire Structures with Metal Support Plane Discrete wire printed boards have been developed specifically for use with surface mounted components. These structures are usually built with a low-expansion metal support plane that also offers good heat dissipation. The interconnections are made by discrete 0.06 mm diameter insulated copper wires precisely placed on a 0.03 mm grid by numerically-controlled machines. This geometry results in a low-profile interconnection pattern with excellent high-speed electrical characteristics and a density normally associated with thick film technology.

The wiring is encapsulated in a compliant resin to absorb local stresses and dampen vibration. Electrical access to the conductors is by 0.25 mm diameter copper vias. The small via size can be accommodated in the component attachment land, thus eliminating the need for fanout patterns when using components with terminals on centers as close as 0.6 mm, and allowing very-high packaging densities.

The high level of water absorbed into polyimide tape automated bonding (TAB) substrate materials during exposure

to high ambient moisture levels has been observed to result in conductor corrosion and delamination.

4.8 Outgassing of Polymer Substrates See also the discussion of solder mask and coatings in Appendix N, and section 6. The printed board may contribute emissions of cleaning solvent, polyglycols, and lighter fractions of flux vehicles in addition to the emission from the solder mask and conformal coating of the printed board and of the component encapsulation materials.

4.9 Assembly Process Effects on Polymer Substrates See also the discussion of rework and repair in section 7.6 and Appendix E.

In addition, fluxes for wave soldering and for water soluble solder pastes can contain high boiling point hydrophilic or hygroscopic solvents such as the polyglycols. These solvents can penetrate the resin-glass fiber interface and contribute to conductive anodic filament (CAF) formation. See Appendix C for DfR information. See also IPC-TR-476.

4.10 Printed Board Solderability The land patterns in IPC-SM-782, particularly for those intended for fine pitch and extra fine pitch components, clearly demonstrate the very small areas available for affecting the solder joint in SM technology. A solderability defect with an area of 125 μm by 250 μm which might be discounted on a through hole board may constitute the single land which is non-solderable on a SM board and render that SM PWA non-functional; worse, the component lead may contact the land and mechanically affect an electrical contact which becomes intermittent in service and the product is a NTF or No Trouble Found at the repair center.

Although solder dipping and hot air solder leveling (HASL) are said to constitute “proof” that the land is solderable, these processes do not characterize solderability of the land at the critical time which is just before the solder paste is applied and the components are placed. Printed board land solderability is degraded by oxides or chlorides of tin and lead oxides or chlorides of tin-lead phases; oxides of tin-copper intermetallic compounds; and organic films such as residues from fluxing oils, finger prints or solder mask. These oxides, chlorides and organic films can form after the HASL process. See also IPC-PE-740 and IPC-S-816. Quantification of the solderability of the SM printed board is difficult but is addressed in ANSI/J-STD-003; an earlier specification is IPC-S-805.

4.11 Design for Reliability of Plated-Through-Hole Vias (PTVs) The material in Appendix B gives a detailed treatment of DfR for PTVs.

5.0 GENERAL COMPONENT SELECTION CONSIDERATIONS

1. During circuit design and verification, primary impact on manufacturing and assembly is the

selection of components.

2. Commonly used components are available with information detail that simplifies layout, assembly, test, and repair. The data includes termination material and finish, termination configuration, land pattern, package construction, etc.
3. Some components are very easy to assemble, test, and repair; others are not. The availability of a component, its performance data, its degree of testability, its reliability and its compatibility with manufacturing and assembly process and equipment influences component selection.

It is important that the electronic circuit designer and the designer of the SM PWA understand that the selection and application of components cannot be isolated from selection and process flow design of the assembly processes, including inspection, test, rework, repair, and service. The surface mount reflow and wave solder processes subject the component to process stresses at levels not achieved in through-hole solder processes. These stresses and especially the components' response to reflow or wave temperatures in excess of 220°C are not normally considered in through-hole component design. Shock and vibration stresses applied to the SM PWA during depaneling can greatly exceed the stresses anticipated in service or transportation. Application-specific ICs (ASIC) and other IC components require thorough testing and test coverage prior to assembly; if the SM PWA is defective at board test, sufficient test pads must be present for effective fault location and component replacement to be made.

5.1 Component Selection Strategy The best strategy is to use parts that meet (as a minimum) JEDEC/EIA footprints and which have been qualified for the process flow including rework/repair. The characterization/qualification process should be conducted with the components mounted on coupons to simulate the process and thermomechanical stresses. These requirements apply to assembly subcontractors, as well as in-house assembly operations. See also IPC-R-700.

Component suppliers may be able to provide data on the reliability of components upon exposure to various accelerated stress conditions after exposure to various simulated reflow processes.

5.2 Package Leadframe and Local Materials Leadframe and lead materials with low CTEs, e.g. Alloy42, Kovar, etc., should be avoided for plastic surface mount components (PSMCs). Such materials lower the composite CTE of components creating large CTE-mismatches with FR-4 or similar printed board materials. Solderability problems have also been encountered with these lead materials. See also Appendix A.

5.3 Package Lead Configuration Selection

1. Surface mount devices (SMDs) are functionally not different from their conventional through-hole counterparts. What is different in surface mounting is the packaging of devices. SMDs provide greater packing density because of their small size. SMDs are available in numerous package types and lead configurations (see IPC-D-275 and IPC-SM-782). For further details on specific components, reference Appendix F.
2. In the selection of SMDs, consider such differentiating factors as termination configuration, availability, and real estate consideration. For complex function SMDs, testability is an additional factor; see Section 8.2 and Appendix J on DfT.

5.3.1 Gull Wing Components The gull-wing leads of small outline integrated circuit (SOIC) packages are easier to inspect than the J-leads on plastic leaded chip carriers (PLCC). Gull-wing leads can be soldered using various processes, are more uniform (simplifying routing) and more accessible for testing purposes (but must not be directly contacted with probe pins to avoid damage at the lead-package interface). The disadvantage is that gull-wing leads protrude from the package (occupying valuable board space), and particularly on packages without corner bumpers, are susceptible to damage during shipping and handling.

5.3.2 J-Lead Components J-leads are more space efficient than gull-wing leads and can also be soldered using most reflow processes. J-leads are sturdier and more resistant to shipping and handling damage. The compactness of J-leaded components, however, can complicate routing and reduce test access. However, some J-leads have higher lead stiffness increasing the fatigue damage to solder joints.

5.3.3 Pin Grid Arrays Pin-grid arrays (PGAs) require more real estate and board layers, especially if a fine line fabrication is not being used. Some PGAs have hundreds of pins that occupy large sections of every routing layer with complex break out patterns.

5.3.4 Fine Pitch Components The potential complications of the fine pitch SMD are balanced by its smaller footprint. Fine pitch SMDs are more difficult to rework, service, and test; they are also more difficult for assembly equipment to handle than standard SMDs. Because fine pitch terminations and tolerances are much smaller, they may require a robotic arm as opposed to pick and place equipment for accurate placement. In many situations, there are no packaging alternatives because some devices are so complex that only one or two package types are available.



5.3.5 Plastic Surface Mount Components (PSMC)

PSMCs, including semiconductors and resistor/capacitor networks, should have measured data on maximum body temperature (T_{max}) for the process flow, including rework/repair. PSMCs should be obtained from suppliers who have control of moulding voids, internal and external package cracks at the bonding fingers, and qualification or characterization of the PSMCs to the peak process temperature while meeting the requirements of IPC-TM-650, Method 2.6.20 (see Appendix F).

Surface mounted plastic ICs absorb moisture from atmosphere humidity by diffusion. During assembly reflow processes, rapid moisture expansion and material mismatches can result in cracking and/or delamination of critical interfaces within the packages. The classification levels defined in IPC-SM-786, Standard for Handling and Shipping of Moisture/Reflow Sensitive ICs, are intended to be used by IC producers and IC users (board assembly operations). The levels of moisture sensitivity of product devised should be used to avoid package cracking and delamination.

Susceptible components should be required to be dried (baked) and bagged by the supplier and subject to appropriate documented internal or subcontractor treatment during production and rework/repair; these treatments limit additional internal delamination and cracking, but do not reverse existing delamination and cracking.

See Appendix F and IPC-SM-786 for more details on PSMC performance under SM solder reflow conditions. See Appendix E for additional detail on rework and repair effects on PSMCs.

5.3.6 Component Termination Coplanarity and Configuration

A critical issue in SMDs is lead coplanarity which is defined as lying or acting in the same plane. Non-coplanarity is the distance between the lowest and the highest leads when the package rests on a perfectly flat surface. The common problem caused by non-coplanarity is the phenomenon known as solder wicking (the solder paste wicks up the lead, causing open solder joints). It should be kept in mind that poor land or lead solderability or uneven or fast heat application during the reflow process also can cause open solder joints. For all these reasons, the lead ends should lie perfectly in the same plane to avoid manufacturing problems.

5.3.7 Component Lead Configuration Each lead configuration has its advantages and disadvantages. Butt-lead or I-lead devices are not commonly used. The advantage claimed for butt-leads is the possibility of converting through-hole components into SM by clipping the leads and accomplishing the soldering of all components in one reflow operation. Butt-lead joints have normally 65% less pull and shear strength than joints to J or gull-wing ter-

nations and are more sensitive to process-related handling, placement and reflow soldering, and are less compliant than J-leads or gull-wing joints.

5.4 Component Termination Finishes Ceramic and ferrite components such as multilayer ceramic capacitors, chip resistors, and chip inductors are generally terminated with a fired-on silver or silver palladium paste. Because the silver content is easily and rapidly dissolved or leached into molten solder, the soldering process window is tightly constrained as to temperature range and peak temperature duration. A high silver content in the solder joint results in loss of ductility. A termination with high loss of silver is weakly adherent to the ceramic (see 5.4.1).

5.4.1 Nickel Barrier Layer An overplating of nickel (which dissolves at 1/10th the rate of silver) is recommended as a barrier layer between the silver bearing paste and molten solder. Nickel oxide and nickel corrosion compounds are resistive and difficult to solder; nickel oxidizes or passivates rapidly. To prevent oxidation and corrosion of the nickel and hence to preserve the solderability of the termination, an easily soldered final metallic termination finish such as tin, tin-lead or gold is used; palladium is used on some compliant leads.

5.4.2 Tin and Tin-Lead Solder Termination Finishes

The most common SM component termination finishes include tin and tin-lead. Tin-lead finishes are also called solder finishes. Because copper diffuses into the tin-lead and forms copper-tin intermetallic compounds (Cu_3Sn or Cu_6Sn_5) at elevated temperatures, an ideal metallurgical system for copper terminations includes a barrier layer of nickel. The formation of the intermetallic compounds results in a lead rich layer on the termination. The oxides and chlorides of lead, copper-tin IMCs, Cu_3Sn , and Cu_6Sn_5 and the chlorides of tin often are difficult to solder.

5.4.2.1 Tin-Only Finishes Tin-only finishes may exhibit tin “whiskers” as a result of stresses in the tin or nickel under-layers; the whiskers may short closely spaced conductors. Tin-only finishes may also exhibit stress induced in tin “pest,” an allotropic transformation of the white tin to a friable grey tin at low temperatures ($\sim -40^\circ C$) alloys with lead, bismuth, or antimony are less susceptible. Lead content $> 3\%$ appears to suppress both whiskers and pest; alloying of the tin with the lead in tin-lead solder pastes or molten wave solder appears to be sufficient to prevent the emergence of either problem according to extensive stress tests conducted on tin-terminated multilayer ceramic capacitors.

Pure tin plating is not recommended.

5.4.2.2 Tin-Lead Finishes Tin-lead finishes can be applied by electroplating or by dipping of the termination into molten solder. Plated (but non-reflowed) finishes are

uniform in thickness. Plating may be followed by a reflow performed in hot oil. Dipped or reflowed solder finishes are thinner at the corners of the terminations. Dipped solder finish processes are sometimes followed by hot air “kniv-ing” to obtain a uniform thickness of metal on the flat portion of the termination; the result is the thinner metal at the corners. Copper terminations are commonly less solderable at the corners due to exposed intermetallics and oxidation of the intermetallics more quickly than areas with thicker tin-lead coating.

5.4.3 Termination Recommendations When Using Electrically Conductive Adhesives Where electrically conductive adhesive is used, component termination finishes of silver, gold or palladium are recommended, since silver oxide is conductive and gold and palladium do not oxidize. Tin, lead, or tin-lead terminations are not recommended, particularly when the service environment exposes the joints to humidity. The moisture permeates the adhesive and oxidizes the adhesive/metal interface, increasing the series resistance.

5.4.4 Gold, Palladium, Silver Termination Finishes Where gold or palladium plating is used, the gold or palladium content in the solder joint should be less than 3 wt%. This level can generally be met if the gold or palladium finish is $\sim 0.1 \mu\text{m}$ thick on both the component termination and the printed board. Alternatively, the component terminations can be dipped in solder to remove the gold; the solder bath must be monitored to prevent excessive gold buildup. The presence of gold plating on the printed board might be driven by the use of pressure contacts such as solder-less or edge connectors.

Copper leads should be separated from gold overplating by a pore-free barrier of nickel plating to prevent diffusion of the copper into the gold; oxidation of diffused copper degrades the solderability of the gold finish.

Where thin, uniform, solderable platings are needed which can be exposed to high temperatures without loss of solderability, precious metal platings are chosen. Silver, palladium and gold are some of the precious metals available. Gold is the best of these materials having excellent solderability and the best shelf life (indefinite). However, it is expensive and prone to intermetallic failure. Gold requires a barrier layer of nickel plating, $\sim 1.5 \mu\text{m}$ thick, to prevent diffusion of copper to the surface of the gold which degrades solderability.

Gold plating requires a careful soldering process to avoid formation of intermetallic phases which may embrittle the solder joint and lead to premature failure. Surface mounted solder joints are more susceptible to embrittlement failure because of the limited amount of solder in the joint and the reliance on the solder joint for mechanical strength. The concentration of the gold in the tinning bath needs to be

monitored to prevent the gold concentration from exceeding 3 wt%.

Silver requires care in handling and storage to avoid tarnishing which can interfere with solderability.

5.5 Solderability of Termination Finishes Solderability describes an observed condition which results from the use of a flux together with a component termination finish or printed board land pattern finish under the influence of a heat source.

The period of time over which tin-lead finishes demonstrate acceptable solderability depends upon the plating thickness, plating conditions and storage conditions; solderability decreases with increases in such factors as temperature, humidity and oxygen content. Benign atmospheres and proper storage conditions may result in a shelf-life on the order of years. Some plated systems are unsolderable after several months under factory floor conditions. Techniques for evaluating and quantifying solderability are found in J-STD-002, Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires. Organic contamination such as oil, grease, and finger prints or particulate contamination such as dust can also degrade solderability. The mild no-clean or “leave-on” fluxes may not be effective in the presence of these contaminants.

Co-deposited organic materials (electroplating brighteners and levelers) will shorten the solderable shelf life of the tin or tin-lead plating.

Tarnished finishes may be difficult to solder and result from the reaction of a silver termination finish with sulfur compounds which may be emitted by chemical processes using sulfur or storage containers made from paper containing residual sulfur compounds. Silver-plated terminations should be stored with an oxidation inhibitor.

Assure solderability through testing by the producer. The wetting balance method permits measurement of the time-for-wetting as well as the degree of wetting. This testing provides a reproducible method of evaluating process variables with a standard sample geometry. At this time, interpretation of the results varies. A cheaper, non-quantitative test is visual examination of the solder tinned surface (“dip and look”).

5.6 Soldering Considerations SMDs must withstand the higher solder process temperatures and must be selected, placed and soldered more carefully to achieve acceptable manufacturing yield. See also Appendix D, Components and PSMCs.

5.7 CTE Mismatch Considerations Difference in the coefficient of thermal expansion (CTE) of the materials of an SMD is very important to its reliability. The thermal

at one temperature, there may be no stress where two materials join but at a different temperature, if there is a difference in CTEs, the same joint may well be under such considerable strain that the part fractures.

Matching the CTEs at a joint is no guarantee of freedom from the problem because electronic components are their own heat sources and because there is a temperature difference between component and substrate. The problem is directly related to the size of the component, the thickness of a solder joint and the compliance of the lead. See Section 3.4 and Appendix A. The major problem arises from thermally induced cyclic stress in the solder joint of the larger leadless ceramic chip carrier (LLCCC) components.

5.8 ESD Packaging Requirements All SM pick-and-place feeder parts, sensitive or not, if they are dispensed adjacent to ElectroStatic Discharge Susceptible (ESDS) components, should be packaged in antistatic materials.

5.9 Specials or Custom Devices Use Precaution

Devices with unusual or exotic characteristics, extremely tight specifications, or low volume “custom” processing are not as reliable as “standards.” The tightened specifications result in a smaller or unknown C_{pk} . The unique process of evaluation and selection used to meet special requirements is more vulnerable to errors. It is very difficult to demonstrate product quality and reliability (or to improve the process) with low volume of product.

5.10 Components to Avoid or to Use with Caution

- Printed board with $T_g < 125^\circ\text{C}$
- Printed board with PTH and PTVs aspect ratio $> 3:1$
- Components not on the preferred parts list
- Components using obsolete technologies
- Components containing liquid and sealed only with rubber
- Components with rotating seals
- Components with thick silver or gold plating or paste as the solderable termination
- Components with corrosive or polar liquids
- Aluminum electrolytics with silver anode (obsolete technology)
- Components with exposed moving electrical contacts
- Electro-Mechanical connections between contact finishes of tin and gold (dissimilar metals)
- Film resistors trimmed more than 50%
- Multilayer ceramic components such as capacitors, inductors, filter networks assembled into PWAs using assembly processes with $\Delta T/\Delta t > 4^\circ\text{C}/\text{second}$.
- Solder immersion or wave soldering of surface mount components other than simple chip resistors and chip

capacitors.

- Components with ESD susceptibility
- Variable resistors, particularly wire-wound
- Variable capacitors
- Multilayer capacitors trimmed to value

5.11 Component Selection Considerations for Military and Space Applications Military and aerospace applications exposed to severe environments may require packages that are more robust. Hermetic packages may be required to be robust to a life cycle environment which includes high relative humidity. However, under extreme levels of shock and vibration, hermetic packages (with flying internal leads) are less robust than plastic encapsulated packages. See Appendix P.

6.0 SOLDER MASK AND CONFORMAL COATING CONSIDERATION

Because of the fine lines and close conductor spacing and the assembly processes utilized in SMT, solder mask and conformal coatings may be a new design requirement. Solder mask performs two functions, one to limit the flow of solder paste, the other to protect adjacent traces from corrosion. Conformal coating protects the solder joints and component conductors from corrosion. Detailed descriptions of solder masks and conformal coatings may be found in Appendix N.

6.1 Solder Mask Considerations for SM The decision to use solder mask for surface mount technology applications is usually based upon the need to prevent migration of solder away from the device pads during solder reflow. An alternative to the use of solder mask is a pads-only approach.

Typically, solder mask openings are designed $125\ \mu\text{m}$ larger than the component land or through-hole pad. This allows for alignment tolerances during solder mask processing. Since solder mask or its residue on surface mount pads will reduce the size of the solder fillet, it is highly recommended that printed boards be procured which exclude solder mask from extending onto these areas.

The “do’s” and “don’ts” of solder mask are important elements in the construction of a reliable surface mount assembly. The type, thickness, coverage areas and proper application are essential parameters in this complex equation. Since surface mount design begins to encroach upon the limits of the solder mask process, it is important for the designer to understand solder mask process capabilities. The solder mask must be compatible with the surface mount processes being used, especially the heat and solvent resistance characteristics. The choice of a particular solder mask should be validated with the proposed assembly processes (reflow, wave and rework soldering; cleaning, conformal coating) to ensure that the solder mask will

interactions. Failure to understand the links between board manufacture, assembly processes and circuit design may result in a choice of solder mask which will be costly to reverse after introduction.

6.1.1 Solder Mask Selection Table 6-1 provides guidelines on solder mask selection.

Table 6-1 Solder Mask Guidelines

SOLDER MASK TYPE	APPLICATION METHOD	THICKNESS	RECOMMENDED FOR THESE SM SOLDERING PROCESSES			
			TENTED VIAS	STANDARD PITCH REFLOW	FINE PITCH REFLOW	WAVE SOLDER
Liquid	Screenprint	8-50 μm	N*	N	N	N
Dry Film	Hot roll Lamination	60-100 μm	Y	Y	N	Y
Liquid Photoimageable	Open Screen Coat Curtain Coat Roller Coat Electrostatic Spray	15-30 μm	N	Y	Y	Y
Combination (liquid photoimageable* dry film cap layer)	Lamination	50-75 μm	Y	N	Y	

*The majority of via holes can be filled by this process but not tented.

6.1.2 Solder Mask Thickness Issues Regardless of the type of solder mask used for surface mount applications, the solder mask must be the correct thickness and consistent. Solder mask plays an important role in forming a gasket between the solder paste stencil and the printed board to reduce the extrusion of paste and limiting smearing. Typical dry film solder masks range from 75 to 100 μm thick, leaving the mask higher than the surface mount pads (see Figure 6-1). Thus, the stencil will rest on the solder mask and leave a gap between the stencil and the pads through which solder paste can flow. However, typical liquid photoimageable masks range from 15 to 30 μm thick. This makes the pad surfaces the highest points on the board so that when the stencil is lowered, it will rest on the pads. The stencil then gaskets the opening around the pads, preventing the solder paste from getting under the stencil.

Excessively thick solder mask, particularly dry film over traces under components with small clearance, can contribute to the formation of crevices which entrap flux. In the case where the solder mask touches the bottom of the component, if insufficient solder paste is used, it may result in chip component drawbridging (tombstoning), insufficient solder fillet or lack of solder joint. (See IPC-SM-782 and IPC-D-275)

Solder joint reliability under temperature cycling or power cycling conditions may be reduced if the solder mask touches the bottom of the component or conformal coating filling the printed board-component gap. (See IPC-SM-785.)

6.2 Temporary Solder Mask and Tapes Temporary sol-

der mask and tapes are used to prevent solder and solvents from causing problems during assembly processes. In SMT the reflow techniques may expose the mask or tape to temperatures which may cause thermal breakdown. This may cause reversion of some materials into a sticky "goo" and others may adhere tenaciously making them difficult to

remove. The cleaning of SM assemblies may also be more aggressive than through-hole. It is necessary to verify that the temporary mask selected is compatible with the assembly processes.

6.3 Conformal Coatings The primary purpose of conformal coatings is to provide environmental protection. Some conformal coatings have been shown to significantly affect the reliability of surface mount solder joints. Parylene (trademark of Union Carbide, chemical name Polyparaxylylene) and silicone conformal coating have been shown to improve accelerated fatigue life of SM solder joints by approximately a factor of two or three. However in thermal shock, some silicone coatings have been reported to decrease life in thermal shock.

7.0 ASSEMBLY PROCESSES AND DESIGN FOR MANUFACTURABILITY

While there are only a few processes used in fabricating an assembly with SMT components, these processes directly impact the formation of the solder joint that provides the reliable attachment of the part to the substrate. It is essential that the designer of surface mount assemblies understand the manufacturing processes involved, including their impact on the reliability of the completed assembly. Design for manufacturability requires that the designer have a clear view of the impact and limitations of the fabrication steps.

IPC-CM-770, Printed Board Component Mounting, includes the following classification scheme for surface mount assemblies:

Type 1 —Components (mounted) on only one side of

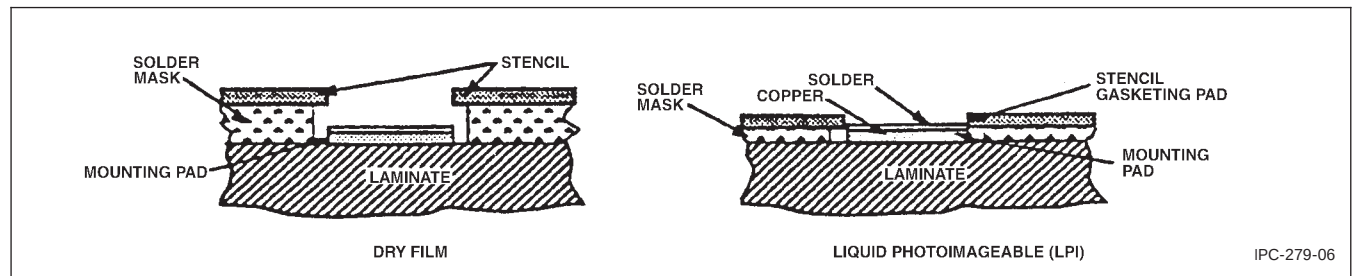


Figure 6-1 Impact of Solder Mask Thickness on Stenciling

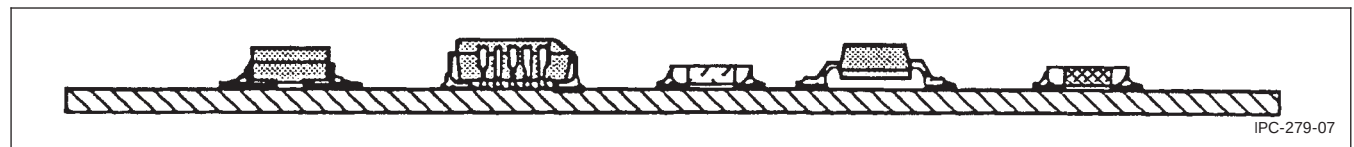


Figure 7-1 Type 1B Assembly - All SMT Components

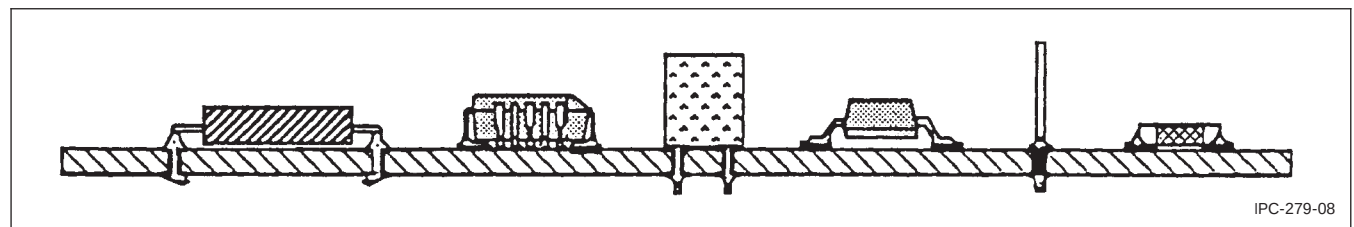


Figure 7-2 Type 1C Assembly - Mixed Technology Assembly

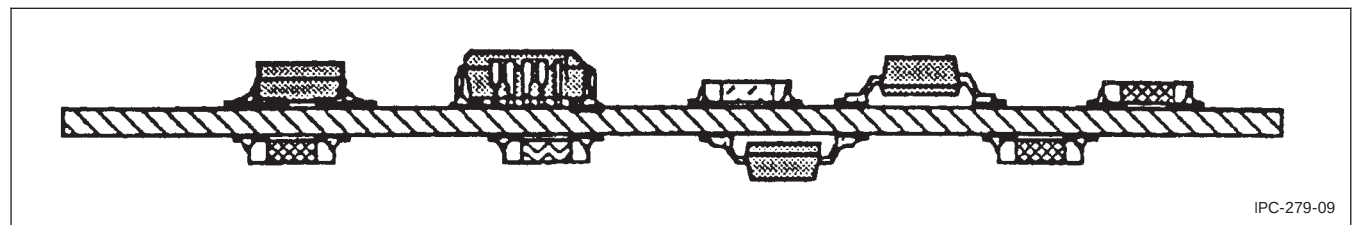


Figure 7-3 Type 2B - All SMT Components

the board

Type 2 —Components (mounted) on both sides of the board

Class A —Through-hole component mounting only

Class B —Surface mounted components only

Class C —A mixture of through-hole and surface mounting

The typical assembly with surface mount components on only one side of the substrate (Type 1B - Figure 7-1) is assembled by one of the following sequences:

1. Apply adhesive, place SM components, cure adhesive, wave solder, clean, test/repair.

or;

2. Apply solder paste, place SM components, reflow solder paste, clean, test/repair.

If the assembly contains both surface mount and through-hole components of a single-sided assembly (Type 1C Fig-

ure 7-2), it may be assembled using one of the following sequences:

1. Apply adhesive, place SM components, cure adhesive, wave solder, clean, insert through-hole components and clinch, wave solder, clean, test/repair.

or;

2. Apply solder paste, place SM components, reflow solder paste, clean, insert through-hole components and clinch, wave solder, clean, test/repair.

When only surface mount components are mounted on both sides of an assembly (Type 2B - Figure 7-3), there are typically two assembly options:

1. Apply solder paste to side 2 (bottom), place SM components, reflow solder paste, clean, invert board, apply solder paste to side 1 (top), reflow solder paste, clean, test/repair.

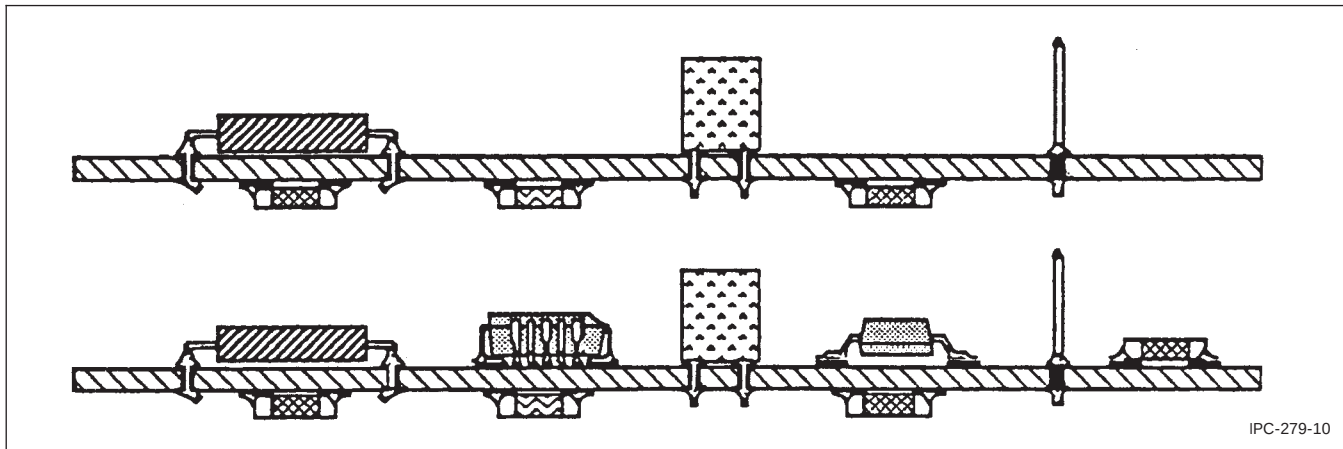


Figure 7-4 Type 2C - Mixed Technology

or;

2. Apply solder paste to side 2, dispense adhesive to side 2, place SM components, cure/bake adhesive/paste, invert board, apply solder paste to side 1, place SM components, reflow solder paste, clean, test/repair.

With mixed technology boards containing surface mounted and through-hole components on more than one side of the substrate (Type 2C - Figure 7-4), there are several typical sequence possibilities:

1. For SM components on side 2 only: Apply adhesive to side 2, place SM components, cure adhesive, clean, invert board, insert through-hole components and clinch, wave solder, clean test/repair.

or;

2. For SM components on both sides: Apply solder paste to side 1, place SM components, reflow solder paste, clean, invert board, apply adhesive to side 2, place SM components, cure adhesive, invert board, insert through-hole components and clinch, wave solder, clean, test/repair.
3. For SM components on both sides: Apply adhesive to side 2, place SM components, cure adhesive, apply solder paste to side 1, place SM components, reflow solder paste, clean, invert board, insert through-hole components and clinch, wave solder, clean, test/repair.

or;

4. For SM components on both sides: Apply solder paste to side 1, place SM components, reflow solder paste, clean, insert through-hole components and clinch, apply adhesive to side 2, place SM components, cure adhesive, invert board, wave solder, clean, test/repair.

7.1 Solder Paste Application Solder paste may be

applied to a substrate either by syringe application or screen/stencil printing. The first issue impacting reliability at this stage is the alloy composition of the solder paste being deposited. Solder comes in a variety of alloys including combinations of tin, lead, silver, antimony, bismuth, indium and cadmium. Each alloy has a distinct set of metallurgical properties and the selection should be based on compatibility with the metals being joined (including leaching and intermetallic formation), the service environment and the service/process temperatures. Reliability will also be affected by the type of flux system used in the solder paste; high reliability applications should be limited to the use of R (rosin) or halide-free RMA (rosin-mildly activated) types.

Another contributor to reliability in this assembly operation is the volume of solder paste deposited since it will dictate the size of the solder joint. Careful consideration should be given to parameters that will affect solder volume such as stencil thickness and aperture sizes, squeegee/syringe pressure, metal content of the solder paste and thickness of solder coating on the printed board or substrate. See Appendix M for details.

7.2 Adhesive Application Adhesive used to mount components for subsequent wave soldering is typically applied via a syringe dispensing method (either manual or automatic). The volume of deposited adhesive should be adequate to restrain the part in place but not impinge on land areas or affect solderability and solder joint formation. All adhesives should be tested for their tendency to form voids that can entrap flux and affect long term reliability. Adhesive voids may also be caused by curing the material too rapidly. Adhesives may outgas even after complete curing.

7.3 Component Placement The placement of components on the substrate may be accomplished either manually or by using a broad range of pick-and-place equipment. Accurate positioning of components is critical

respective land areas is necessary for complete solder joint formation, and thereby contributes to solder joint reliability. Fully automated pick-and-place equipment requires the use of fiducials (which are designed into the bare printed board) for the accurate alignment of the components relative to the substrate. Fine pitch components often require their own set of fiducials near or inside the footprint to assure accurate placement. The type of fiducial (circle, cross, pound sign, etc.) that works best depends on the particular assembly equipment used. Refer to IPC-SM-782 for fiducial and land pattern information.

Bent and skewed component leads may also contribute to improper location of some leads relative to their corresponding pads, leading to solder wicking and incomplete solder joints. Checks for lead coplanarity are often done for high reliability assemblies.

For large volume manufacturing, the placement of smaller substrates in a panelized format with snap-out features or scored edges provides more efficient assembly and results in potentially less handling damage. Care must be taken to design these features correctly to prevent damage to solder joints and board interconnects upon separation of the individual assemblies from the panel.

7.4 Soldering

7.4.1 Solder Paste Reflow Solder paste reflow is typically performed by forced convection, infrared, vapor phase, or laser soldering process. Important parameters that will affect the reliability of the components and assembly include: heating ramp rate, peak temperature in preheat, time above the minimum reflow temperature (20°C above liquidus for copper), peak reflow temperature and cooling rate and duration above the glass transition temperature of the substrate. Control of the reflow profile is required to minimize damage to the components and printed board and to control the formation of intermetallic compounds at the solder-substrate interface. The formation of appreciable intermetallic compounds has been identified as one of the main sources of solder joint failure. See also IPC-SM-816.

High pin count, plastic leaded chip carriers, thin quad flat packs, thin small outline packages and small outline ICs (PLCCs, TQFP, TSOP, and SOICs) may exhibit cracking of the plastic package upon reflow. See 5.3.5 and Appendix F.6.

7.4.2 Wave Soldering The wave soldering of surface mount components requires that the parts be correctly oriented during the design phase. If this is not performed, the terminations may be soldered using specialized wave geometries (e.g. dual or vibrating wave), however, the trailing terminations will exhibit oversized solder fillets that may stress and crack chip components.

A good solder joint can form only if the flux has properly cleaned and prepared the surfaces for the molten solder.

Therefore, activity of the flux is a parameter that needs close monitoring to prevent dewetted and nonwetted solder joints. As with reflow soldering, a good soldering profile is essential to reducing solder defects and preventing thermal shock cracking of chip capacitors.

The presence of contamination in the solder greatly impacts the appearance and integrity of the solder joint. Gold in sufficient quantities (> 3% by weight) can result in seriously embrittled joints. Solder bath contaminant levels should be regularly monitored and limited to the levels found in IPC-S-815.

Active plastic packages such as SOICs and PLCCs may be adversely affected by wave soldering if flux seeps into the lead frame. There is a potential for this to happen since the lead frame and molding compound have different coefficients of expansion. Passive components may exhibit leaching of the precious metal terminations during wave soldering. If dwell time in the solder wave is minimized (3-4 seconds), leaching on these parts can be prevented by a nickel barrier underplating between the precious metal adhesion layer and the solder coating.

7.5 Cleaning Due to the low clearance of many surface mount components, flux residues become entrapped underneath. Remaining flux may eventually cause corrosion and electrical malfunctioning, hence, complete removal of active flux residues are essential to long term reliability. Following soldering, it may be necessary to initiate immediate cleaning to prevent hardening of the flux that makes removal difficult. The effectiveness of the cleaning process should be monitored by measuring ionic residues. See the test procedures in J-STD-001.

Besides flux, it may be necessary to remove a range of other residues such as solder oils, dross particles, strippable solder mask materials, solder balls and particulate matter.

The cleaning medium (solvent) can adversely affect the solder mask, printed board, conformal coating, board or component legends/markings/labels, thin or mechanically stressed sections of plastic components. Appendix I discusses the specifics of solvent compatibility on various plastics and metals.

7.6 Rework/Repair Repair and rework equipment are typically one of two types: hot air devices and conductive tips. When hot air devices are used, care should be taken to prevent thermal damage to adjacent components and the surrounding area of the printed board. The number of times that a part is removed and replaced should be limited in order to prevent internal thermal damage such as interconnect separations within the substrate. Desoldering time when using conductive tips should be limited to three seconds to prevent thermal damage. See IPC-R-700 for rework and repair methods. See 7.8.1.2 for reliability impacts.



RO-L0, RE-L0, RO-L1 flux per J-STD-004 should be used during rework operations and the component should be cleaned immediately following rework. Compatibility of the flux used in repair/rework with the flux used in the original processing should be assumed prior to repair/rework. Only RO-L0 or RE-L0 flux should be used in repair or rework of conformally coated assemblies as typically the conformal coating will not withstand exposure to cleaning processes necessary to completely clean activated flux (e.g., L1, formerly RMA or RA) flux residues. For no-clean manufacturing processes, no cleaning should take place following touchup or repair.

7.7 Depaneling Surface mount assemblies that have been panelized to facilitate handling during the assembly steps will eventually need to be removed from the panel for use. Depaneling may be required before or after electrical testing (based on the design of the test fixture). Individual board assemblies are typically attached together by webs of substrate material that are left following partial routing of the board outline. These webs may contain drilled holes to promote easy “snap-out” of the individual boards. Also common is the use of scoring (either from one or both sides) which produces a groove to assist with depaneling. It is also possible to completely rout the boards from the assembled panel.

The depaneling operation exerts large mechanical stresses throughout the substrate and assembly. Extreme care must be taken to limit these stresses so that their impact on the board interconnects and surface mount solder joints is minimized.

7.8 Design for Manufacturability

7.8.1 Components

7.8.1.1 Soldering Effects The design process must consider the effects of soldering on components in order to produce a reliable assembly.

Components that may be susceptible to degradation from thermal excursions caused by soldering include plastic film capacitors, pulse transformers, inductors, delay lines, passive networks, relays, crystals, and crystal oscillators. In some instances, insulative or reflecting heat shields may provide sufficient thermal isolation. Where the thermal limitations arise from other causes such as internal plastics with low melting or softening point (e.g., plastic film capacitors, light emitting diodes (LEDs)), or internal liquids with low boiling point (e.g., liquid electrolytic capacitors or batteries), internal plastics with high CTE, representing a large fraction of the package volume (e.g., silicon stress relief coating of pulse transformers, passive delay lines), or structural materials of low deflection temperature thermoplastic materials (e.g., connectors or sockets), the

same general alternatives apply.

Where there are thermally massive components such as high pin count connectors, sockets, PGAs or PLCCs with affixed heatsinks, the process design review should include items such as adequate solder joint temperature, as well as overheating of adjacent smaller components.

Where there are laminated ceramic and ferrite components such as multilayer ceramic capacitors (MLCC), chip inductors, and filter networks, they should be characterized for the peak temperature in the process to be used and preheated for a thermal shock $\Delta T/\Delta t < 4^\circ\text{C}/\text{second}$ and a $\Delta T < 100^\circ\text{C}$.

Where there are tall components next to short or low profile components, the process design review should check for thermal shadowing effects from overhanging portions of the taller components.

7.8.1.2 Rework and Repair Effects “Touch up” is the application of heat and solder to a solder joint which is deemed cosmetically imperfect. Rework is the correction of a defect before the SM PWA leaves the plant. Repair is the correction of a defect found in the field. Information on rework and repair may be found in IPC-R-700. Each correction requires the heating of one or more solder joints significantly above the liquidus temperature of lead-tin eutectic solder (183°C) and may involve the removal and replacement of a component. Note that this temperature of 183°C is well above several critical temperatures for the assembly.

These critical temperatures include the printed board glass transition temperature, the temperature at which intermetallic growth occurs, plastic encapsulation glass transition temperature for components, vapor pressure effects on plastic encapsulated components and printed boards, solder melt temperature, temperature excursion (ΔT) and temperature rate of change ($\Delta T/\Delta t$). See Appendix E for a discussion of the effects of exceeding critical temperatures.

8.0 TESTING

Surface mount technology assemblies consist of multiple, high pin count, complex components connected into one circuit with high density interconnections. With this massive increase in density over plated through hole designs, the SMT PWA must be designed for testability. Emerging technologies such as multichip module (MCM), tape automated bonding (TAB), and flip-chip depend on design for testability to be cost effective.

Testability is a design characteristic defined as the ease of testing or the ability to allow cost effective testing. Testability is a measure of the support which a system/module/card/component provides in fault detection and fault isolation. The greatest attention has been paid to digital testability. Previous techniques, including mass production

of test nodes, become less feasible with the smaller dimensions of SMT PWAs and the number of test nodes required for components with 100-400 terminations; the mechanical force exerted by test pins is sufficient to flex and break components and solder joints. IEEE 1149.1 is the digital boundary scan standard; the proposed IEEE 1149.4 will be the analog testability bus standard.

Testability is a particular issue for field repair activities where the full capabilities of the SM PWA may not be exercised due to test equipment limitations or lack of available test time; Built-in-Test-Equipment, Built-in-Test, Built-in-Self-Test (BITE, BIT or BIST) capabilities could be invaluable in these circumstances.

Increased Testability leads to easier, less complex external testing with the following tradeoffs: cost savings associated with increased test fault coverage; shortened test development time; shortened test length/application time; shortened design verification time; reduced defect levels; reduced required tester memory and complexity; reduced test fixture complexity vs. increased costs associated with increased silicon/printed board area; increased number of I/O pins and connectors; increased circuit delay; increased power dissipation; increased design time.

The link between Testability and Design for Reliability for SMT PWAs lies in the provisions for fault detection and fault isolation at the system/SMT module/SMT card/SMT component levels for complex functions. Greater testability should lead to increased system availability through reduced time required for debugging/ trouble-shooting/ repair/ service/ maintenance. Additional benefits include fewer hard or intermittent failures discovered during system operation, fewer failures attributed to marginal performance, and shortened time for failure analysis to root cause.

8.1 Design for Testability (DfT) DfT is the deliberate effort to ensure the inherent testability of a circuit. At the chip, at the board level and at the assembly level, a circuit must be designed for test from the conception of design through its final gate level detail. Testability cannot be added effectively into a complex design after the design is complete. As the density of assemblies increase, manual board probing becomes less and less viable and board test requirements necessitate simulation modeling. The pressure on the hardware designer to reduce the product's Time to Market (TTM) requires that the techniques of Concurrent Engineering be used during product development to consider and implement appropriate Design for Testability measures.

The three goals in implementing testability are controllability, observability, and partitioning. Controllability is the ability to manipulate signal flow within a circuit. Observability is the measure of the extent to which signal activity can be monitored. Partitioning is the reduction of complex

circuitry into a set of minimally interactive subcircuits. For details see Appendix J.

Designing for testability is best achieved through concurrent engineering, where test strategies are defined and incorporated into the design. The appropriate DfT technique may be the placement of adequate test pads for bare board and in-circuit test (ICT). Appropriate DfT technique may be the placement of adequate test pads for bare-board and in-circuit test (ICT). For ICT, supplemental jumpers to be connected or removed as part of the test routine may be required; for bare-board test, test pads at the end-of-net may be required to validate the integrity of PTH and via connections.

8.2 Testing Philosophy Testing is one means of decreasing defects in and increasing the reliability of SMT assemblies. The best strategy in design for testability is to plan for executing every test type available. This is achieved (on bare boards) by providing 100% access to every node of every net from either side of the board. Successful implementation of this strategy on complex, dense designs can be achieved if adopted at the beginning of the design phase.

Testing can be performed at the bare chip, component, bare substrate, and/or loaded substrate levels. The wide range in testing levels allows for detection and isolation of faults or defects at the earliest possible level. The types of fault categories detected include printed board fabrication faults, soldering faults, assembly errors, defective components, and functional failures.

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Multichip Module Technology
Hybrids



Documents

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Substrates:

Rigid Boards and Rigid Board Assemblies
Flexible Boards and Flexible Board Assemblies
Metal Core Boards

Process Parameters:

Statistical Process Control:
Process Control and Troubleshooting

Connectors and I/O Interconnection Adhesives:

Thermally conductive
Insulative (Structural)
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Films (Bonding)

Assembly Design:

Printed Board Component Mounting
Surface Mount Land Patterns (Configurations and Design Rules)

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See also IPC publication on Accelerated Reliability Testing of Surface Mount Solder Attachments

9.18 Solder, Solderability, Soldered Assembly Quality

See ANSI/IPC J-STD publications on various Solder, Solderability, Solder Assembly Quality

9.19 Solder Mask and Conformal Coating

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See also IPC documents on Solder Mask, Conformal Coating, SIR, IR, Cleaning, Surface Mount Land Patterns/Configurations and Design Rules

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