



*THE INSTITUTE FOR
INTERCONNECTING
AND PACKAGING
ELECTRONIC CIRCUITS*

IPC-D-317A

Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

IPC-D-317A

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A standard developed by the Institute for Interconnecting
and Packaging Electronic Circuits

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Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-D-317

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Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

1.0 General

1.1 Purpose The object of this document is to provide guidelines for the design of high speed circuitry. The subjects presented here represent the major factors that may influence a high speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope The goal in electronic packaging is to transfer a signal from one device to one or more other devices, through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the inter-connecting properties effect circuit function and require consideration. Every electrical concept has relevant physical implementation data provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more accurate data.

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

Symbol	Description
AC	Alternating Current
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE _{xy}	X and Y-Axis Coefficient of Thermal Expansion
CTE _z	Z-Axis Coefficient of thermal expansion
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
FR-4	Epoxy Glass Dielectric Material
H _L	High-to-Low Signal Edge Transition
IC	Integrated Circuit
K _B	Backward Crosstalk
K _F	Forward Crosstalk
L _G	Ground Plane Inductance
L _H	Low-High Signal Edge Transition
L _P	Power Plane Inductance
PWB	Printed Wiring Board
R _C	Series Lead Resistance
R _G	Ground Plane Resistance

R _P	Power Plane Resistance
R _T	Sheet Resistance
SM	Surface Mount
TAB	Tape Automated Bonding
Tan (δ)	Dissipation Factor (Loss Tangent)
TDR	Time Domain Reflectometer
T _P	Total Signal Line Propagation Delay Time
T _{PD}	Propagation Delay Per Unit Length
T _R	10%–90% Edge Transition Time (Rise or Fall)
TTL	Transistor Transistor Logic
Z _O	Characteristic Line Impedance (Unloaded)
Z _O '	Characteristic Line Impedance (Loaded)
ε _r	Relative Permittivity
ε _r '	Effective Relative Permittivity
δ	Skin Depth

1.3.2 Terms and Definitions The terms listed below are used in this document. Their definitions are given in order to help the new reader. These definitions are also found in IPC-T-50, "Terms and Definitions for Interconnecting and Packaging Electronic Circuits." Where possible, definitions that appear in the body of this document are referred to as follows: "Bus – 5.6.5.2". This indicates that a definition for "Bus" appears in section 5.6.5.2, and will not be repeated here.

AC Impedance—The combination of resistance, capacitive, reactance, and inductive reactance seen by AC and/or time-varying voltage.

Alternating Current (AC)—A current that varies with time. This label is commonly applied to a power source that switches polarity many times per second, such as the power supplied by utilities. May take a sinusoidal shape, but could be a square or triangular wave shape.

Amplitude—The height or magnitude of a voltage signal as measured with respect to a reference plane, such as signal ground.

Dual-Strip Line—A stripline signal conductor that is embedded between two ground planes, and is not centered between them (closer to one ground plane than the other).

Attenuation—Reduction in the amplitude of a signal due to losses in the media through which it is transmitted.

Backporching—A term used to describe the reflections which follow a fast rise or fall time signal traveling down a long transmission line that has not been properly terminated. Looks like a stair step.

Backward Crosstalk—Noise induced into a quiet line placed next to an active line as seen at the end of the quiet line close to the signal source.

Bus—See section 5.6.5.2.



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Busbar—A large copper or brass bar used to carry high power supply currents onto a printed board or backplane.

Capacitance—A measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them. Measured in Farads.

Characteristic Impedance—The resistance of a parallel conductor structure to the flow of AC current. Usually applied to transmission lines in printed boards and cables carrying high speed signals. Normally a constant value over a wide range of frequencies.

Circuit Board—For the purposes of this specification the term circuit board covers both printed circuit board, and discrete wiring boards where a circuit function is performed.

Coaxial—A term used to describe conductors that are concentric about a central axis. Take the form of a central wire surrounded by a conductor tube that serves as a shield and ground. May have a dielectric other than air between the conductors.

Crossover—Intersection of two conductors separated by insulation.

Crosstalk—See section C 3.2.

Current—Electrons traveling in a conductor as the result of a voltage difference between its ends.

Decoupling—Absorbing noise pulses generated in the power supply lines by switching logic so as to prevent them from disturbing other logic on the same power supply circuit. Usually done with capacitors. See 5.1.3.

Differential Pair—Parallel routed signals exhibiting a mutual impedance between both lines, typically 50 to 120 ohms.

Direct Current (DC)—A current produced by a voltage source that does not vary with time. Normally provided by power supplies to power electronic circuits.

Discrete Wiring Board—Circuit board using round insulated wire to form signal paths, terminated by a plated through hole.

Dissipation Factor—A factor used to express the tendency of insulators or dielectrics to absorb some of the energy in an AC signal.

Edge Rate—The rate of change in voltage with time of a logic signal transition. Usually expressed in volts per nanosecond.

Edge Transition Attenuation—The loss in sharpness of a switching edge caused by absorption of the highest frequency components by the transmission line.

Effective Permittivity (Dielectric Constant)—See section 5.2.2.

Effective Relative Permittivity—See section 5.2.2.

Electromagnetic Interference (EMI)—Radiated electromagnetic energy which couples into conductors where it is not wanted.

Flat Conductor—A rectangular conductor that is wider than it is high. Usually refers to signal conductors in a printed wiring board.

Forward Crosstalk—Noise induced into a quiet line placed next to an active line as seen at the end of the quiet line farthest from the signal source.

Ground—A term used to describe the terminal of a voltage source that serves as a measurement reference for all voltages in the system. Often the negative terminal of the power source, but sometimes the positive terminal.

Impedance—The resistance to the flow of current represented by an electrical network. May be resistive or reactive, or both.

Inductance—The property of a conductor that allows it to store energy in a magnetic field induced by a current flowing through it. Units of measure: Henry.

Line Coupling—Coupling between two transmission lines caused by their mutual inductance and the capacitance between them.

Load Capacitance—The capacitance seen by the output of a logic circuit or other signal source. Usually the sum of distributed line capacitance and input capacitances of the load circuits.

Logic—A general term used to describe the functional circuits used in computers and other digital electronics to perform computational functions. Logic Family—A collection of logic functions or ICs using the same form of electronic circuit to perform computation. Examples: ECL—emitter coupled logic; TTL—transistor-transistor logic; CMOS—complimentary metal oxide semiconductor logic.

Microstrip—See section 5.5.1.

Net—See section 5.6.5.1.

Parallel Pair—Two conductors that travel side by side at a controlled spacing over a long distance.

Permeability—A general term used to express various relationships between magnetic induction and magnetizing force.

Permittivity (dielectric constant)—See section 5.2.

Power Dissipation—Energy used by an electronic device in the performance of its function.

Power Plane Inductance—See section 5.1.2.1.

Printed Wiring Board—A circuit board utilizing etched copper traces for signal interconnections.

Propagation Delay—The time required for a signal to travel along a transmission line, or the time required for a logic device to perform its function and present a signal at its output.

Pulse—A logic signal that switches from one state to the other and back in a short period of time, and remains in the

original state most of the time. Usually used as clocks for logic devices.

Reflection—Energy from a high speed signal edge that is sent back toward the source as a result of encountering a change in impedance in the transmission line on which it is traveling.

Rise Time—Time required for a logic signal to switch from its low state to its high state. Commonly measured between the 10% and 90% voltage levels.

Signal Line—Any conductor used to transmit a logic signal from one circuit to another.

Skin Effect—See section 5.8.1.

Stripline—See section 5.5.3.

Stub—A branch of the main line of a signal net usually used to reach a load that is not on the direct signal path.

Transmission Line—Any form of conductor used to carry a signal from a source to a load. The transmission time is usually long compared to the speed or rise time of the signals, so that coupling, impedance, and terminators are important to preserving signal integrity.

Waveguide—A rectangular or round tube used to transmit microwave energy in the form of an electromagnetic wave rather than a current in a wire.

1.4 Units Unless otherwise specified, dimensions will be metric (SI).

2.0 Applicable Documents

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-L-125 Specification for Plastic Substrates, Clad or Unclad for High Speed/Frequency Interconnections

IPC-MF-150 Metal Foil for Printed Wiring Applications

IPC-D-275 Printed Board Design Standard

IPC-D-249 Design Standard for 1 and 2 Sided Flexible Printed Boards

IPC-DW-424 General Specification For Encapsulated Discrete Wire Interconnections Boards

IPC-DW-425 Design End Product Requirements for Discrete Wiring Boards

3.0 Overview Packaging of electronic equipment has traditionally been an area for mechanical considerations. An assortment of active and passive devices need to be adequately provided with physical support, environmental protection, heat removal, electrical interconnections where specified and electrical insulation where interconnections are not specified, all by a cost-effective means.

Packaging design is becoming more complex. Switching devices typical of digital electronics technology are available in increasingly greater degrees of both switching speed and count of devices per chip. Individual chips are being provided with greater numbers of connections in smaller individual chip package sizes. The competitive need to take maximum advantage of device density and speed has forced packaging designers to pay much more attention to problems of electromagnetic wave-propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. This document is intended to help meet this need and this overview section will introduce in broad terms what is covered.

3.1 Decision Making Process Determine at the start of a project whether packaging concerns need early introduction into the design process. Performance of older systems was limited by the devices available and packaging design could be left for the end of the design activity. High performance systems are limited in speed by packaging, so if the project is concerned with speed, start by considering how to get the most out of the packaging.

There are numerous design options to consider, balanced against mechanical and electrical requirements of the package (see Figure 1). For a proposed system, a choice among types of devices has to be made. This will have an influence on the kinds of packaging materials to be selected. It will become apparent that the design is a collection of compromises to get the best overall performance. Effort early in a program to evaluate many sets of options and their interactions is recommended.

The decision making cycle will consist of proposing a design with selection of devices, packaging materials, and interconnection scheme. The system preferably will be modeled and its deficiencies and limitations identified. This should result in some alterations in the design as the start of another modeling cycle. The process is repeated until further improvement is minimal. If the projected performance is far short of the target then the designer should consider attempting a different design approach.

These guidelines should be helpful in providing awareness of the options available and the principles needed in modeling. There is plenty of room for innovative advances in high speed packaging.

3.2 Design Options Let us consider some of the options to be exercised by the designer, realizing that each selection interacts with the others. These are organized as options that may be considered as givens followed by a list of the resulting requirements.

3.2.1 System Electrical/Mechanical Givens What type of active switching devices will be used? Example options include TTL, Schottky TTL, CMOS, ECL and GaAs, each with its own set of power requirements, operating temperature range, density on a chip, input impedance, output impedance,

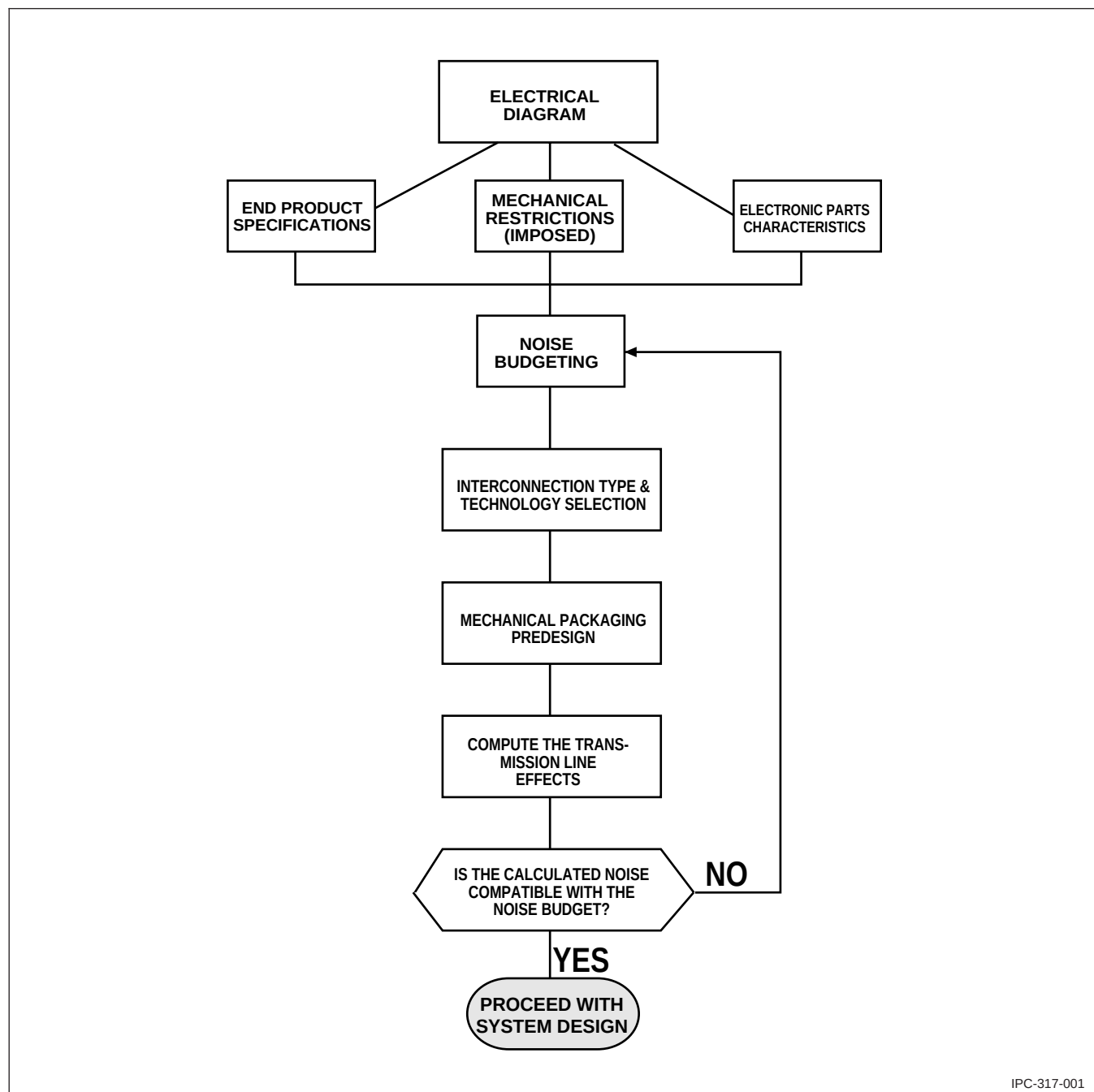


Figure 1 High speed packaging design concept

signal threshold levels, noise sensitivity, response time and output pulse rise/fall time.

How will devices be organized in the final assembly? Chip devices can be prepackaged and individually mounted on a large board or assembled into small boards or multichip modules which will in turn be mounted onto large boards. Large systems will require several large board assemblies and there is yet another option of how this level of interconnection will be applied. Reflection noise and signal degradation will accompany transitions from one packaging level to the next. Organization will have an impact on manufacturability and reparability of the system.

What transmission line geometry on boards will be used for signal interconnections between devices? Options include coplanar coupled pairs, microstrip over a single ground plane, striplines between ground planes, orthogonal striplines sharing a common pair of ground planes, wire over ground plane, and wire between ground plane. For a given geometry the selection of substrate thickness and conductor width will depend on the required characteristic impedance, the relative permittivity (dielectric constant) of the substrate and its thickness.

What interconnect schemes for signal transmission will be used? One could choose single connections from one device

output to another device input. A single output could be connected to several inputs and the multiple connections could be accomplished either by branching or by continuing from one input to the next in daisy-chain fashion. The scheme will affect transmission time, noise, settling time and signal pulse degradation.

3.2.2 System Electrical/Mechanical Requirements The decision on the number of signal layers in multilayer boards or discrete wiring boards will be influenced by the density of interconnections within the board. There will be a compromise of the degree of isolation of one interconnection from another versus the need to get a large number of interconnections in a given board area.

Determine the degree of crosstalk or coupling between signal lines that can be tolerated. This can have a major effect on acceptable interconnection densities.

Relative permittivity (ϵ_r) influences board substrate selection. While a low ϵ_r value means faster signal propagation it also increases the conductor width needed at a given substrate thickness for a given characteristic impedance, thus reducing room for conductors.

Power requirements of the devices will need to be met by an adequate scheme. Often the choice is made to provide voltage planes in circuit boards that serve the dual roles of ground plane for signal conductors and leveled supply of voltage to devices. An alternative is to provide a bus system to the array of chip devices on the board.

3.3 Mechanical Requirements The mechanical requirements list is derived to assure a means to maintain the integrity and performance of electrical interconnections among electronic devices in the system.

3.3.1 Circuit Board Circuit boards are required to provide mechanical support and interconnection of components mounted on them. Space constraints, number and complexity of interconnections, thermal management, power distribution and cost of manufacture are some factors to be considered when determining requirements of how many layers, the thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric composition and the overall length, width, and thickness.

3.3.2 Hybrid This term is often used to refer to assemblies of thin/thick film chip devices mounted directly on thin/thick film ceramic interconnection boards to form a multichip module. Other technologies using polymeric substrates in place of the thin/thick film ceramic could also be used to build multichip modules. Hybrid boards and multichip modules are usually required to provide protection of sensitive chip components from adverse effects of whatever ambient atmosphere may be encountered in service. They also must be able to withstand thermal and mechanical shock during manufacturing and assembly as well as in service.

3.3.3 Component Packaging Unless chip devices are packaged in multichip modules or hybrid subassemblies they are usually prepackaged individually. The component package can be polymeric or ceramic depending on the degree of atmospheric protection required. The package is required to provide protection to the chip and electrical connections from the chip to the board on which it will be mounted. The package also provides a means for connecting to the chip for automated testing of the package prior to its being used in a board assembly.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated through holes provided in the board, as in dual in-line package, to a series of metallized regions along the edge or arrayed over the base of a surface mount device. What type of connection is selected will depend on, among other things, the requirements for electrical performance of the connections.

Requirements for component packaging will be dependent on many factors including space available, economics, electrical performance requirements, reliability, life expectancy, and thermal conditions.

3.3.4 Thermal Management The system must withstand thermal cycling and temperature differences during service. Temperature differences arise, especially in startup, between packages containing chips and the supporting interconnecting boards that will generate strains due to thermal expansion. Use of materials with differing coefficient of thermal expansion (CTE) in different levels of packaging will lead to strain between these levels as temperature changes on the connections.

The packaging materials must handle the heat generated by operating the system. Mechanical properties sufficient to provide mechanical integrity of the system must be retained at the elevated temperature expected to be encountered during system operation. Packaging must provide for removal of excess heat to keep the temperature below the point where impairment of electronic performance would occur.

3.3.5 Component Mounting The component must be provided in a format that is convenient to attach to the circuit board. Mechanical requirements imposed on the board include tolerances of size and location of the features involved in the attachment and ability of it to withstand thermal shock and stress involved in the attachment of the component. Some device packaging categories include:

- a. COB mount device
- b. TAB mount device
- c. Single chip package (DIP, PLCC)
- d. Multichip package



3.4 Electrical Considerations Electromagnetic wave propagation theory must be considered in evaluating the performance of interconnecting conductive conductors and their substrates. High-speed devices are characterized by the short rise time of the pulses. The pulse wave form may be represented as the sum of a series of sinusoidal component signals with certain phase and amplitude relationships. As the rise time of the pulse decreases, the frequency of the important components increases.

3.4.1 Power Distribution For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in electrical current from the power supply. If several devices are demanding current changes at or near the same instant, the power distribution system is required to meet these demands while it is maintaining voltage within specified limits to all devices being supplied. Meeting this requirement demands low inductance connections to devices, with high capacitance among various voltage levels in the distribution system.

3.4.2 Permittivity The relative permittivity (ϵ_r) of the dielectric substrate of an interconnecting device, whether it be a printed board, discrete board and a multichip module, or a chip package will affect electrical performance of the interconnection on or embedded in it. An assumed ϵ_r is used in the design of the interconnection to meet the impedance, capacitance and propagation time requirements as will be discussed. The tolerances of these requirements along with manufacturing tolerances on conductor dimensions impose a tolerance requirement on ϵ_r if the system is to perform as designed. Since ϵ_r of many substrate materials varies with composition, frequency, and environmental conditions this also impacts on allowable tolerances in ϵ_r .

For a given transmission line geometry propagation time will vary directly as the square root of ϵ_r , impedance inversely as the square root of ϵ_r , and capacitance directly as ϵ_r .

There are trade-offs in the selection of high or low ϵ_r values for the substrate that will be discussed later.

3.4.3 Capacitive Versus Transmission Line Environment

For an interconnection from one device to another, the connecting line can either be treated as a transmission line or a capacitive line. For transmission lines the design concept is to provide a known characteristic impedance that is terminated at the destination with a matching impedance to minimize reflections resulting from fast rise time pulses. For a capacitive line, the concept is that of a line whose stored charge requires a certain amount of current flow to result in changed voltage detected at the destination. The critical design parameters and requirements will depend on which concept is appropriate.

3.4.4 Propagation Time In high-speed systems, it is not unusual for the clock cycle time to be shorter than the propagation time for a signal from one device to another, especially

where a signal might originate on one board and be received on a device on another board. For the system to perform correctly at high speeds, a well controlled propagation time is required and in some cases adjustments in the propagation time for certain lines may be required.

3.4.5 Impedance The reason why 50 to 70 ohms characteristic impedance is so often used is that lower Z values cause excessive dl/dt crosstalk, and can double the wattage consumed and the heat dissipation problem. Higher impedances not only permit higher crosstalk values, but produce circuits with greater EMI sensitivity, and greater EMI radiation. There is less and less use of impedances much removed from 50 ohms. The impedance is the square root of the ratio of inductance per unit length to capacitance per unit length. The impedance of a transmission line can be mathematically modeled as a complex function of several parameters:

- a. **Conductor width/diameter**—lower impedance with wider line width or larger diameter
- b. **Type of conductor**—coplanar pair of conductors, microstrip with one ground plane or stripline between two ground planes. With equal ϵ_r , spacing and conductor width, impedance ranking will be coplanar > microstrip > stripline.
- c. **ϵ_r of dielectric**—lower impedance with higher ϵ_r
- d. **Spacing between signal and ground**—lower impedance for smaller spacing
- e. **Proximity to other conductors**—lower impedance as proximity increases

3.4.6 Signal Loading Effects When a conductor proceeds to several loads (termed "signal line"), the issue of signal loading must be considered.

Consider loads connected in daisy chain fashion. If the impedance of the load is low or a near match to the characteristic impedance of the line there will be a decrease in signal amplitude as each load is reached. High-impedance loads relative to the line will result in less decrease in amplitude. A matched load at the end load is needed to prevent a reflection that could send a false pulse to the other points. The transmission line concept is usually appropriate.

With a star connection scheme, each branch point looks like a low impedance load and the amplitude will be diminished on the branches. The capacitive line concept is usually appropriate.

3.4.7 Crosstalk In general, an interconnecting board is populated as densely as possible with chip devices to minimize the size of the system and reduce propagation time. The result is that conductors must be run close to each other and usually the designer must resort to multilayer boards or discrete wiring boards to handle the high interconnect density and the crossover situations in the wiring plan.

Cross talk is the transfer of pulse energy by the electromagnetic field from a source line to a victim line. The intensity of the transferred (coupled) signal decreases with shorter adjacent line segments, wider line separations, lower line impedance, and longer pulse risetimes.

A victim line could run parallel for short distances to several other lines. If a certain combination and timing of pulses on the other lines occurs, it could induce a spurious signal on the victim line. Thus, there are requirements that the crosstalk between lines be kept below some level that could cause a malfunction of the system.

3.4.8 Signal Attenuation High-speed systems have devices that generate short rise time pulses and may respond ambiguously to pulses exceeding a certain maximum rise time. Signal attenuation increases rise time and decreases the amplitude of the pulse. This is best explained in terms of the model of a pulse as a sum of signals of several frequencies. The high frequency components of the pulse attenuate more rapidly than lower frequency components. This is due to the skin effect in the conductor as well as the dissipation effect in the dielectric.

For thin copper, the pre-treatment may raise the copper impedance.

Signals may be further attenuated by the resistance of the copper used in the conductor and by skin effect losses resulting from the finish of the copper surface.

The resistance of the copper may reduce the steady state voltage levels below the levels needed for adequate noise immunity. This is especially true of ECL circuits where a voltage divider is formed by the terminating resistor and the line resistance.

DC resistance can be calculated using the copper resistivity and the geometries of the conductors being used. The effects of surface finish (skin effects) may have to be determined by experiment. The smooth surface of a drawn wire used in discrete wiring boards has lower skin effect losses and other advantages over etched conductors.

4.0 Mechanical Considerations In addition to meeting the predicted performance criteria, circuit board designs must be manufacturable if the system is ever to become a reality. Performance versus cost also factors into the choice of the optimum system design. Yield at manufacture and end product reliability may be, at times, even greater contributors to cost than the obvious costs of raw materials and fabrication. For this reason, the designer should be familiar with the material options available, their properties, capabilities, and tolerances and have a reasonably good understanding of process capabilities and tolerances that may impact, not only performance but also manufacturing yield and reliability.

The development of a close working relationship with the manufacturing engineering group of the captive or vendor board fabrication facility is highly useful to avoid excessive

prototype iterations which are both costly, and time consuming. Designing "based on what worked before" is certainly valid but may be limiting at times if full advantage of advances in both materials and fabrication is to be taken. Therefore, the development of a relationship with in-house advanced materials and manufacturing groups as well as outside industry sources is advisable.

The following is intended to serve as a cursory overview of some of the interactions between raw materials, performance, and manufacturing capabilities. This summary should by no means be considered exhaustive of the technologies available for the production of circuit boards.

4.1 Printed Board

4.1.1 Substrate Materials A table of generally available laminates is in Appendix B. Refer to IPC-L-125, "Specification for Plastic Substrates, Clad or Unclad for High Speed/High Frequency Interconnections" for more detailed information. These materials are classified by the resin system and support material or filler that make up the composite and are responsible for their individual electrical, chemical, and physical characteristics.

4.1.1.1 Resin Systems The resin systems used for circuit board laminates are classified into two basic categories: thermosetting and thermoplastic. Thermosetting resins are crosslinked matrices of smaller, polymeric units. The polar nature of materials generally contributes to higher relative permittivity, loss tangent (dissipation factor) and water absorption. The crosslinked structure of the thermosets generally provides better dimensional and thermal expansion characteristics. Water absorption becomes an issue because its relative permittivity is so high (approximately 75) compared to these resin systems. Therefore, relatively small changes in humidity in the environment may drastically impact performance (i.e., capacitance + Z_o) and necessitate strict environmental controls. Likewise, each resin system has a characteristic response of relative permittivity and loss tangent to temperature and operating frequency.

4.1.1.2 Reinforcements, Supports, and Fillers Although some of the available materials are comprised of resin only, routinely various reinforcements, supports, and/or fillers are incorporated with the various resin systems to enhance the physical or electrical properties of the composite laminate. A typical example is the incorporation of woven E-glass into a resin matrix to enhance dimensional stability and reduce the X-Y coefficient of thermal expansion (CTE_{XY}) which may be unacceptable or undesirable in the unsupported resin. Fillers may be added to modify the relative permittivity and/or to exclude resin and thereby reduce the overall CTE in X, Y, and Z dimensions.

The thicknesses of woven glass reinforced materials are typically even multiples of the reinforcement thickness plus resin

4.1.1.3 Claddings Copper is by far the most common cladding material around which most circuit board processes have been designed. Copper foils are sold by weight, with 1/2 (153), 1 (305), and 2 (610) oz./ft² (gm/m²) being common. These weights roughly translate to 0.7, 1.4, and 2.8 mils in thickness respectively. Thinner foils are available.

For high speed circuitry it may become necessary to provide special cladding material:

- with reduced (inner) surface roughness ($\leq 2\mu\text{m}$) in order to minimize line resistance
- permitting advanced interconnection techniques (e.g. ultrasonic bonding)

Copper foils are available in rolled annealed or electrodeposited forms. Other properties of copper foils relate to their ductility and elongation characteristics which may impact through-hole reliability. For more information on foils, consult IPC-MF-150, "Metal Foil for Printed Wiring Applications." Untreated copper foils shall have the following maximum resistivity at 20°C.

For deposited foil:

Weight Designator

E	0.181 ohm-gram/meter ²
Q	0.171 ohm-gram/meter ²
T	0.170 ohm-gram/meter ²
H	0.166 ohm-gram/meter ²
M	0.164 ohm-gram/meter ²
1 oz. and over (305 gr/m ²)	0.162 ohm-gram/meter ²

For wrought foil (all weights):

Type 5, 8	0.158 ohm-gram/meter ²
Type 6	0.153 – 0.157 ohm-gram/meter ² according to temper
Type 7	0.152 ohm-gram/meter ²

4.1.1.4 Discrete Wiring For high-speed circuitry utilizing discrete wiring boards the following insulated wires are used:

Diameter	AWG	Resistivity @ 20°C
2.5 mil	42	1.80 ohms/ft
4.0 mil	38	0.648 ohms/ft
6.3 mil	34	0.261 ohms/ft

4.1.1.5 Prepregs, Bonding Layers and Adhesives

Various thermosetting and thermoplastic materials are available for laminating the multilayer package. Prepregs are woven glass supported resins in their B-stage or partially cured state. They are used to create the dielectric spacing between layers and are cured or crosslinked in the lamination process. Thermoplastic bonding layers may also be used for dielectric spacing and work by fusion bonding in lamination cycles exceeding their melting point. Thermoplastic bonding films and thermosetting adhesive films are thin unsupported

materials used in configurations where the dielectric spacing is already provided by another material.

4.1.1.6 Material Tolerances Knowing the raw material tolerances from the outset will go a long way toward predicting the probability that a given design will perform within the desired specifications and form the basis for any sensitivity analysis. Impedance calculations are heavily impacted by thickness (dielectric spacing) and relative permittivity; therefore, these are of primary interest.

1. **Relative Permittivity (ϵ_r)**—The relative permittivity of the unreinforced materials should be invariant as these are generally uniform, isotropic materials. The reinforced, supported, and filled materials are combinations of materials of different relative permittivities and will exhibit variations in this value unless the proportions of the combination are strictly controlled.
2. **Thickness**—Changes in the volume percent of resin will impact both thickness and relative permittivity. Thickness uniformity among materials will vary with the technology and the level of process control employed.

4.1.1.7 Material Impact on Board Fabrication/Assembly

The specific details of circuit board manufacture are not discussed here. However, the effect of materials properties on manufacturing issues are listed as they impact design considerations. This list is not exhaustive.

1. **CTE_{xy}**—The expansion characteristics of the printed board under thermal load will impact the choice of components, the style of leads, and the method of mounting to minimize CTE mismatches which may ultimately reduce joint reliability. The reverse is also true. If the choice of component package and lead has already been made, then the material choice follows. In other cases, other materials may be incorporated into the package to further constrain movement in the X-Y plane further reducing any CTE mismatch. Various thermal management schemes may also provide some relief in this regard.
2. **CTE_z**—Thermal expansion in the z-axis may impact through-hole (PTH) reliability in fabrication, assembly and in service. Advanced techniques or controls may be required to utilize high z-axis expansion materials. The number of layers or the overall thickness of the package may have to be limited or in some cases may preclude the use of PTH's altogether. Use of discrete wiring for replacing multiple etched signal layers can significantly reduce board thickness and eliminate z-axis expansion concerns.
3. **Young's Modulus**—The ratio of unit stress to unit strain
4. **Poisson's Ratio**—The ratio of lateral strain to longitudinal strain
5. **Dimensional Stability**—Dimensional changes in the material impact layer-to-layer registration. Advanced techniques or controls may be required to utilize less stable materials.

6. **Thermal Properties T_g** —The glass transition temperature T_g of the material will dictate the thermal processes employed either in fabrication or component attachment.
7. **Chemical and Solvent Resistance**—These properties will dictate chemistries that can and cannot be used for processing and cleaning.
8. **Machinability**—The relative ease with which a material can be drilled, punched, and routed will impact the cost of fabrication.

4.1.1.8 Circuit Board Fabrication and Tolerances A general understanding of the capabilities of board fabrication technologies and the realistic and achievable tolerances is critical to the successful implementation of designs. Areas of particular interest are:

- a. **Hole location and diameter**—impacted by drills, material, dimensional stability, drilling practices, and plating.
- b. **Conductor width and spacing**—impacted by artwork, imaging, copper foil thickness, etching and plating. The DWB conductor is determined by wire size selection, and can be spaced on a variable XY grid or on the 45 degree diagonal.
- c. **Conductor geometry**—impacted by imaging technique, cleaning, etching and plating. The DWB inherent wire uniformity is not affected by subsequent fabrication processing.
- d. **Dielectric spacing**—impacted by choice of prepreg or bonding layer or film and lamination conditions.

Note: Prepreg thickness (and therefore permittivity) may vary with pressing conditions. For calculation purposes, the designer should consider the effective permittivity and thickness of a prepreg after the lamination cycle and account for any permittivity mismatches that may exist between the prepreg and other layers.

4.2 Component Packaging

4.2.1 Device The component package must be considered when selecting high speed design rules and determining properties. The device package will establish thermal and electrical guidelines. In passive components the predominate factor will be the lead length. The leads provide additional inductance and capacitance which will affect propagation speed and switching transients. To minimize these effects the leads should be trimmed as short as possible or removed. Surface Mount Device packaging can provide leadless devices which can be directly mounted to the interconnecting substrate. It is important to note that component data sheets often do not provide parasitic values for high speed noise and propagation speed calculations.

Active devices, such as integrated circuits, are often offered in several package styles that provide various electrical and thermal performances. In general use, DIP packages have been

the predominate package in either plastic or ceramic. These typically are the largest packages and provide the worst high speed operating environment. The next best package style is the Surface Mount Package. These are offered in either Chip Carrier or Small Outline IC packages. These typically will reduce the lead capacitance and inductance. SM packages can easily be automatically assembled and handled. To obtain the optimum performance from the device, assuming operating conditions and reliability standards can be met, the die should be directly mounted to the substrate using either the Chip-on- Board (COB) or Tape Automated Bonding (TAB) approach. These offer the optimum approach since no additional capacitance or inductance is added with the exception of the bond wire (for COB) or copper conductor (for TAB).

4.2.2 Connectors Board to board connections are often the most troublesome high speed connections because a continuous signal path is not possible due to mechanical constraints. There are two primary approaches to reduce the signal discontinuity.

The first approach assumes that the connector style is fixed, so the pinout must be modified to provide a good signal path. Non-differential signals reference between the active signal line and a reference plane; either a voltage or ground plane, whichever is closest.

Board to board connections are often troublesome because of mismatches in characteristic impedance. Non-differential signal conductors rely on controlled geometries and nearby AC reference planes (either DC voltage or ground planes) for impedance control. These geometries are interrupted in the connector.

Efforts to control signal and reference pin quantity and location in the connector should be made to control electrical performance.

To reduce the noise more reference pins must be added to reduce the distance and sharing problems. Generally a 3:1 signal:reference pin ratio is sufficient. The best ratio is 1:1, but may be too expensive, or consume too much real estate.

The second approach is to modify the connector. The intent is to minimize the discontinuity distance between boards. Either shortening the pin length, or adding reference ground plane within the connector can be used.

4.2.3 Cables High-speed cables must provide a good signal environment. There are three areas that must be considered; signal propagation speed, crosstalk, and induced noise.

Crosstalk can be minimized by several methods. The easiest is to put ground lines between the signal lines to isolate adjacency. A ground plane can be added which lowers the signal line impedance. The best method is to completely isolate signals using a coax line environment. This provides total isolation, but also is the least dense approach.

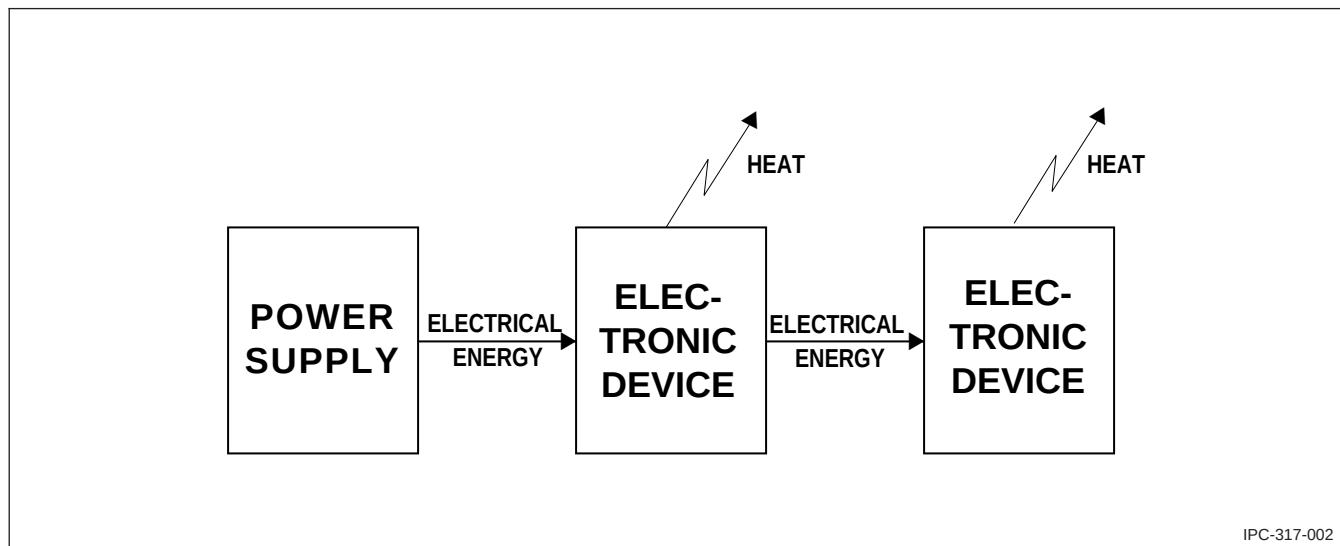


Figure 2 Schematic of information, electrical power, and enthalpy flows

Induced noise coupled onto the lines can be lowered by putting a shield between the signal line and the radiating source. This can be accomplished by using the ground planes mentioned above, or providing an additional shield plane over the entire structure.

4.3 Thermal Considerations Electronic equipment processes information at the expense of electrical energy. The electrical energy fed to the machine is converted into other forms of energy and dissipated into the machine environment. There are two main ways of dissipating this energy;

- electromagnetic radiation and
- heat (thermal energy)

The electromagnetic radiation is generated because interconnections between two points on a board act as an unintentional antenna. The greater the area enclosed by the loop and the higher the frequency and the input current, the higher the level of energy radiated from the system. Even though the continuous increase of signal speed in equipment increases the amount of radiation, the quantity of energy lost in this way is negligible when compared with the quantity of energy converted to heat. Because industry regulations limit the amount of energy radiated from the system in the form of electromagnetic waves, this form of energy is generally captured by enclosures and eventually transformed into heat before it dissipates to the environment.

In order to understand the new aspects of the problem created by increasing the signal speed, one has to start by considering that with slower technologies the partitioning of the board is independent of the electrical signal characteristics. Under such conditions, the device positioning on the board and the interconnect routing can be done keeping a few considerations in mind, such as thermal requirements. Under the high-speed conditions, the characteristics of the signal will practically dictate the positioning of the device, the routing of the interconnections, and the material to be used as well as

the size and characteristics of the device package. All of these determinants will have very strong impact on the selection of the cooling option and the entire thermal design of the system.

4.3.1 System Level Impacts The increasing of the signal speed is necessary because it can increase the quantity of information that is processed per unit of time. As mentioned before, electronic equipment processes information at the expense of energy (electrical) which is absorbed from the source and lastly transformed into heat which must be removed from the system. For example, Figure 2 shows a schematic representation of flows of information, electrical energy and heat in a computer room environment.

With electronics becoming more powerful due to the use of high speed technology the energy required to operate the whole system of information processing and heat disposal is becoming a matter of great concern to both the manufacturer and customer alike. Translating this issue into thermal terminologies; "high speed" often means more heat dissipation per unit volume. Ambient air generally is the ultimate heat sink, therefore it is expected that the temperature of this air will increase resulting in a "hotter" environment for any considered device. The possible solutions at the system level are:

- increasing ventilation in order to reduce the air temperature by injection of cold air from outside
- use of heat exchangers (air to water or coolant) in order to evacuate the heat accumulated in the air in such a way as to reduce the ambient air temperature
- use of active mechanical systems for air conditioning
- replace the air as a cooling agent with other fluids which have a higher specific heat capacity and are easier to circulate and refrigerate (such as water, freons and other organic fluids)

4.3.2 Board Level Impacts The effect of heat on high-speed signals can be immense. Electronic signals typically degrade as the temperature increases. Slower signal transition times result and they may become more sensitive to system electrical transients.

The success of any approach depends mainly on the ability of the designer to find a way to “spread” the concentrated heat over a larger area in order to reduce the peaks of the temperature field created by uneven power dissipation. This task is especially difficult today when we consider the properties of the materials involved in high-speed technology: materials with a low permittivity are needed, but these tend to have very poor thermal conductivity as well. For example, in order to spread the heat conducted by an active device, hybrid technology with a ceramic substrate is usually utilized. If the requirements for speed are very high, ceramic substrates may not be a viable option because they have a permittivity 2 to 4 times that of FR-4 glass epoxy. Possible solutions to confine this problem are;

- better air flow management that ensures directing of the air to overheated areas
- conduction cooling and thermal spreaders (the heat is conducted to larger areas from which it can be removed)
- immersion of the electronics in dielectric fluids

Immersion cooling could be considered a very costly, efficient way of dealing with both high power dissipations as well as uneven dissipations of high concentrations in small volumes.

Beside the capability to spread heat rapidly into the entire volume of the enclosure these fluids can also act as cooling agents by absorbing the heat from the devices and transferring it either to another cooling loop or directly to the environment. The boiling temperature of the immersing fluid can be selected in such a way as to coincide with the maximum temperature admissible in the system. Phase changing of the fluid (boiling and condensation) could practically maintain the temperature of the electronics at a preset constant.

In order to understand the impact that high-speed technology has had on thermal design one has to consider the multi-chip modules symbolized in Figure 3 by double circles. High speed multi-chip modules are created by joining together a certain number of semiconductor chips with controlled impedance transmission lines in order to achieve particular electrical performance. However, grouping the devices close together in order to reduce interconnection distance may produce localized hot spots.

4.3.3 Device Level Impacts The component package has a direct impact on the performance of the device. At the same time the thermal characteristics of the device package are worsening almost linearly with the decrease of the device size. Generally, a way of improving the device package thermal performance is the use of ceramic materials for enclosures. As specified in the previous discussion ceramic materials have higher electrical permittivity which will negatively impact elec-

trical performance of the package if very high-speed devices are involved. Low permittivity materials that improve the electrical performance tend to be very poor thermal conductors and also trap heat inside the semiconductor enclosure. Higher speed is usually associated with a temperature rise in the semiconductor itself and thus presents an important challenge when high reliability of the product is required. Reliability decreases as temperature rises.

4.4 Component Placement Component placement is a critical factor in the design of high-speed systems. The effects of improper placement can be significant and include concerns in the following areas.

- Crosstalk Management
- Impedance Control
- Power Distribution
- Thermal Management
- System Cost

4.4.1 Crosstalk Management Typically, crosstalk is a concern when high-speed devices are used because of the high harmonic frequency content. Mixing logic families also causes concern because of the mixture of various voltage swings, noise margins and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL swings 3 volts and the ECL family has only a 100 mV DC noise margin significant undesired coupling can occur.

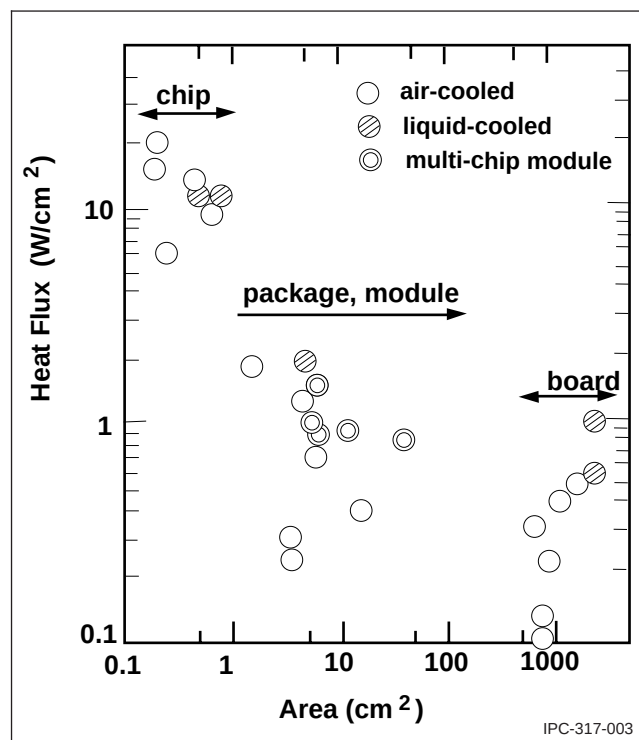


Figure 3 Heat flux vs. component area

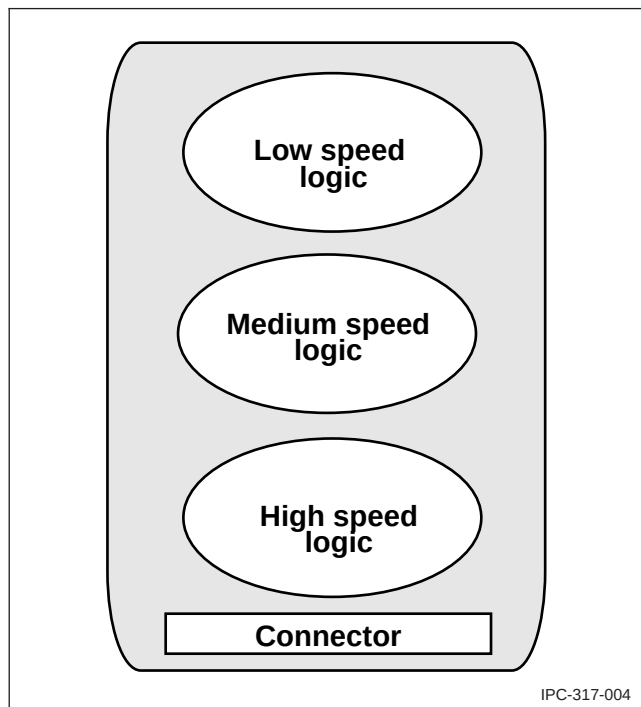


Figure 4 Component placement guideline

When copper planes are used to distribute logic levels, crosstalk (coupling) can also occur through the ground return path for these signals. This is called common mode impedance coupling. Essentially, a returning signal causes a ground potential rise due to the DC resistance of the plane. This problem can be very significant especially in analog circuitry when digital logic is present.

Several techniques can be used to control crosstalk in these environments.

- a. Confine logic families geographically.
- b. Restrict signal conductors for each logic family to those areas.
- c. Provide separate return paths for each logic family.
- d. Place components away from I/O connector in descending order of speed (see Figure 4).
- e. Terminate controlled impedance conductors to reduce reflections which generate more noise.
- f. Restrict conductor parallelism.
- g. Specify and control conductor to conductor spacing.
- h. Place components close together to minimize conductor lengths and parallelism.
- i. Lower the relative permittivity
- j. Reduce the signal to ground separation

The impact on circuit board design due to these considerations will include:

- a. Circuit board technology must now be capable of managing crosstalk.
- b. Multiple power and ground planes required.
- c. Added density due to the addition of terminations and tight placement.
- d. Selective signal routing criteria.

These can greatly increase complexity and place limitations on the available circuit board technology.

4.4.2 Impedance Control In cases where high-speed signals are being transmitted, the signal conductors may need to be considered as transmission lines. This means, as a minimum, specifying the characteristic impedance of those lines. Since transmission lines should be terminated in their own impedance, a designer must provide for termination resistors.

Specifying a controlled impedance board and providing for termination resistors will add complexity to the design.

- a. Termination resistors (one for each signal line) increase density and complexity.
- b. Placement should be made so that each signal travels the shortest path from source (first point) to termination. Poor placement can result in very dense signal routing.
- c. Circuit board technology must now be capable of controlling impedance.
- d. Minimum component to component spacing may eliminate the need for controlled impedance lines but may greatly increase density.

4.4.3 Power Distribution Higher speed devices require the power supply to provide energy quickly. Figure 4 illustrates a typical board placement which shows the highest speed logic near the connector and the lowest speed logic away from the connector (This assumes that power is being provided from off the card). Placement of these devices is not only dependent on performance requirements, but also on thermal requirements and capabilities.

4.4.4 Thermal Management As mentioned, high-speed devices can consume great amounts of power, and consequently dissipate much heat. In the placement of components, the following thermal management techniques should be considered.

- a. When possible, "hot" components should be spaced apart as greatly as possible.
- b. Convection Cooling—Components should be placed such that air flows parallel to component orientation.
- c. Conduction Cooling usually involves the placement of a metal 'heat sink' or 'chill plate' on the surface or buried within the board. In these applications, placement must allow for sufficient metal surface area (i.e. usually requires greater component spacing).

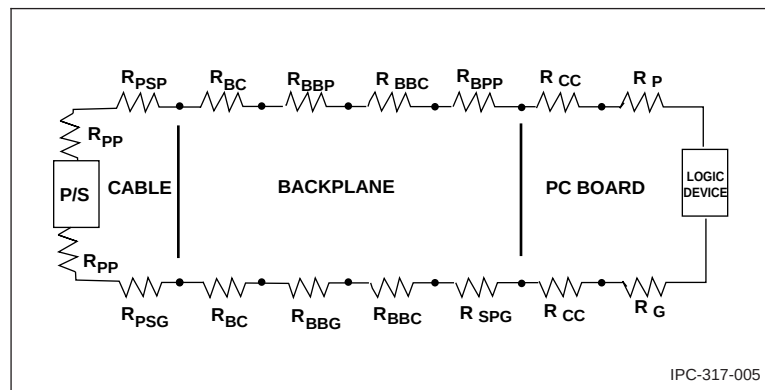


Figure 5 DC distribution model

4.4.5 System Cost Consideration should always be given to the cost of design and manufacturing. Generally, complexity adds density and cost. Cost does not necessarily just mean dollars. Cost can include lead times and reliability. Over-specifying a design "to be sure it will work" can significantly impact total cost.

Designing high-speed circuits is rarely a simple matter. There are many factors to take into consideration which usually act in direct opposition to one another.

Placing high-speed components closely together might reduce the need for transmission line parameters and reduce crosstalk problems, but may result in thermal management problems and increase the number of layers in a circuit board (due to increased density). Increasing the spacing will reduce the thermal problems but could add crosstalk and impedance restrictions. We can see that in high-speed design there are many considerations. It is the job of the circuit designer to understand the system specifications and weigh the alternatives to provide the simplest, cost effective, reliable solution for meeting those specifications.

5.0 Electrical Considerations

5.1 Power Distribution This section presents information used for calculating DC and AC noise characteristics for system power distribution. Factors degrading power distribution may be grouped into two major categories; Metallic losses and dielectric losses. Spurious radiation loss is generally negligible.

The DC power distribution system encompasses the system from the output of the power supply to the input of each device. For systems with many cards and supplies a simulation of the interaction of each component is desirable to verify and assist the design effort.

5.1.1 System DC Model The DC distribution model is comprised of lumped resistance for each element in the system. Figure 5 shows the interconnection and the major sub-sections of the model. This DC model analysis determines the DC voltage drop between the power supply and every inte-

grated circuit location. The major elements in this model are described below.

5.1.1.1 Power Supply To Power Supply Cable (R_{PP}) R_{PP} is the contact resistance of the power supply cable to the power supply output. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc. to keep the voltage drop less than 5 mV.

5.1.1.2 Power Supply Cable/Harness (R_{PSP} , R_{PSG}) This is the resistance due to the interconnection cable or harness from the power supply to the backplane or backplane power distribution busbar. The interconnection can take the form of a cable (circular or flat) or a busbar. R_{PSP} is the resistance of the positive voltage cable. R_{PSG} is the resistance of the power supply ground return cable. Typical resistance for various gauges of copper stranded, rope wound, medium hardness cables at 25°C are listed in Table 1.

5.1.1.3 Power Supply to Busbar Connection (R_{BC}) This is the contact resistance of the power supply cables to the backplane busbar. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc.) to keep the resultant voltage drop less than 5–10 mV.

5.1.1.4 Busbar (R_{BBP} , R_{BBG}) This is the resistance of the backplane power distribution busbars from the power supply

Table 1 Copper Wire Characteristics

Gauge	Number of strands	Diameter (in.)	Area sq. in.	Resistance mΩ/ft.
2/0	19	0.419	0.1045	.08224
1/0	19	0.373	0.0829	.1037
1	19	0.332	0.0657	.1308
2	7	0.292	0.0521	.1649
3	7	0.260	0.0413	.2079
4	7	0.232	0.0328	.2622
5	7	0.206	0.0260	.3306
6	7	0.184	0.0206	.4169
7	7	0.164	0.0164	.5257
8	7	0.146	0.0130	.6629
9	7	0.130	0.0130	.8359
10	7	0.116	0.0082	1.054
12	7	0.092	0.0051	1.676
14	7	0.073	0.0032	2.665
16	7	0.058	0.0020	4.237
18	7	0.046	0.0013	6.738
20	7	0.036	0.0008	10.71

Table 2 Copper Busbar Resistances/ft

Cross-section Area (sq. in.)	Resistance (mΩ)
0.1662	.050
0.1318	.063
0.1045	.080
0.0829	.102
0.0657	.128
0.0521	.162
0.0413	.204
0.0328	.257
0.0260	.324
0.0206	.409
0.0164	.515
0.0197	.650
0.0103	.820
0.0082	1.033
0.0065	1.30
0.0051	1.64

cable contact to the backplane contact. R_{BBP} is the positive busbar resistance. A busbar is a metal strip which has a lower resistance than the backplane or circuit board. R_{BBG} is the ground return busbar resistance. For multiple backplane connections this resistance will be modeled as a series of resistances between each backplane connection point. Cross-sectional resistances for copper (99% pure) at 25°C are listed in Table 2.

5.1.1.5 Busbar to Backplane Connection (R_{BBC}) The contact resistance of the backplane busbar to the backplane. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact.

5.1.1.6 Backplane (R_{BPP} , R_{BPG}) This is the plane resistance from the busbar contact to the circuit board (daughter card) connector. R_{BPP} is the positive voltage plane resistance. R_{BPG} is the ground return plane resistance. Since most power distribution systems have distributed daughter card contacts R_{BPP} and R_{BPG} will be the resistance between each contact point.

5.1.1.7 Backplane to Daughterboard Connector (R_{CC}) This is the backplane to daughterboard connector pin and contact resistance. This resistance should be the value after a large number of insertions and extractions. For a multiple backplane to daughterboard interconnect scheme the resistance will be broken down into each contact. For lumped connector pin locations, the pin resistances can be paralleled. For two piece connector systems R_{CC} is the total resistance for both connectors.

5.1.1.8 Daughterboard (R_P , R_G) This is the power plane or line resistance for the daughterboard. R_P is the positive voltage plane resistance. R_G is the ground return plane resistance.

5.1.2 Power Plane Impedance The power distribution planes utilized in backplanes and daughterboards do not have zero impedance. Likewise the power supply doesn't have a zero source resistance. A high level model of a multilayer power distribution network is shown in Figure 6.

In the above figure the power supply is represented by a voltage, source V_S , R_{SP} , and R_{SG} . The distribution impedances are broken out as backplane and daughterboard sheet inductances, resistances, and plane-plane capacitance.

5.1.2.1 AC Impedance The power distribution AC impedance is subdivided into three components as shown in Figure 7. The first is the switching transient impedance (Z_{SW}).

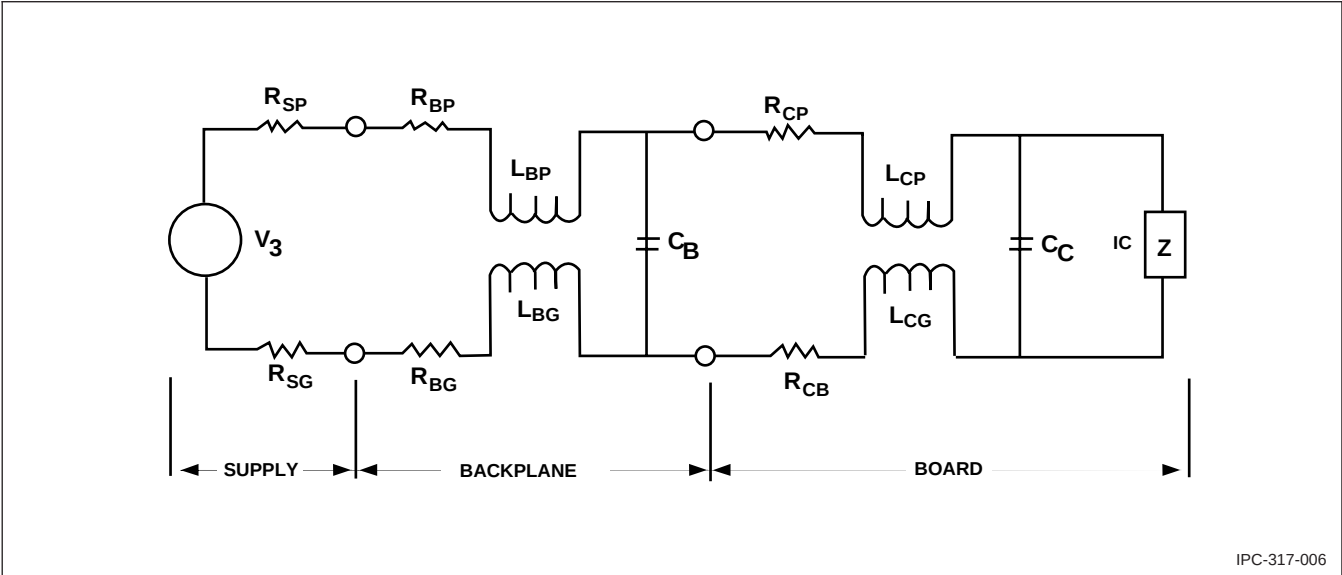


Figure 6 DC power distribution system (without remote sensing)

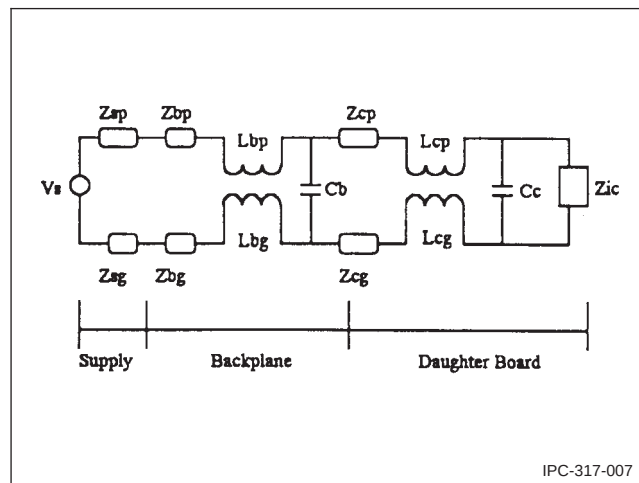


Figure 7 Decoupling impedance model—power supply

This impedance is the interconnect between the closest discrete decoupling capacitor and the component. This impedance can be reduced by using internal power planes that are very close.

The second component is the impedance due to the bulk capacitor charging the IC decoupling capacitors (Z_{BC}). The current in this impedance is lower frequency and higher amplitude than the current in the first component. The voltage drop due to the lower impedance because of the lower frequency involved will be less than the above case.

The bulk decoupling capacitance refresh component (Z_{RC}) is the final element of the circuit board decoupling impedance. This current is responsible for recharging the bulk capacitors. It is supplied from the power supply and will usually have the lowest frequency component of the current.

Each of the board impedance components will be modeled as a transmission line plane-over-plane network. This closely models the worst case configuration because of the regular layout of the printed circuit boards. A brief explanation follows.

The IC's are laid out in regular rows and columns and assuming that every device switches simultaneously then the current will maintain an even distribution as it did in the DC case. The general impedance equation for parallel planes as follows:

$$Z_p = \text{SQRT}(R_p^2 + (L_p^2 - C_p^2)) \quad 5.1)$$

Where L_p = Plane Inductive Impedance
 R_p = Plane Resistance
 C_p = Plane Capacitive Impedance

5.1.2.2 DC Resistance The static voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance, R_T .

$$R_T = 679 / T_p \text{ } \mu\Omega/\text{square} \quad 5.2)$$

where, T_p = thickness of plane (mils)

A model analysis is used to determine R_T between each inte-

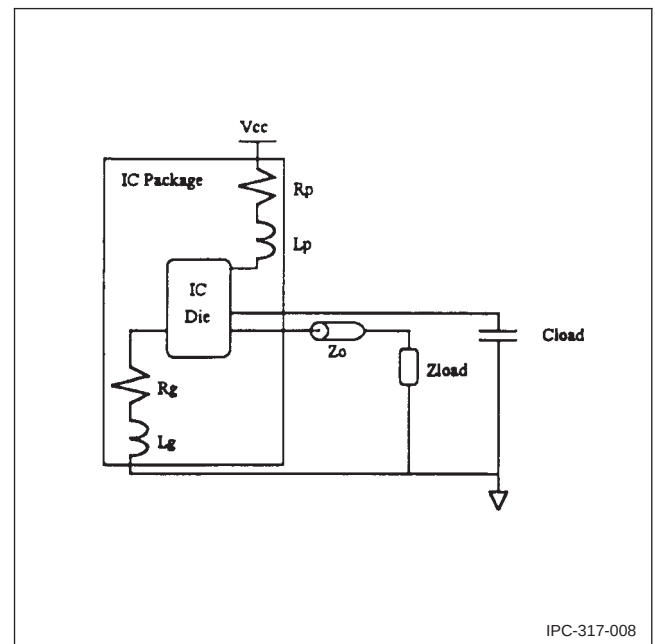


Figure 8 Device decoupling model

grated circuit location. A computer program can be utilized to simplify the calculations. Each device is modeled as a point load and each connector pin is treated as a point source.

5.1.3 Integrated Circuit Decoupling A packaged device must provide sufficient current for its circuitry to operate. This includes high peak current requirements during output switching. The circuit board power system must provide this current without lowering the input supply voltage below its required minimum level.

When the power supply is too far away or the stored energy in the board is insufficient, capacitors are placed near the devices, connected between the power and ground planes to provide this current. In a sense, these capacitors provide the charge current to the device instead of the power planes. The power plane creates a capacitor which can also provide a small amount of high frequency current. These planes should be spaced very close to maximize its capacitance. When they discharge their current into the device they quickly recharge from energy stored in slower discharging capacitors and power supplies in time for the next required discharge.

5.1.3.1 Decoupling Model Figure 8 presents a device decoupling model. Shown are the decoupling capacitor, power planes, signal load, and device models. The device decoupling system is composed of several elements. Every element can be modeled as a network of resistors, capacitors, and inductors. Figure 8 illustrates the interconnection of the following decoupling system components:

- Decoupling Capacitor
- Device Power Lead
- Device Ground Lead
- Transmission Line Load

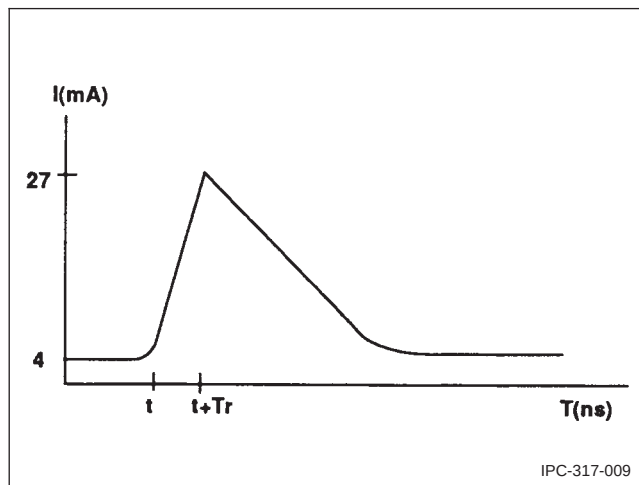


Figure 9 74S00 Typical output switching current

- Capacitive Load – C_L , R_L , L_L
- Power Plane – R_{PL} , C_{PL}

5.1.3.2 Switching Current Frequency Content An integrated circuit has two power supply current components; steady-state bias and output drive. Component data sheet provide these current specifications.

The steady-state bias current is listed over the full temperature and supply voltage specifications. On large devices, such as microprocessors and memories, an average value is provided for power supply size estimation.

The output drive current is typically not specified and must be calculated. Because the signal loads and the device outputs are non-linear, the current is typically best characterized by a time dependent current waveform. Figure 9 presents a typical waveform for a single output of a 74S00 Schottky TTL device.

This waveform shows both the steady-state bias current and output drive current. The 4mA current steady-state level, as shown, raises the entire output switching waveform. As the output switches the current increases at the same rate as the output's risetime. It peaks when the output short circuit current is achieved and decays at a rate based on the output loading characteristics.

The frequency response required by the decoupling capacitor system may be predicted by transposing the time domain waveform into its frequency components using a Fourier Transform. The most critical frequencies are generally the result of the risetime, not just the primary clock frequency.

5.1.3.3 Inherent Plane Electrical Model Section 5.1.2.1 presented the parallel plane impedance of a two plane power distribution system. The power distribution model can be partitioned on a per device basis. In the per device model, the plane inductance (L_P), parallel-plane capacitance (C_P), parallel-plane impedance (Z_P), and plane resistance (R_P) are:

$$L_P = L_G = 0 \quad 5.3)$$

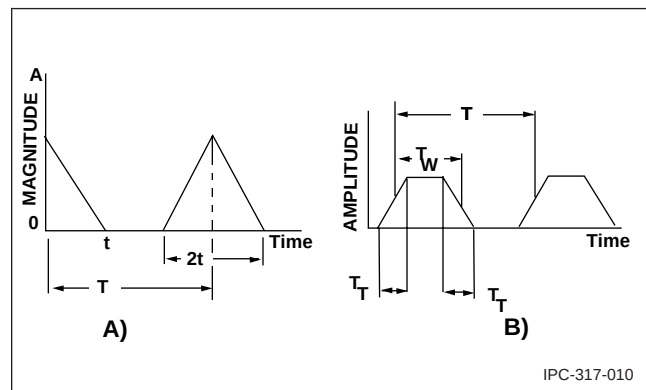


Figure 10 Capacitive and transmission line current pulses

$$R_P = R_G = R_T \cdot N \text{ ohms [from 5.2]} \quad 5.4)$$

$$C_P = \epsilon_r \cdot \epsilon_0 \cdot S / H = 0.225 \times 10^{-6} \cdot \epsilon_r \cdot S / H \text{ pF} \quad 5.5)$$

where, R_T = Power plane resistance

N = Number of squares

S = Plane area (square inches)

H = Plane separation distance (inches)

5.1.3.4 Device Output Load Models The signal line load will have two configurations: capacitive line, and transmission line. A capacitive load requires a triangular current pulse at the rate of the output edge transition rate. The current pulse will only occur during the transition.

The transmission line load behaves resistively to the incident signal. The output provides a trapezoidal pulse to the line while the transmission line is active. The I_{cc} requirements have this trapezoidal wave form versus a triangular waveform for a capacitive load. The I_{cc} waveforms for capacitive and transmission line loads are shown in Figure 10. Figure 11 presents the Fourier Transform for the waveform presented in Figure 10.

5.1.4 Decoupling Capacitance Decoupling capacitors provide current to devices until the power supply can respond. High frequency switching, which is composed of a broad spectrum of current frequencies, requires several low to

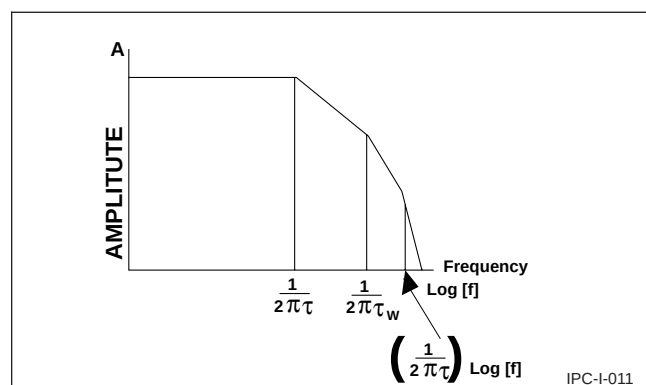


Figure 11 Fourier transform

high frequency capacitors. This is because a single capacitor typically cannot provide such a broad frequency.

5.1.4.1 Switching Transient Capacitance Switching transient capacitance provides very fast energy to charge the output sections of the device during an output transition. This typically is the highest speed content of the waveform and requires the least energy. If insufficient energy is available, the signal transition time will degrade prior to leaving the device package.

In very high-speed devices, the decoupling capacitance may be required to be built into the package to minimize the lead inductance between the capacitance and the device, or located nearby.

When adjacent power planes are provided high speed switching current is provided prior to current being supplied by the discrete decoupling capacitors. This capacitance is increased as the planes are spaced closer together.

5.1.4.2 Line Charging Capacitance Line charging capacitance provides switching current to charge the signal line after the signal reaches the lines. The charge current is required until the line reaches its quiescent state. If insufficient capacitance/ current is provided, the edge transition time will degrade.

Two types of line charging capacitance are required: one for capacitive lines and one for transmission lines. Capacitive line charging requires a relatively slower charging rate than a transmission line, but must provide more current. A transmission line requires a slower, but typically longer pulse to keep the line charged until all of the reflections are over.

When adjacent power planes are provided high speed switching current is provided prior to current being supplied by the discrete decoupling capacitors. This capacitance is increased as the planes are spaced closer together.

5.1.4.3 Low Frequency (Bulk) Capacitance Low frequency capacitance is often termed bulk capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors, and provide switching current for lower frequency requirements.

5.1.4.4 Capacitor Model Capacitors with shorter leads provide current faster because the lead inductance is much lower. In high-speed designs changing the decoupling capacitors from leaded to leadless SMD capacitors can dramatically increase the circuit performance. The optimum scenario is when the capacitance can be provided within the component package, on the MCM, in the hybrid, or in the circuit board.

The lumped constant equivalent circuit of the capacitor is illustrated in Figure 12. R_{SH} is the insulation resistance and has a value >100 Mohms. It has minimal effect on the operation of the capacitor and will be omitted from further discussions. R_C is the series resistance. L_C is composed of lead and plate inductance. C_C is the bulk capacitance of the capacitor. In a

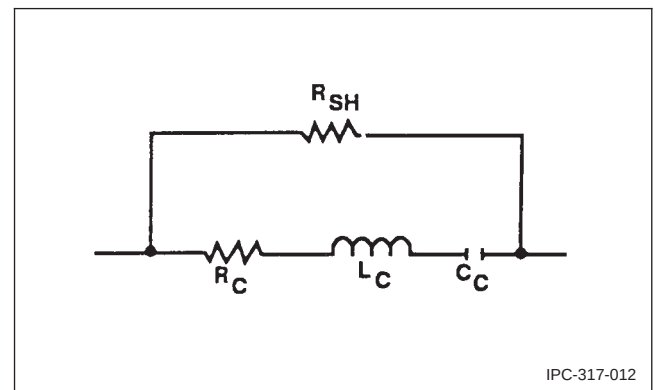


Figure 12 Capacitor equivalent circuit

DIP capacitor the plate inductance is minimal relative to the lead inductance, which is approximately 10 nH/in.

The total effective impedance, Z_C of the capacitor is

$$Z_C = \sqrt{R_C^2 + (X_L - X_C)^2} \text{ ohms} \quad (5.6)$$

where, R_C = Series lead and plate resistance

$$X_L = 2 \cdot \pi \cdot f \cdot L_C \quad (5.7)$$

$$X_C = 1/(2 \cdot \pi \cdot f \cdot C_C) \quad (5.8)$$

The series inductance and capacitance yield a resonant frequency at which the effective impedance will equal the series lead resistance, R_C . Below resonance Z_C is dominated by the capacitive reactance. Above resonance Z_C is primarily inductive reactance. Impedance values for 0.1 μF and 0.01 μF DIP and 1206 style capacitors are presented in Figure 13.

5.1.5 Device Power Dissipation The system power dissipation can be calculated by the addition of the component power dissipations. For example, the power dissipation categories are:

- 1) Bipolar SSI/MSI
- 2) CMOS SSI/MSI

5.1.5.1 Bipolar SSI/MSI The power dissipation has three primary components:

f	DIP Style				1206 Style			
	0.1 μF		0.01 μF		0.1 μF		0.01 μF	
MHz	X_L	X_C	X_L	X_C	X_L	X_C	X_L	X_C
10	0.6	0.16	0.5	1.6	0.1	0.16	0.1	1.6
100	5.9	0.016	4.7	0.16	1.2	0.016	1.2	0.16
150	8.9	0.011	7.1	0.10	1.9	0.011	1.9	0.10
200	11.8	0.008	9.4	0.08	2.5	0.008	2.5	0.08
300	17.6	0.005	14.0	0.05	3.8	0.005	3.8	0.05
350	20.7	0.004	16.5	0.05	4.4	0.004	4.4	0.05
400	23.4	0.004	18.7	0.04	5.0	0.004	5.0	0.04
L_C (nH)	9.4		7.5		2.0		2.0	
R_C (ohms)	0.065		0.15		0.065		0.15	

Figure 13 Impedance for 0.1 μF and 0.01 μF DIP and 1206 capacitors

1. I_{cc1} and I_{cc2} steady state
2. Output load charging
3. Internal dynamic charging

I_{cc1} and I_{cc2} Steady State Currents

These values are obtained from the vendor data sheets. For a statistically accurate worst case analysis 10% above typical values used at a 50% duty cycle are used. Or,

$$\begin{aligned} I_{cc,dc} &= (1.1/2) \cdot (I_{cc1, nom} + I_{cc2, nom}) \text{ [mA]} \\ &= 0.55 \cdot (I_{cc1, nom} + I_{cc2, nom}) \text{ [mA]} \end{aligned} \quad 5.9$$

or,

$$P_{cc, dc} = V_{cc1, nom} \cdot I_{cc, dc} \text{ mW} \quad 5.10$$

Output Signal Load Charging Current

For a worst case analysis use the maximum possible outputs switching at a given time driving their statistically maximum loads. The following decoupling analysis will show that the capacitive load charging current can be approximated as triangular. Thus,

$$I_{cl} = 0.5 \cdot C_L \cdot dV_c/dT \text{ [A]} \quad 5.11$$

$$= 0.5 \cdot C_L \cdot (V_{oh} - V_{ol})/T_{LH} \quad 5.12$$

and,

$$P_{CL} = V_{out} \cdot I_{cl} \cdot N \quad 5.13$$

$$= (V_{CC1, nom} - V_{OH}) \cdot I_{cl} \cdot N \quad 5.14$$

where, I_{cl} = Load charging current
 D_T = Output edge transition rate
 C_L = Load capacitance
 T_{LH} = LH edge transition rate
 P_{CL} = Device power dissipation due to load
 N = Number of outputs

Internal Dynamic Charging

As the system clock frequency increases the dynamic power dissipation will increase due to the inherent device capacitance. Vendor data provides the power increase with frequency.

Total Power Requirements

Total power requirement is:

$$P_{TOT} = K_D \cdot (P_{CC1} + P_{CC2} + P_{CL}) \text{ [W]} \quad 5.15$$

where, K_D = Switching frequency multiplier

5.1.5.2 CMOS Power consumption for CMOS is dependent on the power supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC}V_{CC}$, and the switching power required by each device within the package. The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD})V_{CC}^2 f \quad 5.16$$

5.2 Permittivity

5.2.1 Relative Permittivity The relative permittivity, ϵ_r , of a substance is defined as the ratio of the permittivity of the material to that of free space. The term relative permittivity is preferred to dielectric constant, since this quantity is not a constant, but varies with several parameters. Factors that influence the relative permittivity of a given material include: the electrical frequency at which the measurement is performed, temperature and extent of water absorption. In addition, if the material is a composite e.g. a reinforced laminate, the value of ϵ_r may vary enormously as the relative amount of each component of the composite is changed.

5.2.2 Effective Relative Permittivity The effective relative permittivity, ϵ'_r , is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. An experimental value of ϵ'_r may be obtained using a time domain reflectometry (TDR) technique. However, it is frequently more convenient to calculate a value of ϵ'_r from known values of ϵ_r .

If a stripline signal conductor is surrounded by a single dielectric that extends to the ground planes, then the value of ϵ'_r may be equated to that of ϵ_r for the dielectric measured under the appropriate conditions. However, if more than one dielectric is present between the conductor and the ground planes, a value of ϵ'_r is determined from a weighted sum of values of ϵ_r for all the contributing dielectrics. For the purposes of evaluating electrical characteristics of circuit boards, a composite such as a reinforced laminate, with a given ratio of components, is usually regarded as a homogeneous dielectric with an associated relative permittivity.

Some typical electrical configurations are illustrated in Figure 14. For each of the structures: (a) coaxial, (c) stripline and (f) asymmetric stripline, if a single dielectric is employed, then the value of ϵ'_r is taken to be the value of ϵ_r for that dielectric, but for the remaining structures the situation is more complex.

The microstrip case (c), has a compound dielectric medium consisting of the board material and air. For this configuration, an empirical relationship has been derived (Kaupp, 1967) that gives the effective relative permittivity as a function of the relative permittivity of the board material:

$$\epsilon'_r = 0.475\epsilon_r + 0.67 \text{ for } 2 < \epsilon_r < 6 \quad 5.17$$

In this expression ϵ_r relates to values determined at 25 MHz; see the next section for details of frequency dependence.

For electrical configuration (d), the coated microstrip, the following relationship (of unknown origin) is believed to be applicable:

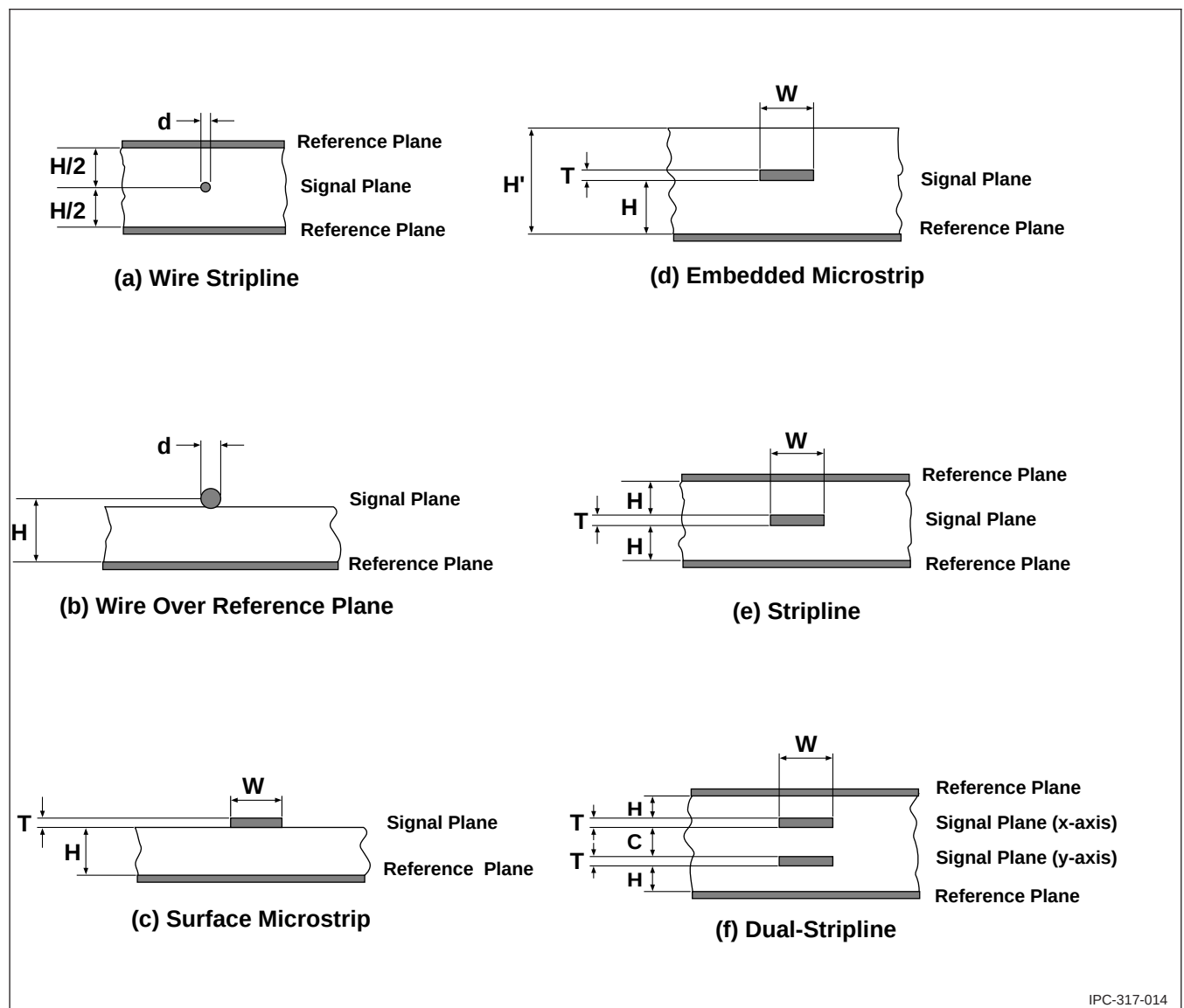
$$\epsilon'_r = \epsilon_r \cdot [1 + e^{(-1.55 \cdot H'/H)}] \quad 5.18$$

H = distance from the reference plane to the signal line

$H' > H + T$

H' is the distance from the reference plane to the top of the dielectric

For the wire-over-ground (b) configuration, if the dielectric



IPC-317-014

Figure 14 Typical electrical configurations

medium extends from the ground plane beyond the conductor, then the latter expression may be employed. If, however, the dielectric extends only to the level of the conductor, then either the latter expression or the relationship derived by Kaupp may be applied.

Unfortunately, none of the relationships provided in this section are applicable to circuit boards constructed of two or more dielectric materials (excluding air). e.g. Microstrip circuitry coated with solder mask, or printed boards fabricated with more than one type of laminate, or discrete wiring boards with their polyimide insulated wires.

5.2.3 Frequency Dependence As has been explained in the preceding section, values of both ϵ_r and ϵ'_r are dependent not only on the material employed, but also on the reinforcement-to-resin ratio (if a composite), temperature, water uptake and the frequency at which the measurement is performed. Once these dependencies are appreciated, steps

may be taken to ensure that electrical measurements are performed under conditions that are pertinent to the final application. However, the frequency dependence of ϵ_r and ϵ'_r is worthy of further comment, since it is not usually obvious at what frequency measurements should be performed.

Some materials, such as an FR-4 epoxy/glass laminate, exhibit a significant frequency dependence of their dielectric properties, and it becomes important to choose carefully the frequency at which measurements are made. It is essential not only to maintain internal consistency, but also to select the frequency such that the dielectric parameters obtained may be used to provide a precise prediction of the electrical characteristics of the finished circuit board. Since most transmission characteristics for a circuit board are determined by TDR measurements, it is appropriate to use the frequency corresponding to these TDR measurements as the frequency of choice for comparing dielectric parameters. Although TDR is a wideband technique and measurements are performed in