



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-D-390A

Automated Design Guidelines

IPC-D-390A

February 1988

A standard developed by IPC

Original Publication
July 1974

2215 Sanders Road, Northbrook, IL 60062-6135

Tel. 847.509.9700 Fax 847.509.9701

www.ipc.org



Documents

Document Sharing Hub

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee (TAEC) that the use and implementation of IPC publications is voluntary and is part of a relationship entered into by customer and supplier. When an IPC standard/guideline is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision.

Adopted October 6, 1998

Why is there a charge for this standard?

Your purchase of this document contributes to the ongoing development of new and updated industry standards. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low in order to allow as many companies as possible to participate. Therefore, the standards revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/790-5372.

Thank you for your continued support.



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-D-390A

Automated Design Guidelines

Developed by the Automated Design Subcommittee of the
Computer-Aided and Design Technology Committee of IPC

Users of this standard are encouraged to participate in the
development of future revisions.

Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798



Documents
Document Sharing Hub

Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Automated Design Subcommittee of the Computer-Aided and Design Technology Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Computer-Aided and Design Technology Committee

Vice-Chairman
Bruce C. Rietdorf
Magnavox Electronic Systems Co.

Automated Design Subcommittee

Chairman
Susan Fitzell
Lange Associate

Technical Liaison of the IPC Board of Directors

Peter Sarmanian
Printed Circuits Corp.

Automated Design Subcommittee

Adams, William C., Data General Corp.
Audeh, Azmi S., Storage Technology Corp.
Baird, John J., General Dynamics
Barbeau, Ed A., Delco Systems Operation
Bever, Bob, Motorola Inc.
Bittle, David W., Beech Aircraft Corp.
Dow, Bruce, Data General Corp.
Faford, Peter R., Data General Corp.
Faris, Fred J., Raytheon Co.
Feldmesser, Howard S., John Hopkins University
Greenwood, Edward C., Raytheon Co.
Hale, Frank, Diceon Electronics Inc.

Hall, William G., Emerson Electric Co.
Kenealey, Gerald W., Control Data Corp.
Klatt, Ken, Scientific Calculations Inc.
Koven, Gary, Dit Mco International
La Porte, Richard L., GTE Government Systems Corp.
Leshinsky, Henry F., Delco Electronics
Mc Caw, Robert, Multiwire
Mc Donald, Robert, Teradyne Telecommunication
O'Connell, John H., GenRad
Parman, Payton, Martin-Marietta Corp.

Partel, Stan, Motorola Inc.
Pericich, Charles E., Mc Donnell Douglas Electric Co.
Rosa, Robert, Scitex America Corp.
Scalia, Philip P., Taylor Instrument
Shaik, Johan S., Automata Inc.
Smith, Monty, Tektronix Inc.
Tande, Marshall, Magnavox Research Labs.
Van Buskirk, Robt. E., Wang Labs.
Veras, J. A., Mc Donnell Douglas Electric Co.
Wedeking, David, Tektronix Inc.
Wetzel, John T., Applied Technology
Wheeler, L. Roy, Boeing Co.
Woodyard, Brian, Advanced Controls

Special Note of Appreciation

The IPC would especially like to thank the following individuals who worked diligently and met several times to complete this document:

Gary M. Ferrari, Advanced Design & Engineering
Susan Fitzell, Lange Associate
Bruce C. Rietdorf, Magnavox Electronic Systems Inc.

Mark A. Savrin, Kulicke & Soffa Industries Inc.
Ernest L. Tibbetts, Martin-Marietta Corp.



Table of Contents

1 SCOPE	1	4.4.1 Introduction	13
1.1 Purpose	1	4.4.2 Types of Checking	14
2 APPLICABLE DOCUMENTS	1	4.4.3 Back Annotation.....	16
2.1 IPC	1	4.5 Approval	16
2.2 AmericanNational Standards Institute	1	4.6 Post Processing.....	16
2.3 Department of Defense	1	4.6.1 Detailed Post Processor.....	17
3 TERMS & DEFINITIONS	1	4.6.3 Line Drawing Procedure.....	18
3.1 Manhattan Distance.....	1	4.6.4 Step and Repeat.....	18
3.2 Crossing Count.....	1	4.6.5 Output Data	20
3.3 Computer Aided Design (CAD)	1	4.6.6 Drill Tapes	20
3.4 Computer Aided Engineering (CAE)	1	4.6.7 Profiling	21
3.5 Computer Aided Manufacturing (CAM)	1	4.6.8 Test.....	21
3.6 Cathode Ray Tube (CRT)	2	4.6.9 Automatic Insertion Tapes	21
3.7 Design Automation (DA).....	2	4.6.10 Documentation.....	21
3.8 Design Rule Checking (DRC).....	2	4.6.11 Wire Wrap Interconnect Lists	25
3.9 Manual Data Input (MDI).....	2	4.7 Final Checking	25
3.10 Numerical Control (N/C)	2	5 DATA MANAGEMENT/CONFIGURATION	
3.11 Packaging & Interconnection Structure (P&IS)....	2	CONTROL	26
3.12 Post Processing.....	2	5.1 Documentation Control	27
3.13 Printed Board.....	2	5.1.1 Document File	27
3.14 Checkplot.....	2	5.1.2 Master Parts File	27
3.15 Net List.....	2	5.1.3 Document/Part Number Assignment	27
3.16 Library	2	5.1.4 Drawing Notes and Peripheral Data.....	27
4 DESIGN PROCESS	2	5.1.5 Parts List Creation (Job Specific File)	27
4.1 Input Package	2	5.1.6 Make-Like Creation	27
4.1.1 Schematic/Logic Diagram.....	2	5.1.7 Data Search	27
4.1.2 Parts List.....	3	5.1.8 Plotter Set-Up Instructions.....	28
4.1.3 End-Product Requirements	3	5.1.9 Master Specification.....	28
4.1.4 Testing Requirements	4	5.1.10 Materials File.....	28
4.1.5 Board Mechanical Outline	4	5.1.11 Notes File	28
4.2 Job Setup	5	5.2 Artwork Layer Identification	28
4.2.1 General Design Rules	5	5.2.1 Mirroring	28
4.2.2 Library Part Shapes.....	8	5.2.2 Layer Number Assignment	28
4.2.3 Board Shape Definition.....	8	5.2.3 Dash Number Assignment	29
4.2.4 Schematic.....	8	5.2.4 New P/W Boards (no change revision level).....	29
4.3 Design	9	5.2.5 Revised P/W Boards	29
4.3.1 The CAD Approach To Placement.....	9	5.2.6 Method of Calculating Dash Numbers for Detail Layers	29
4.3.2 Routers	11	5.2.7 Method of Calculating the Dash Numbers for the Test Coupons.....	29
4.3.3 Completion	12	5.3 Engineering Changes.....	30
4.3.4 Cleanup.....	13	6 DESIGN METHODS AND TECHNOLOGY	
4.3.5 Conclusions	13	CHANGES	30
4.4 Inprocess Checking/Clean-up and Corrections ..	13		



Documents

Document Sharing Hub

6.1	Specific Effects.....	30
6.1.1	Libraries.....	30
6.1.2	Autoplacement.....	30
6.1.3	Autorouting.....	30
6.1.4	Design Rule Check	30
6.2	New Product Development.....	31
7	HARDWARE	31
7.1	Data Entry Devices	31
7.1.1	Lightpens	31
7.1.2	Touchscreens	32
7.1.3	Joysticks.....	32
7.1.4	Trackballs	32
7.1.5	Mice.....	32
7.1.6	Digitizers	32
7.1.7	Voice Data Entry	33
7.1.8	Automated Entry	33
7.2	Output Devices.....	33
7.2.1	Specifying Use	33
7.2.2	Printers.....	34
7.2.3	Plotters.....	34
7.2.4	Copiers.....	35
7.2.5	Camera Systems	35
8	SYSTEM DESCRIPTION.....	35
8.1	Data Entry	36
8.2	Capabilities	36
8.3	Interactive Component Placement	36
8.4	Conductor Routing.....	36
8.4.1	CAD Operation	37
8.5	Output from CAD.....	37
8.5.1	Typical Operation.....	37
8.6	Computer Aided Manufacturing (CAM).....	38
8.7	Automation	39
8.7.1	Levels of Communication.....	39
8.7.2	Levels of Automation.....	39
9	INTERFACE HARDWARE & SOFTWARE.....	39
9.1	Computer Interfacing	40
9.2	Categories of Automation	40
9.2.1	Input/Output Requirements.....	40
9.2.2	A Working Definition of Automation.....	41
9.3	Automation Team	41
9.3.1	Principles of Automation	41
9.4	Interface Techniques.....	43
9.4.1	EDIF Overview	43
9.4.2	IGES Overview	44
9.4.3	PDES	44

9.4.4	IPC Overview.....	45
9.4.5	VHSIC Hardware Description Language (VHDL)	45

Figures

Figure 4-1	Design flow chart.....	3
Figure 4-2	Capacitance vs. line width and spacing for striplines.....	4
Figure 4-3	Conductor thickness and width for surface conductors	6
Figure 4-4	Conductor characteristics	7
Figure 4-5	External annular ring.....	7
Figure 4-6	Solder mask registration.....	8
Figure 4-7	Contact number one dimensioning using secondary datum	8
Figure 4-8	Successive partitions performed by the component placement module	10
Figure 4-9	Automatic router—computer processing	12
Figure 4-10	Number of nonconnects	13
Figure 4-11	Routine check list	15
Figure 4-12	Plot of sample board	19
Figure 4-13	Cookie sheet.....	19
Figure 4-14	Photomaster component side.....	20
Figure 4-15	Photomaster solder side.....	21
Figure 4-16	Dot pattern	21
Figure 4-17	Drill setup for all panels.....	22
Figure 4-18	Single-bit full adder.....	22
Figure 4-19	4-wide 2-input AND-OR-INVERT gate.....	23
Figure 4-20	Symbol outline for 3-input OR element.....	24
Figure 4-21	Logic element drawing for triple 2-input NOR gate.....	25
Figure 4-22	Logic element drawing for dual 2-wide 2-input AND-OR-INVERT gate	26
Figure 5-1	The test coupon, drill drawing, and silk screen would be assigned A -009	29
Figure 5-2	The test coupon, drill drawing and silk screen would advance to -010	29
Figure 5-3		29
Figure 7-1	Pictorial guide to data entry devices	31
Figure 7-2	Impact hammers on writing head strike ribbon to produce dot-matrix image on paper.....	34
Figure 7-3	Images are produced electrostatically. Electrodes place a charge on dielectric paper, which is then passed through a toner.....	34
Figure 7-4	Pen is driven across the paper electro- mechanically with a system of belts and stepper motors.....	35
Figure 7-5	With the electrophotographic method, a beam of light from a fiber optic system projects an image onto light sensitive paper, which is then developed.....	34



Figure 8-1	Interactive computer aided design	36
Figure 8-2	Component relationships	36
Figure 8-3	Conductor movement	37
Figure 8-4	The seven levels of automation	39
Figure 9-1	Workcell elements.....	41
Figure 9-2	Automation matrix for a workcenter	42
Figure 9-3	Electrical neutral data structure roles.....	46

Tables

Table 4-1	Annular Rings (Minimum).....	7
Table 9-1	Long Distance Interfaces	40
Table 9-2	Short Distance Interfaces.....	40
Table 9-3	Mechanization Classes	41



Automated Design Guidelines

1 SCOPE

This guide is a general overview of Computer Aided Design and its processes, techniques, considerations and problem areas with respect to printed circuit design.

1.1 Purpose The purpose of this document is to help the manual Printed Circuit Designer or Design Manager begin to understand how Computer Aided Design affects the design process and how to go about implementing a CAD strategy in an operation which is currently manual.

The guidelines herein describe the CAD design process from the initial input package requirements through to Engineering Change Orders after completed artwork. The impact of technology on CAD, and a general overview of related hardware and software are also discussed.

Although this document outlines CAD operations and definitions, it is not intended as a plan for automation. Each company must develop its own CAD strategy based on its size, product line, facilities and so forth. Providing sufficient detail to fully explain the transition necessary to integrate a CAD system is beyond the scope of this document.

2 APPLICABLE DOCUMENTS

The following documents, of the issue currently in effect, are applicable to the extent specified herein.

2.1 IPC¹

IPC-T-50 Terms and Definitions

IPC-D-310B Guidelines for Phototool Generation and Measurement Techniques

IPC-D-319 Design Standard for Rigid 1 & 2 Sided Printed Boards

IPC-D-350B Printed Board Description in Digital Form

IPC-D-352 Electronic Design Database Description for Printed Boards

IPC-R-700 Modification and Repair of Printed Boards and Assemblies

IPC-CM-770 Component Mounting Guidelines for Printed Boards

IPC-CM-780 Advanced Packaging Guidelines with Emphasis on Surface Mounting

IPC-SM-840 Qualification and Performance of Electrical Insulating Compounds for Printed Board Assemblies

IPC-D-949 Design Standard for Rigid Multilayer Printed Boards

2.2 American National Standards Institute²

ANSI/IEEE Std 91-1984 Graphic Symbols for Logic Functions

2.3 Department of Defense³

MIL-STD-275E Printed Wiring for Electronic Equipment

MIL-STD-2118 Design Requirements for Flexible and Rigid-Flex Printed Wiring for Electronic Equipment

MIL-STD-38510 General Specifications for Semiconductor Devices

MIL-P-55110D General Specification for Printed Wiring Boards

3 TERMS & DEFINITIONS

The definitions of terms used herein shall be in accordance with IPC-T-50 and the following.

3.1 Manhattan Distance The orthogonal distance between any two or more conductivity points of any electrical net.

3.2 Crossing Count The unit for measuring optimum component placement characteristics based on signal of conductor crossovers that are used to provide electrical interconnection between devices.

3.3 Computer Aided Design (CAD) The interactive use of computer systems, programs and procedures in the printed board design process, where decision making activity rests with the operator and the computer provides the data manipulation functions.

3.4 Computer Aided Engineering (CAE) The interactive use of computer systems, programs and procedures in the electronic engineering process, where decision making activity rests with the operator and the computer provides the data manipulation functions.

3.5 Computer Aided Manufacturing (CAM) The processes and methods for using computer systems as tools in any or all phases of product manufacture.

1. IPC, 2215 Sanders Road, Northbrook, IL 60062-6135

2. American National Standards Institute, 1430 Broadway, New York, NY 10018

3. Naval Publications and Forms Center, 5801 Tabor Road, Philadelphia, PA 19120

3.6 Cathode Ray Tube (CRT) That part of the computer terminal used to visually display CAD generated data such as graphics, text, etc.

3.7 Design Automation (DA) The use of computer systems, programs, and procedures in the printed board design process, where the operator provides the input and sets the direction, while the decision making and data manipulation functions rest with computer systems.

3.8 Design Rule Checking (DRC) A computer program that performs continuity verification of all conductive area (signal, power, etc.) and the electrical clearances required to produce an electrical interconnection product.

3.9 Manual Data Input (MDI) Computer input data that is manually generated with or without the aid of data entry devices (keyboard, mouse, light pen, etc.).

3.10 Numerical Control (N/C) The use of mathematics to define, design, or test geometric quantities used in CAD/CAM installations.

3.11 Packaging & Interconnection Structure (P&IS) The general term for a completely processed printed board, ceramic substrate with interconnection wiring, or other combinations of substrates and interconnection wiring, used for the purpose of mounting components.

3.12 Post Processing The “after design” steps required to produce artwork master and other printed wiring tooling.

3.13 Printed Board The general term for a completely processed printed board, ceramic substrate with interconnection wiring, or other combinations of substrates and interconnection wiring, used for the purpose of mounting components.

3.14 Checkplot An interim drawing used for graphical data verification.

3.15 Net List A list of alpha numeric representations, each of which is used to describe a group of two or more points that are electrically common.

3.16 Library A catalog of related items, such as components shapes, land patterns, electrical symbols, etc., that contains all information about the items necessary for processing by the computer systems.

4 DESIGN PROCESS

In electronics today, the design and manufacturing of electronic equipment involves complex conditions. One must evaluate the most cost-effective method for the design of a

system based on the state-of-the-art technology, not necessarily on off-the-shelf components.

With the ever increasing need for integration of various functions, the optimum design is established only through complete component evaluation, proper design, and procurement of existing and fabricated parts.

Without awareness, involvement and proper advice; without the foresight to recognize and take advantage of state-of-the-art technology with maximum integration, a project will not meet market objectives.

Every design usually goes through several phases. These phases are listed below:

- Conceptual Phase
- Conceptual Design Phase
- Preliminary Design
- Product Design Phase
- Validation Phase

Executing these phases requires several design steps. The various steps of the design process are illustrated in the flow chart shown in Figure 4-1.

4.1 Input Package Design and documentation feature requirements that apply to the basic layout, the printed wiring master artwork, the printed circuit board itself, and the end-item printed board assembly, all must be taken into consideration during the design of the board. Therefore, proper data must be supplied to the printed board designer.

When component process and producibility issues have been resolved, substrate circuit layout can commence. This involves coupling component size, pinout, performance, and testability requirements with established design rules.

The inherent electronic performance improvement, resulting from reducing the magnitude and complexity of interconnections, must be balanced against possible interference due to increased packaging density. With experience, design rules will evolve which increase the predictability of this trade-off, but verification is best accomplished by prototype evaluation. Additional trade-off considerations include performance criteria, cost projections, producibility and the status of manufacturing.

4.1.1 Schematic/Logic Diagram The initial schematic/logic diagram designates the electrical functions and interconnectivity of the printed board and its assembly. The schematic diagram should define component identifier, logical connectivity and when applicable, critical circuit layout areas, current requirements, shielding requirements, grounding and power distribution, the allocation of test points, and any pre-assigned input/output connector locations. Schematic information may be hard copy or computer data, generated either manually or automatically.

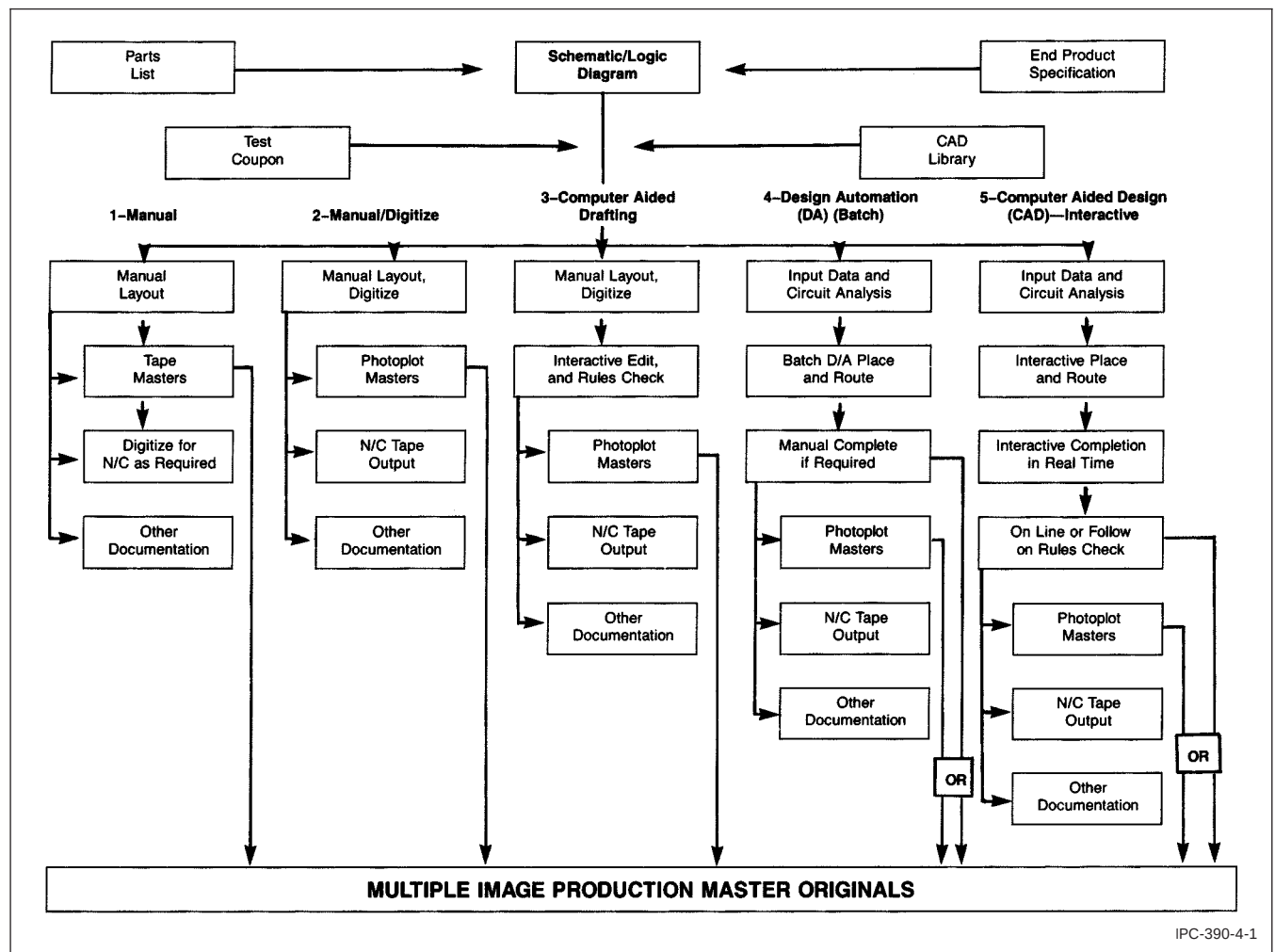


Figure 4-1 Design flow chart

4.1.2 Parts List The parts list may be hand written, typed on a standard form, computer generated, or written on the schematic. When selecting the parts, you should consider the applicability of the parts for printed board mounting (lead lengths and diameters, through holes, surface mount, standard mounting grid, hold downs, adhesives/chips, etc.). The initial parts list must contain the component identifier, quantity of each part, and applicable part number. The initial parts list may also contain a complete description of the part, quantities, manufacturer, and special ordering instructions. Sometimes, for cost analysis purposes, it is also desirable to include the cost of the items needed. What information must be included and how it should be formatted depends upon the standards established by each user.

The parts list is on a separate sheet or in a separate computer file; it must have some identifier which relates it to the schematic. A good practice is to include the name of the board for which the parts list was prepared, the drawing number including the revision and the date with the names of the persons preparing, checking, and approving this document.

Some means of identifying the revision level must be provided.

4.1.2.1 Non-Standard Part Information When non-standard parts are used in the design, the detailed electrical and mechanical/physical description (manufacturer data sheet) shall be provided. Reference this information to the schematic diagram so that the appropriate layout configuration can be determined.

Because non-standard parts are used, and only manufacturing data is available, a specification control drawing should be developed to ensure that future parts match the parts selected for this design. The specification control drawing should provide sufficient details to completely describe the part, including the suggested vendor's part number.

4.1.3 End-Product Requirements The success or failure of a board design depends on many interrelated considerations. For example, the following parameters may affect end-product usage, so the designer should consider them:

- A. Equipment environmental conditions, such as ambient temperature, heat generated by the components, cooling ventilation and vibration.

- B. Maintenance philosophy during the service life of the equipment, especially with respect to component placement that affects component accessibility (Components one-side/Components two-side).
- C. Spacing between boards that might limit lead protrusions and affect the placement of brackets and hardware.
- D. Testing/fault location requirements that might affect component placement, one-sided/two-sided conductor routing, connector contact allocation, etc.
- E. Manufacturability: Production level requirements (quantities) must be considered; i.e., products that will require large quantities of PCBs must be producible at a high production level.
- F. If an assembly is to be repairable, you must consider component/circuit density and the selection of board/conformal coating materials. In general, repair criteria should adhere to the guidelines of IPC-R-700.
- G. Special requirements. Figure 4-2 is one of many charts, tables and illustrations found in the IPC Design Standards such as IPC-D-319, IPC-D-949, etc. to help guide you through your design.

4.1.4 Testing Requirements Good design practice dictates that prior to starting a design, a testability review

should be held. Testability concerns, such as test access, circuit visibility, circuit operation, and special test requirements and specifications are discussed as part of the test strategy. Any conductive pattern board configuration concepts necessary to test the board shall be incorporated into the final board layout.

4.1.5 Board Mechanical Outline The board outline requirements affect good board design. The following should be considered and discussed with the designer:

- A. Electrical restrictions such as the number of layers and layer distribution, material selection criteria.
- B. Mechanical restrictions such as connector locations, cutouts and clearances around the board.
- C. Component mounting, and soldering technologies (wave solder, vapor phase, infrared [IR], etc.), to be used on final board.
- D. Where and how the board is mounted in the next assembly and how it is electrically connected to the assembly. When selecting the location of interconnect points, consider proper flow on and off the board to minimize the effects of electrostatic discharge (ESD) and electromagnetic interference (EMI).
- E. When two assemblies are mounted face to face, component placement considerations relative to component height and interferences must be considered.

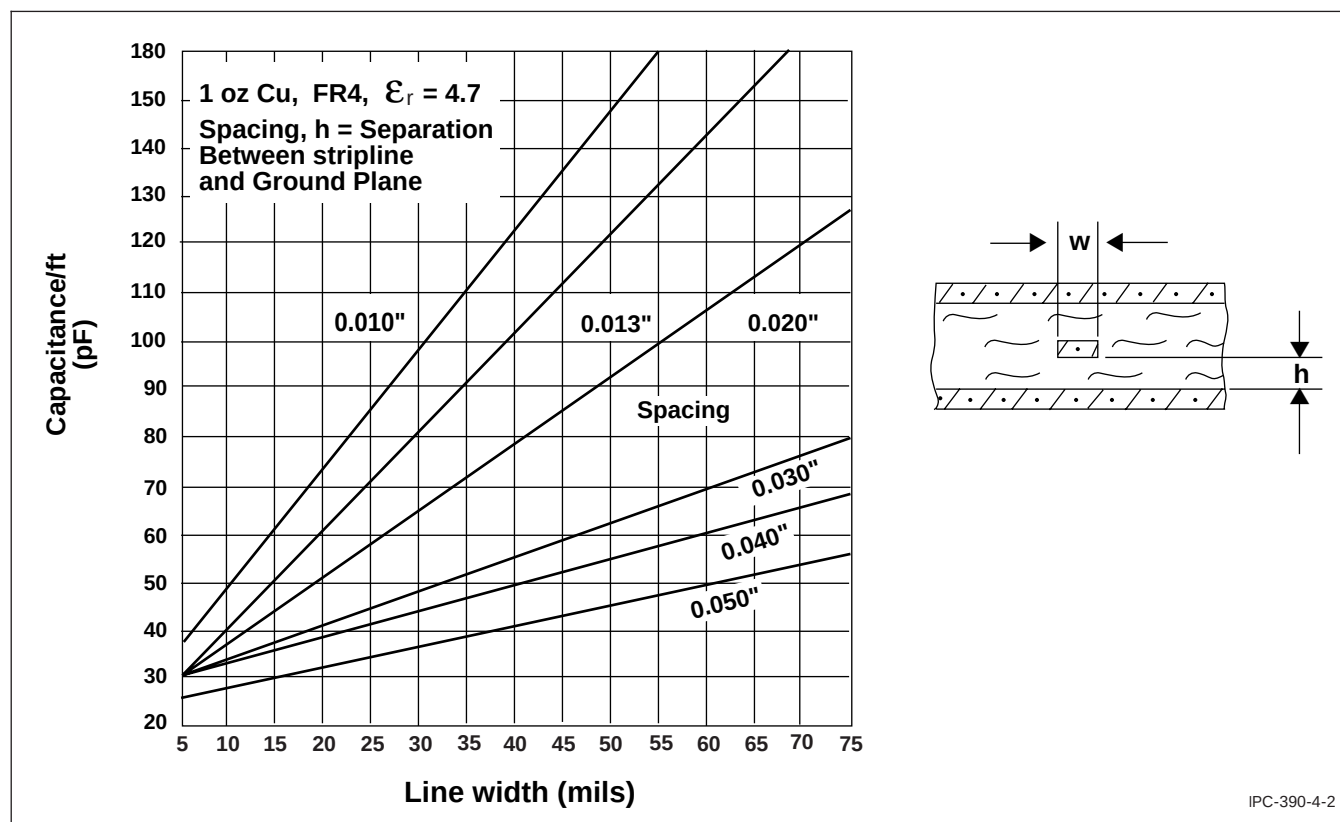


Figure 4-2 Capacitance vs. line width and spacing for striplines

- F. The board outline should be defined in relation to an internal datum. The board outline should be on-grid with the datum located in the lower left corner of the board. Keep cutouts and notches to a minimum. Because both metric and inch base grids are used, the difference between soft (exact) conversion and hard (approximate) conversion can make a difference in the board profile. The design should have one or the other grid reference, not both.

4.2 Job Setup Before a printed board can be designed, certain tasks must be fulfilled in a specific order so that the design process can proceed in a smooth, orderly manner.

4.2.1 General Design Rules In order to take full advantage of the computer aided design capabilities, it is necessary to establish specific rules which the computer will follow. Applicable IPC design standards should be followed in establishing the design rules (see Applicable Documents).

4.2.1.1 Modular Grid Size The choice of the modular grid system used in the design of printed board is based on the dimensioning system used on the majority of the component terminal locations of parts mounted to the printed board. For designs where the majority of component terminal locations are metric (SI) based, the basic modular units of length are 2.0, 1.0, 0.5 or other multiples of 0.5 mm, and shall be applied in the X and Y axis of the Cartesian coordinate system. For designs where the majority of component terminal locations are inch based, the basic modular units of length are 0.100, 0.050, 0.025 or other multiples of .005 inch, and shall be applied in the X and Y axis of the Cartesian coordinate system.

4.2.1.2 Conductor Thickness and Width The minimum width and thickness of conductors on the finished board should be determined on the basis of the current-carrying capacity required, and the maximum permissible conductor temperature rise and etch factor. Figures 4-3 and 4-4 are typical design aids that can be found in the IPC Design Standards IPC-D-319 and IPC-D-949.

Wherever possible, the design should incorporate processing allowances which will allow the manufacturer to produce a part that will meet the end-product requirements.

For some CAD systems, a good practice is to keep the number of different conductor widths to a minimum, to facilitate conductor routing.

4.2.1.3 Land Area and Hole Size Relationship Good practice is to establish a standard which contains component/land to land relationships and holes sizes for a variety of lead diameters. When determining pad-to-hole size relationship, the design must meet land to plated through (UOS) hole requirements per MIL-STD-275E (REF MIL-

STD-55110 page 35 for alternate land area designs). Minimum annular ring requirements, the end product hole characteristics and the processing allowances should be established in accordance with both IPC design standards and any automatic insertion hole requirements. Figure 4-5 and Table 4-1, taken from an IPC Design Standard, illustrate the type and detail of information available.

In addition, minimum hole to hole and hole to board edge requirements should be established. If a mechanical photoplotter is used these same standards may be applied to using laser plotters. However, there is more flexibility since laser plotter limitations are related to laser spot size, not the number of apertures held in any aperture wheel (see IPC-D-310). A photoplotter aperture list should be established based on the user standard component types.

4.2.1.4 Conductor Spacing Minimum conductor spacing should be established for the following conditions:

- A. Between different voltage carrying conductors.
- B. Conductor to land areas.
- C. Conductor to board edges.
- D. Conductor to mounting holes.
- E. Conductor to other metal objects located on the board or used to mount the board to the assembly.

4.2.1.5 Component Mounting and Spacing General rules for component mounting and spacing are established according to IPC standards and IPC Guidelines IPC-CM-770 and IPC-CM-780. Typical considerations include component distance from board edges, spacings between components, component distance from mounting holes, and specific component orientations which affect soldering and/or automatic insertions.

4.2.1.6 Large Conductive Areas The criteria for determining a large conductive area should be specified. Any area that extends beyond a 1-inch diameter circle should contain etched clearance areas that will break up the large conductive area but retain the continuity and functionality of the conductor. An example of this technique is cross hatched ground plane. Large conductive areas should, if possible, be on the component side of the board. Electrical considerations may affect the design of large conductive areas, and may require additional vias and tie planes on alternate layers. Large plane areas may need to be unbroke at certain frequencies and voltages. In addition, thermal relief criteria should be specified for lead attachment to large conductive areas. Thermal relief criteria such as the width of the conductive tie, the width of the clearance, the land size, and the direction of the conductive tie should be specified.

4.2.1.7 Orientation Symbols Special component orientation symbols may be incorporated into the design.

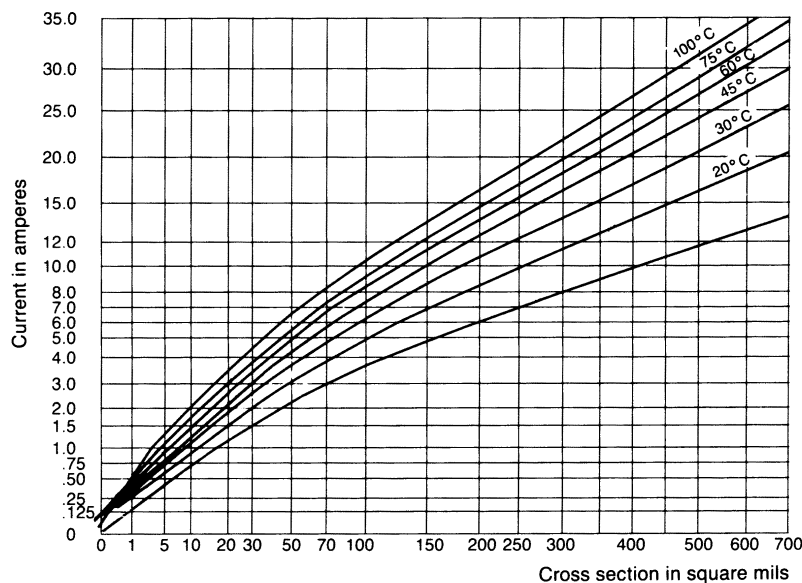


Figure a. External conductors

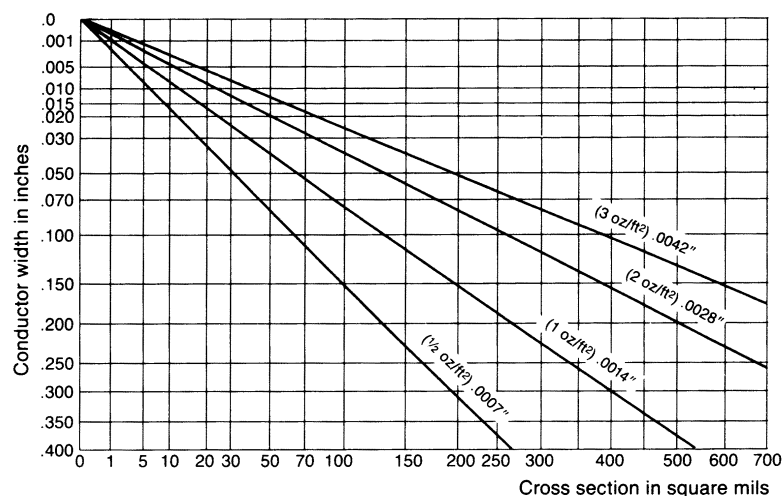


Figure b. Conductor width to cross-section relationship

Notes:

1. The design chart has been prepared as an aid in estimating temperature rises (above ambient) vs. current for various cross-sectional areas of etched copper conductors. It is assumed that, for normal design, conditions prevail where the conductor surface area is relatively small compared to the adjacent free panel area. The curves as presented include a nominal 10 percent derating (on a current basis) to allow for normal variations in etching techniques, copper thickness, conductor width estimates, and cross-sectional area.
2. Additional derating of 15 percent (current-wise) is suggested under the following conditions:
 - (a) For panel thickness of 1/32 inch or less
 - (b) For conductor thickness of 0.0042 inch (3 oz/ft²) or thicker
3. For general use the permissible temperature rise is defined as the difference between the maximum safe operating temperature of the laminate and the maximum ambient temperature in the location where the panel will be used.
4. For single conductor applications the chart may be used directly for determining conductor widths, conductor thickness, cross-sectional area, and current-carrying capacity for various temperature rises.
5. For groups of similar parallel conductors, if closely spaced, the temperature rise may be found by using an equivalent cross-section and an equivalent current. The equivalent cross-section is equal to the sum of the cross-section of the parallel conductors, and the equivalent current is the sum of the currents in the conductors.
6. The effect of heating due to attachment of power dissipating parts is not included.
7. The conductor thicknesses in the design chart do not include conductor overplating with metals other than copper.

IPC-390-4-3

Figure 4-3 Conductor thickness and width for surface conductors

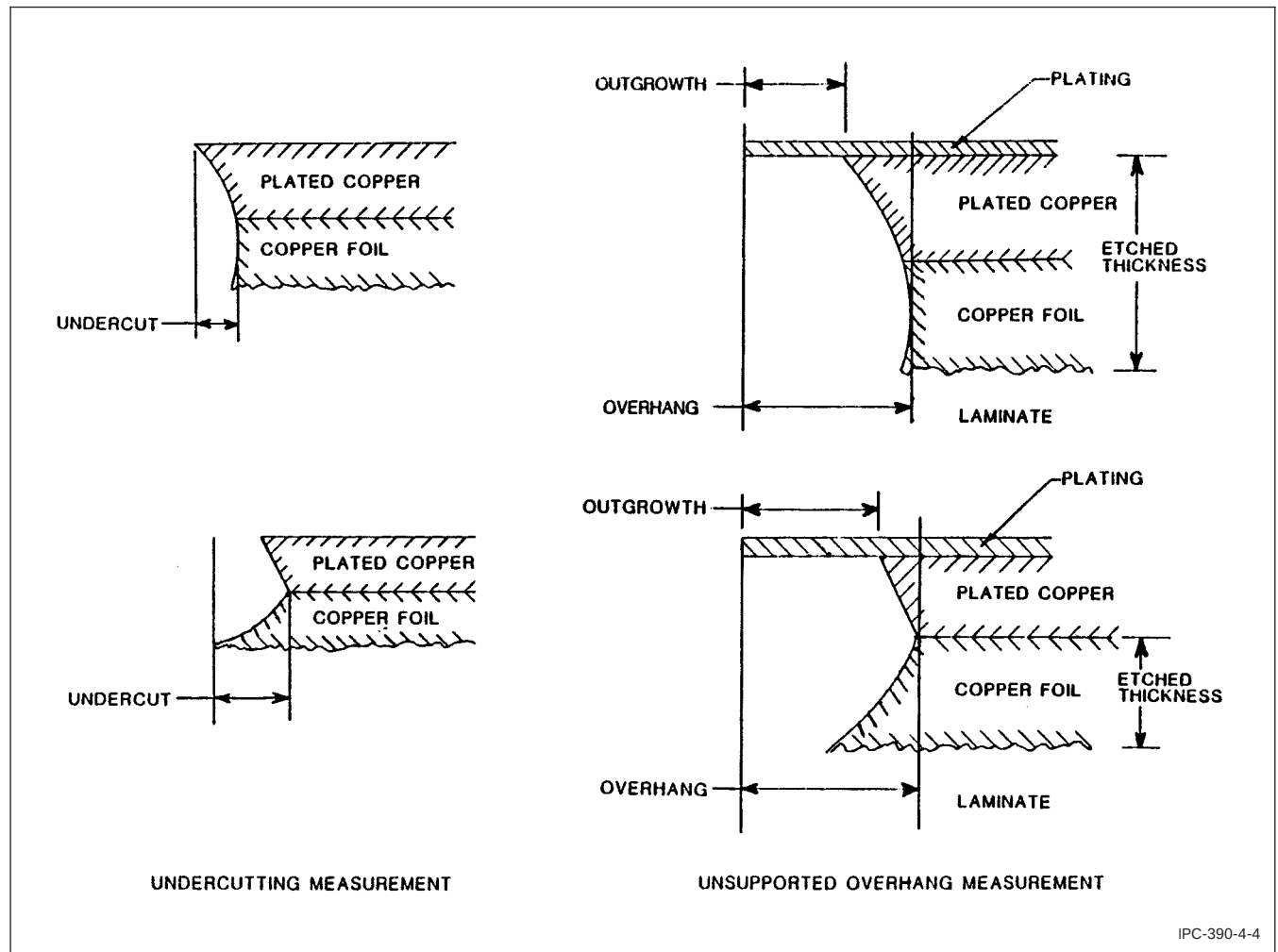


Figure 4-4 Conductor characteristics

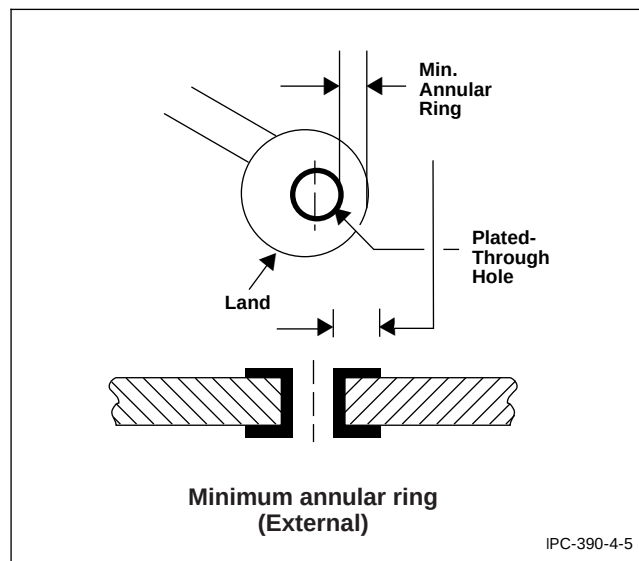


Figure 4-5 External annular ring

for ease of inspection and assembly of the parts. Techniques may include special symbols, or special land configurations for integrated circuits and surface mount devices. Examples of this technique are square pads or dots

Table 4-1 Annular Rings (Minimum)

Annular Ring	A	B	C
Internal supported	0.15 [0.006]	0.05 [0.002]	0.03 [0.001]
External supported	0.25 [0.010]	0.15 [0.006]	0.05 [0.002]
External unsupported	0.40 [0.016]	0.25 [0.010]	0.15 [0.006]

Note: Columns A, B & C represent progressive increases in sophistication of tooling, materials and processes. All dimensions are in millimeters except those in brackets which are in inches.

denoting pin 1 of integrated circuits, plus signs for polarized capacitor anodes, and numbers and letters for connector pin identification.

4.2.1.8 Coatings

4.2.1.8.1 Solder Mask Solder mask coatings are recommended to prevent solder bridging between conductors during the soldering process as well as enhance electrical performance. Various materials can be used as coatings, each having specific characteristics which affect the mask to land area clearance requirements. (See 4.2.1.8.2 Solder Mask)

IPC standards, board assembly technologies, and board complexity determine the minimum solder mask clearances recommended for the land areas used in the design. Different solder mask materials also have differing clearance requirements. Figure 4-6 represents one aid from the IPC Design Standards (IPC-D-319), used to demonstrate critical considerations when designing a solder mask.

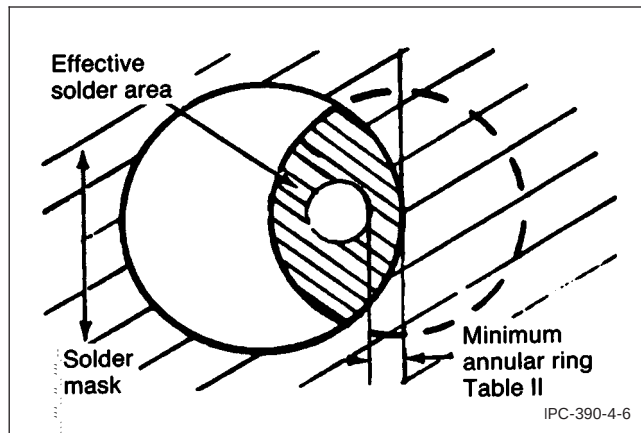


Figure 4-6 Solder mask registration

4.2.1.8.2 Conformal Coating Conformal coatings are used for environmental protection as well as mechanical support for components mounted on a printed board. The designer should incorporate any end product requirements for conformal coating so as to design for proper component mounting as well as circuit routing. Conductor spacing may vary, as well as the number of conductors routed under a component, or the accessibility to via sites under the component.

4.2.2 Library Part Shapes Computer Aided Design systems require libraries of component shapes. These shapes represent both the electrical function and mechanical size and shape of various components. Depending upon the CAD system used, a relationship between the electronic schematic symbol and the mechanical part shape may or may not be required or available.

If a relationship between schematic and part shapes is required, pin assignments and sequence must be consistent between the symbols and the part shapes because of net list extraction. A carefully coordinated effort makes design data transfer easier between schematic & board layout and board layout to CAM postprocessing.

4.2.2.1 Schematic Shapes Schematic symbol shapes depict the electrical representation part. The symbol should contain information such as part number, connection pin numbers, pneumonics and any interchangeability between pin connections.

4.2.2.2 Physical Shapes Physical shapes can be classified into at least two categories. One depicts the outer perimeter of the component body and another category

depicts the actual part configuration. Library figures (component outlines) are usually drawn to the maximum size of the component and lands, rather than nominal or minimum sizes (see IPC-D-319 and IPC-D-949). When establishing the physical shape, consider clearances for automatic insertion equipment and other factors that would affect component placement (IPC-CM-770).

4.2.2.3 Interrelational Data Some CAD systems require a data table that shows the relationship between the physical shape of a component and its electrical symbol. Information such as interchangeable gates within a package, between packages, swappable pins, etc., are examples of this kind of data (See IPC-D-352).

4.2.3 Board Shape Definition The board geometry is entered into the data base. Take care in establishing datum points that are compatible with not only the CAD system, but with the artwork generator, NC drill and automatic insertion equipment.

Be aware of the relationship of the CAD coordinate system origin to the outline drawing datum. Small variations (.03 mm [.012"] or less) can cause significant dimensional anomalies in finished product sizes and locations.

Definition of a board geometry should be in accordance with IPC applicable design standards (see Applicable Documents). Figure 4-7 illustrates typical considerations outlined in the IPC Design Standards.

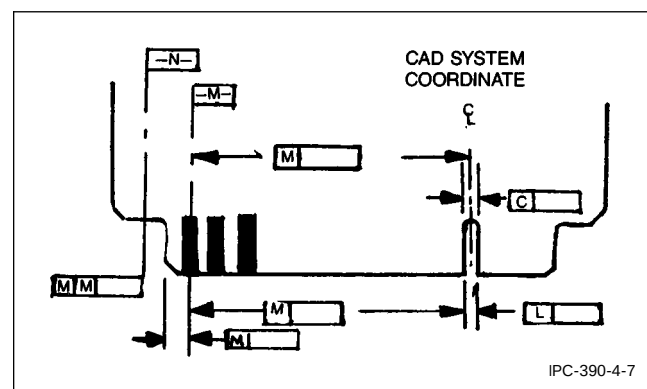


Figure 4-7 Contact number one dimensioning using secondary datum

4.2.4 Schematic Schematic capture, or the capture of the connectivity of the circuit, represents a critical part of the job setup.

4.2.4.1 Schematic Creation A CAD components file can be extracted listing the CAD part shape requiring placement on the board. A library of CAD generated schematic symbols is required before schematic capture can begin (i.e., drawing formats, logic symbols).

The creation of a schematic diagram on the CAD system will give the user a releasable drawing. Some CAD systems will be able to extract the connectivity information

from the schematic diagram and then compare the finished board connections to the schematic diagram or the extracted net list.

4.2.4.2 Net List The input of a net list into the CAD system represents the fastest method of giving connectivity information to your CAD system. However, it does not provide a pictorial schematic diagram for drawing release purposes. Net lists can be hand-entered, down-loaded, or extracted from a CAD schematic generation system or engineering work station.

4.2.4.2.1 On-line Creation As long as a CAD system can support schematic creation, they can be created on the video display terminal, using a light pen, mouse, digitizing pallet, etc.

4.2.4.2.2 Off-line Creation There are a number of ways to create a schematic diagram off-line, thereby making more terminal time available for board design.

Large schematic diagrams are often very difficult to compose on the CAD system due to the limited display area of the CAD terminal. A way around this problem is to draw a rough placement on a separate piece of paper and digitize this into the system using a digitizing tablet. Completion of the interconnections schematic then becomes a simple process. Creating a schematic diagram on a CAE design station is an alternative method of capturing the schematic diagram pictorial as well as the connectivity of the circuit. The CAE station can be part of a large host computer system, a stand-alone work-station, or a networked personal computer system.

When mixing CAD systems for schematic capture, it is important that system compatibility exists. See the IPC-D-35X series standards for data interchange formats.

4.3 Design

4.3.1 The CAD Approach To Placement There are three classes of computerized placement systems; these are categorized by the degree to which they are automated.

The three are:

1. Manual/Interactive
2. Assisted
3. Automated

4.3.1.1 Manual/Interactive The manual/interactive approach provides the designer with the ability to graphically manipulate the placement of the components on the board until he is satisfied with the layout. The quality of the placement in this approach depends entirely on the designer's experience, expertise and judgment.

4.3.1.2 Assisted Approach The assisted approaches include those in which the system, to varying degrees, helps the designer make the placement. One of the simpler assisted techniques is the presentation of the point to point connection (rat's nest). One merit of the rat's nest approach is that the designer can see simultaneously on the video screen all of the board connections to be made. However, systems handle the presentation of the rat's nest differently. Some systems can display a single net, thus suppressing the nets that the designer does not need to view, while in other systems, a net list manipulation is necessary in order to obtain the more selective approach. One assisted method allows the designer to display some or all of the components at the edge of the work area during the placement process. The visual display of the components aids the component placement for the designer.

In the assisted method, the designer allows the computer program to make an initial random or constructive placement just to get started. The computer program may also be used to improve or refine a placement that the designer did manually or with system assistance. The designer then attempts to improve upon this placement by moving parts to more appropriate locations. Some systems assist the designers by using a histogram that identifies high density conductor areas. Moving the components to different locations optimizes the wiring density.

4.3.1.3 Automatic Approach The automatic approaches, as their names imply, automatically place the components of the circuit on the board. The designer must provide some placement parameters, and after the computer placement is complete the designer is allowed to manually change the results. Most automatic placement routines (algorithms) automatically place the components at strictly defined locations on the PC board; other systems allow random positioning of components, restricting only component body interference. All systems attempt to minimize the length of the connection paths. Some routines also consider special design rules for specific designs by measuring the total orthogonal distance (Manhattan distance) between all points of each net connection. Software algorithms used to perform initial placement fall into two separate classes: Random and Constructive. The random initial placement approach places the components without regard to, or with only limited regard to, connectivity and relies on the improvement pass to optimize placement. The constructive initial placement algorithms are iterative. They function by selecting components, one at a time, and placing them on the board in positions that are optimized for connectivity in relation to those components already placed.

4.3.1.4 Comparisons Many studies have been done to decide which type of initial placement is best.

consensus is that for large problems (150 or more components), spending the time to do constructive initial placement is worthwhile, while for smaller problems it is more efficient to choose the best of a number of random initial placements before going to the improvement pass. All algorithms improve the initial placement by moving the components into "better" positions until the "best" placement results.

4.3.1.5 Detailed Placement Techniques The following are additional approaches to component placement.

4.3.1.5.1 Cost Algorithms A cost algorithm evaluates placement and interconnection problems. A cost algorithm provides a mechanism for comparing the cost effectiveness of one placement to another. The algorithm uses net lengths, cross-overs, available wiring (density), etc. to make this determination.

4.3.1.5.2 Board Partitioning Placement Technique In the board partitioning placement technique, the design is reduced to a sequence of "partitioned" problems. First, a vertical boundary line splits the set of component locations into left and right halves. The set of components is then partitioned into halves; the partitioning procedure swaps component groups and components to minimize the crossing count for the vertical boundary line. Next, the set of locations is split into upper and lower halves separated by a horizontal boundary line, and the same component swapping method is used with an additional constraint: All left/right assignments previously developed must be respected (See Figure 4-8).

Each component has now been placed in either the left-upper, right-upper, left-lower, or right-lower quadrant and

the placement of that component has been optimized with respect to the "crossing count" min./max. criteria. This partitioning technique is then applied to each of the quadrants in turn, and then to the resulting octants until each region contains one board location.

4.3.1.5.3 Pairwise Interchange In pairwise interchange, a component is swapped with each other component of its type or class, and a computation is performed to determine whether total connection length is reduced. If the connection length is reduced, the swap remains; otherwise the components are returned to their original positions. This exchange continues until all components have been tried.

4.3.1.5.4 Interactive Placement In practice, some components will normally be positioned by automatic procedures and others by designer defined position entry. That is, the designer can define positions, and later initiate computations so that the placement can be made with respect to the prepositioned components. Alternatively, automatic placement can be initiated for only some components with the remaining components positioned by the designer at a later time.

4.3.1.6 Various CAD Placement Features:

4.3.1.6.1 Renaming Components In many systems, a component designator can be changed to a new name by entering a record at the keyboard, or on some systems from a menu at the graphics terminal. Components are renamed usually left to right, top to bottom, ascending numerical sequence within a specific reference designator class to facilitate test and check-out.

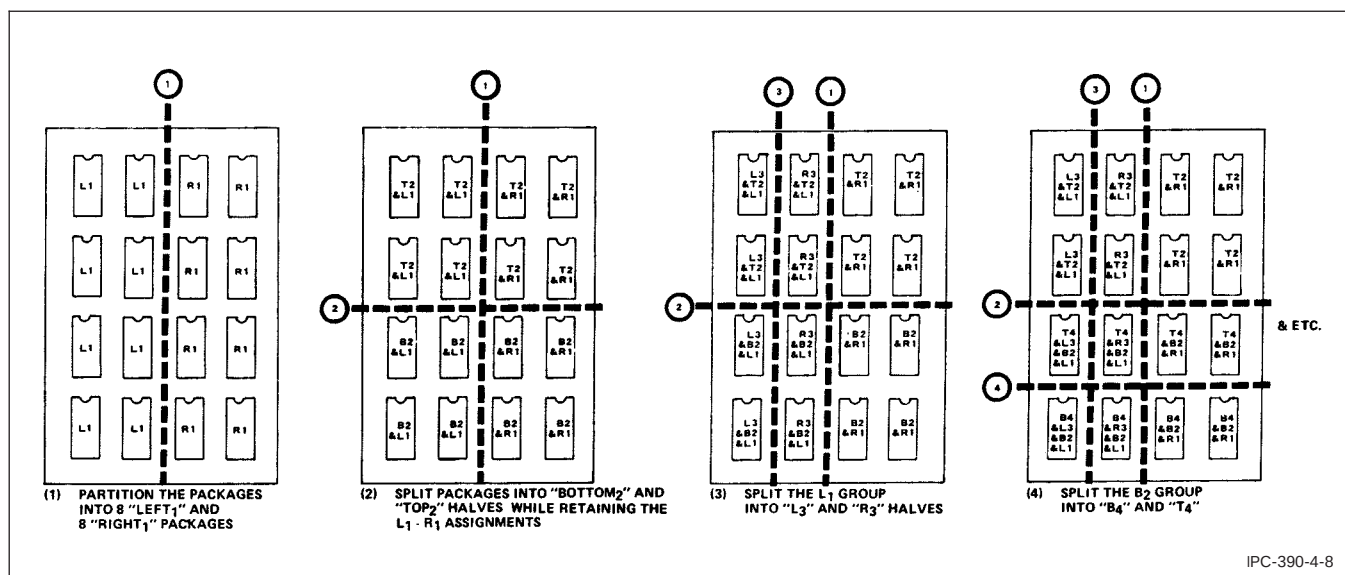


Figure 4-8 Successive partitions performed by the component placement module

4.3.1.6.2 Creating Columns and Rows of Components

In many CAD programs, components can be positioned by defining columns and rows. Each column is defined by an x- coordinate and each row by a y-coordinate. Other methods used to position in columns are to define a matrix with step increments for the placement of the components, define columns & rows by specific irregular increments, or by system default columns and rows.

4.3.1.6.3 Function Assignment and Component Placement

Some CAD systems allow you to define functions of components as fixed and free functions and then execute commands that automatically swap those free functions between component packages for the best possible placement and shortest connectivity length. In other systems, function assignment is done on the schematic or in the net list, and any swaps must be edited.

4.3.1.6.4 Automatic Component Swapping Another possible feature of the CAD design systems is the ability to swap the positions of like components so that the possibility of 100% interconnection is enhanced.

4.3.1.6.5 Moving and Rotating of Single Components

This is usually an interactive design tool accessed from a menu during the design placement phase. It enables the designer to move and or rotate any individual part in the design. Smarter software packages also have the ability to move and rotate a complete group, or to rotate a complete component type.

4.3.2 Routers

4.3.2.1 Router Types Figure 4-1 shows where routing fits into the automation design sequence. The various routing techniques may be applied individually or sequentially as multistage routers. A good routing program attempts to make all the required circuit connections using the shortest total connection paths and simultaneously reduce the number of vias or optimum points at which the connection paths change from one layer of the board to the next to avoid obstructions. The process must be capable of constructing an intelligent routing pattern while constantly checking clearances and connectivity. All this must be done while keeping both routing and circuit costs to a minimum without sacrificing circuit quality.

Many automatic implementations are restricted to routing between pairs of layers using vias for feed throughs, and can only be extended to multilayer configurations by concatenating layer pairs. This approach does not result in efficient multilayer routes. All layers must be taken into consideration simultaneously to accomplish this end. Most of the routers are grid based, and as such can only make horizontal or vertical interconnection routes. In limited cases, some routers allow diagonal interconnection runs.

Some routers do not allow connection paths to run under components. Automatic routers are really the most effective for digital circuits, not analog circuits with many discrete components.

The three broad categories of automatic routers used for printed wiring design are listed below:

- Maze-Running Routers
- Line Probe Routers
- Channel Routers

4.3.2.1.1 Maze-Running Router The maze-running routers are variously known as “exhaustive search,” “wave-front,” or “Lee’s” routers. It is the characteristic of an unrestricted maze-running router to never fail to resolve a connection if a valid path exists. The router makes interconnections by expanding out from the grid primary connection point until the secondary point is found and connected. The unrestricted maze runner will complete every possible path from the primary to the secondary component, compare all the successful connections, and pick the best (shortest path and/or least vias) available. It will repeat this exercise for all connections to be made. In essence, the maze runner consists of finding a conductor route to connect them whenever one exists. In general, this method requires considerably more processing time than the other two methods. The primary-user parameter employed is the size of the wiring rectangle defined. The smallest wiring rectangle is the area encompassed by the two points to be connected. The area can then be expanded, usually by grid increments, until it reaches the full routing area.

Early connections will impact the quality of later connections with the maze router. Therefore, when using a multi-router system it is best to use the maze router as the last step in interconnect, thereby minimizing the probability that an early route will block further routing capability.

4.3.2.1.2 Line Probe Router Line-probe routers have significant performance advantages over the maze runners. Since they only keep track of line-end points, they do not require the large amounts of storage used by the maze runners. Line probe routers also use a much simpler and more deterministic approach which requires significantly less execution time and therefore less cost.

The line probe router connects a pair of points by constructing simultaneously a sequence of line segments (probes) out from each point to be connected. When the two-line segment sequences intersect, the connection path is complete. The drawback to this method is that the line-probe router, unlike maze runners, will be unable to route some connections that are routable. However there is a relatively high completion rate for line-probe routers, usually over 95%.



4.3.2.1.3 Channel Router The channel router and its many enhanced versions is second in implementation popularity only to the maze runners. Channel routers, unlike the maze-running and line-probe routers, require a more rigid and disciplined component layout. They do an excellent job under ideal conditions. As the name “channel-router” implies, circuit components must be placed in such a way as to leave vertical and horizontal channels between the components through which connection paths may be run. The components must be placed in an ordered matrix providing for spaces between the rows and columns of pins that serve as the routing channels. The basic channel-router algorithm operates on two-sided boards, making vertical connections in vertical columns on one side and horizontal connections in horizontal rows on the other. Any two points to be connected must lie in the same channel (column or row) for the router to make the connection.

The path may meander within the channel to avoid barriers, previously routed paths, vias, and other obstructions. The meander is controlled to allow fixed amounts of horizontal movement in vertical channels and vice versa.

The router proceeds by connecting the shortest paths first and progresses until it has completed all the connections possible within a channel. It will then move on to the next channel and eventually to the other side. At this point, the basic channel-router algorithm is complete. Most implementations go one step further by making use of a fixed- or floating-position via. With this modification, the router will attempt remaining connections by changing sides during the construction of the path. The router continues to follow the basic channel rules during this process (i.e., vertical channels on one side, horizontal on the other).

4.3.2.2 Router Performance Router performance is measured from two perspectives: economic and technical.

The economic factors are simply based upon comparing the cost to produce the circuit with a particular router method to manual or other routing method costs. The cost includes the resources necessary to complete the layout as well as the production cost for the circuit.

Technical performance is somewhat more difficult to measure because it compares the quality of the finished circuit in terms of signal degradation, noise, crosstalk, and electronic reliability.

4.3.2.2.1 Specific Application Comparison The performance of a routing algorithm is measured against 3 criteria: percentage of routing completed, (or conversely, the amount of manual effort to complete routing of the layout), execution time and system storage resources required. The best algorithms balance all three criteria. See Figure 4-9 for an example of completion rates based on density and routing completion time.

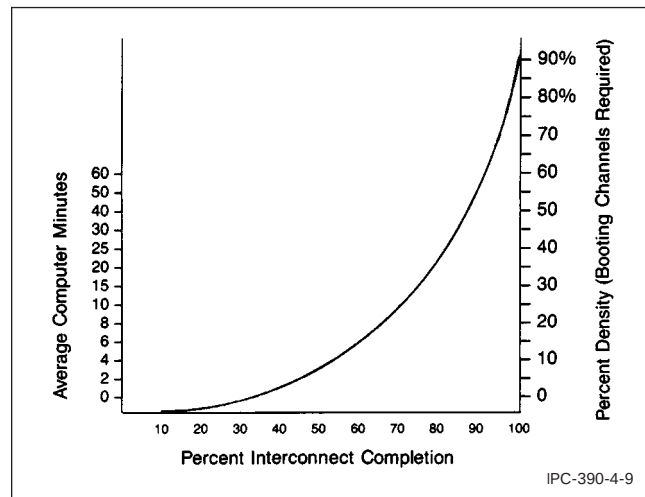


Figure 4-9 Automatic router—computer processing

Auto-interactive graphic systems that include a routing subset must allow the designer to interact with the system in order to guide and complete the routing process. If the result of the router is less than 100 percent completion, facilities must be provided by the system that allow the user to attempt to finish all incomplete connections. The system must balance the capabilities of the automated routing subsystem with effective graphic editing functions. The system must provide an adequate man/machine interface that allows the user to complete the connections while the system monitors his actions against the original ground rules for interconnection, and signals the user when any of the rules are violated. With these facilities, the user can develop connections based on experience and creativity that are beyond the capabilities of the system alone.

A re-entry capability in routers is desirable. Re-entrance means that the user can stop the routing procedure at some intermediate point, inspect the results in a graphic form (usually presented on the CRT), manually edit changes in physical positions, and restart the routing procedure. The manual changes can involve movements or deletions of conductor lines or components. Re-entrant capability is often used in making changes on previously laid-out printed boards.

Some routers have a preroute step that displays a “rat’s nest.” This helps the user identify potential routing problems. The user can then change the placement, choose one of many different routers for the job, or set parameters appropriately.

Designers will require significant training and practice to become proficient at systems with both automated routing and user involvement capability. It may be months before predicted time and cost reductions are obtained.

4.3.3 Completion There currently is no router that can route every board 100% every time. Most designs beyond minimum complexity will require manual routing with the