



*The Institute for
Interconnecting
and Packaging
Electronic Circuits*

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Design Standard for Thick Film Multilayer Hybrid Circuits

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A standard developed by the Institute for Interconnecting
and Packaging Electronic Circuits

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Users of this standard are encouraged to participate in the development of future revisions.

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Design Standard for Thick Film Multilayer Hybrid Circuits

1.0 SCOPE

This standard covers the requirements and considerations for the design of multilayer hybrid circuits based on industry manufacturing capabilities.

1.1 Purpose The purpose of this standard is to establish rules, principles, and other considerations for mechanical, electrical, and producible properties which the designer can use to select design features, and properties that will result in a multilayer hybrid circuit that will meet performance and cost requirements.

1.2 Classification When appropriate, this standard will provide three design complexity classes of features, tolerances, or measurements which reflect progressive increases in sophistication of tooling, materials, or processing and, therefore, progressive increases in cost. These classes are: A) Simple, B) Moderate, and C) Complex. The use of one class for a specific feature does not mean that other features must be of the same class. Selection should be based on the minimum need. In the event of conflict between the design requirements and the classes defined herein, the former shall take precedence and be reflected on the master drawing.

Design requirements such as precision, performance, and conductive pattern density determine class. Class definitions identify the precision needed to meet design/performance requirements of the hybrid circuit.

Classification of design complexity requirements should not be confused with the performance classification of end-item use, as referenced in other IPC documentation, such as IPC-HM-860, which refers to Class 1—consumer products; Class 2—general industrial; and Class 3—high reliability equipment types. The need to apply certain design concepts should depend on the complexity and precision required to produce a particular hybrid circuit. Any design class for any circuit characteristic may be applied to any of the end-product equipment categories and the classes described from each, as required. Therefore, a consumer product designated as Class 1 could require Class A, B or C design complexity for different attributes of the circuit.

1.2.1 Circuit Type The multilayer hybrid circuit types defined in the IPC-HM-860 include both refractory and nonrefractory metal co-fired types (Type I) and thick film and thin film inorganic types (Type II).

This standard will address only Type II(a), thick film inorganic multilayer hybrid circuits.

1.3 Presentation All dimensions and tolerances are expressed in metric [and inches, shown in brackets], and are not direct conversions. Users should employ a single system, and not intermix millimeters and inches. Reference information is shown in parentheses ().

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue currently in effect, form a part of this document to the extent specified herein.

2.1 IPC

IPC-T-50 Terms and Definitions

IPC-D-300 Dimensions and Tolerance for Printed Wiring Applications

IPC-D-310 Guidelines for Artwork Generation and Measurement Techniques

IPC-D-325 End-Product Documentation for Printed Wiring Boards

IPC-D-350 End Product Description in Numeric Form

IPC-D-351 Printed Wiring Board Documentation in Digital Form

IPC-D-352 Electronic Design Data Base Description for Printed Boards

IPC-D-353 Automatic Test Information Description in Digital Form

IPC-D-354 Library Format Description for Printed Board Digital Data Bases

IPC-TM-650 Test Methods Manual

IPC-SM-780 Guidelines for Component Packaging and Interconnection with Emphasis on Surface Mounting

IPC-SM-782 Surface Mount Land Patterns (Configurations and Design Rules)

IPC-CC-830 Qualification and Performance of Electrical Insulating Compounds for Printed Board Assemblies

IPC-SM-840 Permanent Polymer Coating (Solder Mask) for Printed Wiring Boards

IPC-HM-855 Microelectronics Design Guide

IPC-HM-860 Specification for Multilayer Hybrid Circuits**2.2 Government Documents****2.2.1 Military****MIL-C-14450** Copper Plating (Electro-deposited)**MIL-M-38510** General Specification for Microelectronics**MIL-G-45204** Gold Plating (Electro-deposited)**MIL-P-81728** Plating, Tin-Lead (Electro-deposited)**MIL-STD-883** Test Methods and Procedures for Microelectronics**2.2.2 Federal****QQ-N-290** Nickel Plating (Electro-deposited)**QQ-S-571** Solder; Tin Alloy; Lead-Tin Alloy; and Lead Alloy**2.3 Other Publications****2.3.1 ASTM****F 72** Gold Wire for Semiconductor Lead Bonding**F 487** Fine Aluminum—1% Silicon Wire for Semiconductor Lead Bonding**F 638** Fine Aluminum—1% Magnesium Wire for Semiconductor Lead Bonding**2.3.2 EIA****JEDEC Publication 95** Registered and Standard Outlines for Solid State Products**3.0 DESIGN CONSIDERATIONS**

The information contained in this document describes general and specific requirements for the design of thick film multilayer hybrid circuits intended to meet the performance and end product requirements of IPC-HM-860.

The success or failure of a hybrid design depends on many interrelated considerations. The effect of the following parameters on the design should be considered:

1. Equipment environmental conditions, such as ambient temperature, heat generated by the components, and ventilation.
2. Maintenance philosophy during the service life of the equipment, especially with respect to component placement that affects component accessibility.
3. Spacing between circuits particularly "mother board/

daughter board" designs that might affect placement on interconnecting lead frames.

4. Testing/fault location requirements that might affect component placement, conductor routing, connector contract allocations, etc.
5. If an assembly is to be repairable, consideration must be given to component/circuit density and the selection of board/conformal coating materials. In general, design should promote ease of package repair which must be initiated by delidding.

3.1 Terms and Definitions Definitions of all terms used herein shall be as specified in IPC-T-50 and as follows.

Abrasive trimming Trimming a film resistor to its nominal value by notching resistor with a finely adjusted stream of an abrasive material, such as aluminum oxide, directly against the resistor surface.

Active trim Trimming of a circuit element (usually a resistor) in a circuit that is electrically activated and operating to obtain a specified functional output for the circuit (see Functional trimming).

Add-on component Discrete or integrated prepackaged or chip components that are attached to a film circuit to complete the circuit functions.

Analog circuits Circuits that provide a continuous (vs. discontinuous) relationship between the input and output.

Aspect ratio The ratio between the length of a film resistor and its width; equal to the number of squares of the resistor.

Back bonding Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry face up. The opposite of back bonding is face down bonding.

Back mounting See *Back bonding*.

Ball bond A bond formed when a ball shaped end interconnecting wire is deformed by thermo-compression against a metallized land; also called "a nail head bond" from the appearance of the flattened ball.

Beam lead A long structural member not supported everywhere along its length and subject to the forces of flexure, one end of which is permanently attached to a chip device and the other end intended to be bonded to another material, providing an electrical interconnection or mechanical support or both.

Beam lead device An active or passive chip component possessing beam leads as its primary interconnection and mechanical attachment means to a substrate.

Bond An interconnection which performs a permanent electrical and/or mechanical function.

Bond deformation The change in the form of the lead produced by the bonding tool, causing plastic flow, in making the bond.

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Bond envelope The range of bonding parameters over which acceptable bonds may be formed.

Bond interface The interface between the lead and the material to which it was bonded on the substrate.

Bond lift-off The failure mode whereby the bonded lead separates from the surface to which it was bonded.

Bond off See *Bond lift-off*.

Bond land See *Bonding area*.

Bond schedule The values of the bonding machine parameters used when adjusting for bonding. For example, in ultrasonic bonding, the values of the bonding force, time, and ultrasonic power.

Bond separation The distance between the attachment point of the first and second bonds of a wire bond.

Bond site The portion of the bonding areas where the actual bonding took place (see *Bonding area*).

Bond strength In wire bonding, the pull force at rupture of the bond interface measured in the unit gram-force.

Bond surface See *Bonding area*.

Bond-to-bond distance The distance measured from the bonding site on the die to the bond impression on the post, substrate land, or fingers, which must be bridged by a bonding wire or ribbon.

Bond-to-chip distance In beam lead bonding the distance from the heel of the bond to the component.

Bond tool The instrument used to position the lead(s) over the desired bonding area and impart sufficient energy to the lead(s) to form a bond.

Bondability Those surface characteristics and conditions of cleanliness of a bonding area which must exist in order to provide a capability for successfully bonding an interconnection material by one of several methods, such as ultrasonic or thermo-compression wire bonding.

Bonding, die Attaching the semiconductor chip to the substrate, either with an epoxy, eutectic or solder alloy.

Bonding area The area, defined by the extent of a metallization land or the top surface of the terminal, to which a lead is or will be bonded.

Bonding island Same as *Bonding land*.

Bonding land A metallized area at the end of a thin metallic strip to which a connection is to be made.

Bonding wire Fine gold or aluminum wire for making electrical connections in hybrid circuits between various bonding lands on the semiconductor device substrate and device terminals or substrate lands.

BTAB The acronym for tape automated bonding when the raised bump for each bond site is prepared on the tape material as opposed to the bump being on the component.

Bugging height The distance between the hybrid substrate and the lower surface of the beam lead device which occurs because of deformation of beam leads during beam lead bonding.

Chip The uncased and normally leadless form of an electronic component part, either passive or active, discrete or integrated. chip-and-wire. A hybrid technology employing face-up-bonded chip devices exclusively, interconnected to the substrate conventionally (i.e. by flying wires).

Chip carrier A special type of enclosure or package used to house a semiconductor device or a hybrid microcircuit which has metallized electrical terminations around its perimeter rather than an extended lead frame or plug-in pins.

Chopped bond Those bonds with excessive deformation such that the strength of the bond is greatly reduced.

Co-firing Processing the thick-film conductors and resistors through the firing cycle at the same time.

Contact angle The angle made between the bonding material and the bonding land.

Coplanar leads (flat leads) Ribbon-type leads extending from the sides of the circuit package, all lying in the same plane.

Cratering Defect in which a portion of chip under the ultrasonic bond is torn loose, leaving a pit, by excessive amount of energy transmitted through the wire bond.

Die An uncased discrete or integrated device obtained from a semiconductor wafer (see *Chip*).

Die bond Attachment of a die or chip to the hybrid substrate.

Dielectric Materials that do not conduct electricity and that are used for making capacitors, for insulating conductors (as in crossover and multilayer circuits), and for encapsulating circuits.

Digital circuits Applied normally for switching applications where the output of the circuit normally assumes one or two states (binary operation); however, three state operation is possible.

Direct contact A contact made to the semiconductor die when the wire is bonded directly over the part to be electrically connected, as opposed to the expanded contact.

Doping The addition of an impurity to a semiconductor to alter its conductivity.

Face bonding The opposite of back bonding. A face bonded semiconductor chip is one that has its circuitry side facing the substrate. Flip-chip and beam lead bonding are the two common face bonding methods.

Field trimming Trimming of a resistor to set an output voltage, current, etc.



Film Single or multiple layers of coatings of thin or thick material used to form various elements (resistors, capacitors, inductors) or interconnections and crossovers (conductors, insulators). Thick films are deposited by screen printing.

Film conductor A conductor formed in place on a substrate by depositing a conductive material by screening, plating, or evaporation techniques.

Film network An electrical network composed of a thin and/or thick film components and interconnections deposited on a substrate.

Final seal The manufacturing operation that completes the enclosure of the hybrid microcircuit so that further internal processing cannot be performed without delidding or disassembling the package.

Fire The term used to describe the act of heating a thick-film circuit so that the resistors, conductors, capacitors, etc., will be transformed into their final form.

Firing sensitivity Refers to the percentage change caused in the fired film characteristics due to a change in peak firing temperature. The firing sensitivity is expressed in units of %/°C.

Flip chip A leadless, monolithic structure, containing circuit elements, which is designed to electrically and mechanically interconnect to the hybrid circuit by means of an appropriate number of bumps located on its face which are covered with a conductive bonding agent.

Flip-chip mounting A method of mounting flip chips on thick or thin film circuits without the need for subsequent wire bonding.

Functional trimming Trimming a circuit element (usually resistors) on an operating circuit to set a voltage or current on the output. (See *Active trim*)

Glassivation A method of semiconductor passivation by coating the element with a pyrolytic glass deposition.

Header The base of a hybrid circuit package that holds the leads.

Hybrid circuit A microcircuit consisting of elements which are a combination of the film circuit type and the semiconductor circuit type, or a combination of one or both of these types and may include discrete add-on components.

Hybrid group (electrically and structurally similar circuits). Hybrid microcircuits which are designed to perform the same type(s) of basic circuit function(s), for the same supply, bias, and single voltages and for input-output compatibility with each other under an established set of loading rules, and which are enclosed in packages of the same construction and outline.

Hybrid integrated circuit A microcircuit including thick film or thin film paths and circuit elements on a supporting

substrate, to which active and passive micro-devices are attached, either prepackaged or in uncased form as chips, usually all enclosed in a suitable package (hermetic or epoxy type). Used interchangeably with hybrid circuit and hybrid integrated circuit.

Hybrid microcircuit A microcircuit that involves an insulating substrate on which are deposited networks, consisting generally of conductors, resistors, and capacitors, and to which are attached discrete semiconductor devices and/or monolithic integrated circuits and/or passive elements to form a packaged assembly. Used interchangeably with hybrid circuit and hybrid integrated circuit.

Integrated circuit A microcircuit (monolithic) consisting of interconnected elements inseparably associated and formed in place on or within a single substrate (usually silicon) to perform an electronic circuit function.

Junction (1) in solid state materials, a region of transition between p- and n- type semiconductor material as in a transistor or diode. (2) A contact between two dissimilar metals or materials (e.g., in a thermocouple or rectifier). (3) A connection between two or more conductors or two or more sections of a transmission line.

Junction temperature The temperature of the region of transition between the p- and n-type semiconductor material in a transistor or diode element.

Land A portion of a conductive pattern usually used for electrical connection, component attachment, or both.

Layer One of several films in a multiple film structure on a substrate.

L cut A trim notch in a film resistor that is created by the cut starting perpendicular to the resistor length and turning 90° to complete the trim parallel to the resistor axis thereby creating an L-shaped cut.

Lead frames The metallic portion of the device package that completes the electrical connection path from the die or dice and from ancillary hybrid circuit elements to the outside world.

Loop The curve or arc by the wire between the attachment points at each end of a wire bond.

Loop height A measure of the deviation of the wire loop from the straight line between the attachment points of a wire bond. Usually, it is the maximum perpendicular distance from this line to the wire loop.

Micro-bond A bond of a small wire, such as 0.025 mm [0.001 inch] diameter gold, to a conductor or to a chip device.

Microcircuit A small circuit (hybrid or monolithic) having a relatively high equivalent circuit element density, which is considered as a single part on (hybrid) or with (monolithic) a single substrate to perform an electronic circuit function. (This excludes printed wiring boards).

card assemblies, and modules composed exclusively of discrete electronic parts.)

Microcircuit module An assembly of microcircuits or an assembly of microcircuits and discrete parts, designed to perform one or more electronic circuit functions, and constructed such that for the purposes of specification testing, commerce, and maintenance, it is considered indivisible.

Micro-components Small discrete components such as chip transistors and capacitors.

Microwave integrated circuit A miniature microwave circuit usually using hybrid circuit technology to form the conductors and attach the chip devices.

Monolithic ceramic capacitor A term sometimes used to indicate a multilayer ceramic capacitor.

Monolithic integrated circuit An integrated circuit consisting of elements formed in place on or within a semiconductor substrate with at least one of the elements formed within the substrate.

MOS device Abbreviation for a metal oxide semiconductor device.

Multichip integrated circuit An integrated circuit whose elements are formed on or within two or more semiconductor chips which are separately attached to a substrate or header.

Multichip microcircuit A microcircuit consisting solely of active dice and passive chips which are separately attached to the major substrate and interconnected to form the circuit.

Nailhead bond See *Ball bond*.

Neck break A bond breaking immediately above gold ball of a thermo-compression bond.

Off bond Bond that has some portion of the bond area extending off the bonding land.

Overglaze A glass coating that is over another component or element, normally for physical or electrical protection.

Package The container for an electronic component(s) with terminals to provide electrical access to the inside of the container. In addition, the container usually provides hermetic and environmental protection for, and a particular form factor to, the assembly of electronic components.

Package cap A cuplike cover that encloses the package in the final sealing operation.

Package lid A flat cover plate that is used to seal a package cavity.

Packaging and Interconnecting (P/I) structure The general term for a completely processed printed board, ceramic substrate with interconnection wiring, or other combinations of substrates and interconnection wiring, used for the purpose of mounting components.

Purple plague One of several gold-aluminum compounds formed when bonding gold to aluminum and activated by re- exposure to moisture and high temperature. Purple plague is purplish and very brittle, potentially leading to time- based failure of the bonds. Its growth is highly enhanced by silicon to form ternary compounds.

Push-off strength The amount of force required to dislodge a chip device from its mounting land by application of the force to one side of the device, parallel to the mounting surface.

Resistor paste calibration The characterizing of a resistor paste for Ω/square value, thermal coefficient of resistance, and other specified parameters by screening and firing a test pattern using the paste and recording the results.

Sagging or wire sag The failure of bonding wire to form the loop defined by the path of the bonding tool between bonds.

Search height The height of the bonding tool above the bonding area at which final adjustments in the location of the bonding area under the tool are made prior to lowering the tool for bonding.

Semiconductor carrier A permanent protective structure which provides for mounting and for electrical continuity in application of a semiconductor chip to a major substrate.

Semiconductors Solid materials such as silicon that have a resistivity midway between that of a conductor and a resistor. These materials are used as substrates for semiconductor devices such as transistors, diodes, and integrated circuits.

Serpentine cut A trim cut in a film resistor that follows a meandering repetitive pattern to effectively increase the resistor length and increase resistance.

Smeared bond A bond impression that has been distorted or enlarged by excess lateral movement of the bonding tool, or by the movement of the device-holding fixture.

Squash-out The deformed area of a lead which extends beyond the dimensions of the lead prior to bonding.

Substrate (of a microcircuit or integrated circuit) The supporting material upon which the elements of a hybrid microcircuit are deposited or attached or within which the elements of an integrated circuit are fabricated.

Tail (of the bond) The free end of wire extending beyond the bond impression of a wire bond from the heel.

Tail pull The act of removing the excess wire left when a wedge or ultrasonic bond is made.

Thick film A film deposited by screen printing processes and fired at high temperature to fuse into its final form. The basic processes of thick-film technology are screen printing and firing.



Thick-film circuit A microcircuit in which passive components of a ceramic-metal composition are formed on a suitable substrate by screening and firing.

Thick-film hybrid circuit A hybrid microcircuit that has add-on components, usually chip devices added to a thick-film network to perform an electronic function.

Thick-film network A network of thick-film resistors and/or capacitors interconnected with thick-film conductors on a ceramic substrate, formed by screening and firing.

Thick-film technology The technology whereby electrical networks or elements are formed by applying a liquid, solid, or paste coating through a screen or mask in a selective pattern onto a supporting material (substrate) and fired. Films so formed are usually 5 µm or greater in thickness.

Top hat resistors Film resistors having a projection out one side allowing a notch to be cut into the center of the projection to form a serpentine resistor and thereby increase the resistivity.

Trim notch The notch made in a resistor by trimming to obtain the design value.

Trimming Notching a resistor by abrasive or laser means to raise the nominal resistance value.

Ultrasonic bonding A process involving the use of ultrasonic energy and pressure to join two materials.

Uncased device A chip device.

Via An opening in the dielectric layer through which a conductive riser passes.

Wedge bond A bond made with a wedge tool. The term is usually used to differentiate thermo-compression wedge bonds from other thermo-compression bonds. (Almost all ultrasonic bonds are wedge bonds.)

Wedge tool A bonding tool in the general form of a wedge with or without a wire-guide hole to position the wire under the bonding face of the tool, as opposed to a capillary-type tool.

Wobble bond A thermo-compression, multi-contact bond accomplished by rocking (or wobbling) a bonding tool on the beams of a beam lead device.

3.2 Design Features The design features of the thick film multilayer hybrid circuits shall be in accordance with this standard. Quality conformance test circuitry should be included on each panel and shall be in accordance with Section 6. Test circuitry shall be not more than 10 mm [0.400 inch] and shall be not less than 5 mm [0.200 inch] from the edge of the hybrid circuit, and shall reflect the design of the circuit and all the manufacturing processes. Quality conformance test circuitry shall also be included on the master pattern, master drawing and artwork in accordance with Section 6.

3.3 Documentation Package The designer shall establish the documentation package necessary to define, produce, and test a hybrid microcircuit which is adequate for the customer's end-use requirements. This section will describe a typical documentation package that includes the details required by the various disciplines involved with the manufacturing processes.

3.3.1 Master Drawing Package The master drawing package is composed of the various individual drawings, or combinations necessary to specifically define the physical, electrical, and environmental criteria applicable to the hybrid microcircuit.

Master drawings shall be prepared in accordance with IPC-D-325. Dimensioning and tolerancing practices used in master drawings shall be in accordance with IPC-D-300.

3.3.1.1 Schematic The schematic is a diagram of a functional electronic circuit consisting of symbols of all active and passive elements and their interconnections that form the circuit. The schematic should include the following information:

1. Power supply voltages
2. Input signal requirements
3. Pin-out numbers and functions
4. Test points
5. Active and passive circuit element reference identification, part number, value, and tolerance.

3.3.1.2 Assembly Drawing The Assembly Drawing shows package outlines with the components mounted in their proper locations and denotes interconnection instructions. This drawing should contain:

1. Package outlines
2. List of material
3. Special handling (electrostatic discharge [ESD] caution, fragility, assembly environments, coatings, tailoring, radiation- hardening, etc.)
4. Marking requirements (traceability, federal code, part number, etc.)
5. Applicable procedures (Assembly Test Plan (ATP), visual characteristics, customer specifications, etc.)
6. Component locations and provisions for use of alternate components
7. Burn-in circuit and other conditions that may be a part of other documentation, such as an ATP.
8. As-required material (e.g., wire, epoxy, etc.)

3.3.1.3 Artwork Artwork is required to produce:

1. Dielectric screens
2. Via screens

3. Conductor screens
4. Overglaze screens
5. Solder screens
6. Thick film masks
7. Marking artwork or stamps

3.3.1.4 Piece-Part and Material Procurement Specifications Piece-part and material procurement specifications define the physical, electrical, and environmental criteria applicable to purchased items. Special requirements should include shipping and packaging instructions, if required. The conventional vehicle for these documents are Specification and Source Control drawings.

3.3.2 Viewing Unless otherwise specified, conductor layers shall be numbered consecutively, starting at the substrate, as shown in Fig. 3-1.

3.3.3 Location Dimensioning All vias, test points, terminal areas, and overall completed circuit dimensions shall be dimensioned by use of a modular grid system, except where necessary to mate parts not on grid. The choice of the primary modular grid system used in the design of hybrid circuits shall be metric (SI) and the basic modular units of length shall be .5 mm and 0.05 mm; in that order of preference, and shall be applied in the X and Y axis of the Cartesian coordinates. The secondary modular grid system is inch based, where the basic modular units of length shall be 0.025 or other multiples of 0.005 inch; in that order of preference, and shall be applied in the X and Y axis of the Cartesian coordinates.

3.3.4 Hole Location Tolerance Unless otherwise specified, the location of holes and/or vias shall be dimensioned with respect to single or secondary grid systems.

3.3.5 Processing Allowances The processing allowances which were considered in the design and artwork preparation for the hybrid circuit shall be documented and defined on the master drawing in accordance with IPC-D-325, in either note form, or by reference to another drawing which contains artwork specifications (see Section 5).

3.3.6 Datums There shall be a minimum of two datum features to establish the mutually perpendicular datum reference frame for each circuit. Each datum shall be established by at least two holes, points, symbols, or other datum features, but not edges, and be included on all conductive layers. Critical design features may require the use of more than one set of datum references. The master drawing shall establish the relationship and acceptable tolerance between all datum features. All datum features shall be located on grid, or establish grid criteria, as defined on the master drawing, and should be within an outline of the hybrid circuit.

3.4 Electrical Requirement Considerations

3.4.1 Conductor Thickness and Width The minimum width and thickness of conductors on the finished circuit should be determined on the basis of the current-carrying capacity required, and the maximum permissible conductor temperature rise; processing allowances (see 3.3.5) shall be considered in the evaluation. Conductor width and thickness values shall be not less than the dimensions established in Table 3-1. In general, the designer should base dimensions on supplier data for the specific conductor material used. For impedance/capacitance control considerations see paragraph 3.4.3. For ease of manufacture and durability in usage, these parameters should be maximized while maintaining the minimum recommended spacing requirements defined herein (see Table 3-1).

3.4.2 Electrical clearance Spacing between conductors on individual layers (same plane) in multilayer hybrid circuits shall be in accordance with the requirements of Table 3-1.

3.4.3 Impedance/Capacitance Control Considerations Multilayer hybrid circuits are ideally suited for providing interconnection wiring that is specifically designed to provide desired levels of impedance and capacitance control. Techniques commonly referred to as "strip-line," or "embedded microstrip," (see Figure 3-5) are particularly suited for impedance and capacitance requirements.

As shown in Figure 3-5, there are four basic types of transmission line constructions. These are:

1. Microstrip or "open-line," where the external center conductor is separated from the reference plane (shield) by a single thickness of dielectric material.
2. Embedded microstrip, where the center conductor is bounded on all sides by dielectric material that separates it from a single reference plane (shield).
3. Balanced stripline, where the center conductor is bounded on all sides by dielectric material that separates it equally from two reference planes.
4. Unbalanced stripline, where two or more layers of conductors are separated from a combination of reference planes in an unbalanced configuration.

The characteristic impedance of a microstrip can be calculated using the formula:

$$Z_0 = \frac{87}{\sqrt{e_r + 1.41}} \ln \frac{(5.98h)}{(0.8W + t)}$$

where e_r = relative dielectric constant of substrate material (see Table 3-5)

w, h, t are dimensions indicated in Figure 3-7.

The most commonly used microwave circuit technique is microwave stripline (Figure 3-6A).

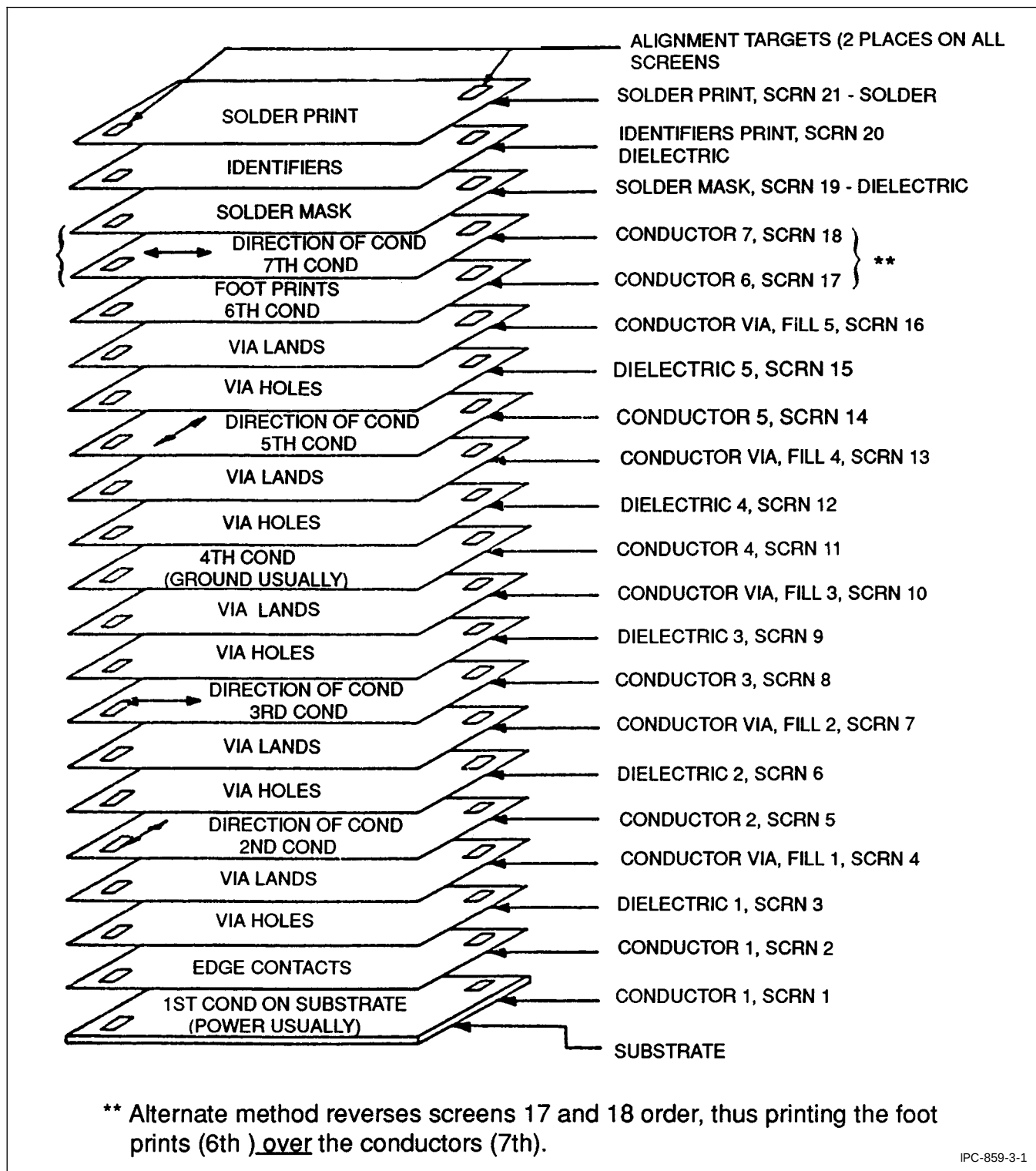


Figure 3-1 Screening masks typically required for thick film processing

typically transmitted in a mode such that all the energy is propagated in the direction of the electric field and none in the direction of the magnetic field.

Figure 3-7 illustrates the electric field and typical parameters involved in microstrip design.

When the conductor is covered with a dielectric material such as solder mask (embedded microstrip), the impedance characteristics will be reduced depending on the thickness and dielectric constant of the material (approximately 5 percent).

Table 3-1 Dimensional Constraints for Thick-Film Conductors and Lands

Conductor and Land Sizes and Spacing	Minimum Dimension mm [inch]	Nominal Dimension mm [inch]	Maximum Dimension mm [inch]	Figure Item
Conductor to edge of substrate for conductors ≤ 0.38 mm [0.015 inch]	0.25 [0.010]	0.51 [0.020]	None	3-2 ¹
Conductor to edge of substrate for conductors > 0.38 mm [0.015 inch]	0.25 [0.010]	0.32 [0.0125]	None	3-2 ²
Exit bonding lands (width and length)	0.25 [0.010]	0.32 [0.0125]	None	3-2 ³
Wire bonding lands (width and length—one or two wires on same land) (preferred)	0.25 [0.010]	0.32 [0.0125]	None	3-2 ⁴
Wire bonding lands (width and length—one wire per land (special)	0.25 [0.010]	0.32 [0.0125]	None	3-3 ⁵
Conductor width (preferred)	0.25 [0.010]	0.51 [0.020]	None	3-2 ⁶
Conductor width (special)	0.13 [0.005]	0.25 [0.010]	None	3-3 ⁷
Conductor-to-conductor spacing (preferred)	0.25 [0.010]	0.51 [0.020]	None	3-2 ⁸
Conductor-to-conductor spacing (special)	0.13 [0.005]	0.25 [0.010]	None	3-3 ⁹
Conductor-to-resistor spacing (on untrimmed side of resistor)	0.25 [0.010]	0.38 [0.015]	None	3-4 ¹⁰
Conductor-to-resistor spacing (on trimmed side of resistor)	0.38 [0.015]	0.51 [0.020]	None	3-4 ¹¹
Conductor-to-resistor spacing, top-hat configuration	0.76 [0.030]	0.89 [0.035]	None	3-2 ¹⁵
Upper and lower conductor widths at crossover junction	0.25 [0.010]	0.38 [0.015]	None	3-4 ¹²
Crossover conductor-to-connecting-conductor overlap-length	0.25 [0.010]	0.32 [0.0125]	None	3-4 ¹³
Conductor crossover dielectric overlap	0.25 [0.010]	0.38 [0.015]	None	3-4 ¹⁴
Dielectric to resistor spacing	0.51 [0.020]	0.51 [0.020]	None	3-4 ¹⁶

Plane sequences should be arranged so that the signal layers are symmetrical about the ground or voltage plane. This may be accomplished several ways provided that any adjacent signal layers, not separated by a ground or voltage plane must have their key axes running perpendicular to each other. (see Figure 3-1).

DC power and ground planes also function as AC reference planes. Power and ground connector pins should be evenly distributed along the edge of the board for AC reference.

3.4.3.1 Capacitance Considerations The capacitance associated with a single crossover (see Figure 3-8) is very small and is typically a fraction of a picofarad. As the number of crossovers per unit length increases, the intrinsic capacitance of the transmission line also increases. The crossover lumped capacitance adds to the intrinsic line capacitance. Crossover capacitance may be approximated:

$$C(\text{pF}) = 5.72 E_r(l + 0.8h) \frac{(W + 0.8h)}{h}$$

provided that $l \geq 0.5h$
 $W \geq 0.5h$

Where:

E_r = dielectric constant
 h = dielectric thickness between crossovers (mm)

l = length (mm)

W = width (mm)

The distributed coupling capacitance between two parallel conductors on the same layer (see Figure 3-9), assuming 0.015 mm [0.0006 inch] print thickness, is given by

$$C_C = \sum_{n=1}^N 6.7 \times 10^{-4} \frac{l_n}{d_n} \text{ pF}$$

Where: l_n = length of parallelism between the conductors
for separation d_n
 d_n = perpendicular distance between the conductors

The above equation is a first order approximation which disregards capacitance contributed by all other conductors distributed across the entire substrate. It is assumed that the first order contributions constitute 90% or more of the coupling capacitance, and that coupling between adjacent conductors is the prime concern.

Circuit design shall specify the allowable capacitances from which the required spacing and maximum parallelism shall be determined.



Documents

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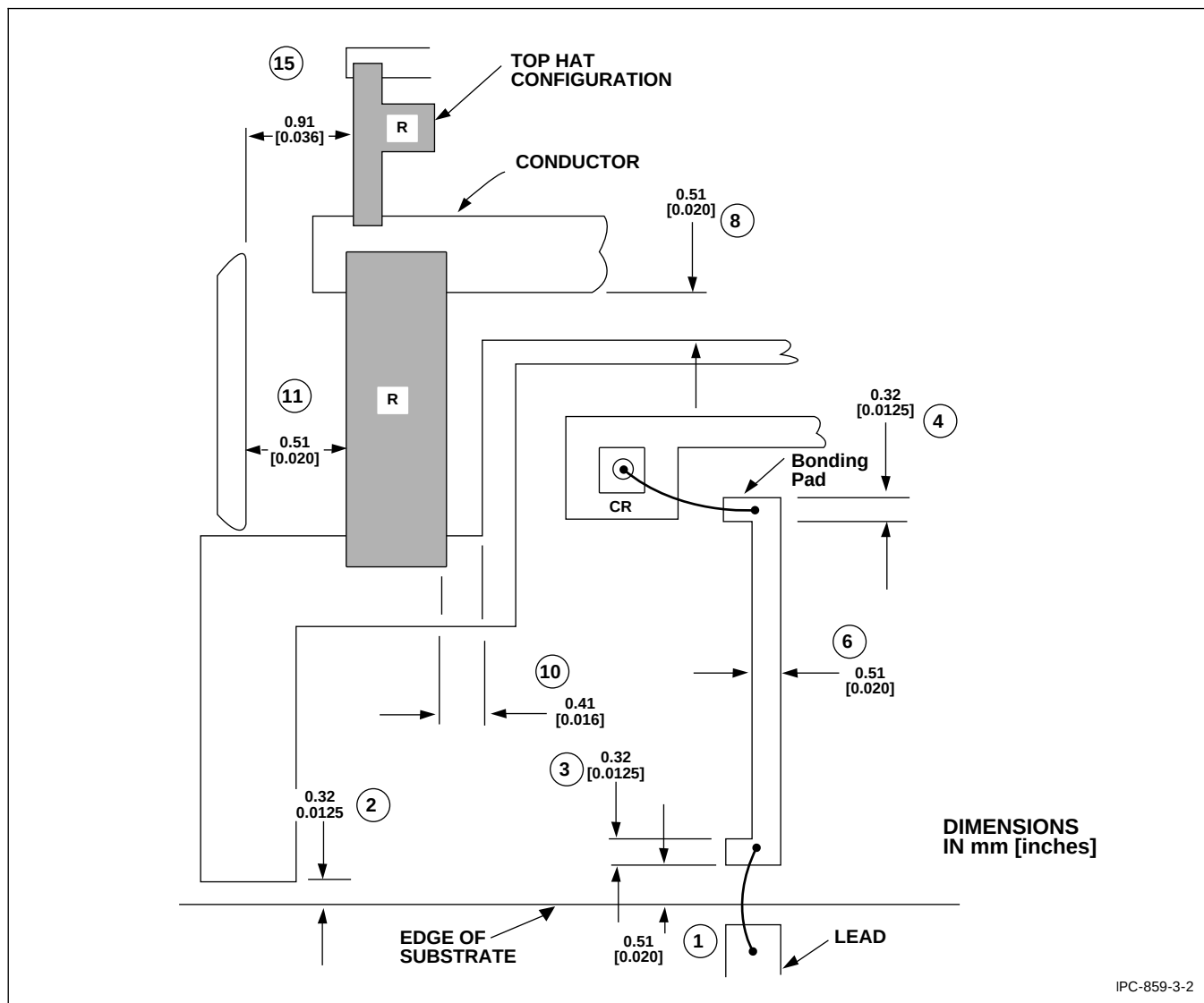


Figure 3-2 Nominal thick film conductor and land dimensional constraints (see Table 3-1)

3.4.4 Power Distribution Considerations Power distribution is important in the design of a multilayer hybrid circuit. The grounding scheme, as a part of the distribution system, provides not only a DC power return, but also provides an RF return plane for digital logic to be referenced.

In a typical multilayer design, a combination power/ground plane is screened directly on the substrate. Vias for the power and ground connections are often made larger than the vias for signal interconnection because the power and ground connection vias carry more power and they traverse more layers. Above this are alternate layers of dielectric and interconnect metallization.

The top layer contains all device I/O bonding lands and the substrate I/O lands. If space permits, this layer may also contain some interconnections.

Metallization lands are provided for physical attachment of the integrated circuit chips. These lands are normally con-

nected to ground or a voltage supply. Eight metallization layers are generally considered to be a reasonable maximum. The base metal in coated metal-core substrates may be utilized as a ground plane that is contacted directly by printing a circuit directly over a via through the coating.

The following items should be taken into consideration:

1. Maintain a lower RF impedance throughout the DC power distribution. An improperly designed ground can result in RF emissions as a result of radiated field gradients developed across the uneven circuit impedance, and its inability of decoupling capacitors to efficiently reduce the EMI.
2. Decouple the power distribution at the hybrid circuit connector using a 1.0 to a 10.0 microfarad tantalum capacitor.
3. A ceramic capacitor of approximately 0.01 microfarads should be connected across VCC or source voltage.

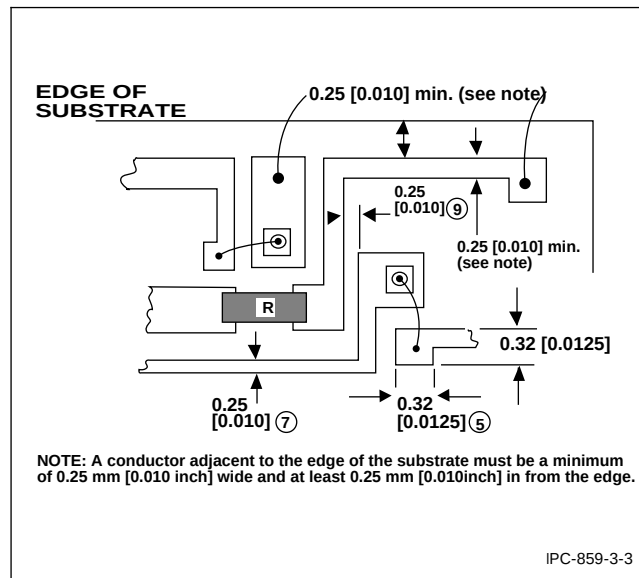


Figure 3-3 Special fineline conductor dimensions (nominal) and positioning constraints (see Table 3-1)

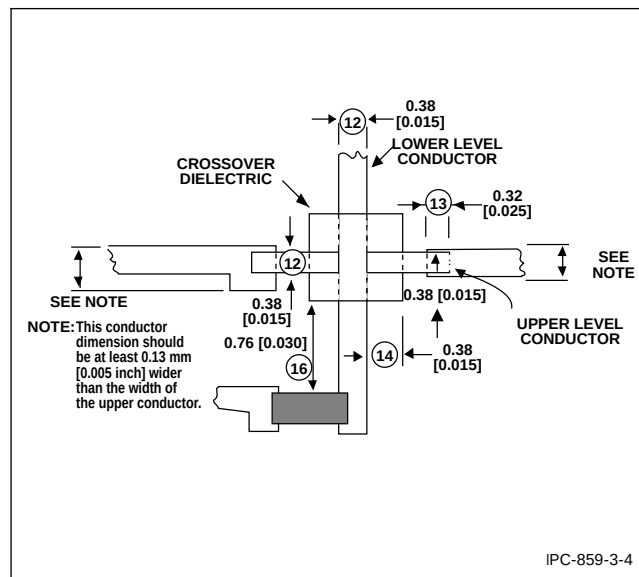


Figure 3-4 Nominal thick film crossover dimensions (see Table 3-1)

one capacitor for not more than five logic devices and one for no more than two memory devices.

4. Minimize the impedance and radiation loop of the decoupling capacitor by keeping capacitor leads as short as possible, and locating them adjacent to the integrated circuit.

The power and ground planes are solid when using the gold system.

The power and ground planes are typically gridded with 0.4 mm [0.015 inch] conductors, and 0.25 mm [0.010 inch] spaces as shown in Figure 3-10 when using the copper system.

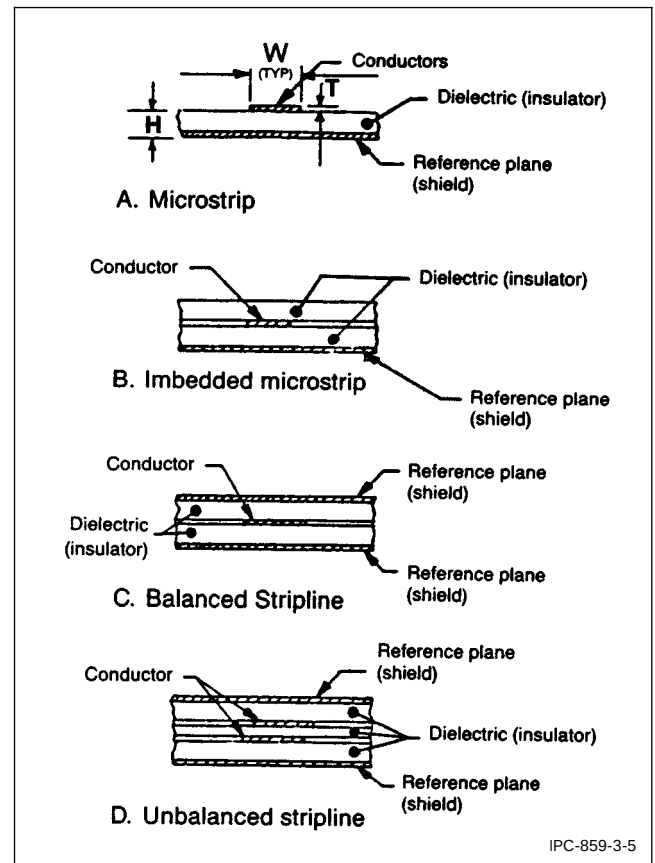


Figure 3-5 Transmission line multilayer hybrid circuit construction

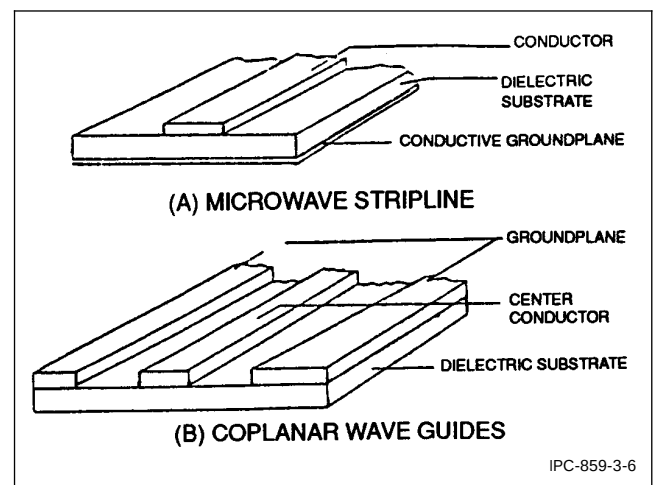


Figure 3-6 Typical microwave circuit types

In digital power distribution schemes, the grounding and power should be designed first, not last, as is typically done. All interfacing, including power, should be routed to a single reference edge, or area. Avoid opposing end interconnections. At the interconnection reference edge, all ground structures are to be made as heavy as possible.

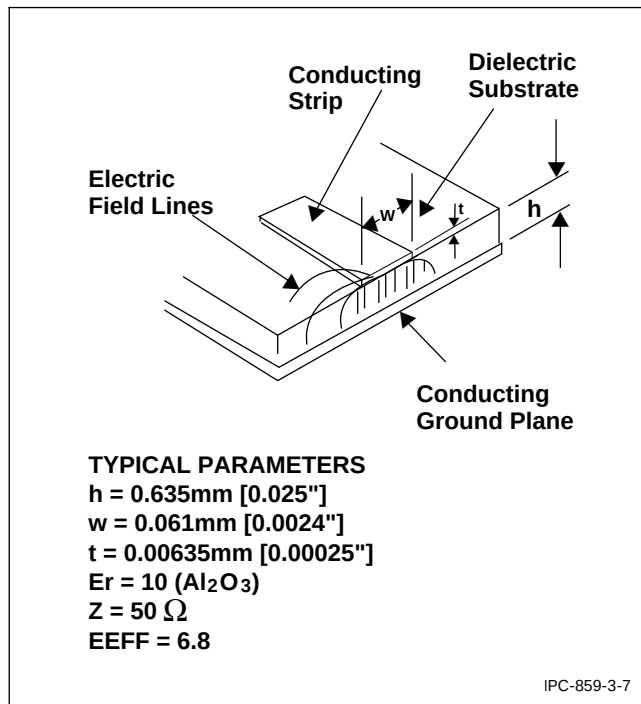


Figure 3-7 Stripline electric field

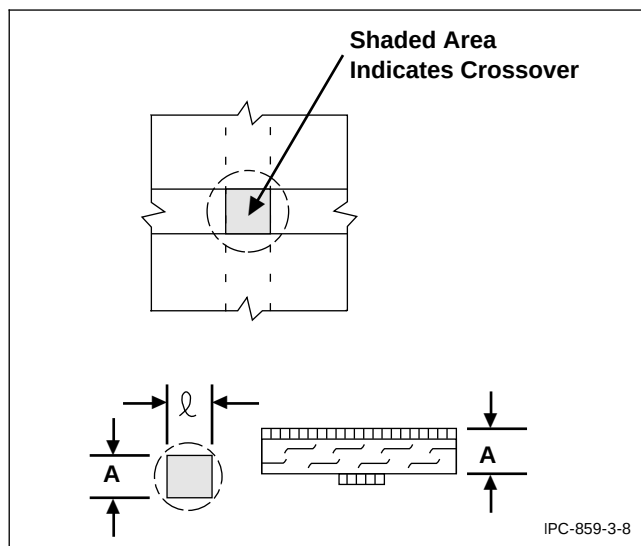


Figure 3-8 Crossover capacitance

The shortest possible conductor length should be used between devices. The hybrid circuit should be separated into areas for high, medium, and low frequency circuits.

3.4.5 Circuit Type Considerations

3.4.5.1 Digital Circuits Digital circuits are composed of electronic components that can provide state information (1 or 0), as a function of the performance of the overall circuit. Normally, logic integrated circuits are used to perform this function; however, discrete components may also be used sometimes to provide digital responses.

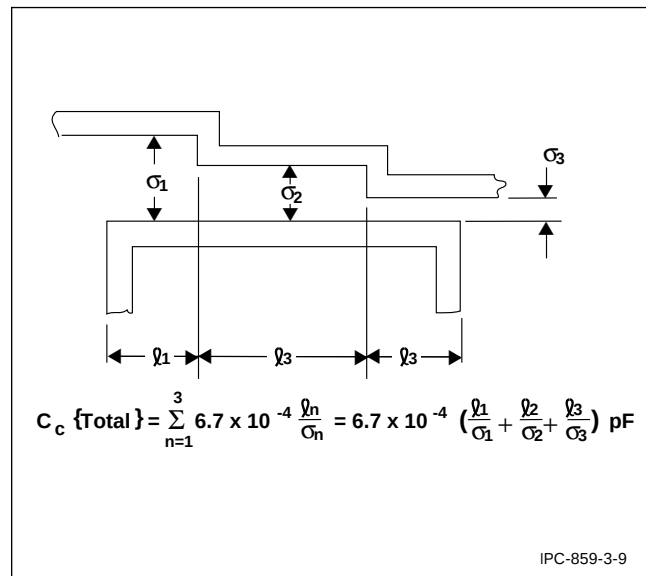


Figure 3-9 Example of parallel line coupling capacitance calculation

Integrated circuit devices use a variety of logic families. Each family has its own parameters regarding the speed of the digital transmission, as well as the temperature rise characteristics necessary to provide the performance. In general, a single board usually uses the same logic family in order to facilitate a single set of design rules for conductor length for signal driving restrictions. Some of the more common logic families are:

- TTL—Transistor Transistor Logic
- MOS—Metal Oxide Semiconductor Logic
- CMOS—Complimentary Metal Oxide Semiconductor Logic
- ECL—Emitter Coupled Logic
- The following guidelines should be used on all logic designs to improve the testability of the multilayer printed board assembly.

1. Connect the set, clear, or reset of all flip-flops to reset terms. Power up reset is ideal. See Figure 3-11.
2. Connect the clear or master reset of counters to reset terms or provide preset logic. See Figure 3-12.
3. Provide a method to disable free-running oscillators, and provide a pin-out to an unused I/O on the oscillator clock line.
4. Provide outputs to unused I/O pins for feedback or "deep" logic loops. This also applies for serial logic.
5. Keep direct output control, wherever possible, on all LSI devices to enhance their testability.
6. Provide jumper lines from the delay line clock circuits to unused I/O pins, so that intermediate clocks may be controlled.

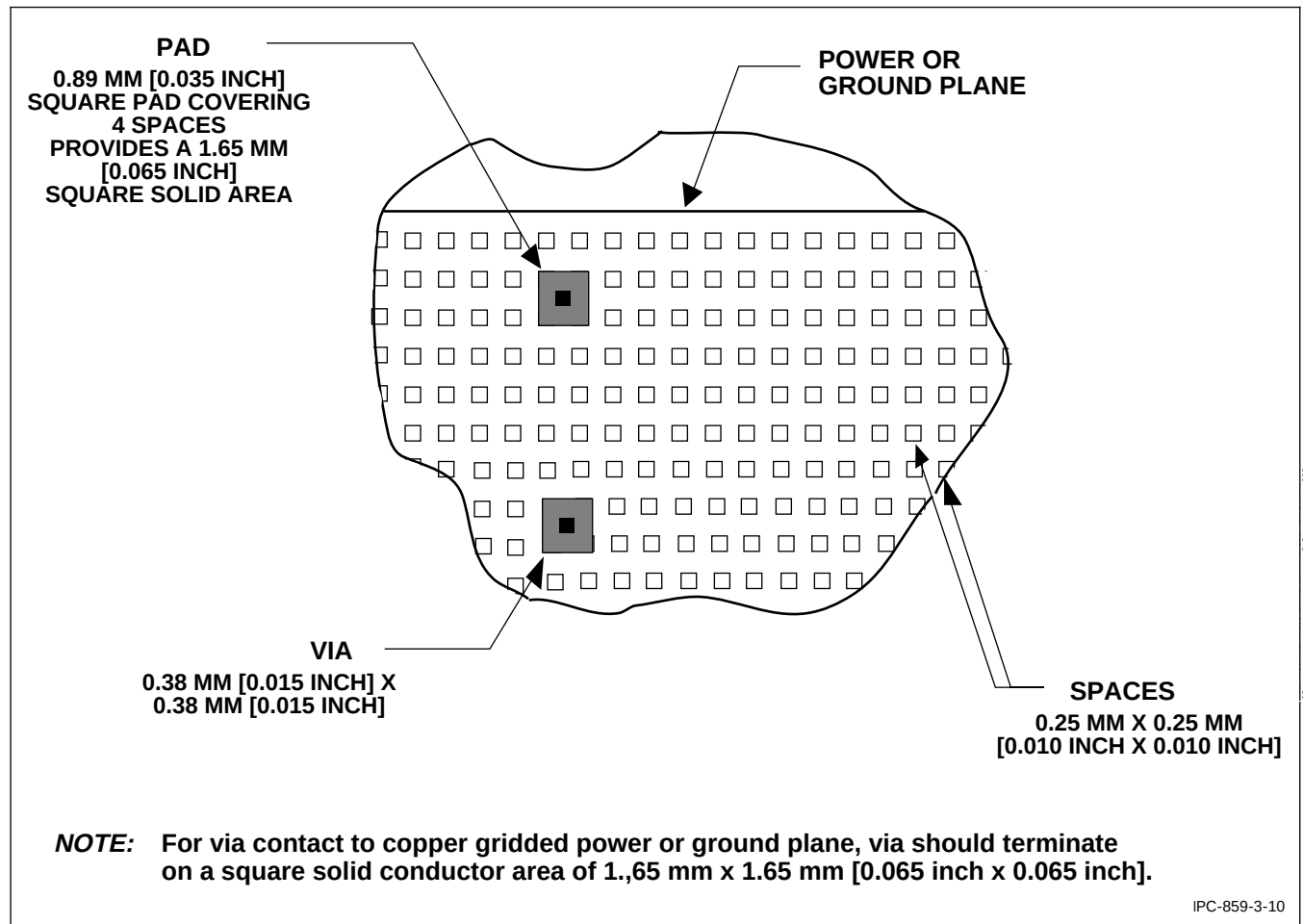


Figure 3-10 Power and ground planes along with conductor areas exceeding 6.45 square mm [0.01 square inch] (0.38 mm [0.015 inch] conductors and 0.25 mm [0.010 inch] spacing on a 0.64 mm [0.025 inch] grid [CAD]).

7. Provide test points to appropriate conductors in untestable circuits.
8. The maximum unterminated line length for a high speed digital circuit is given by:

$$l_{mw} = \frac{t_r}{2t_{pd}}$$

where:

t_r = rise time (10–90%) in nanoseconds
 t_{pd} = propagation delay (see Table 3-2)

9. Provide wrap-around test capability of resistors.
10. Provide test points to control lines in memory circuits for off-line testing.

3.4.5.2 Analog Circuits Analog circuits are usually made from discrete devices, and provide the wave-form characteristics necessary to describe a circuit. Standard discrete components (resistors, capacitors, diodes, transistors, etc.), as well as power transformers, coils and chokes, are usually the types of components used for analog circuits.

Some of the rules to be followed when designing analog printed board assemblies are:

1. Always determine correct polarity of the component, if applicable.
2. Transistor emitter/base and collector should be properly identified (ground transistor case where applicable).
3. The maximum allowable lead length for analog signal interconnections shall be in the order of:

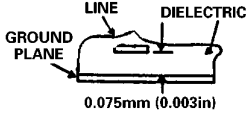
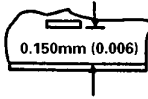
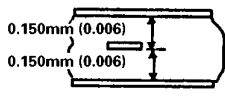
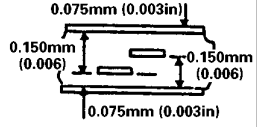
$$l_{MAX} = \frac{\lambda}{8} \text{ mm [inch]}$$

where: λ = signal wave length in mm [inches]

In instances where line lengths approach maximum, an evaluation shall be made to insure that excessive impedance mismatches that may result will not adversely affect electrical performance.

4. If different grounds are used, keep grounding busses as far away as possible.
5. As opposed to digital signals, analog design should have signal traces considered first, as ground planes, or ground conductors can be used to complete circuit connections.

Table 3-2 Conductor Electrical Parameters (10 Mil wide Conductors, Experimental Results)

	Configuration	Parameter Units*	Gold System**	Copper System***
	Microstrip ~0.152 mm [0.006]	C	0.311	0.220
	Dielectric	R	0.015	0.014
	Thickness (h)	t pd	0.0079	0.0079
		Z ₀	33.30	43.40
		S ₂₁	-7.20	-5.87
		E _R	5.70	3.30
	Microstrip ~0.152 mm [0.006]	C	0.185	0.141
	Dielectric	R	0.015	0.015
	Thickness (h)	t pd	0.0079	0.0075
		Z ₀	46.20	62.30
		S ₂₁	-5.93	-5.31
		E _R	5.20	2.90
	Stripline ~0.305 mm [0.012]	C	0.295	0.202
	Dielectric	R	0.015	0.0122
	Thickness (h)	t pd	0.0087	0.0079
	t ≅ 0.0127 mm [0.0005]	Z ₀	35.50	46.10
		S ₂₁	-5.91	-4.94
		E _R	5.30	2.80
	Unsymmetrical Stripline ~0.2286 mm [0.009]	C	0.370	0.276
	Dielectric	R	0.0106	0.0106
	Thickness (h)	t pd	0.0087	0.0083
	t ≅ 0.0127 mm [0.0005]	Z ₀	30.00	36.20
		S ₂₁	-6.47	-5.31
		E _R	4.80	2.50

*C (Capacitance) pF/mm; R (Resistance) Ohm/mm; t pd (Propagation Delay) ns/mm;
Z₀ (Characteristic Impedance) Ohms; S₂₁ (Forward Transmission Loss at 300 MHz) dB;
E_R (Apparent Dielectric Constant—estimated from Z₀)

**Solid ground and voltage planes used for Gold System

***Gridded ground and voltage planes (0.38 mm lines and spaces) used for Copper System

- Keep heat sensitive and heat radiating components as far apart as possible (incorporate heat sinks whenever necessary).

3.4.5.3 Conductor Spacing In high frequency analog and high speed digital circuits, a minimum of one line width shall be maintained as spacing between any two adjacent signal conductors. Very critical signals shall have line width and spaces or shielding as required to insure sufficient isolation and to minimize noise coupling as specified.

3.5 Thermal Requirement Considerations Hybrid electronic technology is capable of performing within the temperature range of -55° to +125°C. In fact, the basic thick-film technology can perform satisfactorily at temperatures significantly beyond this range. The limiting factor is most often the performance of the attached active components or the inherent power dissipation of the circuit.

Power dissipation has a major influence on circuit partitioning and ultimate package size. Also, all material and component operating capabilities are limited by inherent maximum operating temperatures, above which their performance may either degrade seriously or catastrophic failure may occur. With semiconductors, this temperature is usually specified in terms of a maximum junction tempera-

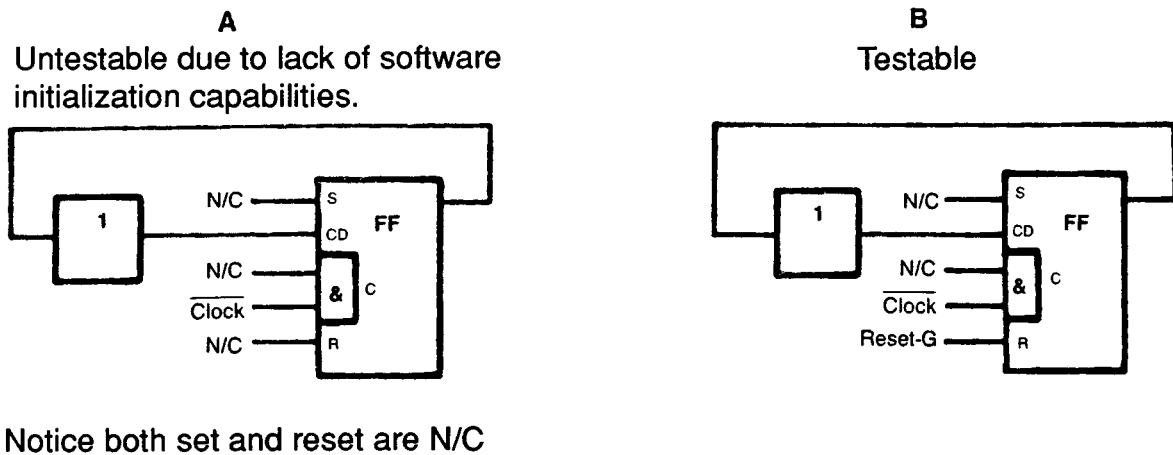
ture. For other components, the maximum body temperatures and hot-spot temperatures are commonly used as the figures of merit.

In any case, the maximum operating temperature of an electronic material or component is a direct result of the electrical power dissipated in the element and/or the temperature and heat-transfer characteristics of the environment associated with the component. All components, especially resistors and active devices, will dissipate heat in the performance of their normal electrical function. Therefore, the problem is to remove the heat as quickly as possible to prevent temperature rises within the heat-generating elements.

Because of their small size and high component densities, microcircuits are subject to high power densities and poor heat transfer capabilities. As a result, thermal power density, rather than component density, may be the limiting factor in certain microcircuit designs.

Thermal design considerations and thermal analysis techniques are very important steps in the design cycle. Therefore, the hybrid designer should have a thorough knowledge of thermal design guidelines, the thermal properties of materials, thermal analysis techniques and the thermal evaluation of thick-film circuits.

Connect the set, clear or reset of Flip Flops to reset terms. Power up reset is ideal for this.

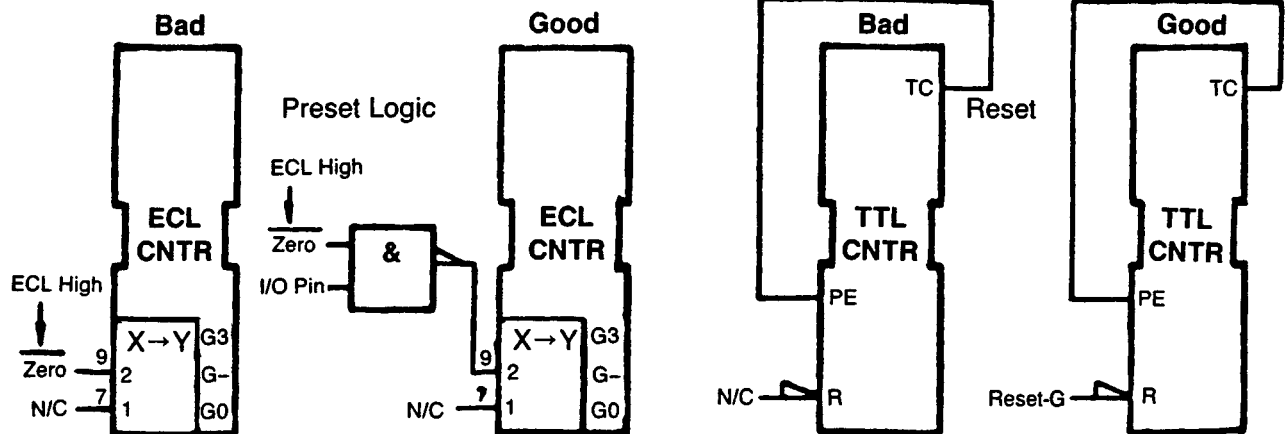


IPC-859-3-11

Figure 3-11 Flip-flop testability

Connect the clear or master reset of counters to reset terms or provide preset logic.

Untestable due to lack of software initialization capabilities.



IPC-859-3-12

Figure 3-12 Master clear for counters

The following are important heat transfer considerations.

3.5.1 Material Selection Select materials with good thermal conductivity. Table 3–3 is a useful guide for material selection.

Table 3–3 Typical Hybrid Materials Thermal Conductivity

Material	Thermal Conductivity W/°C/mm
Silicon	58.4
Kovar	9.1
Molybdenum Tab	99.1
Alumina (Al ₂ O ₃)	17.5
Beryllia (BeO)	139.7
Conductive Epoxy	1.02
Epoxy Preform	0.25
AuSi Eutectic Bond	144.8
AuSn Solder	114.3

3.5.2 Substrate Dimensions Use a thick substrate for best heat transfer and distribution unless it is to be bonded to a heat sink, in which case the thinnest possible substrate should be used.

The substrate area required for a given electronic circuit is greatly dependent upon power levels of components. Thus, low power level circuitry can be packaged more densely than power circuits.

The use of some first approximation “rules-of-thumb” for the number of devices (chips) that can be accommodated with a given technology in various package sizes, would provide a starting point, together with the thermal considerations, for deciding if the given circuitry needs to be partitioned. Another deciding factor in partitioning is the input/output (I/O) requirements of the circuitry.

3.5.3 General Guidelines

- Distribute power sources as evenly as possible over the substrate surface to reduce hot spots and to maintain a uniform thermal profile.
- Locate the highest-power sources over or near heat sinks.
- Do not locate high-power sources near substrate corners or edges unless heat sinking is provided in that vicinity.
- Design power resistors as large as possible and assure that sufficient area will be maintained after adjustment.
- High-heat dissipating components should be attached to the substrate in such a manner as to provide the lowest possible thermal resistance between the components and the substrate.
- Components should not be attached over the other heat

dissipating elements, i.e., chip capacitors over thick-film resistors.

- For best thermal performance, make the junction between a backside-mounted semiconductor chip and the substrate with a material of low thermal resistance that is as thin as possible, and provide a uniform contact area that is free from voids. (In this regard a knowledge of process capability is critical. If the worst-case die-attachment wettability is 50%, base heat transfer calculations on the reduced area.)
- When wire leads or pins are attached to a substrate: (1) make leads or pins as short as possible, (2) select a pin material of high thermal conductivity and a pin size with the maximum possible cross-sectional area, (3) use as many leads as possible, and (4) locate heat sources as near to the pins as possible.
- In final packaging: (1) select a package configuration that will provide the best thermal conductivity for a specific application, (2) provide a good thermal conduction path between the substrate and the package case, and (3) avoid air spaces in the thermal conductivity path if possible. Plastics with high thermal conductivity can be used to fill voids and improve heat transfer.

3.5.4 Heat Dissipation Calculations The rise in temperature of each component can be estimated using a model of thermal resistance and power dissipation in which the temperature rise is calculated as:

$$T = R \times P$$

- where
- T = temperature rise of the device above the hybrid case (°C)
 - R = total thermal resistance between the device and the hybrid case (°C/W)
 - P = power dissipated in the device (W)

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case (see Figure 3–13). Thus:

$$R_t = R_1 + R_2 + R_3 + R_4 + R_5$$

- where
- R_T = total thermal resistance from the top of the device to the bottom of the hybrid case.

If parallel thermal paths are involved, the parallel thermal resistances are totaled in the same manner as are parallel electrical resistances.

The thermal resistance of a particular material layer is calculated as:

$$R = \frac{t}{KA}$$



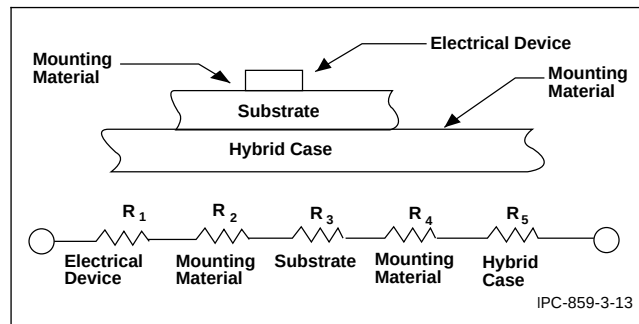


Figure 3-13 Example of total thermal resistance calculation

where R = thermal resistance of the material layer ($^{\circ}\text{C}/\text{W}$)
 t = thickness of the material layer (mm)
 K = thermal conductivity of the material in ($\text{W}/^{\circ}\text{C}\text{-mm}$)
 A = cross-sectional area of the material layer (mm^2)

Table 3-3 gives the thermal conductivity of typical materials used in hybrids.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. As illustrated in Figure 3-14 it is adequate to assume that spreading occurs at a 45 degree angle.

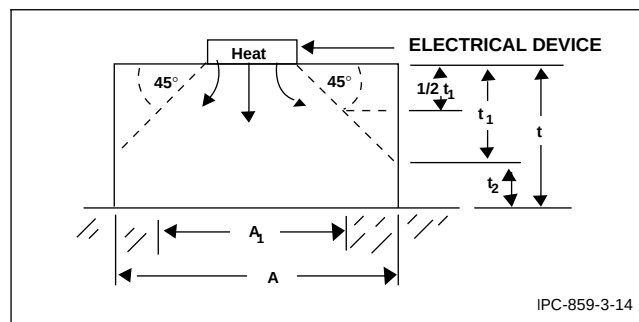


Figure 3-14 Thermal resistance during heat spreading

To calculate thermal resistance when heat spreading occurs, the average cross-sectional area should be used over the range of spreading. As shown in Figure 3-13 the total thermal resistance (R_T) will be:

$$R_T = R_1 = \frac{1/2t_1}{KA_1} + \frac{t_2}{Ka}$$

Notes: 1. Use average area A over thickness $1/2t_1$. 2. Use area A over thickness t_2 . 3. No spreading occurs over t_2 .

To the maximum extent possible, devices dissipating significant amounts of power should be spaced in the hybrid in such a manner as to spread the heat flow throughout the case. When devices are close enough that their areas of heat spreading overlap, based on the 45 degree assumption, their thermal interaction should be taken into account. This

can be done by limiting the cross-sectional area used in the thermal-resistance calculations to areas that do not overlap the heat spreading of other devices.

When device power dissipation becomes significant, steps may be taken to minimize the temperature rise. Devices may be eutectically mounted directly to the substrate or to ceramic, molybdenum, or kovar "tabs" to increase heat spreading and to reduce thermal resistance. In extreme cases, but at considerable cost, devices can be mounted on Beryllia substrates or metal heat-sinks.

Note that in the above discussion the temperature rise is related to the hybrid case temperature, not to the ambient air or to the hybrid mounting surface. The hybrid case temperature will in turn be a function of the ambient air and mounting surface temperature, the thermal properties of the mounting surface, and the hybrid to mounting surface interface.

3.5.5 Thermal Matching A primary thermal concern with ceramic surface-mounted components is the thermal expansion mismatch between the component and the substrate. This mismatch may result in fractured solder joint interconnections if the assembly is subjected to thermal shock, thermal cycling, power cycling and high operating temperatures. The number of fatigue cycles before solder joint failure is dependent on, but not limited to, the thermal expansion mismatch between the component and the substrate, the delta temperature excursion over which the assembly must operate, the solder joint size, the size of the component, and the power cycling that may cause an undesirable thermal expansion mismatch if a significant temperature difference exists between the component and the substrate.

With surface-mount components, the number of fatigue cycles can be increased by reducing the thermal expansion mismatch, reducing the temperature gradient, increasing the height of the solder joint, using the smallest physical size component wherever possible, and by optimizing the thermal path between the component and the substrate.

3.6 Mechanical Requirement Considerations

3.6.1 Camber All multilayer hybrids will warp to some degree unless rigidly supported along all edges. The construction of the board should be as symmetrical as possible with respect to conductor area distribution and to a lesser degree, the amount of dielectric applied in which there exists a Coefficient of Thermal Expansion (CTE) mismatch between the dielectric and the supporting substrate. Warping is more likely to occur on the boards having large width-to-length ratios and in boards having large conductor areas on one side.

3.6.2 Support All hybrid circuit assemblies should be supported in order to minimize stress on the components.

and electrical connections. This support should also be sufficient to help prevent cracking or loosening of conductors, breaking of part leads or wire bonds, or cracking or chipping of the substrate resulting from flexing stress on the assembly.

3.6.3 Shock and Vibration The ultimate ability of components to survive shock and vibration environments will depend upon the degree of consideration given to the following factors

- A. The worst-case levels of shock and vibration environment for the entire structure in which the hybrid circuit assembly resides, and the ultimate level of this environment that is actually transmitted to the components. (Particular attention should be given to equipment that will be subjected to random vibration.)
- B. The method of mounting the assembly in the equipment to reduce the effects of the shock and vibration environment, specifically the number of mounting supports, their interval, and their complexity.
- C. The attention given to the mechanical design of the assembly, specifically its size, shape, type of material, material thickness, and the degree of resistance to bowing and flexing that the design provides.
- D. The shape, mass and location of the components mounted on the assembly.
- E. The component lead wire stress relief design as provided by its package, lead spacing, lead bending, or a combination of these, plus the addition of restraining devices.
- F. The attention paid to workmanship during assembly, so as to insure that component leads are properly bent, not nicked, and that the components are installed in a manner that tends to minimize component movements.
- G. Conformal coating may also be used to reduce the effect of shock and vibration on the assembly.

The selection of components to be mounted on assemblies subjected to severe shock and vibration should favor, where circuit design permits, the use of components that have lightweight, low-profile packages and that have inherent strain relief provisions. Where discrete components must be used, preference should be given to axially-leaded types that present a relatively-low profile, and that can be mounted and easily clamped in intimate contact with the board surface.

The use of irregularly-shaped components, especially those having a large mass and a high center of gravity, should be avoided where practical. If their use cannot be avoided, they should be located toward the outer perimeter of the assembly where the guides and/or connectors can help to

provide resistance to flexing. Depending on the severity of this problem, the use of mechanical clamping, adhesive bonding, or embedding may be required.

3.7 Test Requirement Considerations The circuit layout configuration, uniformity of the hybrid circuit size, shape and functional connector interface will have an effect on the manufacturability, testability, and cost of the finished assembly. These aspects must be considered early in the design stage of product development. Some important test considerations are specified in the following paragraphs.

3.7.1 Hybrid Circuit Layout Design The design layout from one design to another should be such that designated areas are identified by function, i.e., power supply section confined to one area, analog circuits to another section, and logic circuits to another, etc. This will help to minimize cross-talk, simplify test fixture design, and facilitate trouble-shooting diagnostics. In addition, the design should:

- Have circuit elements placed away from the assembly edges to allow adequate test fixture clearance.
- Have design grid layout compatible with testing plan.
- Allow provision for isolating parts of the circuit to facilitate testing and diagnostics.
- Where practical, group test points and jumper points in the same physical location on the circuit.
- Consider Large Scale Integrated (LSI) circuit socketing for components so that parts can be easily replaced for further testing.
- Consider surface mounted components and their patterns require special consideration for test probe access.
- Allow adequate space between devices for rework access.
- Orient devices in same direction if possible for ease of trouble-shooting and rework.

3.8 Materials The effect that one material may have upon another material within a hybrid is of extreme concern. Therefore, contemplated material substitutions should be reviewed to determine whether the proposed design is susceptible to failure mechanisms.

Nonconforming materials can result in failure of the hybrid circuit caused by one or more of the following conditions:

- A. Metal migration
- B. Corrosion or oxidation
- C. Ionic contamination
- D. Improper adhesion
- E. Intermetallic formation



- F. Differences in thermal coefficients of expansion
- G. Variations in electrical characteristics of screened components

3.8.1 Substrates The substrate serves as the supporting structure for the circuitry. It acts as a surface for depositing the conductive, dielectric, and resistive materials that form the passive circuit elements. Also, it is a base for mechanical support of all active and passive chip components. It must be an electrical insulator to isolate the various conductive paths of the circuit, and it must have sufficient thermal conductivity to remove heat generated by the circuit components. See Table 3-4 and 3-5 for substrate selection criteria.

The material most suitable for the particular application should be determined by examining the following properties of substrate materials:

- A. **Thermal conductivity**—The ability of the material to conduct heat away from critical circuit components. Normally measured as cal-cm/sec-cm²-°C. High thermal conductivity is desired.
- B. **Electrical insulation**—The ability of the material to insulate various circuit components from one another. Normally measured in ohm/cm. High resistivity is desired.
- C. **Mechanical strength**—The ability to withstand mechanical shock. Young's modulus, flexural strength, tensile strength, and compressive strength are considered measures of mechanical strength. High strength is desired.
- D. **Refractory property**—The ability of the material to withstand high temperatures. Melting point is an indicator of this property. This property is usually desirable, and absolutely mandatory for processes requiring heat treatment.
- E. **Thermal expansion**—This property is an important consideration, especially when the structure is placed into a metal case or mounted to an organic interconnection substrate.
- F. **Chemical susceptibility**—The ability to withstand exposure to chemicals. It is very desirable for substrates to be inert to processing chemicals.
- G. **Weight**—Weight may or may not be a consideration based on the application.
- H. **Metallizability**—The ability of the material to be successfully metallized.
- I. **Cost**—There are wide variations in the cost of substrate materials.

Table 3-4 Nonphysical Substrate Selection Criteria

Material	Cost per 25 x 25 mm [1 x 1-inch] Substrate for			Applications	Remarks
	100	5000	100K		
Alumina	Medium	Medium	Very low	General Use	Very popular
Beryllia	High	Medium	Low	Heat dissipating	Low thermal resistance
Porcelainized steel	Medium	Low	Low	Special shapes	Becomes cost effective for large substrates
Cofired multilayer ceramic	Very high	High	Medium	Package	May be cost effective in large quantities

Table 3-5 Important Characteristics of Substrates

Material	Tensile Modulus MPa	Coefficient of Thermal Expansion (ppm/°C)	Tensile Strength MPa	Thermal Conductivity (W/°C-mm)	Dielectric Constant (1 MHz)	Dissipation Factor
Alumina (90%)	324.07	6.70	317.17	16.74	9.40	*
Alumina (96%)	324.07	7.11	317.17	25.10	9.90	0.0001-0.0002
Alumina (99.6%)	344.75	6.30	448.18	37.40	10.00	0.0001-0.0002
Aluminum Nitride	291.66	4.30	367.50	170.00	8.80	*
Beryllia	319.93	8.00	*	250.00	7.00	0.0001
Quartz	72.40	0.72	*	0.75	3.80	0.0002
Sapphire	344.75	7.74	0.00	25.00	0.00	0.002
Porcelainized steel	*	4.40	89.64	1.67	5.50	*

* Indicates data not available

3.8.1.1 Alumina Substrates Alumina substrates are made of polycrystalline Al_2O_3 with small amounts of metal oxide glasses to achieve certain physical properties. Alumina is the most popular substrate material since it is readily available in sizes ranging from tiny chips to large area substrates, in thicknesses ranging from 0.25 mm [0.010 inch] to 1.25 mm [0.050 inch] or greater, and in a variety of shapes and designs. It is refractory and the finished substrate can be drilled or cut with diamond tools or lasers.

3.8.1.2 Beryllia Substrates Beryllia (polycrystalline BeO), with impurities for physical properties, is primarily used in applications requiring rapid heat removal from the circuit. Like alumina, Beryllia substrates are available in a large variety of sizes, thicknesses, shapes and designs. Beryllia is less-widely used than alumina due to its toxic nature in the powder form and its higher cost.

3.8.1.3 Coated Metal-Core Relatively new as a substrate, porcelainized steel substrates provide strength, shock resistance, a built-in ground plane, and relatively low cost for larger sized substrates. Prior to coating, the metal can be inexpensively shaped and punched to allow it to be used as a mounting bracket.

As a combination hybrid and discrete component mounting surface, porcelainized steel substrates can withstand such harsh environments as automobile engine compartments. Processing of these substrates requires low temperature firing and pastes compatible with that condition.

3.8.1.4 Quartz Substrates Quartz is available in two forms: (1) fused quartz or silica, and (2) single-crystal quartz.

- A. Fused Quartz—Fused quartz is similar to glass and is used in microwave applications because of its consistent dielectric constant and low RMS surface finish. As with glass, it is a poor thermal conductor and cannot be used in high heat dissipation applications. It is very fragile and extreme care must be exercised when it is handled. Its cost is moderate and the material is readily available from many sources.
- B. Single-crystal quartz—Single-crystal quartz is used in applications where an ordered crystal structure is necessary, e.g., in acoustic wave devices. The tensile strength of quartz varies according to the axis in which the crystal has been cut. The material is brittle and must be handled carefully. Its cost is generally considered to be exorbitant and, as with most crystals, its thermal conductivity is poor. However, single-crystal quartz does offer a very low RMS surface finish and it exhibits little or no camber.

3.8.1.5 Sapphire Substrates Sapphire is used in micro-

wave applications as a replacement for alumina substrates when a superior surface finish and low camber are required. Sapphire is an expensive single-crystal material (Al_2O_3) and is limited in size to the diameter of the boule from which it is cut.

The material is relatively strong but is a poor conductor of heat. The dielectric constant, as well as other mechanical and physical properties, will vary depending upon the crystal orientation. Therefore, care must be exercised to specify the proper crystal orientation.

3.8.1.6 Ferrite Substrates Ferrites are typically used in microwave applications where a magnetic material is required. Circulators are one example of this application. The material maintains a uniformity of substrate properties, e.g., dielectric constant and dissipation factor. Ferrites can be obtained with good surface finish qualities and low camber. However, ferrites are brittle and highly susceptible to impact shock breakage.

3.8.2 Conductive Materials The conductor, analogous to the wire in older technologies, is fabricated from materials of very low resistivity that is used to advance the signal (information to be processed or used) to the desired location with minimal losses.

3.8.2.1 Thick-Film Metallizations Thick-film conductors are typically silver, gold and alloys of these materials with either platinum or palladium. Glass frits and other additives are used which will affect the electrical characteristic of these materials. Copper-and nickel-based thick-film pastes are emerging as a new low-cost thick film conductor. (These materials are, however, in the development stage.)

3.8.2.1.1 Sheet Resistivity and TCR Table 3–6 lists nominal sheet resistivities and temperature coefficient of resistance (TCR's) of various thick-film conductor metallizations.

3.8.2.1.2 Thick-Film Conductors

- A. Gold (Au) conductors are used where high conductivity combined with long-term reliability are required.
- B. Platinum gold (PtAu) conductors are used where soldering is the only viable means of component attachment.
- C. Palladium gold (PdAu) is limited to use in those areas discussed under PtAu and where cost is to be kept as low as possible. PdAu is a relatively low cost alternative to PtAu.
- D. Silver (Ag) is used primarily in commercial applications where low cost is essential. Typical applications are in microcircuit displays and polymeric composites, adhesives, and sealants.

Table 3-6 Typical Film Conductor Resistivities and TCR's

Conductor compositions	Sheet Resistivity (O/square)	TCR PPM/°C	Line Resistance	
			25.4 x 0.5 mm [1 x 0.020]	25.4 x 0.13 mm [1 x 0.005]
Platinum gold	0.100	+800	5 ohms	20 ohms
Gold	0.003	+1250	0.15 ohms	0.6 ohms
Palladium silver	0.035	+1400	1.75 ohms	7 ohms
Silver	0.002	+1800	0.1 ohm	4 ohms

- E. Platinum silver (PtAg) is used where soldering of component is employed. Its application is limited presently to nonmilitary applications.
- F. Palladium Silver (PdAg) is a low-cost solderable conductor designed for good solder-leach resistance.
- G. Palladium platinum silver (PdPtAg) is a ternary metal composition which attempts to reduce the silver migration which has limited the utilization of silver-bearing inks in military applications. It provides a solderable conductor with good solder-leach resistance.
- H. Copper (Cu) was developed primarily for high conductivity and to reduce costs associated with noble conductors. The use of this material must be carefully evaluated, as the process employs tighter controls than those associated with noble metals.
- I. Nickel (Ni) is another low-cost substitute for noble metals. It finds its greatest use in display applications.
- J. Tungsten/molybdenum manganese (W/MoMn) materials require reducing atmospheres. The firing conditions require considerably greater controls which are generally not available in small laboratories. The inks are not readily available.

3.8.2.2 Attributes Table 3-7 lists typical attributes for thick-film conductors.

3.8.3 Resistive Materials A variety of characteristics are provided by materials that impede signal flow in a circuit and these entities are considered separately as passive elements in the circuitry. Table 3-8 lists the properties of thick-film resistors.

3.8.3.1 Ceramic Thick-Film Resistors Ceramic thick-film resistors have sheet resistivities in a large range of values and are available in a range from a very few ohms/square to high megohms/square. The resistivity is controlled by varying the metal-to-glass content which causes large variations in all mechanical and physical properties.

After screen printing, the pastes are dried and fired. Firing temperatures range from 750° to 900°C.

Most thick-film resistor systems are based on the use of ruthenium-oxide or lead/bismuth ruthenate metallurgies. These are relatively inexpensive systems which can be formulated in a range of sheet resistivities from 10 ohms/square to 1 Mohm/square.

Temperature coefficients as low as +50 PPM/°C are readily achievable in the mid-range of from 100 ohms/square to 100 Kohms/square. In the extended ranges, TCR's of +100 PPM/°C are available in resistors as low as 10 ohms/square and as high as 1 Mohm/square.

Table 3-7 Conductor System Attributes

Thick films	Die Bondability Methods			Wire Bondability		Solder Wetting	Solder Leach Resistance	Corrosion Resistance
	Eutectic	Solder	Organic	Gold	Aluminum			
Au	Good	Poor	Excellent	Excellent	Good	Excellent	Poor	Excellent
PtAu	NG	Good	Excellent	Fair to poor	Fair	Excellent	Good	Excellent
PdAu	NG	Fair	Excellent	Fair to poor	Fair	Good	Good	Excellent
Ag	NG	Poor	Excellent	Good	NG	Excellent	Poor	Poor
PtAg	—	Good	Excellent	Good	NG	Excellent	Fair to Good	Good
PdAg	—	Good	Excellent	Good	Good	Good to Exc.	Fair to Good	Good
PdPtAg	—	Good	Excellent	Good	Good	Good	Good	Good
Cu	NG	Good	Excellent	NG	Fair	Good	Excellent	Poor
Ni	NG	NG	Excellent	NG	NG	NG	Excellent	Excellent
W/MoMn	NG	NG	Excellent	NG	NG	NG	NG	Good