



*The Institute for
Interconnecting
and Packaging
Electronic Circuits*

IPC-DW-424

General Specification for Encapsulated Discrete Wire Interconnection Board

IPC-DW-424

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A standard developed by the Institute for Interconnecting
and Packaging Electronic Circuits

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- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feed back system on use and problems for future improvement

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- Increase time-to-market
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Developed by the Discrete Wiring Subcommittee of the Subassembly Interconnections Committee of the Institute for Interconnecting and Packaging Electronic Circuits

Users of this standard are encouraged to participate in the development of future revisions.

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General Specification for Encapsulated Discrete Wire Interconnection Boards

1.0 SCOPE

1.1 Scope This specification establishes the qualification and performance requirements for encapsulated discrete wire interconnection boards having wires which terminate in plated holes.

1.2 Classification The interconnection boards covered by this specification shall be classified by type, class, dielectric material, and metallization process.

1.2.1 Type (See Figure 1)

Type 1—Rigid boards having discrete wires terminating in plated through-holes only.

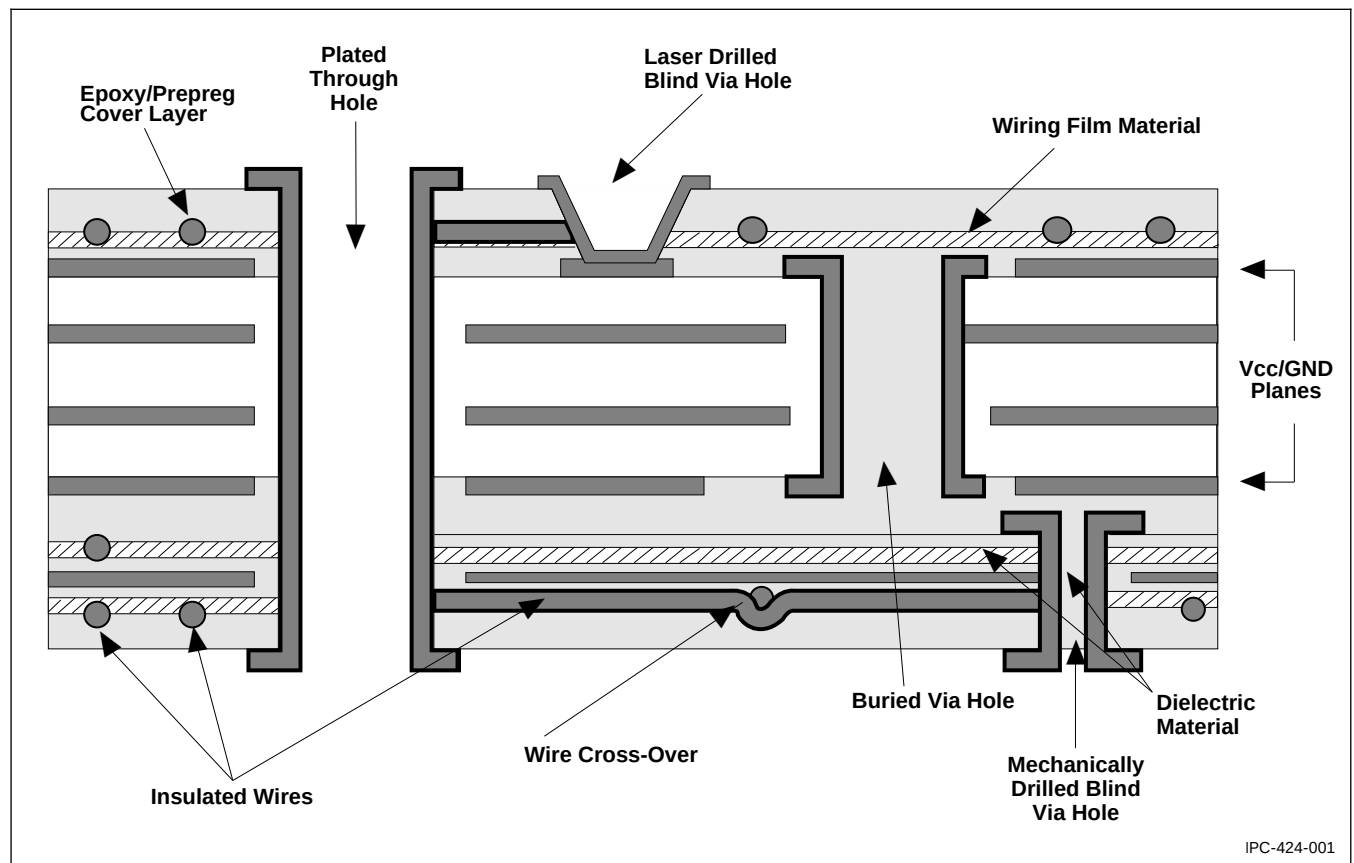
Type 2—Rigid boards having discrete wires terminating in plated through-holes and/or wires traversing blind via holes.

Type 3—Rigid boards having discrete wires terminating in buried via holes as well as plated-through and/or blind via holes.

1.2.2 Class It is recognized that products supplied under this specification will be subject to classification according to intended end use. Therefore, several classes have been established and will be referred to throughout this document in order to reflect progressive increases in sophistication, functional performance requirements, and testing inspection frequency. Since there may be overlap between these class definitions, it is the responsibility of the end user to determine and to specify the class into which this product belongs. Qualification to a particular class automatically qualifies to all lower classes. The classes are as follows:

Class 1—General Electronic Products

Product in this classification includes consumer products, some computer peripherals, as well as general military hardware suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed board.



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Figure 1 Typical Board Construction

Class 2—Dedicated Service Electronic Products

Product in this classification includes communications equipment, sophisticated business machines, instruments and military equipment where high performance and extended life is required, and for which uninterrupted service is desired, but not critical. Certain cosmetic imperfections are allowed.

Class 3—High Reliability Electronic Products

Product in this classification includes the equipment for commercial and military products where continued performance on demand is critical, equipment downtime cannot be tolerated, and equipment must function, when required (e.g., life support, airborne, or space applications).

1.2.3 Dielectric Materials A two number designator as referenced in IPC-L-108 or IPC-L-115 shall be used to identify dielectric materials.

1.2.4 Metallization Process An alphabetic designator shall be used following the class number in order to identify the type of copper plating used to metallize the holes of the board.

Process E — Denotes electroless followed by electrolytic copper plating.

Process A — Denotes full build electroless alone.

1.2.5 Specification Order For ordering purposes, type, class, dielectric material, and metallization process shall be as shown below:

First Digit – Type 1, 2 or 3 (as defined in Paragraph 1.2.1).

Second Digit – Class 1, 2, or 3 (as defined in Paragraph 1.2.2).

Third and Fourth Digits – Materials (as defined in Paragraph 1.2.3)

Fifth Digit – Process A or E (as defined in Paragraph 1.2.4).

As an example, 12XXE would designate a rigid board having discrete wires terminating in plated through-holes only, used in dedicated service electronics products, utilizing type XX dielectric material and electroless followed by electrolytic copper plating.

1.3 Statistical Process Control (SPC) When SPC is required, the guidelines of IPC-PC-90, “General Requirements for Implementation of Statistical Process Control,” or as agreed upon, should be followed.

1.4 Order of Precedence In the event of a conflict between documents, the following order of precedence shall apply:

1. Purchase order and/or contract
2. Master drawing
3. Specification sheet
4. This specification
5. Other applicable specifications

2.0 APPLICABLE DOCUMENTS

The following documents of the issue currently in effect, form a part of this specification to the extent specified herein. Subsequent issues of, or amendments to, these documents may become a part of this specification.

2.1 Institute for Interconnecting and Packaging Electronic Circuits¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-PC-90 General Requirements for Implementation of Statistical Process Control

IPC-L-108 Specification for Thin Metal Clad Base Materials for Multilayer Printed Boards

IPC-L-109 Specification for Resin Preimpregnated Fabric (Pre-preg) for Multilayer Printed Boards

IPC-L-115 Specification for Rigid Metal Clad Base Materials for Printed Boards

IPC-MF-150 Metal Foil for Printed Wiring Applications

IPC-CF-152 Composite Metallic Material Specification for Printed Wiring Boards

MIL-D-275 Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies

IPC-AM-372 Electroless Copper Film for Additive Printed Boards

IPC-DW-425 Design and End Product Requirements for Discrete Wiring Boards

IPC-A-600 Acceptability of Printed Boards

IPC-TM-650² Test Methods Manual

2.1.1 Microsectioning

2.3.38 Surface Organic Contaminant Detection Test (In-House Method)

2.3.39 Surface Organic Contaminant Identification Test (Infrared Analytical Method)

1. Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL 60062-6135

2. For convenience, all IPC-TM-650 test methods referenced herein are reprinted at the end of this standard.

2.4.10 Plating Adhesion

2.4.22 Bow and Twist

2.4.28.1 Adhesion, Solder Mask

2.4.36 Rework Simulation, Plated-Through Holes

2.5.7 Dielectric Withstanding Voltage, Printed Wiring Material

2.6.3 Moisture and Insulation Resistance, Rigid, Rigid/Flex and Flex Printed Wiring Boards

IPC-QL-653 Qualification of Facilities That Inspect/Test Printed Boards, Components and Materials

IPC-R-700 Suggested Guidelines for Modification, Rework, and Repair of Printed Boards and Assemblies

IPC-CC-830 Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

2.2 Joint Industry Standards

J-STD-003 Solderability Tests for Printed Boards

J-STD-004 Requirements for Soldering Fluxes

J-STD-006 General Requirements and Test Methods for Electronic Grade Soft Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

2.3 Military³

MIL-STD-810 Environmental Test Methods

MIL-G-45204 Gold Plating, Electrode Deposited

MIL-I-45208 Inspection System Requirements

MIL-STD-45662 Calibration System Requirements

MIL-P-81728 Plating, Tin Lead, Electrodeposited

MIL-W-82598 Wire, Copper-Cadmium Alloy

2.4 Federal³

QQ-N-290 Nickel Plating (Electrodeposited)

QQ-W-343 Wire, Electrical, Copper (Uninsulated)

J-W-1177/15 Wire, Magnet, Electrical, Class 220, Type M, Aromatic Polyimide Coated, Round

2.5 Other Publications

2.5.1 The American Society for Testing Materials (ASTM)⁴

ASTM B-487 Measurement of Metal and Oxide Coating Thicknesses by Microscopical Examination of a Cross Section

ASTM D-2307 Relative Thermal Endurance of Film Insulated Round Magnet Wire

ASTM D-3951 Commercial Packaging

ASTM E-8 Tension Testing of Metallic Materials

ASTM E-53 Chemical Analysis of Copper (Electrolytic Determination of Copper)

ASTM E-345 Tension Testing of Metallic Foil

2.5.2 Underwriters Laboratories, Inc. (UL)⁵

UL 94 Tests For Flammability Of Plastic Materials

UL 796 Standard For Printed Wiring Boards

3.0 REQUIREMENTS

3.1 General Encapsulated discrete wire interconnection boards furnished under this specification shall meet all the requirements of this specification, the requirements of the master drawing, and the design requirements of IPC-D-235 for any etched layers of the boards. The detailed requirements contained in this section shall apply to all coupons, sample boards, and deliverable product. Anomalies or defects noted on coupons or sample boards (or both) defined in inspection (Tables 1 through 11) shall be recorded and the proper corrective action shall be initiated.

3.2 Qualification Boards furnished under this specification shall be products which have been produced by a manufacturer with valid qualification certification (see 4.5).

3.3 Terms and Definitions The definitions of all terms used herein shall be as specified in the IPC-T-50.

Bead—The external (surface) annular ring of copper plating around a plated through-hole, on a fully additive circuit board, which functions to conduct heat and promote solder wicking during soldering of components.

Conformance Test Coupon Set—A compliment of test coupons which are comprised of various coupon types, each of which is designed for specific tests, but which were all made in the same manufacturing lot.

3. To obtain documents, write Standardization Documents Order Desk, Building 40, 700 Robbins Avenue, Philadelphia, PA 19111-5094

4. Application for copies should be addressed to American Society for Testing Materials, 1916 Race Street, Philadelphia, PA 19103

5. Application for copies should be addressed to Underwriters Laboratories, Inc., 333 Pfingsten Road, Northbrook, IL 60062

Cover Layer—A polymeric material which is applied to a circuit board, over surface wired levels. This layer serves to protect underlying wires from mechanical damage and/or dislocation.

Cross-over—A point where two or more discrete insulated wires intersect and cross each other.

Bounce Pad—An isolated area in a copper plane, beneath the discrete wiring, which acts solely as a stop for the laser drill operation.

Wire Stub—The short end of an insulated wire which extends beyond the wall of a plated hole.

Wire Insulation Removal—The chemical removal of wire insulation at the wire entry into the plated hole, and the lateral plating of copper within this region which is in contact with the wire core metal.

Wire Overcoat—A secondary polymeric coating of the wire, which has been applied over the insulation. This overcoat serves strictly to aid in the bonding of wires during the wiring operation.

Wire Poke-Through—A condition of the insulated wire breaking through the epoxy cover layer, thus exposing the insulated wire, especially at a wire crossover.

Wiring Layer—A polymeric material which is applied to the circuit board and serves as the material into which the insulated wires are imbedded in forming the wired pattern.

Thermal Plane—(same as Heatsink Plane, see IPC-T-50)

3.4 Materials

3.4.1 Wire The wire shall be an insulated wire which meets or exceeds all of the requirements of J-W-1177/15, and shall be of a size as specified on the master drawing. The core conductor shall be composed of either copper conforming to the material requirements of QQ-W-343, copper-cadmium alloy conforming to the material requirements of MIL-W-82598, or as specified on the master drawing. The insulation shall be composed of cured, aromatic polyimide which exhibits a thermal rating of Class 220 when evaluated in accordance with ASTM D-2307.

3.4.2 Metal-Clad Laminates The metal-clad laminate for individual layers of boards shall be in accordance with IPC-L-108 or IPC-L-115.

3.4.3 Bonding Material The bonding interlayer material for boards shall be as specified on the master drawing and shall be in accordance with IPC-L-109. Other bonding materials may be utilized providing they conform to the performance requirements of IPC-L-109. Sufficient bonding material shall be used to provide for a minimum dielectric layer thickness specified in 3.8.10 between adjacent etched conductor layers.

3.4.4 Metallic Foils

3.4.4.1 Copper Foil Copper foil used shall be in accordance with IPC-MF-150. The foil designation shall be specified on the master drawing.

3.4.4.2 Composite Metallic Materials When specified on the master drawing, composite metallic material shall be in accordance with IPC-CF-152. The type designation shall be specified on the master drawing.

3.4.4.3 Resistive Foil When required, resistive foil shall be of a type as specified on the master drawing.

3.4.5 Copper Plating

3.4.5.1 Electrolytic Copper Electrolytic copper plating shall be such that, when tested as specified in 4.3.1, the deposit meets the following requirements:

Purity—99.8% Cu minimum (for copper sulfate type plating solutions), or

99.5% Cu minimum (for pyrophosphate type plating solutions).

Elongation—6% minimum.

Tensile Strength—248184 KPa [36000 lb/in²] minimum.

3.4.5.2 Full Build Electroless Copper When tested in accordance with 4.3.1, the full build electroless copper deposit shall meet the following requirements:

Purity—99.8% Cu minimum.

Elongation—6.0% minimum.

Tensile Strength—248184 KPa [36000 lb/in²] minimum.

3.4.6 Solder Coating The solder used for solder coating shall be in accordance with composition Sn60, Sn62, or Sn63 of J-STD-006.

3.4.7 Fusing Fluids and Fluxes Fusing fluids and fluxes used on the board shall produce no detrimental effects to the board. Subsequent to their use and removal, the board shall meet all ionic cleanliness requirements of 3.10.4.

3.4.7.1 Fusing Fluid A fusing fluid, generally a water soluble flux, may be used with appropriate equipment for the fusing or reflowing of tin-lead plating on the board. The flux shall be capable of cleaning the tin-lead plating and bare copper to allow for a smooth adherent coating and shall act as a heat transfer and distribution media to prevent damage to the bare laminate of the board. The type and composition of the fusing fluid shall be optional to the board manufacturer.

3.4.7.2 Solder Coating Flux A flux, generally water soluble, may be used with appropriate equipment for the

coating the bare copper conductors and features on the board. The flux shall be capable of cleaning the bare copper to allow for a smooth, adherent solder coating. The type and composition of the flux shall be optional to the board manufacturer.

3.4.8 Tin-Lead Plating Tin-lead plating shall be in accordance with MIL-P-81728.

3.4.9 Gold Plating Gold plating shall be in accordance with the requirements of MIL-G-45204.

3.4.10 Nickel Plating Nickel plating shall be in accordance with the requirements of QQ-N-290.

3.4.11 Solder Resist When use of permanent solder resist coating is specified on the master drawing, it shall be a polymer coating conforming to IPC-SM-840, and shall meet the requirements of 3.6.8 and 3.7.1.

3.4.12 Marking Ink Marking ink used shall be a permanent, non-nutrient, and nonconductive ink.

3.4.13 Thermal Planes Thermal planes, when required, shall be as specified on the master drawing.

3.4.13.1 Hole-Fill Insulation Material for Thermal Planes The insulation material used for hole-fill dielectric shall be as specified on the master drawing.

3.4.13.2 Adhesive The adhesive used for bonding thermal planes shall be of a type as specified in 3.4.3, and shall provide for a minimum dielectric layer thickness as specified on the master drawing.

3.5 Visual Requirements The boards shall be inspected to verify that the design, construction, physical dimensions, marking, and workmanship are in accordance with the applicable requirements (see 3.0 through 3.13, inclusive), and the master drawing. Features of the board shall be inspected using an optical apparatus or aid which provides a minimum magnification of 2.5X. Referee inspection of board features shall be accomplished at a magnification of 10X.

Microsection inspections (such as plated hole, plating thickness, and foil thickness) shall be accomplished by using methods in accordance with either IPC-TM-650, method 2.1.1 or ASTM-B-487. Automatic microsectioning techniques may be used in lieu of IPC-TM-650, test method 2.1.1 or ASTM B-487.

Plated-through holes shall be microsectioned in the vertical plane at the approximate center of the wire, and inspected for wire and plating integrity at a magnification of 100X. Referee inspections shall be accomplished at a magnifica-

tion of 200X. Each side of the hole shall be viewed independently. A minimum of one microsection containing at least three holes of each type (plated-through, buried, or blind via) shall be made for each sample tested. Inspection (such as laminate thickness, foil thickness, plating thickness, solder coating, lay-up orientation, laminating resin smear and plating voids) shall be accomplished at magnifications specified above. If resin smear is suspected on a vertical microsection, a referee microsection shall be prepared and evaluated in the annular (horizontal) plane.

Measurements shall be reported as the average of three determinations per each side of the hole. Isolated thick or thin sections shall not be used for averaging; however isolated areas of reduced copper thickness shall be measured and shall meet the requirements of 3.8.2 and 3.8.3.

3.5.1 Edges of Boards When inspected in accordance with 3.5, burrs, nicks, and haloing along the edges of boards, internal slots or non-plated holes, shall be acceptable provided the penetration does not reduce the edge spacing more than 50% of the edge spacing specified on the master drawing. If no requirement is specified on the master drawing, the penetration shall not exceed 2.5 mm [0.100 in].

3.5.2 Surface Imperfections When inspected in accordance with 3.5, surface imperfections (such as weave texture, haloing, scratches, pits, dents, and wire poke-through) shall be acceptable provided the imperfection meets the following:

- A. The laminate fiber is not cut, disturbed or exposed.
- B. The imperfection does not bridge between etched conductors.
- C. The dielectric spacing between the imperfection and an etched conductor is not reduced below the minimum requirements of 3.6.4.
- D. The conductive portion of the wire is not exposed.
- E. Poke-through is not acceptable for boards manufactured under Process E.

3.5.3 Subsurface Imperfections When inspected in accordance with 3.5, subsurface imperfections (such as blistering, haloing, and delamination) shall be acceptable providing the imperfection meets the following:

- A. Imperfection is translucent.
- B. Does not bridge more than 25% of the distance between etched conductors or plated-through holes. No more than 1% of the board area on each side shall be affected.
- C. Does not reduce etched conductor spacing below the minimum requirements of 3.6.4.
- D. Does not propagate as a result of testing (such as bond strength, rework simulation, thermal stress, or thermal shock).

There is no requirement for subsurface imperfections which are located between discrete, insulated wires (see Figure 2).

3.5.3.1 Foreign Inclusions Foreign inclusions shall be permitted when: they are identified as translucent, or are located at least 0.25 mm [0.010 in] from the nearest etched conductor if located between etched conductors and there is more than 50% space remaining, the longest dimension is no greater than 0.813 mm [0.032 in] in non-circuitry areas and there are no more than two inclusions per side of the board.

3.5.3.2 Subsurface Spots Subsurface spots shall be permitted when they are: known to be nonconductive; known to be weave texture other than delamination, disbonding, or measling; isolated white spots which are at least 0.254 mm [0.010 in] from the nearest etched conductor; white spots which do not propagate as a result of any soldering operation; isolated black spots which are at least 0.254 mm [0.010 in] from the nearest etched conductor. (Gelation particles are acceptable regardless of location.)

3.5.3.3 Measling/Crazing Measling and crazing shall be evaluated in accordance with IPC-A-600.

3.5.4 Marking Unless otherwise specified, each individual board, each qualification board, and each set of quality conformance test circuit strips (as opposed to each individual coupon) shall be marked in accordance with the master drawing. The marking shall be produced by the same process used in producing the conductor pattern; or by the use of a nonconductive, permanent fungistatic ink or paint (see 3.4.12) applied to the board or to a label which is applied to the board. The label shall be a polyamide film with acrylic, pressure sensitive adhesive that shall withstand solder fluxes, cleaning solvents, molten solder, and conformal coating encountered in the manufacture of interconnection boards. Electrical pencil marking on a metallic area provided for marking purposes may also be used. Conductive marking shall not reduce the spacing requirements specified in 3.6.4. All marking shall be compatible with materials and parts, legible after all tests, and in no case affect board performance.

3.5.4.1 Traceability For traceability, each quality conformance test circuit strip and microsection shall be identifiable with those corresponding production boards produced on the same panel that also produced the quality conformance test circuitry. All separated individual coupons shall have their traceability maintained back to the quality conformance test circuit strip or qualification specimens from which the coupons were separated.

3.5.5 Workmanship When inspected in accordance with 3.5, boards shall be processed in such a manner as to be

uniform in quality and show no evidence of dirt, foreign matter, oil, fingerprints, flux residues, extraneous copper, and other contaminants that affect life or serviceability. Boards shall be free of defects in excess of those allowed in this specification. There shall be no evidence of any lifting or separation of platings from the surface of the conductor pattern, or of the conductor from the base laminate in excess of that allowed. There shall be no whiskers of solder or plating on the surface of the conductor pattern.

3.5.6 Solderability The applicable test coupon shall be used for this test.

3.5.6.1 Surface Solderability When inspected as specified below, 95% of the specimen shall exhibit proper wetting of the surface. There shall be no separation or other forms of degradation of the pattern.

Specimens shall be inspected in accordance with J-STD-003, except the temperature shall be 260°C [500°F] for 5 ±1 seconds.

3.5.6.2 Hole Solderability When inspected as specified below, the specimen shall exhibit proper wetting of the wall of the plated hole and the associated land.

Specimens shall be inspected in accordance with J-STD-003, except the temperature shall be 260°C [500°F] for 5± seconds.

3.6 Dimensional Requirements

3.6.1 Dimensions The finished boards shall meet the dimensional requirements specified herein and on the master drawing.

3.6.2 Hole Pattern Accuracy The accuracy of the hole pattern on the board shall be as specified on the master drawing.

3.6.3 Bow and Twist Printed boards shall be examined in accordance with the following test method. The entire portion of the specimen or production board shall have a maximum bow and twist of 1.5%, unless otherwise specified on the master drawing.

The printed wiring board shall be inspected for bow and twist in accordance with IPC-TM-650, test method 2.4.22.

3.6.4 Etched Conductor Width and Spacing The etched conductor width and spacing shall be as specified on the master drawing.

3.6.5 Etched Conductor Pattern Unless otherwise specified on the master drawing, when the etched conductor pattern is inspected as specified in 3.5, the conductor pattern shall have no tears or cracks. Any

edge roughness, nicks, pinholes, and scratches exposing the base material shall not reduce the conductor width more than 20% of the minimum specified on the master drawing for each conductor width. There shall be no occurrence greater than 12.7 mm [0.50 in] in a conductor length.

3.6.6 Etched Layer-to-Layer Registration (See Figure 2) Unless otherwise specified on the master drawing, etched layer-to-layer pattern misregistration shall not exceed 0.356 mm [0.014 in], when measured as specified below. In addition, the requirements of 3.6.7 shall be met.

Etched layer-to-layer registration shall be determined by the microsectioning of two coupons from diagonally opposing panel corners, which shall then be evaluated in accordance with 3.5. Registration shall be measured at a magnification of 100X after microsectioning both coupons in the vertical plane, but one coupon is to be sectioned in the panel's length direction while the other is to be sectioned in the width direction. These microsections shall be evaluated by computing the difference in centerline location of the two lands found to be most eccentric to one another within each section. The applicable test coupons shall be used in this test.

3.6.7 Annular Ring (External) (See Figure 3) When evaluated in accordance with the procedure below, the minimum external annular ring shall meet the requirements of Table 1.

Table 1

External Annular Rings	Class 1, 2	Class 3
External Supported	0.05 mm [0.002 in]	0.10 mm [0.004 in]
External Unsupported	0.15 mm [0.006 in]	0.25 mm [0.010 in]

When examined in accordance with 3.5, the measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the board.

3.6.8 Solder Resist When inspected as below, the solder resist shall be in accordance with the master drawing. In the event that nothing is specified, the solder resist shall meet the requirements of IPC-SM-840.

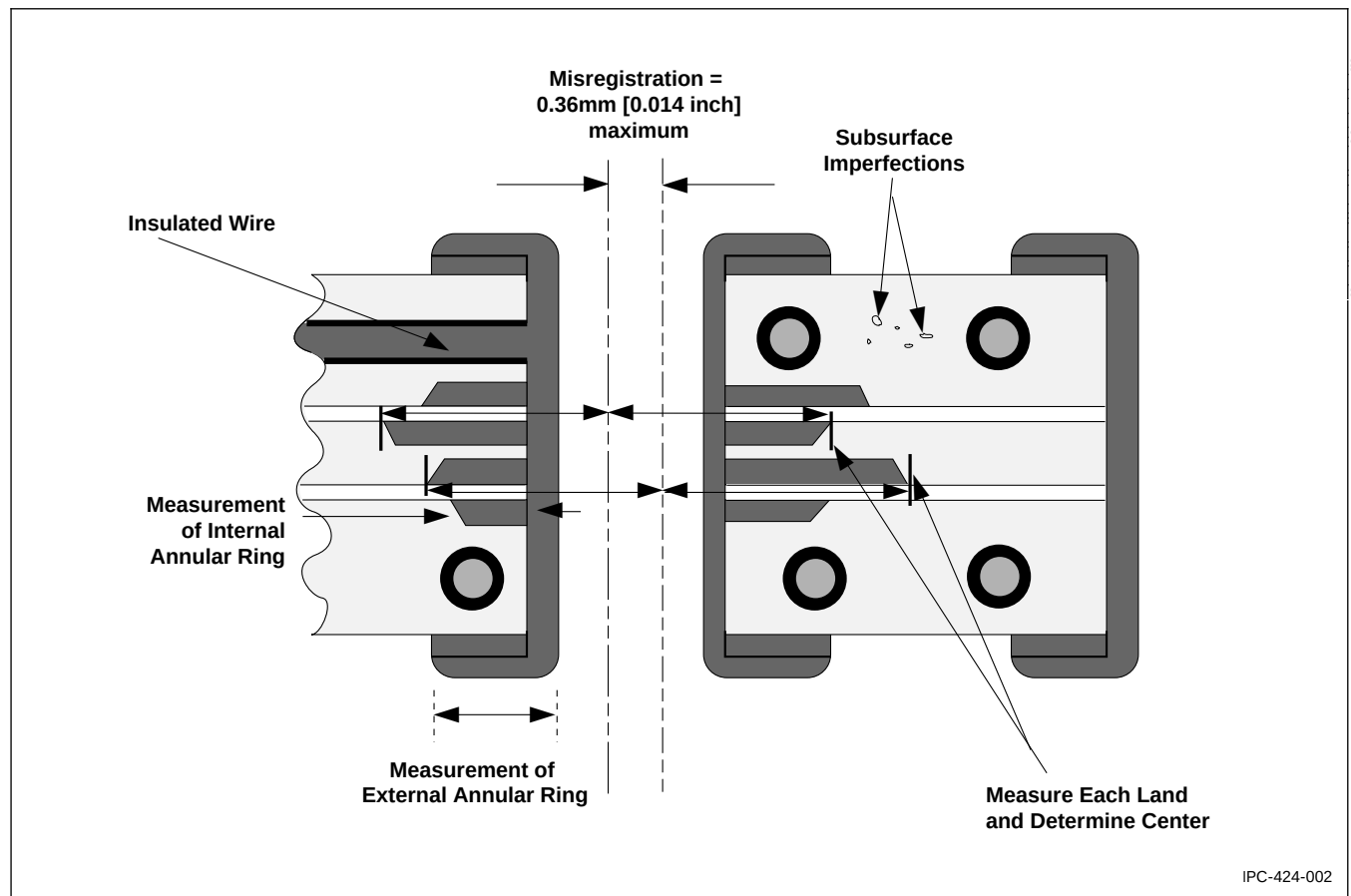


Figure 2 Etched layer-to-layer registration and internal annular ring measurement

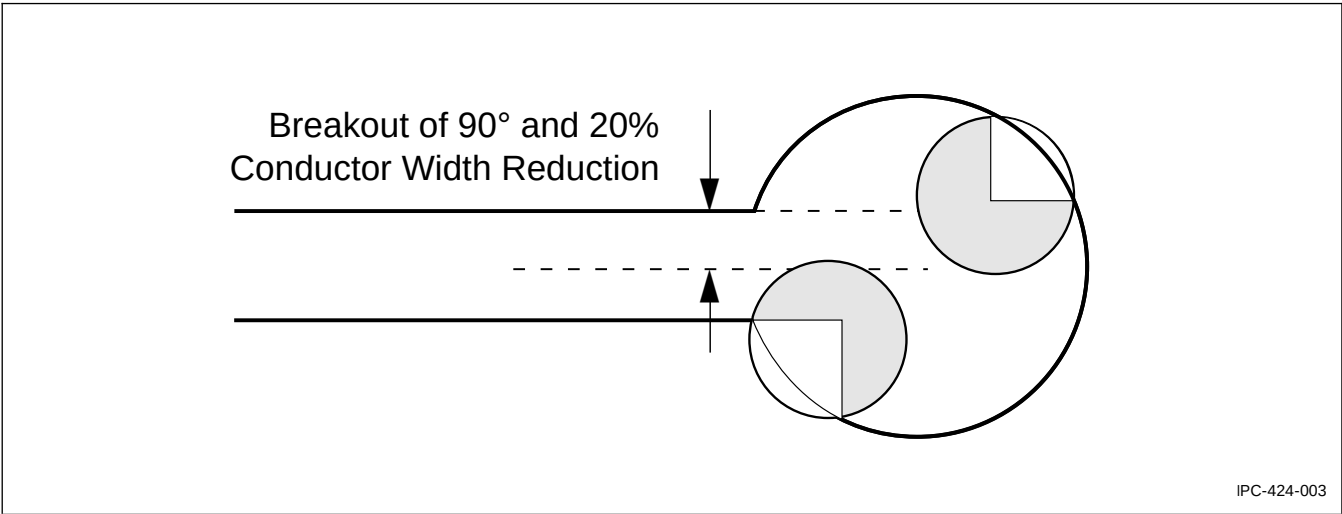


Figure 3 External Annular Ring Measurement

Solder resist thickness shall be inspected by any micrometer or indicator accurate to 0.0076 mm [0.0003 in] or microsection in accordance with 3.5. If microsectioning is employed, the applicable test coupon shall be used.

3.6.8.1 Solder Resist Registration Unless otherwise specified on the master drawing, solder resist registration shall meet the requirements of IPC-SM-840.

3.6.9 Plating and Coating Thickness Unless otherwise specified on the master drawing, the plating or coating thicknesses shall be in accordance with Table 2 and inspected in accordance with the procedure outlined below. After tin-lead is fused, or solder is reflowed, or boards are subjected to hot air solder leveling, no measure of solder thickness is required, but solderability in accordance with J-STD-003 shall be performed and visual inspection of complete copper coverage by solder shall be performed. Complete copper coverage by solder does not apply to the vertical conductor edges.

Tin-lead plating thickness, prior to fusing, reflow, or hot air solder leveling, shall be measured by either microsection (see 3.5) or nondestructive means. If microsectioning is employed, the applicable test coupon shall be used.

3.6.10 Wire Stub Clearance Wire stub clearance shall

be a minimum of 0.0254 mm [0.001 in] between the stub end and the outer insulation surface of an adjacent wire. The clearance between the wire stub and the adjacent plated hole shall meet the requirements of 3.6.4. The clearance space shall be filled with dielectric material.

3.6.11 Bead Height For Process A boards, the height of the plated bead shall be a minimum of 0.013 mm [0.0005 in] when inspected in accordance with the procedures outlined below (see Figure 7b).

For Process A boards, the height of the plating bead shall be measured via microsection in accordance with 3.5.

3.7 Physical Requirements

3.7.1 Solder Mask Cure and Adhesion When inspected in accordance with the following procedure, the cured solder mask coating shall not exhibit tackiness, blistering, or delamination, and the maximum percentage of cured solder resist lifted from the surface of the base material, conductors, and lands of the coated board shall be in accordance with Table 3.

The permanency and adhesion of cured solder resist to printed wiring shall be determined in accordance with IPC-SM-840 and method 2.4.28.1 of IPC-TM-650. Testing shall

Table 2 Plating and Coating Thickness*

Property	Class 1	Class 2	Class 3
Copper Plating Thickness	0.020 mm [0.0008 in] avg. min. (no value less than 15 mm [0.0006 in])	0.025 mm [0.001 in] avg. min. (no value less than 0.020 mm [0.0008 in])	0.025 mm [0.001 in] avg. min. (no value less than 0.020 mm [0.0008 in])
Solder Thickness (tin/lead fused and solder coatings)	Thickness is not specified. Solder coating and fused tin/lead shall meet the solderability requirements of J-STD-003.		
Gold Plating Thickness	0.00075 mm [0.00003 in] min.	0.0013 mm [0.00005 in] min. 0.0025 mm [0.0001 in] max.*	0.0013 mm [0.00005 in] min. 0.0025 mm [0.0001 in] max.
Nickel Plating Thickness	0.003 mm [0.0001 in] min.	0.005 mm [0.0002 in] min.	0.005 mm [0.0002 in] min.

*a coupon prior to reflow may be required (see 4.6 and Table 7)