



*The Institute for
Interconnecting
and Packaging
Electronic Circuits*

IPC-HM-860

Specification for Multilayer Hybrid Circuits

ANSI/IPC-HM-860

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A standard developed by the Institute for Interconnecting
and Packaging Electronic Circuits

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Users of this standard are encouraged to participate in the
development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Hybrid Circuits Committee are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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		Yau, G., Sperry Computer Systems
		Zimmerman, E., Boeing

Specification for Multilayer Hybrid Circuits

1.0 SCOPE

1.1 Scope This specification covers the qualification and performance requirements of multilayer circuits used in hybrid packaging. These circuits consist of three or more layers of conductor patterns separated from each other by insulating materials and interconnected by a continuous metallic interlayer connection. The substrate structure may include passive elements.

1.2 Purpose The purpose of this specification is to provide qualification and acceptance requirements for commercial and government procurement of multilayer circuits used in hybrid packaging.

1.3 Classifications This specification recognizes that a multilayer hybrid circuit assembly will be subject to classifications by intended end item use. Toward this end, three general classes of assemblies have been established. It should also be recognized that there may be an overlap of equipment between classes. The user has the responsibility to determine the class into which the product belongs. The three classes are:

Class 1—Consumer Products

(Includes TV sets, toys, entertainment electronics, personal computers, and non-critical consumer or industrial control devices.) Circuits in this class are suitable for applications where cosmetic defects are not important and the only requirement is function of the completed circuit. These circuits represent a low cost alternative due to the lack of required inspection and testing.

Class 2—General Industry

(Includes computers, communication equipment, sophisticated business machines, instruments and certain non-critical military application.) Circuits in this class are suitable for use where circuit design, process yield, and specification conformance requirements allow localized areas to be defective. These circuits have minimal inspection, testing, and application requirements.

Class 3—High Reliability

(Includes those equipments where continued performance is critical, equipment downtime cannot be tolerated or the equipment is a life support item.) Circuits in this class are suitable for applications where high levels of assurance are required. Major difference is improved surface condition and a higher level of inspection, testing, and certification.

Requirements in this specification have been separated so that the performance of the multilayer products may be tested to any one of the three classes. The use of one class for a specific attribute does not mean that all other attributes must meet that same class. Selection should be based on minimum need. However, cross-over between classes requires complete definition of test requirements in the procurement document.

1.3.1 Circuit Type This specification includes the following types:

TYPE I Co-Fired Ceramic

- a) Refractory Metal
- b) Non-Refractory Metal

TYPE II Inorganic

- a) Thick Film
- b) Thin Film

1.4 Dimensions and Tolerances All dimensions and tolerances specified herein are applicable only to the end product. Dimensions are expressed in millimeters. Inches, shown in brackets [], are not direct conversions in order to provide usable numbers. Users are cautioned to employ a single system and not intermix metric and inch-based equivalents. Reference information is shown in parentheses ().

2.0 APPLICABLE DOCUMENTS

The following documents, the issues in effect on the date of issuance of this specification, form a part of this specification to the extent specified herein. Subsequent issues of or amendments to these documents shall become part of this specification unless otherwise stated.

2.1 IPC¹

IPC-T-50 Terms and Definitions

IPC-D-325 Documentation Requirements for Printed Boards

IPC-TM-650 Test Method Manual²

2.1.1.1 Microsectioning, Ceramic Substrates

2.3.38 Inspection Test for Organic Contaminants on Printed Wiring Boards and Assembly Surfaces

1. Institute for Interconnecting and Packaging Electronic Circuits, 2215 Sanders Rd., Northbrook Illinois 60062-6135.

2. For convenience, all IPC-TM-650 Test Methods referenced herein are re-printed at the end of this standard.



- 2.3.39 Identification of Residual Organic Non-Ionic Contaminant(s) on Printed Wiring Board and Assembly Surfaces
- 2.4.1 Adhesion Plating
 - 2.4.1.2 Adhesion of Conductors on Hybrid Substrates
 - 2.4.1.3 Adhesion, Resistors (Hybrid Circuits)
 - 2.4.1.4 Adhesion, Overglaze (Hybrid Circuits)
- 2.5.5.1 Dielectric Constant and Dissipation Factors of Printed Wiring Materials
- 2.5.7 Dielectric Withstand Voltage, Printed Wiring Material
- 2.5.10 Insulation Resistance, Multilayer Printed Wiring (Between Layers)
- 2.5.31 Current Leakage (Through Overglaze Films)
- 2.5.32 Resistance Test, Plated Through Holes
- 2.6.3 Moisture and Insulation Resistance, Printed Wiring
- 2.6.4 Outgassing, Multilayer Printed Wiring Boards
- 2.6.5 Physical (Mechanical) Shock, Multilayer Printed Wiring
- 2.6.6 Temperature Cycling, Printed Wiring Boards
- 2.6.8 Thermal Stress, Plated-Through Holes
- 2.6.9 Vibration, Rigid Printed Wiring Boards
- 2.6.19 Environmental and Insulation Resistance Test of Hybrid Multilayer Substrates

IPC-SM-840 Qualification and Performance of Permanent Polymer Coatings (Solder Mask)

IPC-HM-855 Microelectronics Design Guide

IPC-D-859 Design Standard for Multilayer Hybrid Circuits

2.2 Military³

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-F-14256 Flux, Soldering, Liquid (Rosin Base)

MIL-I-45208 Inspection System Requirements

2.3 Federal³

FED-SPEC-AA-113 Tape, Pressure Sensitive

FED-STD-406 Federal Test Method Standard

3.0 REQUIREMENTS

3.1 General Hybrid circuits furnished under the specification shall meet or exceed all the requirements of the specific class of this specification for which the order was

made. Circuits which must meet other special requirements beyond those specified in Section 3 will be as specified by the procurement document.

Hybrid circuits furnished under this specification shall be as specified by drawing. They shall be fabricated in lots that include sufficient spares to facilitate the testing requirement of the class to which the circuit was produced. When test specimens are required per this specification, they shall be processed using the same materials, equipment and processes used to fabricate the circuits.

Circuits furnished under this specification shall be processed in such a manner as to be uniform in quality and be free from defects in excess of those allowed in this specification.

All reworked circuits shall conform with all requirements of this specification.

3.1.1 Master Drawing The master drawing shall be prepared in accordance with IPC-D-325 and shall establish the size and shape of the multilayer hybrid circuit, the size and location of all holes and/or vias therein, and the shape or arrangement of both conductive and nonconductive patterns or elements. Any and all pattern features not controlled by the hole or via sizes and locations shall be dimensioned either specifically or by notes.

If this specification is referenced on the master drawing, any permanent exceptions or deviations required shall be documented thereon.

3.1.2 Production Master The multilayer hybrid circuit manufacturer shall be responsible for the accuracy of the production master and for verification of compatibility with the master drawing and patterns and the specific manufacturing facilities and processes used. The manufacturer shall insure that the end product hybrid circuit meets the requirements of this specification. When specified on the procurement document or master drawing, the position of the appropriate test patterns on the production master may not be changed.

3.1.3 Modification/Repair Repair or modification will require approval prior to such action; modification/repairs on Class 3 hybrid circuits require approved documented procedures. Touch up or repair of surface imperfections in the base material, removal of residual plated material will be permitted when such action does not affect the functional integrity of the circuit.

3.2 Terms and Definitions The definition of terms applicable to this specification shall be in accordance with IPC-T-50 and the following. Terms with an asterisk (*) are

3. To obtain documents, write Naval Publications & Forms Center, 5801 Tabor Road, Philadelphia, PA 19120.

direct excerpts from IPC-T-50, and are repeated here for convenience.

3.2.1 Multilayer Circuit The general term for completely processed circuit configurations consisting of alternate layers of conductive patterns and insulating materials together, with conductive patterns interconnected as required. Circuits may include passive elements.

3.2.3 Modification Changes to the original design functions by such means as adding circuits or isolating circuits either externally or internally.

3.2.4 Production Circuit Any multilayered circuit manufactured in accordance with master drawings, applicable specifications and procurement requirements.

3.2.5 Qualification Testing Qualification testing is performed to demonstrate the vendor's ability to meet all of the requirements of the specification invoked by the user.

3.2.6 Quality Conformance Tests Tests intended to demonstrate the ability of a producer to consistently comply with paragraph 4.6 of this specification.

3.2.7 Test Specimens A special hybrid multilayer circuit manufactured with the same material, equipment and processes as the production circuits, used to determine the acceptability of the circuit(s).

3.2.8 Repair The restoration of the functional capability of a defective circuit without necessarily restoring appearance, while maintaining interchangeability and uniformity.

3.2.9 Rework The repeating of one or more manufacturing operations for the purpose of improving the yield of acceptable circuits.

3.3 Conflict When a conflict exists between this specification, the engineering drawing, and the purchase order or contract, the following order of precedence shall apply:

1. Purchase order and/or contract
2. The master drawing (see 3.1.1)
3. This specification
4. Applicable documents (see 2.0)

3.4 Vendor Qualification and Conformance When required, vendors of multilayer circuits to this specification shall be qualified per paragraph 4.5 as specified by the user, and for the class of product represented by the qualification sample. Qualification to a class of this specification is considered evidence of qualification to any lower class(es), i.e., qualification to Class 3 is extended to cover qualification to Class 1 and Class 2. Certification to MIL-STD-1772

may be used as evidence of qualification to this specification for all classes.

The multilayer circuits furnished under this specification shall, as a minimum, meet the requirements of paragraph 4.6.

3.5 Materials All materials used in construction of the multilayer circuits shall comply with applicable specifications and the master drawing. The user has the responsibility to specify on the master drawing, materials capable of meeting the requirements of this specification and end item use. When possible, material call-out information shall be reviewed with the vendor so as to obtain concurrence that the part will meet the requirements of this specification and, if necessary, to update the master drawing accordingly.

If no materials are specified, or the vendor alters those specified materials, then the vendor has the responsibility to meet the requirements of this specification. Agreement or approval by the user of vendor selected materials shall not be construed as a guarantee of acceptance of the finished end item.

3.5.1 Substrate Materials Substrate materials shall conform to specifications on flatness, thickness, and dimensional tolerances. Material may be of two types.

3.5.1.1 Alumina Composition and surface finish as specified.

3.5.1.2 Beryllia Composition and surface finish as specified.

3.5.2 Dielectrics Dielectrics shall meet or exceed the minimum electrical and physical requirements of the design document, IPC-D-859.

3.5.2.1 Thick Film Inorganic Dielectrics Thick film inorganic dielectrics shall include those produced by tape or screen printing technology, and may consist of vitreous glass-refractory systems or crystallizable glass systems.

3.5.2.2 Inorganic Dielectrics Inorganic dielectrics may be used where they will meet the environmental and electrical characteristics of the design.

3.5.3 Component Materials Component materials shall meet or exceed the minimum performance design requirements. Included in these materials are:

- Resistive Materials: cermets, metallic oxides and nitrides, organic based materials.
- Capacitive Elements: combinations of previously specified dielectric and conductive materials.
- Metallization: metal phase bonded by reactive metal compounds or glass as specified by the master drawing.

3.5.4 Plating All plating materials and processes shall comply with applicable specifications as shown in Table 1. Plating types may be applied as panel plating of the entire surface, or pattern plating selectively, over base metallization surfaces, as specified in the design document.

Plating type will be specified in the specific design document. Designs requiring pattern plating must include shorting bars or permit other means of providing continuity for electrodeposition of plating material.

Table 1 Plating Specifications

Plating Type	Applicable Specification
Gold, Electrodeposited	MIL-G-45204
Copper, Electrodeposited	MIL-C-14550
Silver, Electrodeposited	QQ-S-365
Nickel, Electrodeposited	QQ-N-290 or MIL-P-27418 (USAF)
Tin-Lead, Electrodeposited	MIL-P-81728

3.5.5 Cover Coats

3.5.5.1 Solder Stop Solder stops may include the use of glass overglaze or permanent polymer solder mask and shall be defined on the engineering drawing. When permanent solder mask coating is specified, it shall conform to IPC-SM-840. The specific class of solder mask referenced in IPC-SM-840 shall match the class definition of the hybrid circuit being produced.

3.5.5.2 Passivation Passivation shall be incorporated as specified in the design document and can include glass overglaze or protective inert chemical coatings.

3.5.6 Solder Solder systems may be applied to the surface metallization as specified in the design document and should be compatible with surface metallization and subsequent processing.

3.5.7 Fluxes Fluxes may be used in the preparation of surfaces to accept solder. Noncorrosive fluxes should be used and all residues removed.

3.6 Design The design and construction of multilayer circuits shall be in accordance with IPC-D-859.

3.7 Visual Requirements Class 1 circuits when examined in accordance with 4.6.1 shall be of uniform quality and any defects shall not impact form, fit or function.

Class 2 and 3 circuits when examined in accordance with 4.8.1 shall conform to the following paragraphs.

3.7.1 Foreign Material (See Figure 1.) Foreign material which is attached shall be permitted on the surface of the dielectric provided it does not interfere with component

mounting, marking or electrical performance. Nonconductive material which appears to be easily removable shall not be cause for rejection unless it is excessive and imbedded in the conformal coating material. Attached conductive foreign material which reduces the separation between any two metallization paths to less than 0.025 mm [0.001 in] or 50% of design width, whichever is greater, shall be cause for rejection. Marking material shall be considered to be nonconductive material.

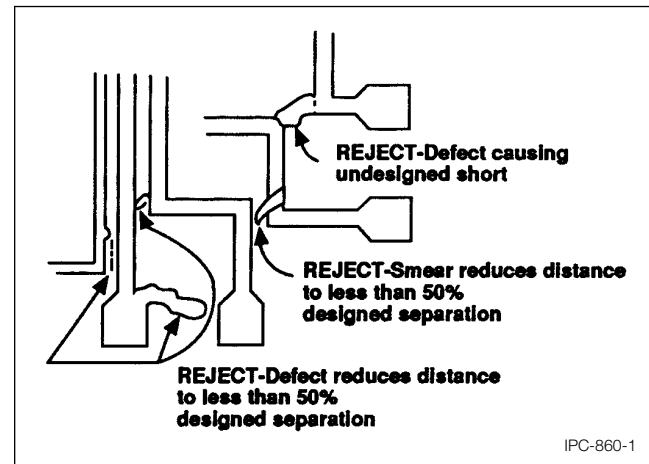


Figure 1 Foreign material.

Note: Verification of attachments of foreign material shall be accomplished by a light touch with an appropriate mechanical device (i.e., needle, probe, pick, etc.).

3.7.1.1 Chemical Residue The circuits shall be free of all chemical residue or liquid droplets resulting from production or handling that bridge any combination of unglazed or passivated operative metal surface.

3.7.2 Substrate Material (See Figure 2.)

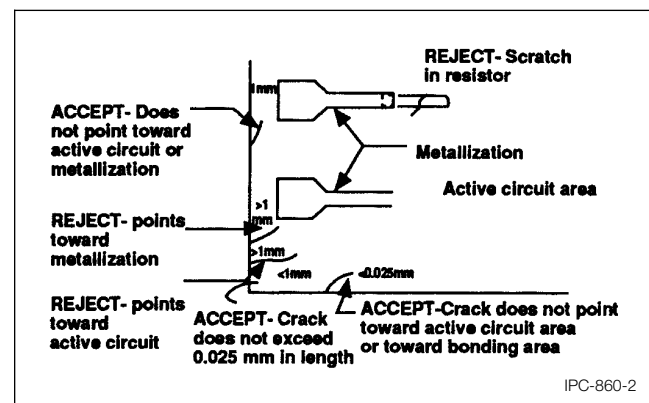


Figure 2 Substrate material.

3.7.2.1 Cracks Any crack that does not originate at an edge shall be cause for rejection. No cracks shall be permitted which appear to intersect active metal.

cracks which exceed 0.125 mm [0.005 in] in length and which point toward active metallization or come within 0.025 mm [0.001 in] thereof shall be permitted. Cracks which intersect the boundary surfaces of the circuit or originate thereon shall be considered to define a potential chip-out and shall be so evaluated. Substrates having a section broken out around any substrate mounting hole greater than 25% of the mounting hole circumference, when designed for substrate to post attachment, shall be rejected.

3.7.2.2 Chip-Outs Chip-outs shall be acceptable provided they do not cause the circuit assembly to deviate from any defined dimensional limits. No chip-outs shall extend into or under the dielectric or metallization of the circuit for Class 3 hybrids. No chip-out in the substrate shall reduce the supporting structure to less than 25% of the original thickness. Chip-outs in Class 1 or 2 hybrids shall not reduce any active metallization to less than the allowable conductor reduction specified in paragraph 3.8.1. No chip-out shall be acceptable which comes within 0.025 mm [0.001 in] of any active metallization that has already been reduced. Chip-outs may involve edge pads provided the affected pad area is not reduced by more than 20% of the design minimum. Edge chips may be a maximum of 2.5 mm [0.100 in] in length provided they do not involve more than one layer and are otherwise acceptable.

3.7.2.3 Pits and Voids Pits and voids in the substrate material shall be evaluated by criteria governing chip-outs (paragraph 3.7.2.2).

3.7.3 Pattern Defects (See Figure 3.)

3.7.3.1 Blistering, Peeling and Corrosion No blistering or peeling shall be permitted for Class 3 hybrids. No blistering or peeling of metallization shall be permitted in excess of 50% of the conductor width or 0.15 mm [0.006 in] for Class 2, whichever is less. There shall be no more than 6 blisters for Class 2 circuits per cm² of metallization. Blistering of dielectric for Class 2 and 3 hybrids shall be permissible provided that the unit is designed to be hermetically sealed and that the blistering does not exceed 20% of the total area of the dielectric. Peeling of edge pad metallization shall not be permitted in any case. Minor discoloration of copper metallization is permissible but any evidence of deep oxidation or corrosion shall be cause for rejection. Some color changes in thick film metallization is normal and is permissible.

3.7.3.2 Pits and Voids No pit or void shall be permitted which reduces the width of the active metallization by more than 50% of the design minimum or below the requirements for conductor reduction shown in paragraph 3.8.1. No pit which exceeds 25% of the pad area shall be permitted on edge pad metallization.

Pits and voids shall be permitted in dielectric material except that no void or pit shall be permitted which exceeds 0.2 mm [0.008 in] in any dimension and which exposes buried metallization within 0.1 mm [0.004 in] of other unconnected active metallization.

3.7.3.3 Scratches No scratch in the circuit metallization shall be acceptable which:

- Reduces the width of a conductor by more than 50%.
- Occurs in the metallization over a capacitor and exposes the underlying dielectric.
- Occurs at or over a dielectric step where there is a cross-over.
- Reduces the contact area between conductor and resistor by more than 25%.
- Reduces the effective area of die bonding and wire bonding pads by more than 25%.
- Completely crosses a metallization strip and exposes the underlying circuit at any point.

3.7.3.4 Bridging No metallization smear or bridge shall extend continuously to reduce the distance to any adjacent conductor pattern to less than the percent spacing reduction shown in paragraph 3.8.2 (see Figure 4) or decrease the distance to unconnected metallization to less than 0.1 mm [0.004 in].

3.7.3.5 Cracks No crack shall be permitted which reduces the width of metallization by more than 40% or the conductor reduction limits of paragraph 3.8.1, whichever is less. No cracks shall be permitted in either metal or dielectric where the crack or any combination of cracks shall be present along 40% or more of the periphery of a bonding pad with an integral via structure.

No cracks in the dielectric material shall be permitted which cumulatively expose more than 5% of the underlying metal. No crack in dielectric material which points toward bonding pads and comes closer than 0.1 mm [0.004 in] to said bonding pad shall be acceptable.

3.7.3.6 Burrs and Projections No protruding surface imperfection shall exceed 0.2 mm [0.008 in] in height or 0.6 mm [0.024 in] in any other dimension. In addition, no such protrusion imperfection shall be permissible which extends beyond the reference surface by more than the maximum specified below.

Seal area (unmetallized) 0.05 mm
[0.002 in] max.

Chip/chip carrier attach surface 0.05 mm
[0.002 in] max.

Contact surface (unmetallized) 0.05 mm



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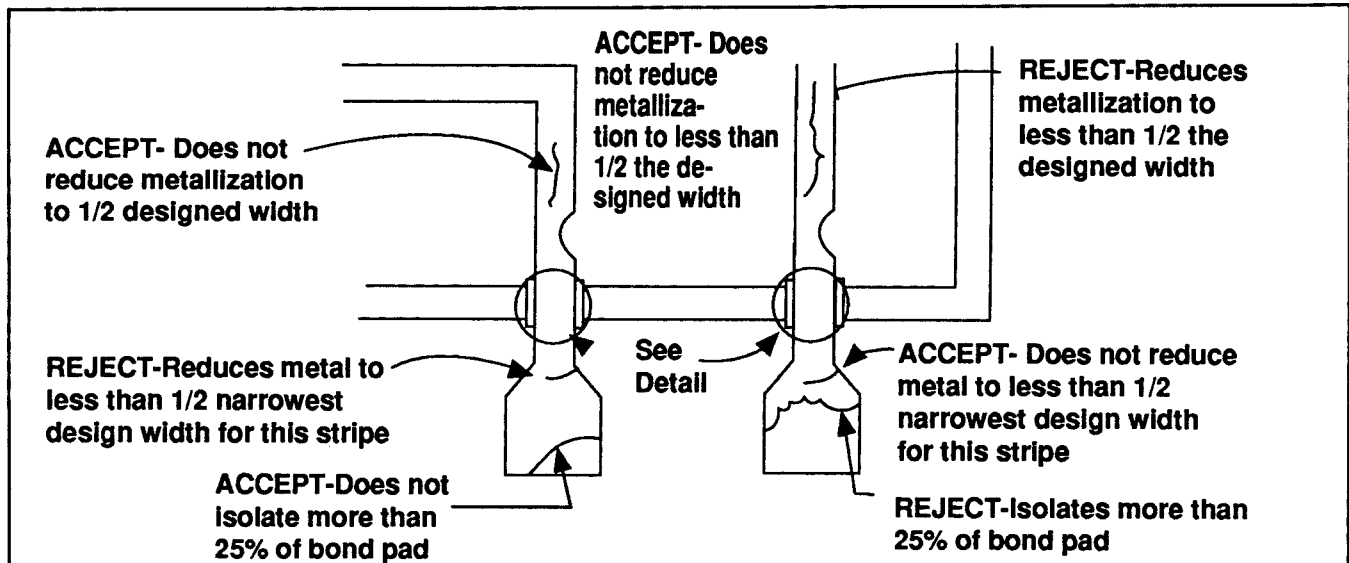


Figure 3A.

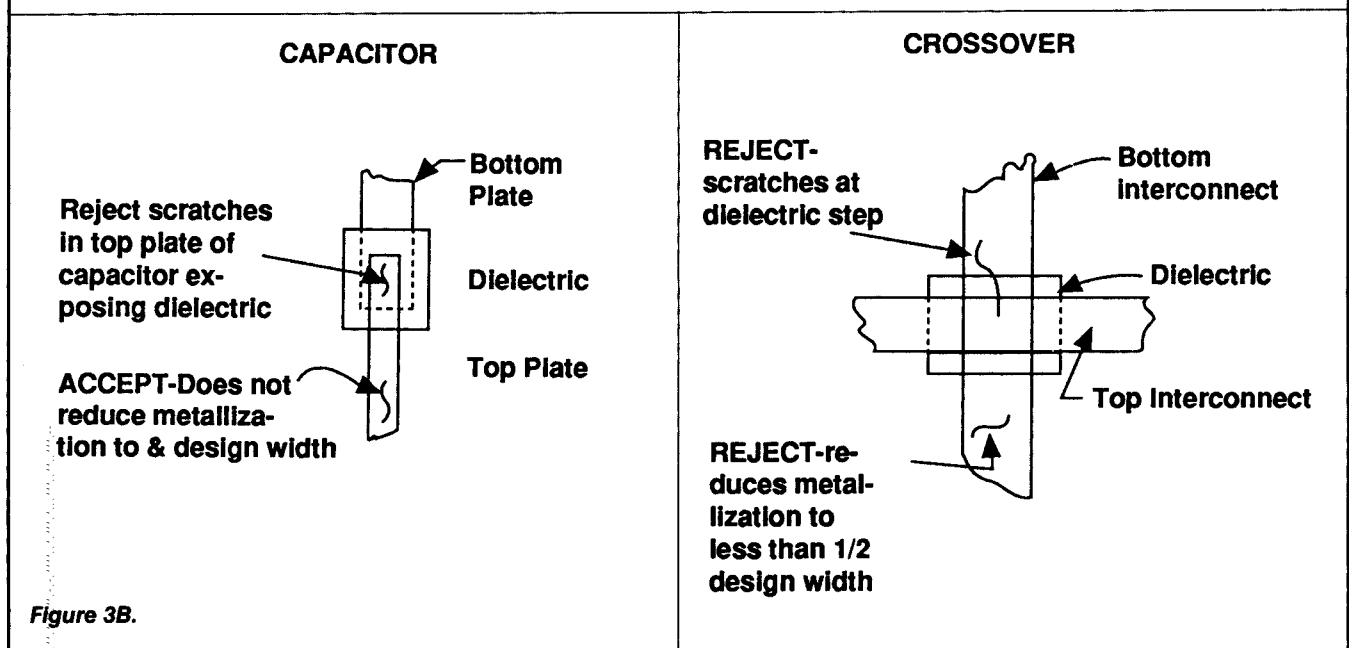


Figure 3B.

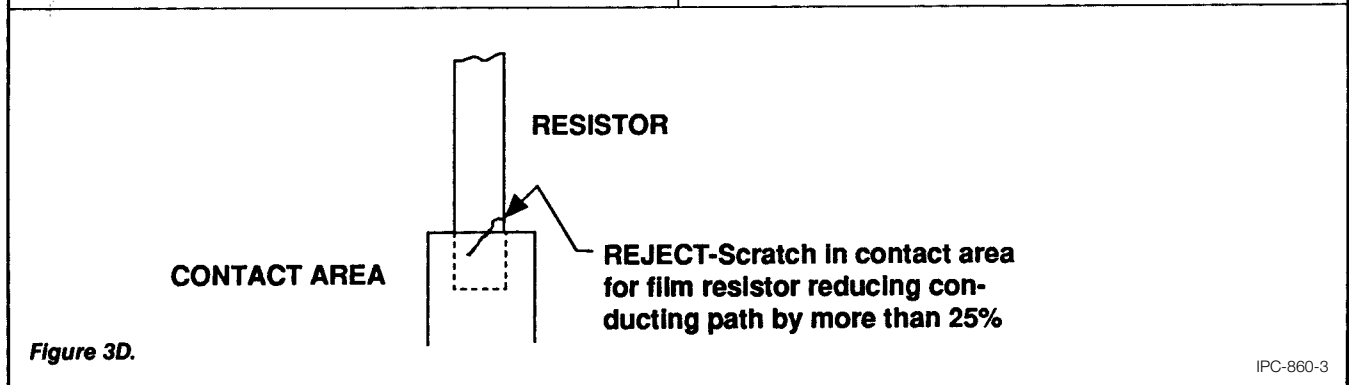


Figure 3D.

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Figure 3 Pattern defects.

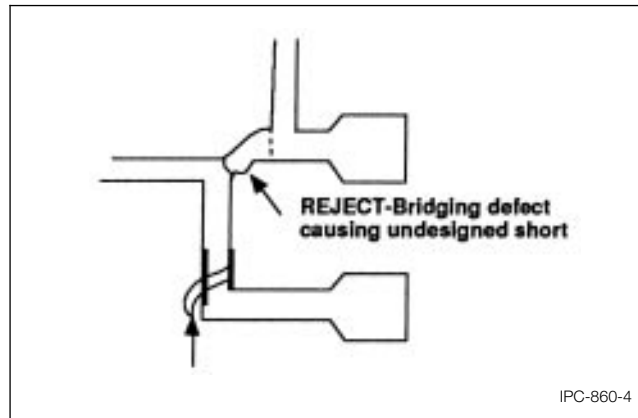


Figure 4 Bridging.

3.7.3.7 Inclusions Inclusions shall be permitted in the dielectric material only, provided that such inclusions do not approach closer than 0.1 mm [0.004 in] to a via or bonding pad which is exposed on the top surface. Inclusions shall not exceed 0.3 mm [0.012 in] in any dimension and shall not protrude from the surface of the dielectric by more than 0.1 mm [0.004 in].

3.7.3.8 Dielectric Dielectric material shall not overlap die bonding areas, wire bond pads or any other metallized attachment area. Dielectric material shall exhibit no pin holes in excess of those defined in Table 2 provided that no underlying metallization is exposed and not in more than 10% of the area. Conductors shall have 65% or greater of their area opaque to transmitted light.

Table 2 Dielectric Pinhole Allowances

Final Product Intended Use	Class 1	Class 2	Class 3
Uncoated or Unsealed	0.1 mm [0.004 in]	0.05 mm [0.002 in]	No Pin Holes
Conformally Coated or Hermetically Sealed	0.25 mm [0.010 in]	0.1 mm [0.004 in]	No Pin Holes

3.7.4 Thick Film Resistors/Capacitors.

3.7.4.1 Cracks No screened thick film resistor shall be acceptable that exhibits cracks or fissures which expose the underlying circuit in the remaining active area and which exceed 0.1 mm [0.004 in] in length.

3.7.4.2 Voids No screened resistor shall exhibit voids in the active area which exceed 0.1 mm [0.004 in] or 20% of the width, whichever is greater. Voids in resistor areas shall be limited to those under 0.1 mm [0.004 in] in diameter or smaller; such voids shall be included with trim zones to evaluate resistors for minimum dimensions.

3.7.4.3 Trimming No resistor shall be acceptable which exhibits a reduction to a width of less than 0.1 mm [0.004 in], or 20% of the minimum design width, whichever is greater.

3.7.4.4 Terminations All resistors shall overlap their termination area by at least 0.1 mm [0.004 in] in width or length unless designed otherwise.

3.7.4.5 Alignment No resistor shall be acceptable which exhibits misalignment sufficient to come closer than 0.1 mm [0.004 in] to unconnected metallization except by design. (See Figure 5.)

Any resistor which does not, except by design, contact the metallization over the entire width of the resistor shall not be acceptable.

Any capacitor or crossover in which the dielectric does not overlap the top and bottom metallization plates or which shows any visible bump or indentation in the overlaying metallization shall not be accepted.

3.7.5 Workmanship Multilayer hybrids shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life and serviceability.

3.8 Dimensional Requirements The following paragraphs define dimensional requirements and test criteria for conductor width and spacing, circuit flatness and thickness. The finished multilayer hybrid circuit shall meet the dimensional requirements of the engineering drawing and the information specified herein.

3.8.1 Conductor Width Any combination of edge roughness, nicks, pin holes, and scratches exposing the substrate material shall not reduce the conductor width more than that specified in Table 3 of the minimum design width indicated on the master drawing. There shall be no more than 5 occurrences of the percent reduction per conductor layer and no occurrence shall be greater than 6.25 mm [0.25 in] in length.

3.8.2 Conductor Spacing When inspected in accordance with 4.6.2, the conductor spacing of the multilayer hybrid circuit shall be as specified on the master drawing. The spacing specified on the master drawing shall not be reduced by more than that indicated in Table 4.

3.8.3 Circuit Length, Width, and Thickness When measured as specified in 4.6.2 the hybrid circuit shall meet the requirements of Table 5. Thickness shall be per the engineering drawing as measured in five locations.

3.8.4 Camber Unless otherwise specified on the master drawing, when examined in accordance with 4.6.2.1, camber shall not exceed the requirement specified in Table 6.