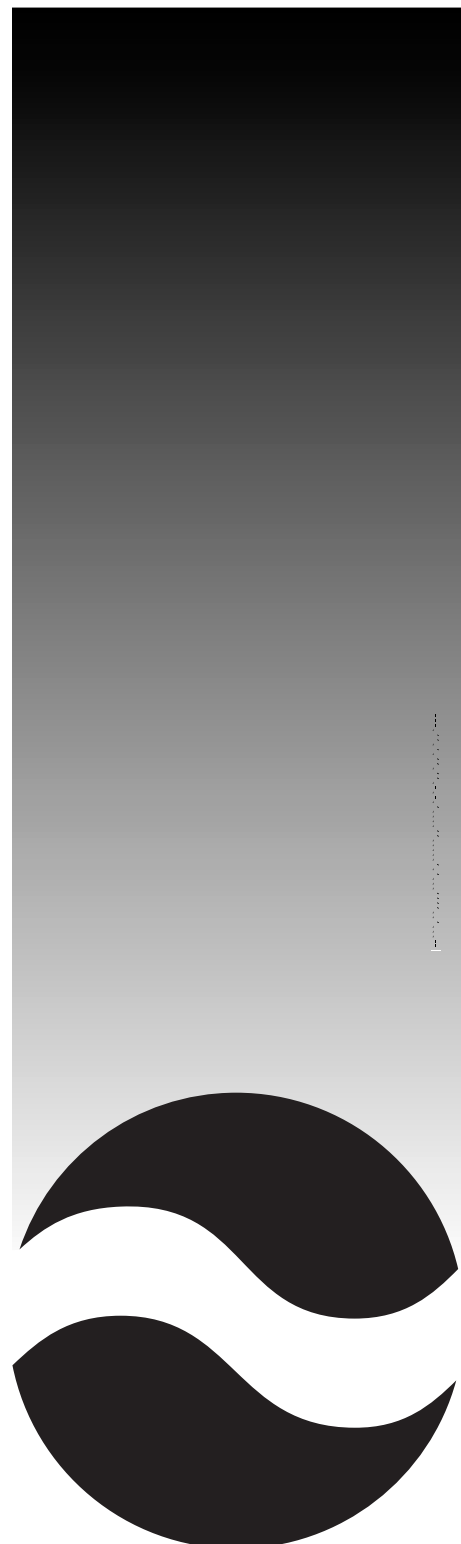


IPC/EIA J-STD-026
AUGUST 1999

JOINT INDUSTRY STANDARD

Semiconductor
Design Standard
for Flip Chip
Applications



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For Technical Information Contact:

Electronic Industries Alliance

Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201
Phone (703) 907-7500
Fax (703) 907-7501

IPC

2215 Sanders Road
Northbrook, IL 60062-6135
Phone (847) 509-9700
Fax (847) 509-9798

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ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES



IPC/EIA J-STD-026

Semiconductor Design Standard for Flip Chip Applications

About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

Contact:

EIA

Engineering Department
2500 Wilson Boulevard
Arlington, VA 22201
Phone (703) 907-7500
Fax (703) 907-7501

IPC

2215 Sanders Road
Northbrook, IL 60062-6135
Phone (847) 509-9700
Fax (847) 509-9798



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Members of the EIA Soldering Technology Committee (STC) and the IPC Device Manufacturers Interface Committee (A-10) have worked together to develop this document.

We would like to thank them for their dedication to this effort. Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Flip Chip Task Group are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the EIA and IPC extend their gratitude.

Device Manufacturers Interface Committee	Flip Chip Task Group	EIA Soldering Technology Committee
Chair Ray Prasad R. Prasad Consultancy Group	Chair Keith DeHaven Motorola	Chair Mark Kwoka Harris Semiconductor
Flip Chip Task Group		
J. Mark Bird, Amkor Technology Syed Sajid Ahmad, Micron Technology Bernie Aronson, EIA Pamela Ashcraft, Delphi Delco Electronics Systems Dieter Bergman, IPC Mike Brownell, Intel Dick Carpenter, IBM Keith DeHaven, Motorola Robert K. Doot, Motorola Werner Engelmaier, Engelmaier Associates	Marty Freedman, AMP, Inc. Joe Fjelstad, Tessera Kuan-Shar Lei, Compaq Helen M. Low, Celestica Rob Lyn, Celestica (IBM Canada Sub.) Susan Mack, Delphi Delco Electronics Systems Paul A. Magill, MCNC Phil Marcoux, Chip Scale Inc. Tze W. Poon, Sematech	Glenn Rinne, MCNC Ray Rinne, IBM Paul Totta, IBM East Fishkill Iwona Turlik, Motorola Dan Ward, Delphi Delco Electronics Systems James Rausch, Delphi Delco Electronics Systems Rod Frantz, Delphi Delco Electronics Systems

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Semiconductor Design Standard for Flip Chip Applications

1 SCOPE

This standard addresses semiconductor chip design. It is intended for applications utilizing standard substrates, materials, assembly, and test methods as well as established semiconductor fabrication and bumping processes.

1.1 Purpose The purpose is to provide flip chip design standards which are commensurate with established fabrication, bump, test, assembly, handling and application practices. Addressed are electrical, thermal, and mechanical chip design parameters and methodologies as well as the reliability associated with these items. These standards are intended for new designs as well as modifications of non-flip chip designs.

1.2 Classifications

1.2.1 Bump Process Technologies The following processes for forming bumps on semiconductor die intended for flip chip mounting have proven effective. Some are in full production, others are in development.

- (A) Evaporation (tin-lead)
- (B) Solder Paste Deposition
- (C) Electroplated Tin Lead
- (D) Gold Stud Bumping
- (E) Conductive Epoxy
- (F) Electroless Nickel

Design rules for process technologies A, B and C are well-defined and are detailed in this standard; future revisions will incorporate those rules for the other processes listed as they become available.

1.2.2 Substrate Technologies Four typical mounting structure technologies are listed and affect the design rules of the bare die. These pertain primarily to the precision capability, pitch of bonding site locations, and CTE characteristics.

- (W) Organic (Rigid) (see IPC-2222 and IPC-6012)
- (X) Flex (Flexible Organic) (see IPC-2223 and IPC-6013)
- (Y) Ceramic
- (Z) Silicon

1.2.3 Application Classes The reliability of flip chip assemblies will be determined by design decisions. Assumptions are made for each design as to how long it has to survive and in what environment the product will be deployed. In addition, many companies have to determine what is an acceptable failure probability. Table 1 shows the worst case anticipated use thermal environment for nine specific categories. Information is provided on their minimum and maximum temperature excursion, as well as the delta of which the equipment usually sees. Other information provides the details for the cycle time hours, cycles per year, and the years of service expected by the customer. Table 1 also indicates levels of accelerated temperature testing which might correspond to these environments.

Accelerated testing is generally applied in electronics to examine product robustness to anticipated environmental exposures. Common methods include, but should not be limited to, high and low temperature storage, power temperature cycling, thermal cycling/shock and mechanical cycling/shock.

1.2.4 Producibility Level In general, the largest bump pitches are associated with the lowest bump and flip chip assembly process defectivities, the cheapest substrate costs and the most repeatable probe and test results. Tight pitch on the device and substrate lead to high test costs and more complex substrates. Designers should always defer to the largest pitch for manufacturability, consistent with other design goals. Cost tradeoffs should be compared for the substrate and die, (whole system), as the cost can be dominated by either.

Table 1 Representative Realistic Worst Case Use Environments for Surface Mounted Electronics and Recommended Accelerated Testing for Surface Mount Attachments
(Table Originates in IPC-SM 785)

Use Category	Tmin °C	Tmax °C	$\Delta T^{(1)}$ °C	Cycle time hrs.	Cycles per year	Yrs of Service	Accept. Failure Risk %	Tmin °C	Tmax °C	$\Delta T^{(2)}$ °C	t ₀ min
1. Consumer	0	+60	35	12	365	1-3	-1	+25	+100	75	15
2. Computers	+15	+60	20	2	1460	-5	-0.1	+25	+100	75	15
3. Telecom	-40	+85	35	12	365	7-20	-0.01	+25	+100	75	15
4. Commercial Aircraft	-55	+95	20	12	365	-20	-0.001	0	+100	100	15
5. Industrial Automotive Passenger Compartment	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	-10	-0.1	0	+100	100 & COLD ⁽³⁾	15
6. Military Ground & Ship	-55	+95	40 & 60	12 12	100 265	-10	-0.1	0	+100	100 & COLD ⁽³⁾	15
7. Space leo geo	-269	+95	3 to 100	1 12	8760 365	5-30	-0.001	0	+100	100 & COLD ⁽³⁾	15
8. Military Avionics	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	-10	-0.01	0	+100	100 & COLD ⁽³⁾	15
9. Automotive Underhood	-55	+125	60 &100 &140	1 1 2	100 300 40	-5	-0.1	0	100 & COLD ⁽³⁾	100 & LARGE	15 $\Delta T^{(4)}$

& = in addition

- 1) ΔT represents the maximum temperature swing, but does not include power dissipation effects.
- 2) All accelerated test cycles should have temperature ramps <20 °C/minute and dwell times at temperature extremes should be 15 minutes measured on the test board. This will give 24 test cycles/day.
- 3) The failure/damage mechanism for solder changes at lower temperatures; for assemblies seeing significant cold environment operations, additional "COLD" cycling from perhaps -40 TO 0 °C with dwell times long enough for temperature equilibration and for a number of cycles equal to the "COLD" °C operational cycles in actual use is recommended.
- 4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain -20 to +20 °C transition region; for assemblies seeing such cycles in operation, additional appropriate "LARGE T" testing with cycles similar in nature and number to actual use is recommended.

1.3 Presentation All dimensions and tolerances in this standard are expressed in metric units with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off or the required precision. Users are cautioned to employ a single dimensioning system, and not intermix millimeters and inches. Reference information is shown in parentheses ().

1.4 Interpretation **Shall**, the emphatic form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** requirement may be considered if sufficient data is supplied to justify the exception.

The words *should* and *may* are used whenever it is necessary to express non-mandatory provision.

Will is used to express a declaration of purpose.

To assist the reader, the word **shall** is presented in bold characters.

1.5 Organization of Design Information This standard is organized into various sections in order to provide information for the design of flip chip devices. The main sections with their points of emphasis are:

- Section 3 Design Considerations
- Section 4 Quality Assessments

1.6 Order of Precedence In the event of any conflict in the development of new designs, the following order or precedence should prevail:

1. The customer requirements.
2. Substrate design rules.

3. Bump design rules.
4. This standard.

2 APPLICABLE DOCUMENTS

The following documents contain provisions which, through reference in this text, constitute a part of the J-STD-026. At the time of publication, the editions indicated were valid. All documents are subject to revision and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions.

J-STD-012	Implementation of Flip Chip and Chip Scale Technology
J-STD-027	Mechanical Outline Standard for Flip Chip or Chip Scale Configurations
J-STD-028	Performance Standard for Flip Chip/Chip Scale Bumps
IPC-2221	Generic Standard On Printed Board Design
IPC-2222	Sectional Design Standard for Rigid Organic Printed Boards
IPC-2223	Sectional Design Standard for Flexible Printed Boards
IPC-2226	Design Standard for High Density Interconnect Structures (HDIS)
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
IPC-6013	Qualification and Performance Specification for Printed Boards, Flexible and Rigid-Flex
IPC-7078	Sectional Requirements for Flip Chip Mounting (Direct Chip Attach)
IPC-T-50G	Terms & Definitions

3 DESIGN CONSIDERATIONS

3.1 Terms and Definitions The terminology used in this standard shall be in accordance with IPC-T-50 and the normative terminology and acronyms shown in Annex A.

3.2 General Designing IC pad locations for wire bonding is generally well understood; this is unfortunately not true for flip chip technology. Flip chip offers new freedoms such as placing bumps internal to the die edge, over circuitry or in array format depending on the bump technology. Along with these new freedoms comes different constraints with the bump process capability and the ability to route the next level of assembly. To produce a successful bump footprint design, it takes much more than just following design rules. It takes a design team with packaging expertise to ensure that the final product is a success.

The drive for flip chip technology often stems from a need to miniaturize, to obtain electrical performance improvements or to accommodate interconnect density demands. All of these needs highlight the critical nature of a comprehensive design - a footprint design that is completed in concert with the design of the next level of assembly.

There are many dangers for those unwilling to address the design requirements up front. For miniaturization, a poor IC footprint design may result in assembly process or substrate yield losses as trace width and pitch are reduced, resulting in increased system costs. For electrical performance, the next level of assembly design may have routing parasitics which eliminate the benefits achieved in the die design. A poor chip footprint design with high interconnect density, may require extra routing layers driving system costs much higher. Hence, interactive design is crucial to obtaining a viable flip chip product.

A final reason for interactive design is that substrate capabilities and bump capabilities are ever evolving in terms of mechanical, electrical, thermal and fanout capabilities as well as in terms of cost. This document can not foresee these changes so it is imperative that the IC footprint design be completed interactively with those up to date on the latest capabilities and costs.

A bumping alternative for those chips which weren't designed specifically for flip chip is to redistribute the pads into pad configuration which meets the bumping design rules and which can be flip chip assembled more readily. See Section 3.4.3 for more information on the redistribution process.

3.3 Footprint Design The simplest flip chip design occurs when the footprint is compatible with the wire bond footprint allowing two interconnect types and multiple packaging options. This would be considered a peripheral design where the pad pitch is large enough to accommodate the bumping and next level of assembly capabilities. See Figure 1. Peripheral Footprint Design.

A more typical footprint utilizes a staggered approach or random footprint where the bump pitch or fanout capability force the pinouts to be distributed across the die face. See Figure 2. Staggered pitch or fanout strategy can be utilized to minimize the coupling between the bump and the circuitry below. It is possible to change the pad patterns to accommodate the pitch staggering without adding white space (non-functional die area) or overlapping sensitive circuitry. The fanout constrained footprint has a lower density of bumps internally since the substrate vias utilized for escape are generally large in size and pitch.

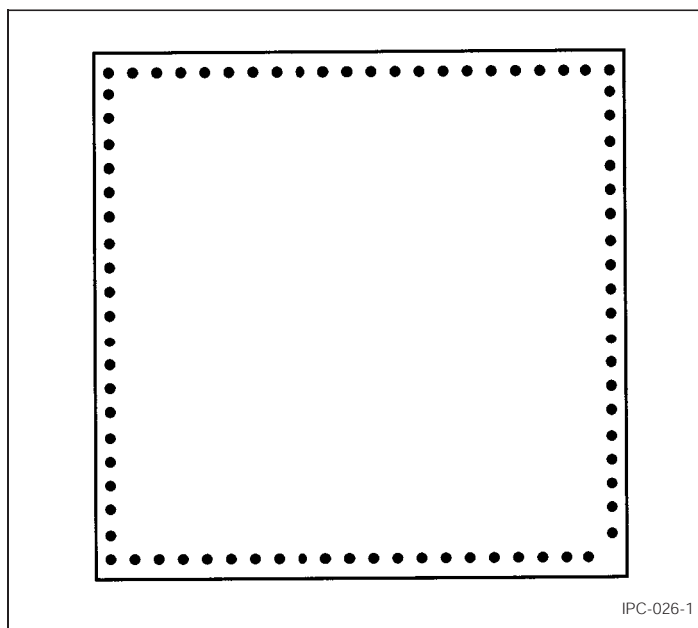


Figure 1 Peripheral Footprint Design

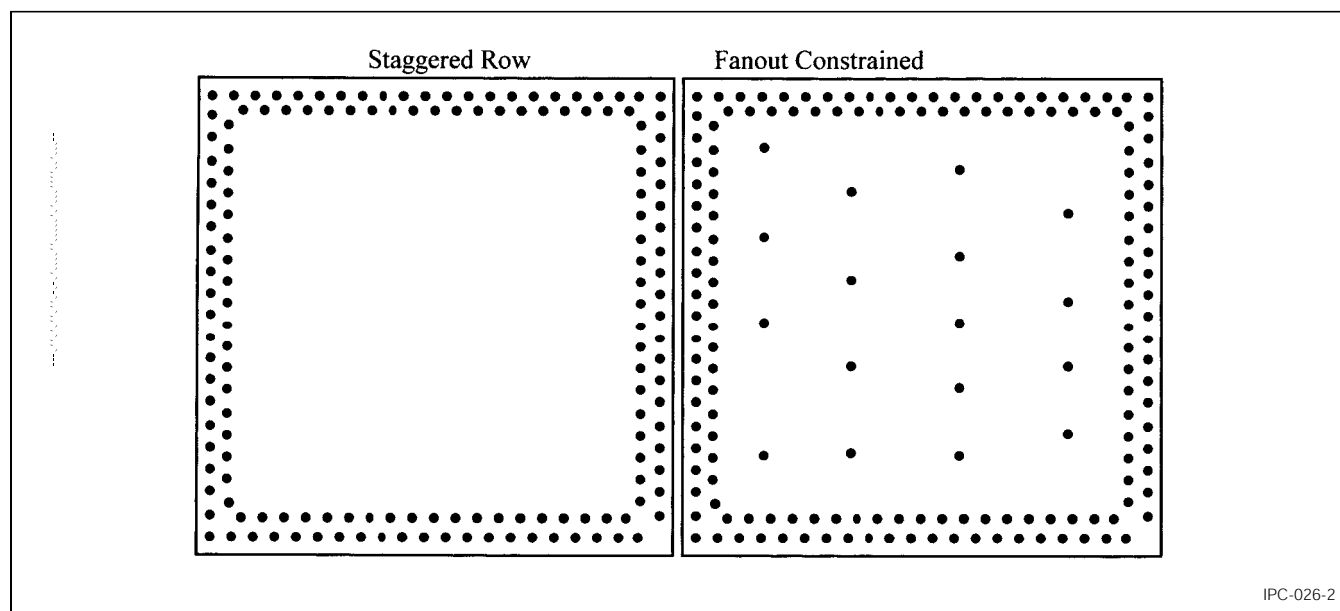


Figure 2 Staggered Row and Fanout Constrained Footprint Design

If an additional metal layer (redistribution metal) is utilized to route from wire bond pads to bump pads in the die center, these bump pads should be for signals such as test pads and control signals that are not sensitive to wiring parasitics. The fanout constrained case is usually targeted for low cost where tighter pitches may increase the cost of the next level of assembly or the bumping process. The drawback to this scheme is that it may not accommodate a die shrink.

Cost reduction is a major goal of every IC design. This is often achieved through successive die shrinks of the original design yielding a smaller die and a lower die cost. Oftentimes, it is undesirable to redesign the next level of assembly particularly when the next level of assembly is complex or expensive (where a redesign might be expensive or jeopardize the product functionality). The bump footprint design should encompass the die shrink strategy and a universal footprint should be used where possible as shown in the Universal Die Footprint Design, Figure 3.

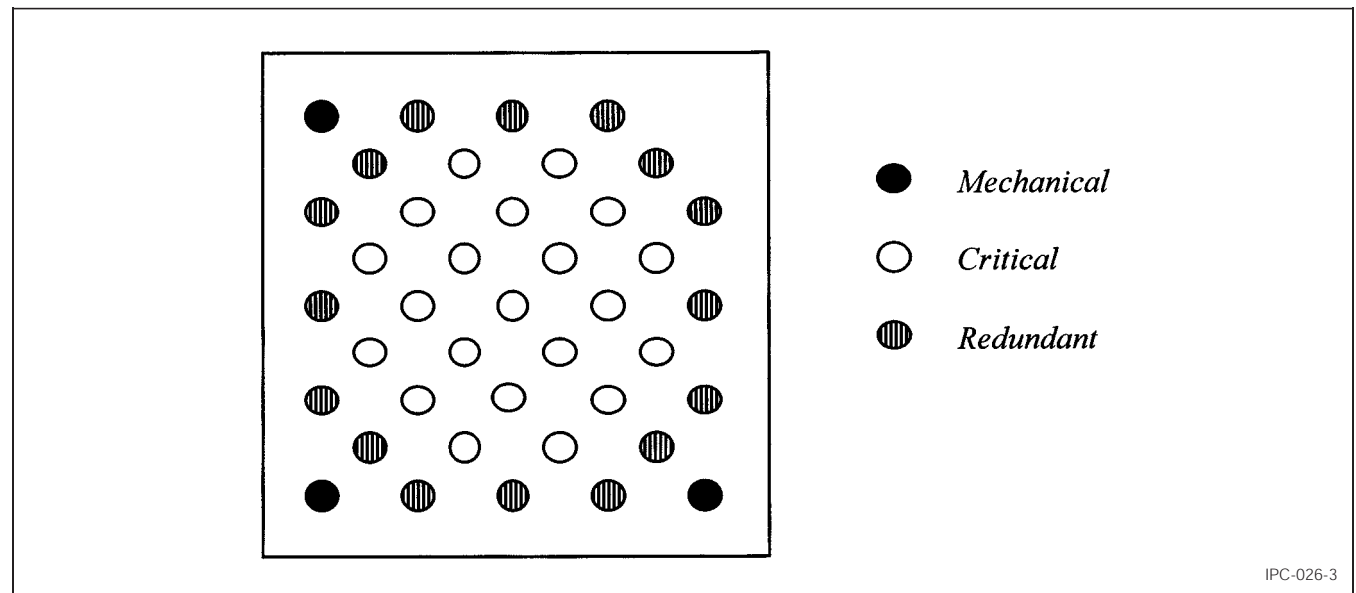


Figure 3 Universal Die Footprint Design

To accommodate die shrink, all the critical bumps should be located in the die interior and the outer bumps used for redundant and mechanical bumps. When the shrink occurs, the outer, less essential rows will be lost, but the critical bumps will not be affected. As the chip shrinks so does the Distance to the Neutral Point (DNP) - making the loss of redundant and mechanical bumps less of a reliability issue. It should be noted that with this approach, the next level of assembly is not affected by the bump footprint as the non-critical connections simply become open pins. Caution should be exercised when shrinking the IC area so that the bump footprint and minimum bump pitch does not change without customer approval.

Provision must be made for orientation and alignment of the shrunk die. In this strategy, the bumps must be allowed over active circuitry and the next level of assembly must be able to fan out the interconnections. The last metal functions as a redistribution metal in that it routes the bump pad locations to the pad pattern with its Electrostatic Discharge (ESD) structures. Since the redistribution metal requires additional processing and cost, the tradeoff should be considered in relation to a redesign for the next level of assembly. For example, some Chip Scale Packages (CSP) carriers may be cheaper to revise than using a redistribution metal layer and relaying out the metal layer. Another reuse concept is to design a substrate which accommodates the bump footprint of many die. This would decrease substrate costs thereby lowering the system cost.

With the chip bumping process, nearly the entire chip surface can be utilized for interconnect pad locations. In fact, over 6000 bumps on a chip has been demonstrated and chips with over 2200 bumps are in production. These bump counts are generally utilized in an array format for high performance applications. See the bumped flip-chip array example in the right hand side of Figure 4, Wire Bond Connections versus Bump Connections.

Chip bumping can enable increased interconnect density depending on the die size and the bumping process. Signal, clock and power connections can be placed almost anywhere on the chip and redundancy means distributions can be optimized for minimum noise and skew, current density and line length. Additionally, on-chip wiring can be reduced since the z-axis escapes are available where needed. Figure 4, Wire Bond Connections versus Bump Connections compares single row wire bond and bump chips. Each chip is 8 mm square. Wire bond pad size is 76 μm with pads on 100 μm centers. Bump size is 100 μm bumps on a 200 μm center. In this example, interconnect density is increased over 2.4X using bump technology.

When the interconnect density is increased, finer and more accurate features are required on the next level of assembly to fanout these connections. In addition, the layer count may need to be increased to help route out the connections. Both requirements for finer features and added layers increase cost impacting the final product cost. Thus, it is important to understand the pitch constraints and capabilities of the next level of assembly while designing the bump footprint.

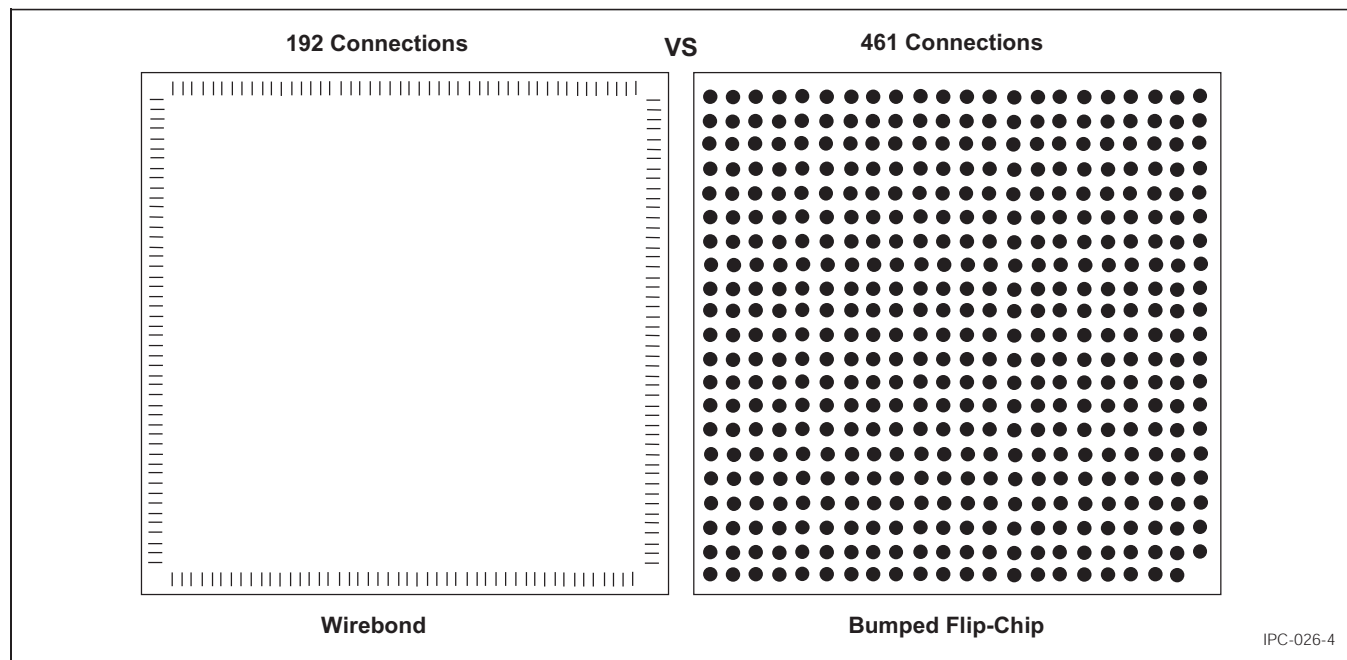


Figure 4 Wire Bond Connections Versus Array Bump Connections

The number of bumps needed varies with the electrical, thermal, and mechanical requirements. Besides just being an electrical interconnect, bumps may be added specifically for mechanical support, improving thermal dissipation, adding redundancy, and making the chip orientation unique.

There are important mechanical and reliability considerations for the bump footprint. The bump footprint provides mechanical support during the attachment process. In addition, the thermal cycle performance can be affected by the footprint balance and the Distance to the Neutral Point (DNP). These issues should be worked with the package reliability engineer to ensure that the product lifetime meets the product requirements. More information is provided in Section 3.5 Reliability Considerations.

There are important electrical considerations for the bump footprint as well and these are addressed in Section 3.4 Electrical Considerations.

Each footprint design may be unique due to the product's cost targets, die size, shrink paths, performance, packaging constraints, etc.

3.4 Electrical Considerations

3.4.1 Interconnect Parasitics Primarily because of the very short electrical paths of the bumps, parasitic inductance and capacitance are significantly less than for wire bond or TAB. Although chips designed for wire bond or TAB can be converted to bumped flip chip, optimal performance is gained by initially designing for a bumped flip chip. Chips designed for bumped flip chip can take advantage of its flexible area array capability to optimally place I/O for minimized interconnect parasitics both on and off chip. Additional flexibility is also gained for sensitive I/O, where location and guarding can be more effectively utilized.

A cross section of a joined bump is shown in Figure 5 where it can be seen that the bump is relatively short. Since the dimensions of the bumps are very small, their electrical behavior appears lumped to very high frequencies (>150 GHz). Appropriate parasitics are suggested in Table 2 although these can vary depending on the bump. These levels of parasitics are very small and for many simulation applications, they can be neglected.

3.4.2 Power and Ground Bumps There are several performance concerns when considering the attributes of the power and ground scheme. In particular, those items to consider are power losses, power and ground voltage level variation (bounce), package or board fanout efficiency, and sensitive node interconnect crosstalk.

Power losses can seriously affect performance and functionality in the IC. The number and placement of power and ground bumps should be chosen such that the power losses do not impact the performance and functionality. Unlike most other bumps, power and ground bumps are not designed to be as small as the other bumps. They are designed to be larger to provide a low impedance path for power and ground. The number and placement of power and ground bumps should be chosen such that the power losses do not impact the performance and functionality.

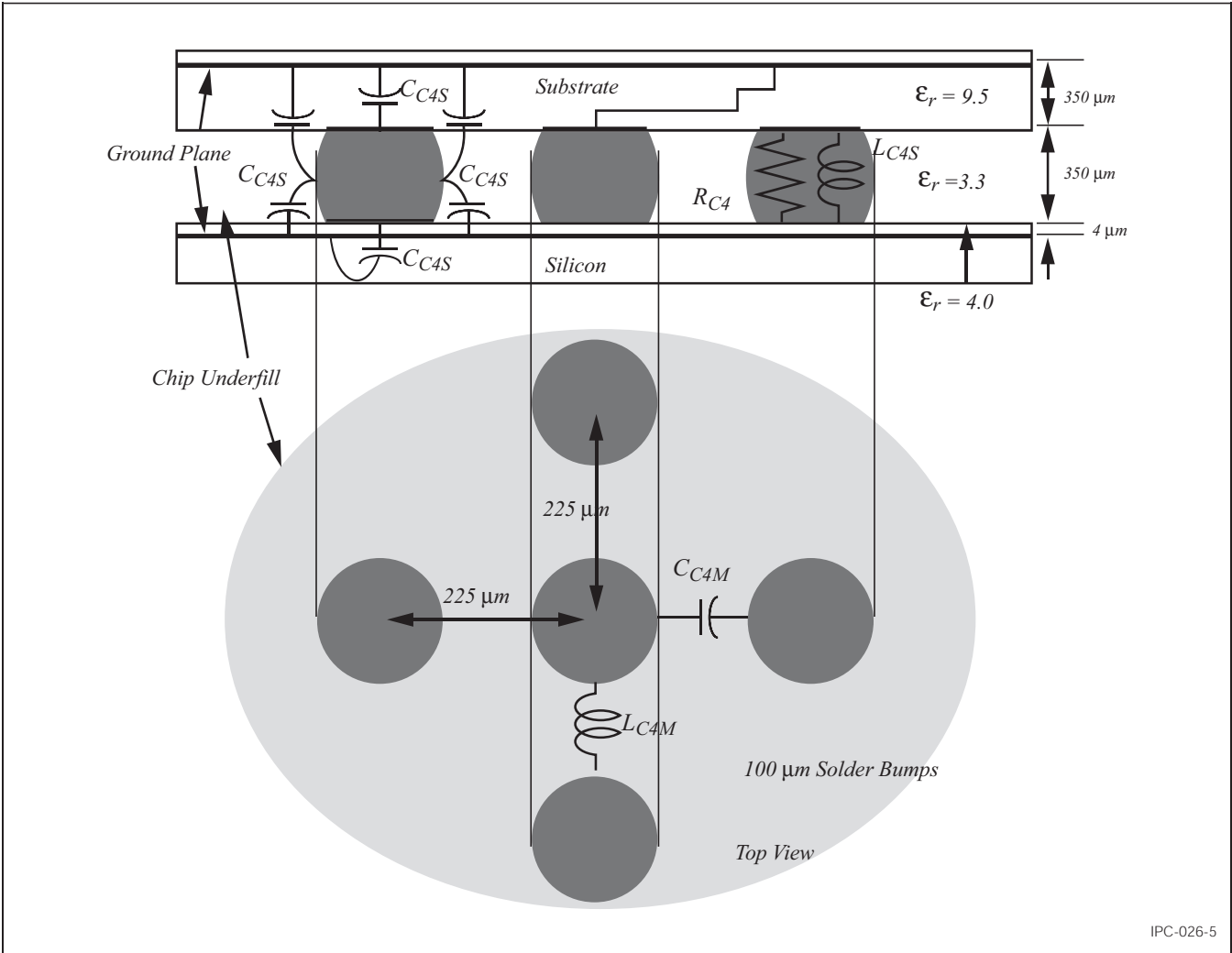


Figure 5 Bump Parasitics

Table 2 Typical Bump Parasitics

Electrical Characteristics	Value
Self capacitance	170 fF
Mutual capacitance	4.8 fF
Self inductance	160 pH
Mutual inductance	110 pH
Bump resistance	< 20 mΩ

designs which run all interconnects to the edge of the chip, bumps may be located near the circuitry that it connects to the substrate for less power loss. Some bump technologies allow placement of bumps over active circuitry. This should be utilized to prevent problems of increased resistance of longer trace length particularly on large die.

Ground and power bounce can seriously slow system level performance, so the number of power and ground bumps must be set appropriately. Although the required number varies from case to case, for high performance digital chips:

$(P + G)/S > .33$

where P + G is the total number of power and ground bumps and S is the number of signal bumps.

Generally the cross coupling between flip-chip interconnects is low as compared to wire bond due to the bump interconnects short length and large separation. If coupling is a concern, it is possible to nest or surround the sensitive bump with power and ground bumps as in Figure 6. Package or board fanout efficiency can be affected by the location of the bumps on the die. It is recommended to place the power and ground bumps internal to the circuit to permit routing of the signal bumps.

signals while allowing a short path to ground or power planes. Figure 7 demonstrates this approach. The substrate/board layout engineer should be consulted to discuss the tradeoffs in electrical performance and routability.

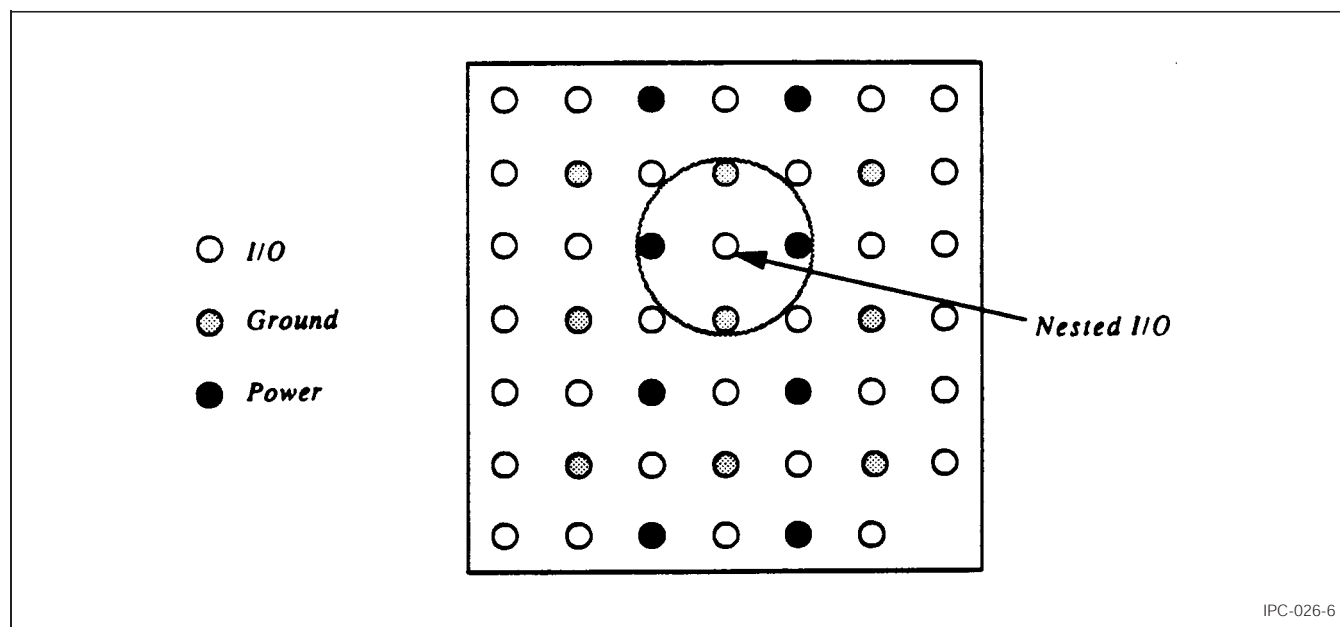


Figure 6 Nested I/O Footprint

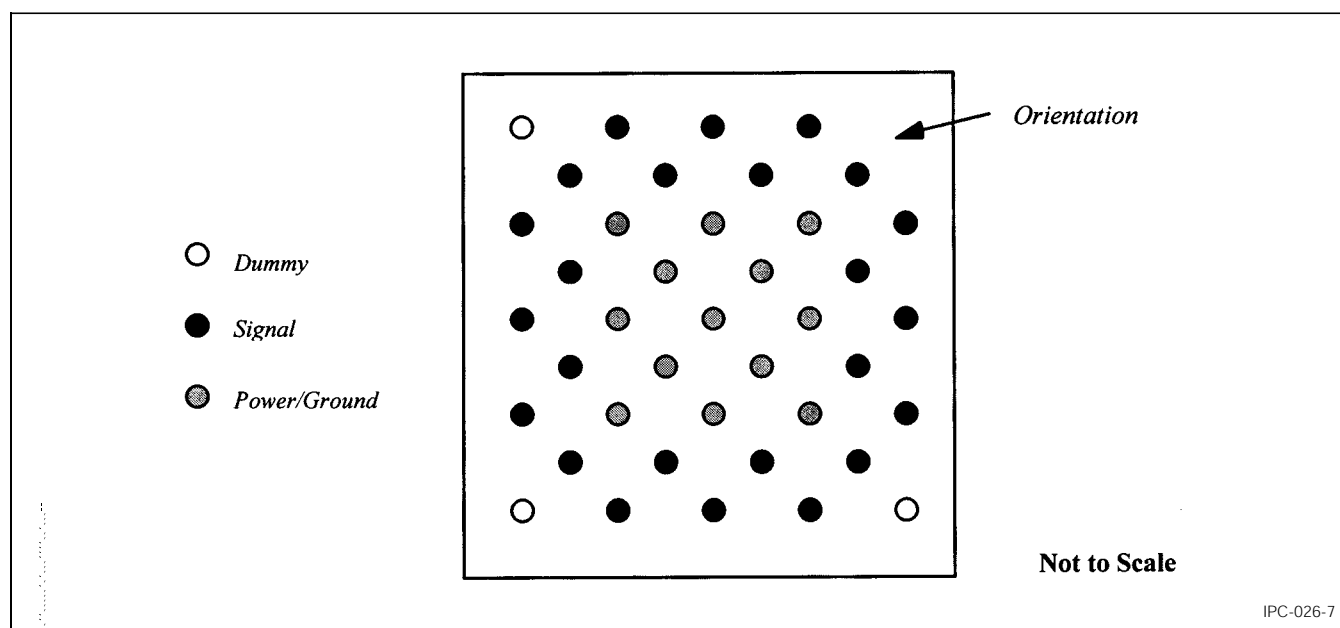


Figure 7 Central Power and Ground Footprint

3.4.3 Redistribution Effects Ideally, chips should be designed from the start for flip chip and chip scale attachment. Chips that have not been designed for solder bumping require additional processes to reconfigure the existing I/O geometries and/or relocate them from the perimeter to a centrally located area array (see Figure 8). Thus, the term redistribution is utilized when the existing chip pad locations are rerouted to accommodate the flip-chip applications.

The flip-chip pitch requirement may be limited by the bumping process or by the substrate layout. The redistribution processing adds cost but in return allows the fabrication facility to utilize an existing design for flip chip. The concern with redistribution is its impact on ESD, current carrying capability over device lifetime, functionality and performance.

If properly designed, the parasitics of the redistribution layer(s) can be minimized compared to the resistance and capacitance of the ESD elements. Caution should be exercised to ensure that the redistribution is capable of handling the

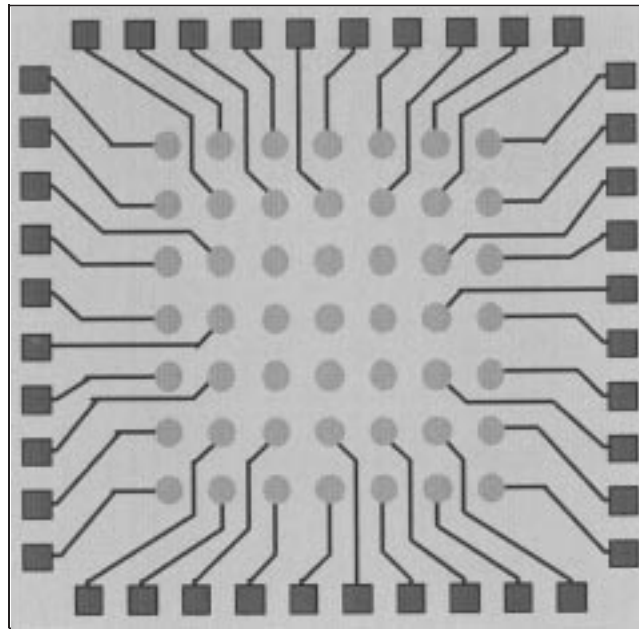


Figure 8 Redistribution of Peripheral to Area Array

instantaneous currents and voltages in the via and conductor design. In particular, narrow conductors and limited via structures (via diameter and metallization) should be avoided. Dielectric breakdown between conductors or to underlying traces is usually not an issue if the planarization/dielectric process is robust with reasonable redistribution conductor spacing.

Another consideration is the redistribution current carrying capability. This must be checked to the standard design rules applicable for the metallization layer: aluminum, nickel, copper, etc. The only caution is that the current is in one conductor whereas it may have been fanned out on underlying layers.

Perhaps the greatest danger lies in affecting functionality due to capacitive coupling to sensitive circuits. In particular, unshielded capacitors, high frequency modules, and capacitively balanced conductors should be avoided or simulated to ensure functionality. Coupling of adjoining redistribution traces should also be considered as crosstalk may cause functionality problems. Extraction programs can be utilized on the redistribution layout to extract the parasitic capacitance and resistance and then modeling can determine if there is a detrimental impact.

One of the advantages of flip-chip is that the interconnect parasitics are reduced over standard wire bond techniques and this can afford some performance improvements. The danger of the redistribution is that the added parasitics can mitigate the interconnect benefits. The specific concerns revolve around power losses for Power and Ground conductors or the conductor inductance impact on switching speeds. Again the redistribution resistance and capacitance can be extracted from the layout and added to the spice models for evaluation.

The bump pitch depends on the size of the bump and the number of I/O which must be redistributed. Large chips with low I/O allow for coarse pitch and simple routing. Small chips and high I/O call for creative bump placement and routing solutions. A first iteration for bump pitch (BP) and row pitch can be calculated based on the following equation.

$$BP = PD + 2 \cdot S + ((L + S) \cdot N)$$

BP = bump pitch

PD = pad diameter

S = space between conductors

L = conductor line width

N = number of lines between bump pair

Note: The extra space included in $2 \cdot S$ is to provide a corner bump allowance.

3.4.4 Electromagnetic Radiation Bumped flip chip designs can produce much less radiation than wire bonded or TAB parts because of the short interconnect. To achieve this benefit, routing to and from bumps must be appropriately designed, either short in length or shielded.

Although the flip chip die itself does not represent an EMI problem, as it produces less radiation than wire bonded or TAB parts, there are still EMI issues that must be addressed. For high I/O count flip chips, the electromagnetic field is concentrated