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JOINT INDUSTRY STANDARD

Performance
Standard for
Construction of
Flip Chip and
Chip Scale Bumps



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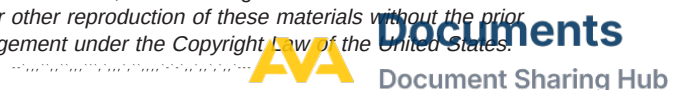
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ASSOCIATION CONNECTING
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IPC/EIA J-STD-028

Performance Standard for Construction of Flip Chip and Chip Scale Bumps

About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Members of the EIA Soldering Technology Committee (STC) and the IPC Device Manufacturers Interface Committee (A-10) have worked together to develop this document.

We would like to thank them for their dedication to this effort. Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Flip Chip Task Group are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the EIA and IPC extend their gratitude.

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Performance Standard for Construction of Flip Chip and Chip Scale Bumps

1 SCOPE

This standard establishes the construction detail requirements for bumps and other terminal structures on flip chips and chip scale carriers. All flip chip and chip scale device terminals shall meet the designated standards detailed in this document which includes such diverse terminations as solder bumps, columns, non-melting stand-offs and conductive polymer deposits. The specific standards for different terminations will therefore be appropriately matched to the particular interconnection.

1.1 Purpose The purpose of this document is to establish a set of designations and expectations for product performance for the manufacturer and user of flip chip or chip scale devices. Included in this will be the flexibility to implement the best commercial practices and evolving improvements on those practices.

1.2 Intent The intent is to recognize a large variety of terminal structures for a wide range of applications ranging from highest reliability computer, space and military applications to disposable commodity applications. Subsections in this document will provide for the flexibility to meet the cost and performance requirements.

1.3 Presentation All dimensions and tolerances in this standard are expressed in metric units with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off or the required precision. Users are cautioned to employ a single dimensioning system, and not intermix millimeters and inches. Reference information is shown in parentheses ().

1.4 Interpretation **Shall**, the emphatic form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** requirement may be considered if sufficient data is supplied to justify the exception.

The words *should* and *may* are used whenever it is necessary to express non-mandatory provision.

Will, is used to express a declaration of purpose.

To assist the reader, the word **shall** is presented in bold characters.

1.5 Organization of Design Information This standard is organized into various sections in order to provide information for the design of flip chip devices. The main sections with their points of emphasis are:

Section 3 Design Considerations
Section 4 Quality Assessments

1.6 Order of Precedence In the event of any conflict in the development of new designs, the following order or precedence should prevail:

1. The customer requirements.
2. Substrate design rules.
3. Bump design rules.
4. This standard.

2 APPLICABLE DOCUMENTS

The following documents contain provisions which, through reference in this text, constitute a part of the J-STD-028. At the time of publication, the editions indicated were valid. All documents are subject to revision and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions.

IPC-T-50 Terms/Definitions for Interconnecting and Packaging Electronic Circuits

J-STD-006 Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications

J-STD-012 Implementation of Flip Chip and Chip Scale Technology

J-STD-026 Semiconductor Design Standard for Flip Chip Applications

3 REQUIREMENTS

3.1 Terms and Definitions The terminology used in this standard shall be in accordance with IPC-T-50 and the normative terminology and acronyms shown in Annex A.

3.2 General Performance Requirements The solder bump forms the electrical and mechanical bridge between the chip and next level assembly. The bump absorbs the strain between the chip and next level of assembly caused by variations in their relative thermal expansion rates.

The solder composition of the flip chip bumps varies according to required mechanical and thermal properties. Common bump compositions include:

- Sn03Pb97
- Sn05Pb95
- Sn10Pb90
- Sn63Pb37
- In50Pb50
- In addition, conductive polymer bumps are also used.

Controlled Collapse Chip Connection (C4) is an interconnect technology invented and developed by IBM during the 1960's as an alternative to manual wirebonding. Often called "flip chip," C4 attaches a chip with the circuitry facing the substrate. In its most common form, C4 uses solder bumps deposited through a metal or polymer mask onto wettable chip pads that connect to matching wettable substrate pads. Flipped chips are aligned to corresponding substrate metal patterns and interconnections are formed by reflowing the solder bumps, thereby simultaneously forming the electrical and mechanical connections.

Electrodeposition offers a wider range of SnPb composition than evaporation, and thus offers greater control over mechanical and thermal properties. Electrodeposition can produce very small diameter bumps.

Printing solder compositions offers very tight control of solder paste compositions and offers a wide selection of different solder types.

This standard also discusses other bump metallurgy used in the industry. Although the degree of detail used to discuss other bump metallurgy is less than that used in the discussion of meltable solder bumps, greater detail will be added to future revisions of this standard.

3.2.1 Bump and Joint Expectations Bump and joint expectations are identified by the following terms:

- Mechanical strength and stability
- Dimensional uniformity, required volume, height, diameter
- Electrical conductivity
- Chemical and metallurgical stability, corrosion resistance, wettability

3.3 Classes of Flip Chip Joints There are four major classes of flip chip joints. These are:

- Meltable solder bumps (see subclause 3.4)
Examples: High Pb based SnPb (i.e., Sn03Pb97, Sn05Pb95, and Sn10Pb90), Eutectic (i.e., Sn63Pb37), Indium-based solder joints (i.e., In50Pb50)
- Partially meltable bumps (see subclause 3.5)
Examples: Cu stud tipped with eutectic, lead stud tipped with eutectic solder

- Non-meltable bumps (see subclause 3.6)
Examples: Cu ball standoff, NiAu bump, Au Bump, ball bump stud or direct chip attach.
- Polymeric/conductive adhesive bumps (see subclause 3.7)
Examples: Ag, Au, or Cu filled epoxy, Ni particle filled epoxy, plated polymer balls in adhesive, Ag filled thermoplastics, Au plated Ni particles, etc.

3.4 Meltable Solder Bump Process

3.4.1 Solder Evaporation Process (see 4.1) In the evaporative process, the necessary metal structure including metal under the bump and the bump itself are sequentially evaporated. This structure is deposited in an array of pads on the wafer surface. This can be a batch process in which the underlying metal pads and the solder bumps are deposited onto many wafers at the same time.

Prior to evaporation or sputter of this metal structure, an in-situ sputter clean is commonly performed. This is done to remove undesirable oxides and photoresist prior to metal deposition. This cleaning step generally assures low contact resistance, and the surface roughening enhances the adhesion of the metal to the organic or inorganic insulating layer.

As a part of this process, it is necessary to provide a mask that controls the shape and formation of the pattern formed on the wafer. A metal mask is commonly used for this process. This metal mask/wafer assembly typically consists of five parts: 1) a backing plate, 2) a spring, 3) the wafer to be bumped, 4) the metal mask, and 5) a clamp ring. These typically have been assembled and aligned manually. This manual procedure permits alignment to within 25 μm .

Of primary concern in any bumping process is the ability to control the uniformity of the bumps. The uniformity of the bumps formed in an evaporative process is primarily controlled by the geometry of the evaporator. The uniformity function consists of the source, the object area, and the distance separating them.

Baffles may be added to enhance the uniformity of the evaporated material. The height of the bumps, as determined by the volume of the deposited material, is a function of the standoff of the metal mask and the opening in the mask. The deposited material is conical in shape. This is controlled by the opening, which will gradually close off as material builds up on the mask during deposition.

3.4.2 Solder Electroplating Process (see 4.2) A second commonly used process for the formation of solder bumps is electroplating. This is usually done by plating through a patterned photoresist mask.

This process begins with the blanket evaporation of an Under Bump Metallurgy (UBM) layer consisting typically of an adhesion layer such as chromium or titanium and then a thicker wettable layer such as copper.

Prior to deposition of this layer, it is necessary to clean the via surface in order to remove any contaminants such as oxides or organic residues. Typically a sputter clean has been used, however, wet processing to clean these surfaces is also a possibility.

The plating process capability determines whether or not a solder dam must be deposited with the UBM or not. Two methods are generally used for forming the solder limiting layer or solder dam. The method chosen is determined by the sequence of steps used prior to reflow.

The first method consists of blanket depositing a layer of chromium or some other non-wettable metal on top of the UBM. This can be deposited sequentially with the UBM. Next, a layer of photoresist is coated and patterned. At this point, the chromium is etched open and the solder is then plated on top of the copper.

The second method consists of patterning the non-wettable layer, e.g., chromium. This layer can be patterned in photoresist; the metal can then be deposited and lifted off. After this step, a second photo-pattern is formed to plate up the solder. The second method offers greater control of the size and dimension of the bump. An example of an array of plated bumps prior to reflow is shown below in Figure 1.

At the conclusion of the plating process, the photoresist is stripped and the excess UBM blanket is ready to be removed. This excess UBM must of course be removed completely in order to prevent shorting between the bumps. At present, there are two methods used for removing the UBM. The metal can be removed by either wet or dry etching method.

The wet removal process can be handled a number of ways. It is possible with large solder bumps to etch the metal in the intervening areas using the solder as a mask, after which the solder would be reflowed. This generally works better with larger bump sizes as some undercutting may result if a wet removal process is used.