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Design Guide for High Density Interconnects (HDI) and Microvias

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A standard developed by IPC and JPCA

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Design Guide for High Density Interconnects (HDI) and Microvias

Developed by the High Density Interconnect (HDI) Design Subcommittee (D-41) of the High Density Interconnect (HDI) Committee (D-40) of IPC and the Build-Up PWB Committee of the Japan Printed Circuit Association (JPCA)

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Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the High Density Interconnect (HDI) Design Subcommittee (D-41) of the High Density Interconnect (HDI) Committee (D-40) and the JPCA Build-Up PWB Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC and JPCA extend their gratitude.

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Design Guide for High Density Interconnects (HDI) and Microvias

1 SCOPE

This document describes various via formations, materials, and design guidelines used in high density interconnects (HDI) and microvias. Microvias are processed/plated holes ≤ 0.15 mm in diameter.

1.1 Introduction This document is intended to educate the user on the formation of microvias and the selection of wiring density, design rules, interconnects, and materials. It is intended to provide design guidelines for PWBs utilizing microvia technologies.

1.2 General This document is intended to help in the selection of the preferred advanced technology for electronic packaging. The microvia PWBs are commonly referred to as build-up (BU) or sequential build-up (SBU) PWBs. These design rules apply to the BU and SBU interconnects using materials defined in IPC/JPCA-4104. The characteristics of these materials are found in Section 5.

1.3 HDI Design Selection Guideline This guideline provides an easy to follow tutorial on the selection of HDI and microvia design rules and structures. This document brings the user through various considerations to be addressed when designing an HDI PWB, including:

- Design examples and processes
- Selection of materials
- General descriptions
- Various microvia technologies (i.e., variable depth vias and stacked vias)

1.4 Design Figures Figure 1-1 is a color key to be used with all of the figures in this document. The key shows the color next to the material it represents.

2 APPLICABLE DOCUMENTS¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC/JPCA-4104 Specification for High Density Interconnect (HDI) and Microvia Materials

IPC/JPCA-6801 Terms and Definitions, Test Methods, and Design Examples for Build-Up/High Density Interconnect (HDI) Printed Wiring Boards



Figure 1-1 Color Key

3 TERMS AND DEFINITIONS

Terms and definitions shall be in accordance with IPC-T-50, IPC/JPCA-6801, and IPC/JPCA-4104.

3.1.1 Capture Land Land where the microvia starts; varies in shape and size based on use (i.e., component mounting, via entrance, and conductor).

3.1.2 Target Land Land on which a microvia ends and makes a connection.

3.1.3 Stacked Vias A via formed by stacking one or more microvias on a PTH that provides an interlayer connection between three or more conductive layers.

3.1.4 Stacked Microvia A microvia formed by stacking one or more microvias on a microvia that provides an interlayer connection between three or more conductive layers.

4 MICROVIAS

Microvias, which began in the late 1980s, are the central characteristic of HDI PWBs (see Figure 4-1). The original methods for developing microvias were by plasma desmear

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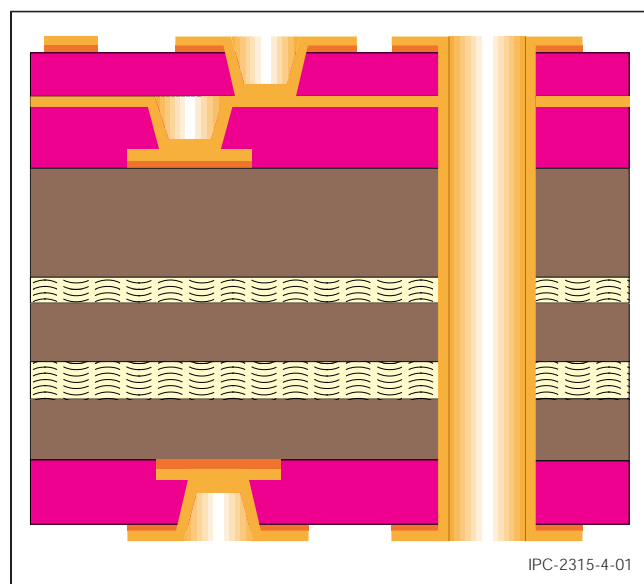


Figure 4-1 Cross Section of a General HDI with Microvias

and photodeveloping. As explained in 4.1, there are now five general ways of producing microvias.

4.1 Via Formation There are five general processes for microvia formation:

- Laser drilling
- Wet/dry etching
- Photo imaging

- Conductive ink-formed vias
- Mechanical formation

Although this section is not intended to describe all microvia formation methods, microvias can be grouped into the following three methodologies:

- Create hole then make conductive.
- Create conductive via then add dielectric.
- Create conductive via and dielectric simultaneously.

The microvia can be any shape, including straight wall, positive or negative taper, or cup. All drawings in this guideline are the artist's rendering; the hole wall shape doesn't represent the actual finished product. The techniques shown in Figure 4-2 and Figure 4-3 could be used for producing microvias.

All of these technologies require approximately the same HDI design rules and have four to eight times the wiring density of conventional, drilled PTHs.

4.1.1 Laser Ablated Vias Laser ablation is a single or multiple via generation technology that replaces mechanical drilling with lasers. Laser ablation differs from mechanical drilling in that the focused beam used to create the vias can produce smaller holes. These lasers are generally categorized by their wavelength of light. They can be used to create both blind vias and through holes. The process normally occurs after multilayer lamination and is

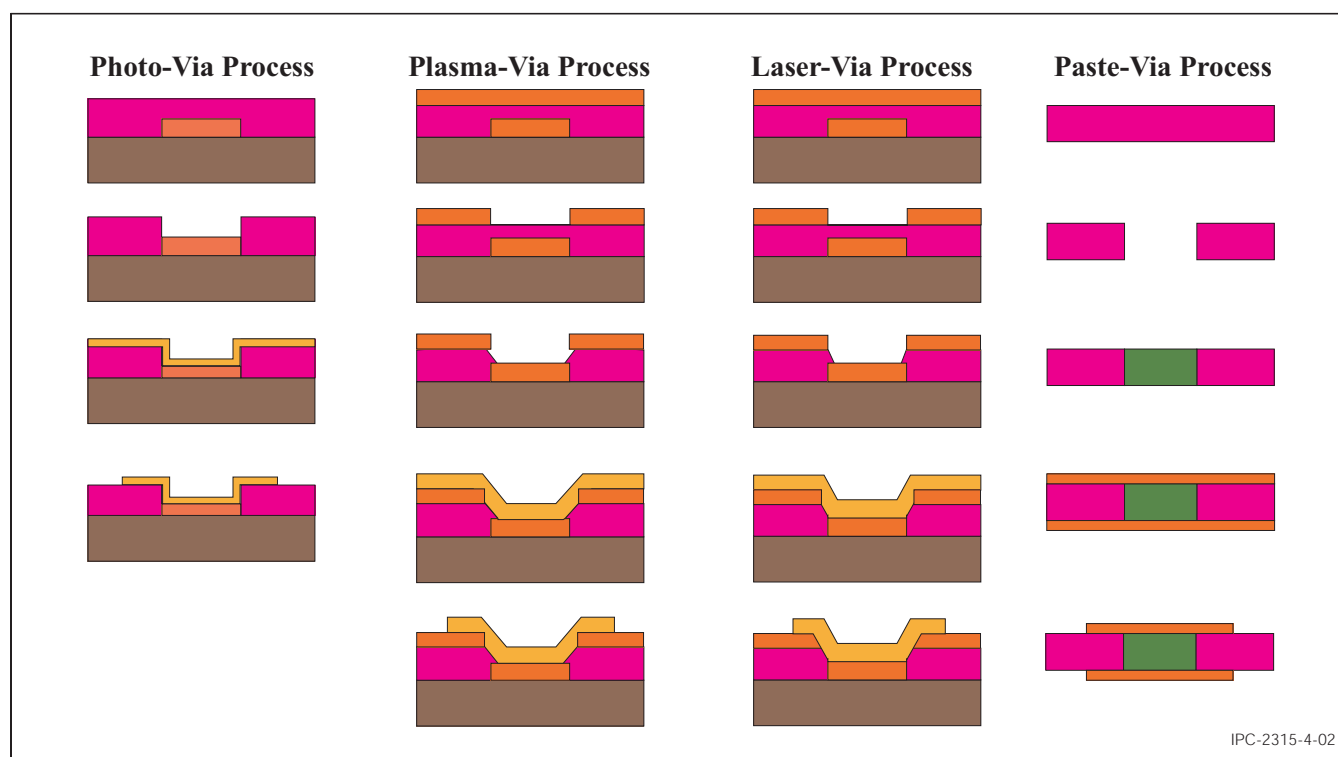


Figure 4-2 Microvia Manufacturing Processes

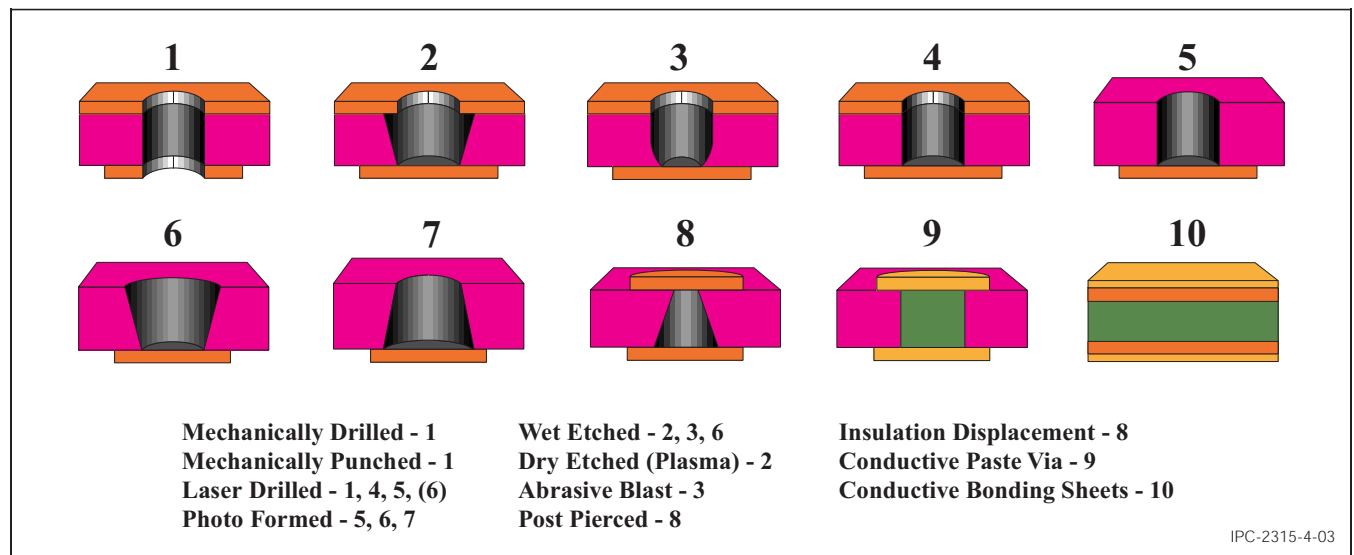


Figure 4-3 Cross-Sectional Views of Methods to Make HDI with Microvias

compatible with most materials. Laser-based microvia technologies are capable of smaller features and use standard plating technology. In the majority of cases, laser ablation produces blind or through vias one at a time, but there are processes for generating multiple laser vias simultaneously.

The four technologies represented in Figure 4-4 are just a few of those published in literature and being developed as of publication of this document. These are the oldest of the HDI technologies, employing lasers to produce microvias.

4.1.2 Wet/Dry Etched Vias Microvias can be formed by various etching techniques. The most common etching

technique is a microwave gas plasma, dry etching process. Wet etching by hot KOH has been used historically for polyimide films. Because of the chemical effects, these formation techniques are isotropic, that is they etch in all directions while they etch down. Alternate processes show that anisotropic etching can give more perpendicular sides. These formation techniques are mass via generation in that they form all vias at the same time without regard to number or diameter.

Figure 4-5 gives four examples of technologies that are developed through wet and dry etching and mechanical formation.

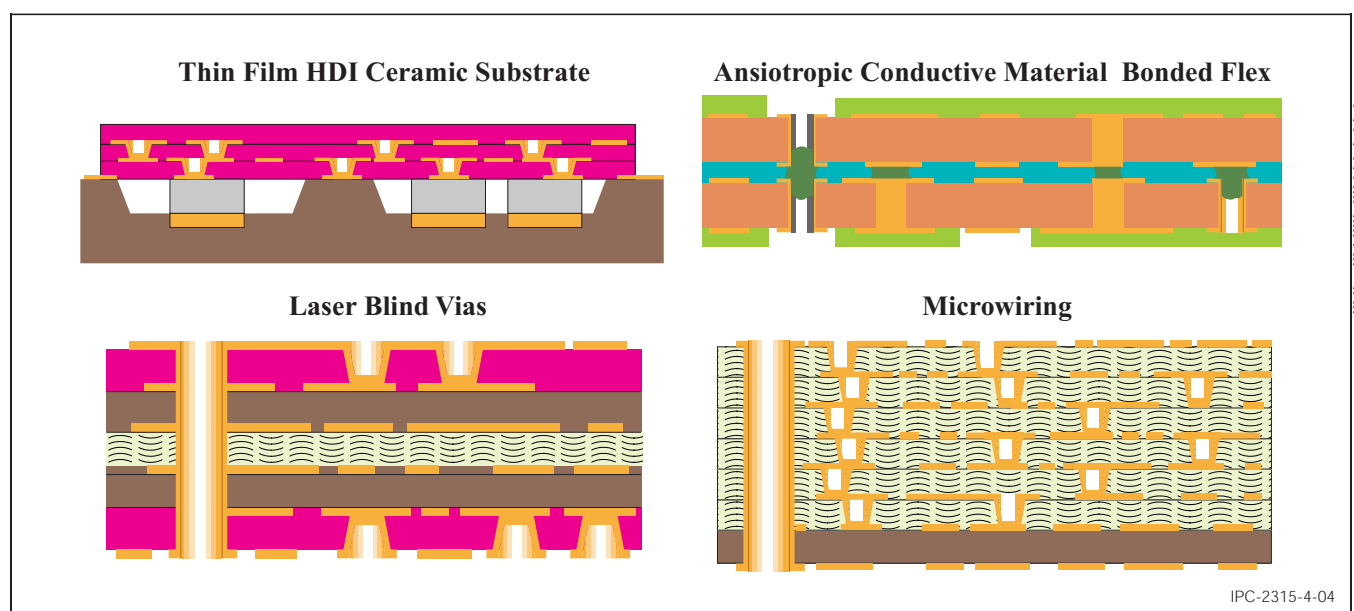


Figure 4-4 Four Typical Constructions that Employ Lasers for Via Generation

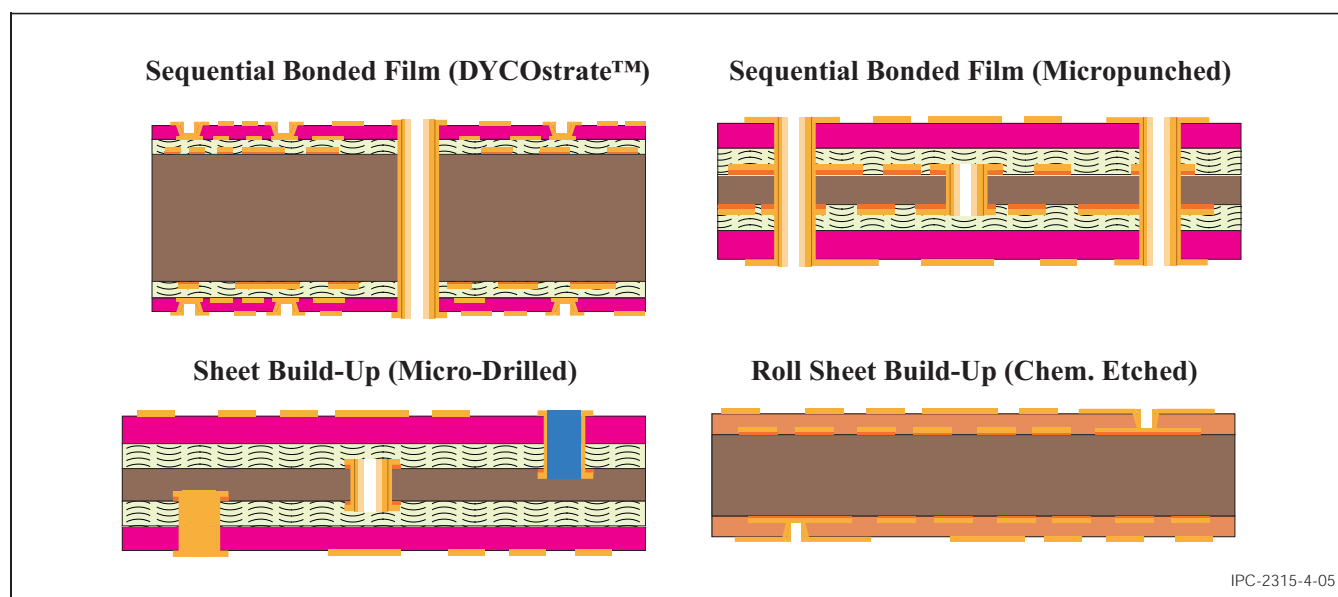


Figure 4-5 Four Typical Constructions Utilizing Etched or Mechanically Formed Vias

4.1.3 Photodielectric Vias Figure 4-6 displays a dielectric layer coated over a core substrate with PTHs and/or plugged holes. Microvias are formed by photoimaging. A layer of dielectric is coated over the base substrate. The microvias or circuit paths are imaged, developed, cured, and subsequently metallized to allow for patterning.

First used in 1988, the photoimageable dielectric was a modified solder mask. Today, modern photoimageable dielectrics (PID) are optimized as a dielectric in liquid or dry film and can be positive or negative acting. This is also a mass via generation technique, forming all vias in a single operation.

4.1.4 Conductive Inks/Insulation Displacement Figure 4-7 shows a dielectric layer with microvias formed by photoimaging, laser, or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished by either laminating copper foil onto the dielectric surface or by chemical deposition.

4.1.5 Process Flow for Via Formation Figure 4-8 is a process flow diagram of the manufacturing processes that employ PIDs, UV, or CO₂ laser ablation, and plasma etching to form microvias.

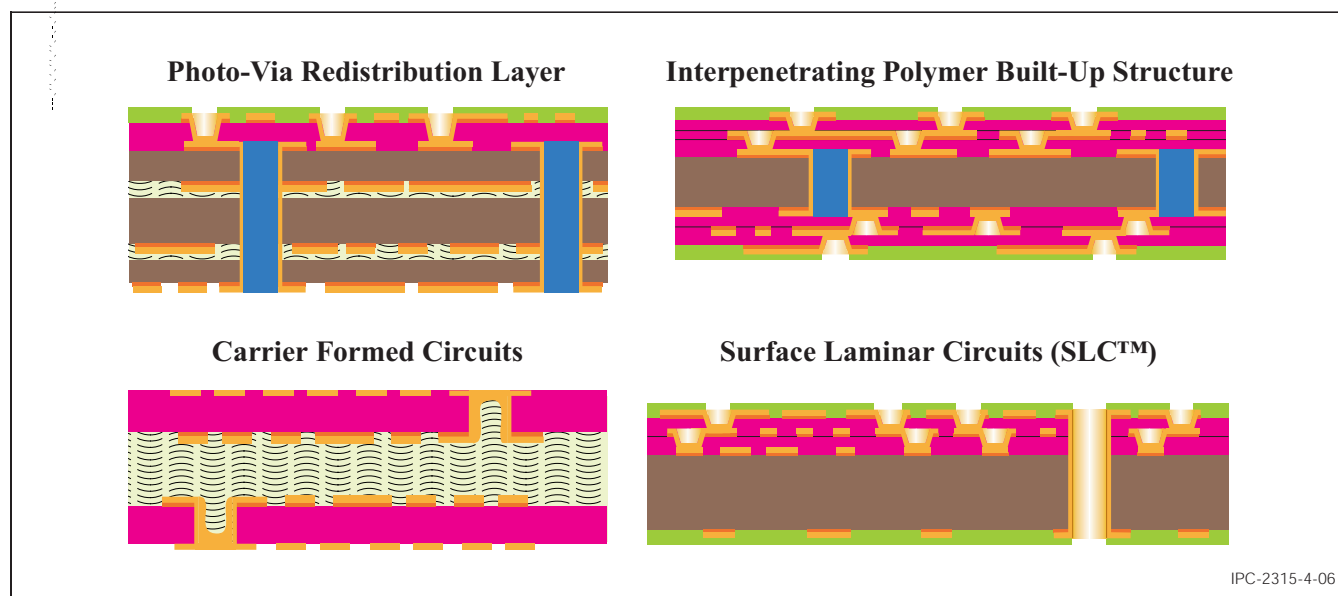


Figure 4-6 Four Commercially Produced PID Boards