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IPC/JPCA-4104

Specification for High
Density Interconnect (HDI)
and Microvia Materials

IPC/JPCA-4104

May 1999

A standard developed by IPC and JPCA

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Specification for High Density Interconnect (HDI) and Microvia Materials

Developed by the Microvia/High Density Interconnect Materials Subcommittee (D-42) of the High Density Interconnect (HDI) Committee (D-40) of IPC and the Build-Up PWB Committee of JPCA



Users of this standard are encouraged to participate in the development of future revisions.

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Foreword

IPC-4104 was developed with consideration to High Density Interconnect (HDI) layers that use modified “conventional” plated-through hole (PTH) processes and chemistries. The industry does not yet have enough experience to develop specification standards for materials used to make HDI layers. The added layers are formed by novel processes that are drastically different from “conventional” PTH constructions (i.e., non-plated copper processes). As experiences are gathered, additional specifications may be added. In the meantime, the customer and manufacturer should work together to set the criteria for acceptance of product using the new technologies.

Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Microvia/High Density Interconnect Materials Subcommittee (D-42) of the High Density Interconnect (HDI) Committee (D-40) and the Build-Up PWB Committee of JPCA are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

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Table of Contents

1 SCOPE	1	3.9.3 Mechanical Requirements of Dielectrics with Conductive Materials	15
1.1 General	1	3.10 Chemical Requirements.....	15
1.2 Designation System	1	3.10.1 Chemical Requirements of Dielectric Materials.....	15
1.2.1 Dielectric Insulator Designations	3	3.10.2 Chemical Requirements of Conductive Materials.....	15
1.2.2 Conductor Designations.....	4	3.10.3 Chemical Requirements of Dielectrics with Conductive Materials.....	16
1.2.3 Dielectric with Conductor Designations	5	3.10.4 Chemical Resistance of Dielectrics and Conductors	16
1.3 Application Levels.....	6	3.11 Electrical Requirements.....	16
2 APPLICABLE DOCUMENTS	6	3.11.1 Electrical Requirements of Dielectric Materials.....	16
2.1 IPC.....	6	3.11.2 Electrical Requirements of Conductive Materials.....	16
2.2 American Society for Testing and Materials (ASTM).....	7	3.11.3 Electrical Requirements of Dielectric with Conductive Materials.....	16
2.3 Underwriters Laboratories (UL).....	7	3.12 Environmental Requirements	17
2.4 American National Standards Institute (ANSI).....	7	3.12.1 Environmental Requirements of Dielectric Materials	17
3 REQUIREMENTS	7	3.12.2 Environmental Requirements of Conductive Materials.....	17
3.1 Terms and Definitions.....	7	3.12.3 Environmental Requirements of Dielectrics with Conductive Materials	17
3.1.1 Microvia (Build-Up Via)	7	3.13 Non-Nutrient	17
3.1.2 High Density Interconnection (HDI) (Build-Up PCB)	7	3.14 Workmanship	17
3.2 Specification Sheets	7	3.15 Material Safety Data Sheets (MSDS)	17
3.3 Manufacturer's Quality Profile.....	7	3.16 Shelf Life	17
3.4 Qualification (Characterization) Testing	7	3.17 Marking	18
3.4.1 Material Qualification	7	4 QUALITY ASSURANCE PROVISIONS	18
3.4.2 Qualification Testing Dielectric Materials	9	4.1 Quality System.....	18
3.4.3 Qualification Testing of Conductive Materials.....	9	4.2 Responsibility for Inspection.....	18
3.5 Verification of Material Supplier's Quality System	9	4.2.1 Test Equipment and Inspection Facilities	18
3.6 Conflict.....	9	4.2.2 Standard Laboratory Conditions.....	18
3.7 Materials.....	9	4.3 Qualification (Characterization) Testing	18
3.7.1 Dielectric Materials.....	10	4.3.1 Samples	18
3.7.2 Materials for Conductive Paths (In-Plane or Inter-Plane).....	10	4.3.2 Structurally Similar Construction.....	18
3.7.3 Materials with Dielectric and Conductive Functionality	10	4.3.3 Tolerances.....	18
3.8 General Acceptability	10	4.4 Quality Conformance Inspection.....	18
3.8.1 Dielectric and Conductive Materials	10	4.4.1 Frequency	18
3.8.2 Inspection Lot	11	4.4.2 Inspection of Product for Delivery	18
3.8.3 Visual Properties	11	4.4.3 Acceptance Criteria.....	18
3.8.4 Dimensional Requirements.....	13	4.4.4 Rejected Lots	18
3.9 Mechanical Requirements.....	14	4.5 Statistical Process Control (SPC)	18
3.9.1 Mechanical Requirements of Dielectric Materials.....	14		
3.9.2 Mechanical Requirements of Conductive Materials.....	15		

5 PREPARATION FOR DELIVERY	19
5.1 Packaging	19
6 NOTES	19
6.1 Ordering Data	19
6.2 References	19
APPENDIX A	20

Figures

Figure 1-1 Cross-Section of a General HDI with Microvias	2
Figure 1-2 Cross-Sectional Views of Methods to Make HDI with Microvias	2
Figure 1-3 IC Chip Carrier on HDI/Microvia Substrate (Application I)	6
Figure 1-4 BGA Package (on MCM-L Substrate Using HDI-PCB Technology) (Application I)	6
Figure 1-5 PCB-HDI/Microvia Substrate Application H)	6
Figure 3-1 Layout of Materials Section	9
Figure 3-2 Visual Properties	11
Figure 3-3 Dimensional Requirements	13

Figure 3-4 Mechanical Requirements	14
Figure 3-5 Chemical Requirements	15
Figure 3-6 Electrical Requirements	16
Figure 3-7 Environmental Requirements	17

Tables

Table 1-1 Sample Dielectric Insulator Designation	3
Table 1-2 Sample Conductor Designation	4
Table 1-3 Sample Dielectric with Conductor Designations ..	5
Table 3-1 Reference Information and Test Frequency of Materials	8
Table 3-2 Visual Inspection Criteria of Dielectrics (Maximum Allowable Points)	11
Table 3-3 Sample Point Counts for Voids and Inclusions	12
Table 3-4 Visual Inspection of Solid Conductor Material (Maximum Allowable Points)	12
Table 3-5 Point Counts for Scratches for Solid Conductor Material	12
Table 3-6 Point Count for Pin Holes & Porosity	13



Specification for High Density Interconnection (HDI) and Microvia Materials

1 SCOPE

This document describes various materials that can be used for the fabrication of high density interconnection (HDI) and microvias. It provides information on general classifications and associated characteristics of HDI materials. The document **shall** be used as a qualification and conformance standard for designers and users when designing or constructing HDI and microvias.

This document contains material designation, conformance (requirements), qualification (characterization), and quality assurance requirements. IPC-4104 should be used in conjunction with IPC-2315 and IPC-6016.

1.1 General This document covers the requirements for dielectric and conductive materials that are used with conventional core materials for the manufacture of HDI. The added HDI layer(s) is ≤ 0.15 mm in thickness.

A microvia substrate contains reduced geometries. The microvia is used to reduce size and weight and enhance electrical performance. Its nature also allows innovation in three-dimensional packaging. A microvia substrate represents the combination of multichip modules (MCM) and conventional PCB manufacturing technologies (see Figure 1-1).

Microvias are the PCB technology solution in the form of blind and buried vias ≤ 0.15 mm in diameter and pad diameters ≤ 0.35 mm. These vias are the central characteristic of HDI, as shown in Figure 1-2.

1.2 Designation System The system in 1.2.1 through 1.2.3 identifies materials used for HDI structures. This is a general identification system and does not in any way imply that all the permutations of properties and forms exist. See the series of specification sheets at the end of this document for the specific materials available. Each specification sheet outlines engineering and performance data for materials that can be used to manufacture HDI. These materials include dielectric insulators, conductors, and dielectric/conductor combinations. The specification sheets are provided with letters and numbers for identification and ordering purposes. For example, a user wishing to order from specification sheet 1 would substitute the number "1" for the "S" in the designation examples (i.e., IPC-4104/1) shown in 1.2.1 through 1.2.3. To start the ordering process, one can use the specification sheets in this document in combination with relevant IPC documents for each material sets (i.e., IPC-CF-148, IPC-MF-150, or IPC-4101).

The materials contained in this standard represent general material categories. As new materials become available, they will be added to future revisions. Users and material developers are encouraged to supply information on new materials for review by the IPC Microvia/High Density Interconnect Materials Subcommittee (D-42). Users who wish to invoke this specification for materials not listed **shall** list a zero for the specification sheet number (IPC-4104/0).

The committee may approve new or revised specification sheets independent from revision of the document text. When this occurs, the new or revised specification sheet **shall** be printed and made available through IPC-4104. The effective date of the new or revised specification sheet **shall** be clearly indicated on the individual sheet. Specification sheets **shall** be transferred from IPC-4104 to the appropriate parent document whenever that document is revised.

The designation system recognizes three general material types used in manufacturing HDI:

- Dielectric insulators only
- Conductors only
- Combinations of conductors and insulators

The first level of the designations system is the material type.

Level 1 Material Type
 IN = Dielectric Insulator
 CD = Conductor
 CI = Conductor and Insulator

The other levels used to designate a particular material depend upon Level 1. Table 1-1, Table 1-2, and Table 1-3 illustrate the designation system for each of the material types. The designation listed in the specification sheets can be used to determine the exact material construction by first looking at the Level 1 designation (IN, CD, or CI) and then looking in the correct section (1.2.1, 1.2.2, or 1.2.3) for that material type. These sections contain the description of the remaining designation levels with an example table to aid in deciphering the designation.

The default designations are non-photoimageable and unreinforced. They will not be used as descriptors for simplicity (see Table 1-1, Table 1-2, and Table 1-3).

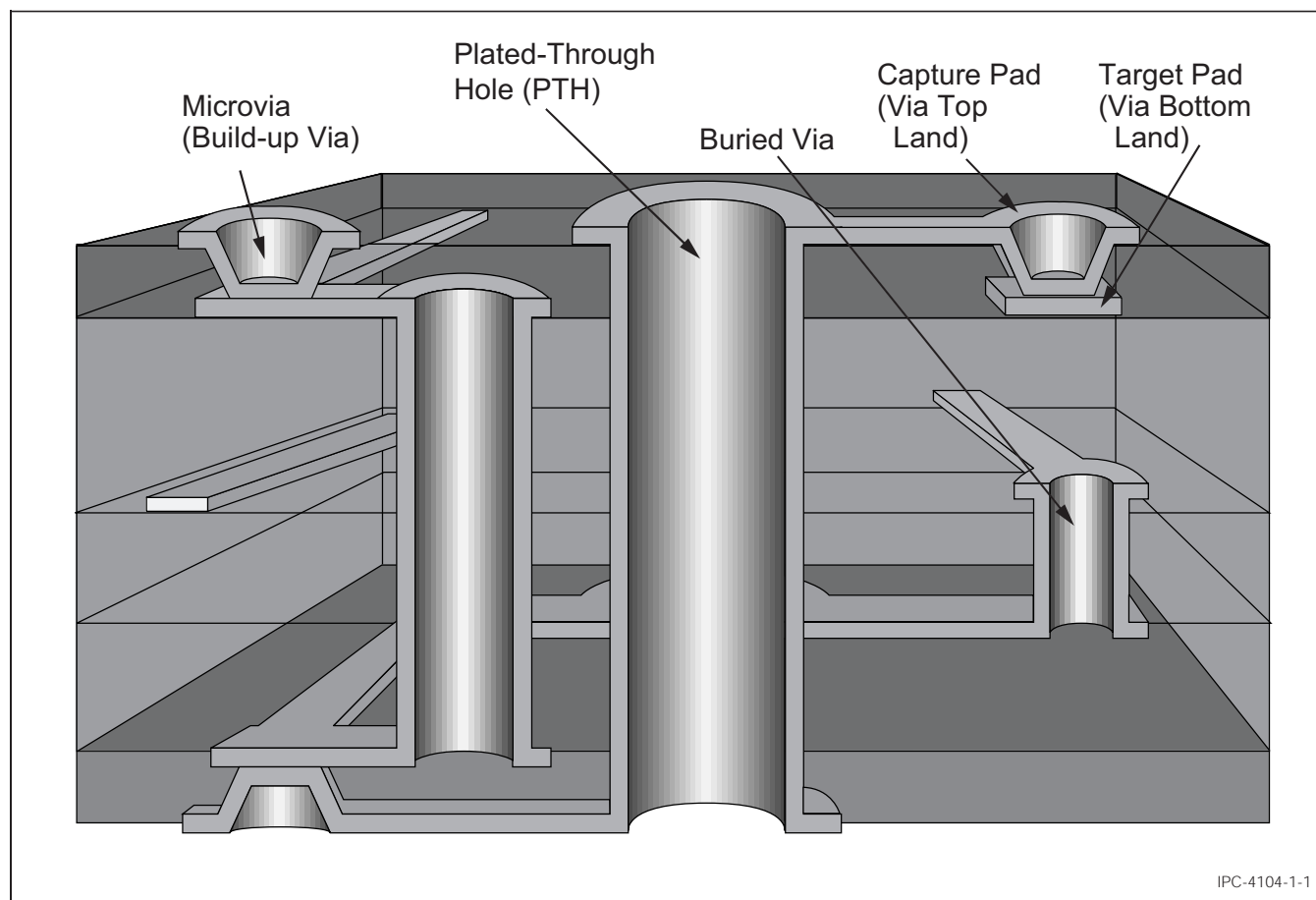


Figure 1-1 Cross-Section of a General HDI with Microvias

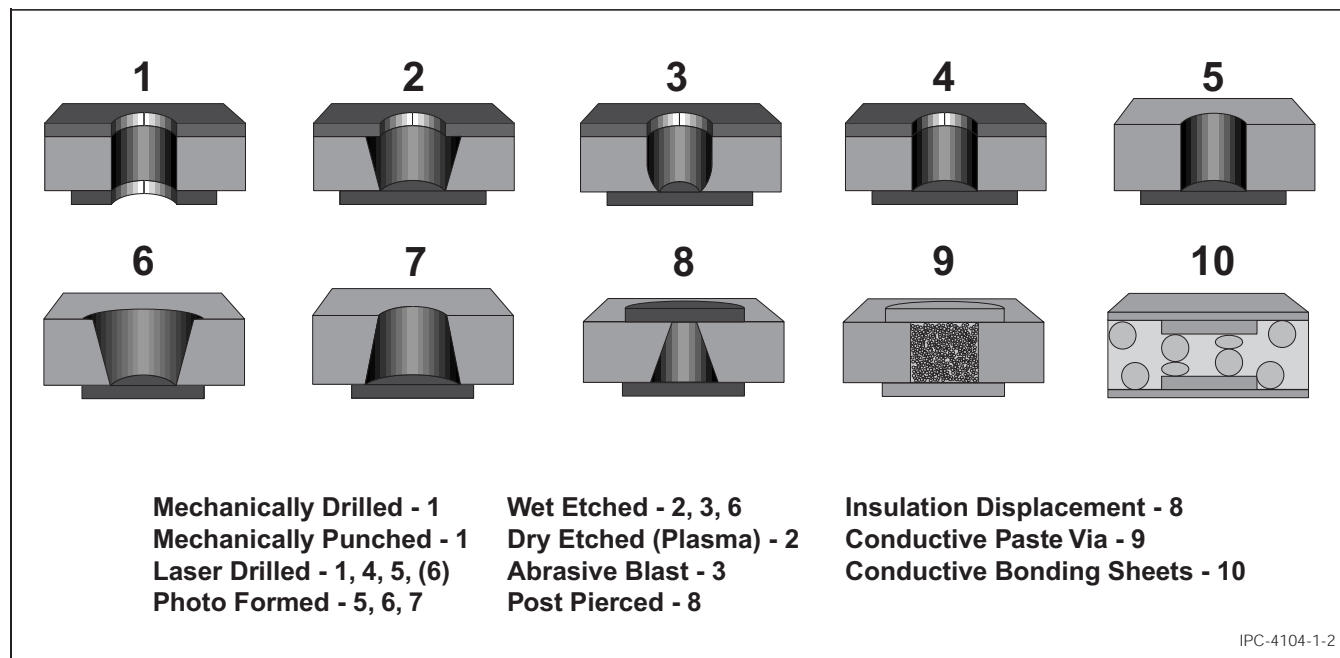


Figure 1-2 Cross-Sectional Views of Methods to Make HDI with Microvias

1.2.1 Dielectric Insulator Designations

Example The sample from Table 1-1 will be written as IN F 1 N 1.

Note The letter “X” **shall** be entered into the designation where an item is not specified and does not matter.

Table 1-1 Sample Dielectric Insulator Designation

IPC-4104	Level 1	Level 2	Level 3	Level 4	Level 5
4104 / S	IN	F	1	N	1
Where S is specification (slash) sheet number	Material Type	Form of Dielectric	Photosensitivity	Reinforcement	Chemistry

Level 1 IN = Material Type

Level 2 Form of Dielectric

L = Liquid
P = Paste
F = Film
R = Reinforced (prepreg)
C = Adhesive Coated Film

Level 3 Photosensitivity

1 = Non-photoimageable
2 = Photoimageable

Level 4 Reinforcement

G = Woven Glass
M = Nonwoven Matte Glass
A = Nonwoven Aramid
E = E-PTFE (expanded PTFE)
N = None
O = Other

Level 5 Chemistry

1 = Epoxy
2 = Epoxy blends
3 = Polyimide
4 = Polyester
5 = Acrylics
6 = BT resins
7 = Cyanate ester
8 = BCB (benzocyclobutene)
9 = PEEK (polyetheretherketone)
10 = FEP (fluorinated ethylene propylene)
11 = LCP (liquid crystal polymer)
12 = PPE (polyphenylene ether)
13 = PNB (polynorborene)
O = Other

1.2.2 Conductor Designations

Note The letter “X” shall be entered into the designation where an item is not specified and does not matter.

Table 1-2 Sample Conductor Designation

IPC-4104	Level 1	Level 2	Level 3
4104 / S	CD	P	3
Where S is specification (slash) sheet number	Material Type	Form of Conductor	Type of Form

Level 1 CD = Material Type

Level 2 Form of Conductor

F = Metal Foil

S = Solution Plate

P = Printable/Paste

V = Vacuum Deposit

O = Other

Level 3 Type of Form

1 = Copper

2 = Nickel

3 = Other

Solution Plate (S):

1 = Electrolytic Copper

2 = Electroless Copper

3 = Direct plate initiation

4 = Other metal plate

Printable Paste (P):

1 = Silver particle loaded

2 = Other conductive particle loaded

3 = Transient liquid phase sintering

4 = Organometallic

5 = Conductive polymers

Vacuum deposited (V):

1 = Evaporative

2 = Sputtering

3 = Other



1.2.3 Dielectric with Conductor Designations

Note The letter “X” shall be entered into the designation where an item is not specified and does not matter.

Table 1-3 Sample Dielectric with Conductor Designations

IPC-4104	Level 1	Level 2	Level 3	Level 4	Level 5	Level 6	Level 7
4104 / S	CI	F	1	N	1	CF	1
Where S is specification (slash) sheet number	Material Type	Form of Dielectric	Photo-sensitivity	Reinforce-ment	Chemistry	Type of metal/conductor	Type of conduction

Level 1 CI = Material Type

Level 2 Form of Dielectric

L = Liquid

P = Paste

F = Film

R = Reinforced

C = Adhesive Coated Film

Level 3 Photosensitivity

1 = Non-photoimageable

2 = Photoimageable

Level 4 Reinforcement

G = Woven Glass

M = Nonwoven Matte Glass

A = Nonwoven Aramid

E = E-PTFE (expanded PTFE)

N = None

O = Other

Level 5 Chemistry

1 = Epoxy

2 = Epoxy blends

3 = Polyimide

4 = Polyester

5 = Acrylics

6 = BT resins

7 = Cyanate ester

8 = BCB

9 = PEEK

10 = FEP

11 = LCP

12 = PPE

13 = PNB

O = Other

Level 6 Type of metal/conductor

CF = Copper foil

CP = Copper particle/post

SP = Silver particle/post

NP = Nickel particle/post

AP = Alloy particle/post

OP = Other particle/post

Level 7 Type of conduction

1 (e.g., copper foil) = In plane (x-y)

2 (anisotropic conductive adhesive)

= Through plane (z-axis)

3 (e.g., post) = Both

1.3 Application Levels All applications for microvias require high reliability. This includes equipment where continued performance is critical, equipment downtime cannot be tolerated, or the equipment is a life support item.

The application levels used in IPC-4104 slash sheets are:

H – Printed Circuit Board/ High Density Interconnect Applications (see Figure 1-3)

I – Integrated Circuit Packaging Applications (see Figure 1-4 and Figure 1-5)

U – User Defined Applications

Application level H (see Figure 1-3) does not require moisture resistance of PCB materials testing (see IPC-TM-650, Method 2.6.16.1). Application level I (see Figure 1-4 and Figure 1-5) does not require Relative Thermal Index testing (see UL 796). User defined applications are just like application levels H or I, except the exact values and slash sheets are not defined. The values for application level U will be agreed upon between user and supplier.

The intended application level is listed on each slash sheet. Certain materials may have more than one application level.

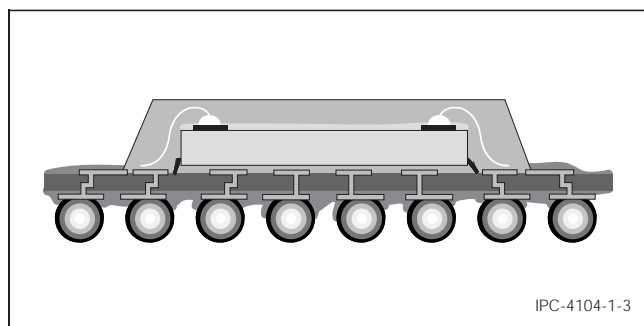


Figure 1-3 IC Chip Carrier on HDI/Microvia Substrate (Application I)

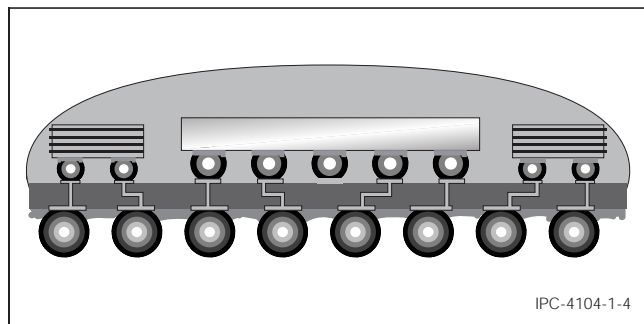


Figure 1-4 BGA Package (on MCM-L Substrate Using HDI-PCB Technology) (Application I)

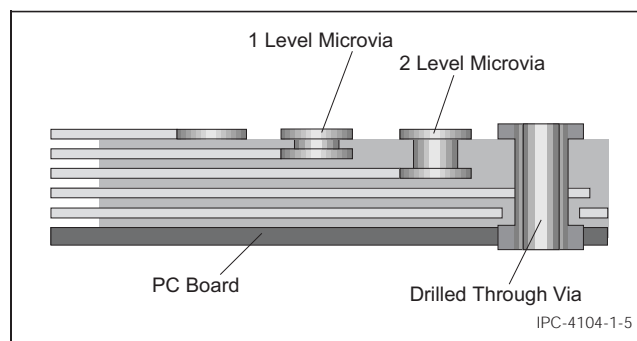


Figure 1-5 PCB-HDI/Microvia Substrate (Application H)

2 APPLICABLE DOCUMENTS

The following documents of the issue in effect at the time of order form a part of this specification to the extent specified herein. If a conflict exists between IPC-4104 and the listed applicable documents, IPC-4104 **shall** take precedence.

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-PC-90 General Requirements for Implementation of Statistical Process Control

IPC-MF-150 Metal Foil for Printed Wiring Applications

IPC-TM-650 Test Methods Manual

- 2.1.2 Pinholes Evaluation, Dye Penetration Method
- 2.2.21 Planarity of Dielectrics for High Density Interconnection (HDI)/Microvia Technology
- 2.3.2 Chemical Resistance of Flexible Printed Wiring Materials
- 2.4.18.3 Tensile Strength, Elongation, and Modulus
- 2.4.24.4 Glass Transition and Modulus of Materials Used in High Density Interconnection (HDI) and Microvias - DMA Method
- 2.4.24.5 Glass Transition Temperature and Thermal Expansion of Materials Used in High Density Interconnection (HDI) and Microvias - TMA Method
- 2.4.25 Glass Transition Temperature and Cure Factor by DSC
- 2.5.5.9 Permittivity and Loss Tangent, Parallel Plate, 1 MHz to 1.5 GHz
- 2.5.6.1 Dielectric Strength, Polymer Solder Mask, and/or Conformal Coatings
- 2.5.17.1 Volume and Surface Resistivity of Dielectric Materials

1. IPC, 2215 Sanders Rd., Northbrook, IL 60062-6135, 847-509-9700, www.ipc.org

- 2.5.17.2 Volume Resistivity of Conductive Materials Used in High Density Interconnection (HDI) and Microvias, Two-Wire Method
- 2.6.1 Fungus Resistance Printed Wiring Materials
- 2.6.2.1 Water Absorption, Metal Clad Plastic Laminates
- 2.6.16.1 Moisture Resistance of High Density Interconnection (HDI) Materials Under High Temperature and Pressure (Pressure Vessel)

IPC-2315 Design Guide for High Density Interconnects (HDI) and Microvias

IPC-4101 Specification for Base Materials for Rigid and Multilayer Printed Boards

IPC-6016 Qualification and Performance Specification for High Density Interconnection (HDI) Layers or Boards

2.2 American Society for Testing and Materials (ASTM)²

ASTM-D-374 Test Methods for Thickness of Solid Electrical Insulation

2.3 Underwriters Laboratories (UL)³

UL 94 Standard Tests for Flammability of Plastic Materials for Parts in Devices and Appliances

UL 796 Printed Wiring Boards

2.4 American National Standards Institute (ANSI)⁴

ANSI/NCSS Z540-1-1994

ISO 10012-1 Quality Assurance Requirements for Measuring Equipment

3 REQUIREMENTS

3.1 Terms and Definitions Terms and definitions **shall** be in accordance with IPC-T-50 and as stated in 3.1.1 and 3.1.2.

3.1.1 Microvia (Build-Up Via) Blind and buried vias that are ≤ 0.15 mm in diameter and have pad diameters that are ≤ 0.35 mm.

3.1.2 High Density Interconnection (HDI) (Build-Up PCB) A HDI substrate contains reduced geometries. The HDI is used to reduce size and weight and to enhance electrical performance. Its nature also allows innovation in three-dimensional packaging. A HDI substrate represents the combination of multi-chip modules (MCM) and con-

ventional printed circuit board (PCB) manufacturing technologies.

3.2 Specification Sheets The individual item requirements **shall** be as specified herein and in accordance with the applicable specification sheets. Where there is no specification sheet available, the individual requirements **shall** be as specified in complementary documents such as master drawings or ordering data sheets (see 6.1). In the event of any conflict between requirements of this specification and the specification sheet or complementary documents, the latter **shall** govern.

3.3 Manufacturer's Quality Profile Suppliers of dielectric and conductive materials **shall** assess their manufacturing capability and make such data available either electronically or in hard copy.

3.4 Qualification (Characterization) Testing Dielectric and conductive materials furnished under this specification **shall** be qualified as in Table 3-1. The supplier **shall** retain on file data that support that the material meets the requirements of this specification using the test methods described herein. Qualification testing **shall** be performed to demonstrate the supplier's ability to meet all of the requirements of each applicable specification sheet for each dielectric and conductive material.

Qualification is synonymous with characterization testing of materials and is done one time to verify material properties (conformance is synonymous with requirement).

3.4.1 Material Qualification Material qualification **shall** be performed on test specimens that are produced with equipment and procedures normally used in production or in accordance with the test method procedure indicated. Material characterization provides the material supplier with a method to specify the characteristics of their products, which may be useful for the PCB fabricator, designer or end user to know. This group of tests is typically performed by the material supplier a single time and reported on the specification sheets. The PCB fabricator and/or end user may also utilize this group of tests, if desired.

3.4.1.1 Samples When required under the provisions of Table 3-1, samples **shall** be selected from normal production for each material for which qualification is sought. The number of samples required for the individual test methods **shall** be as specified in the test method or as outlined in 3.8 through 3.12.3.

2. ASTM, 100 Barr Harbor Dr., West Conshohocken, PA 19428-2959

3. UL, 333 Pfingsten Rd., Northbrook, IL 60062-2002

4. ANSI, 655 15th St., N.W., Ste. 300, Washington, D.C. 20005-5794

Table 3-1 Reference Information and Test Frequency of Materials

Properties	Section	Test Method (IPC-TM-650 or as noted)	Qualification Testing	Conformance Testing	Frequency	Samples per unit/measure
Visual	3.8.3					
Inclusions	3.8.3.1.1 3.8.3.2.2			✓	A	3
Holes and Tears	3.8.3.2.3			✓		
Voids (Surface)	3.8.3.1.2			✓	A	3
Wrinkles, Creases & Indentations	3.8.3.1.3			✓	A	3
Scratches	3.8.3.2.1					
Tears and Delaminations	3.8.3.1.4 3.8.3.2.3			✓	A	3
Dimensional	3.8.4			✓	A	3
Thickness	3.8.4.1.1			✓	A	3
Length and Width	3.8.4.1.2			✓	A	3
Weight	3.8.4.2.1			✓	A	3
Mechanical Requirements	3.9					
Tensile Strength	3.9.1.1, 3.9.2.1	2.4.18.3	✓		C	per TM
Elongation	3.9.1.2 3.9.2.2	2.4.18.3	✓		C	per TM
Young's Modulus	3.9.1.3 3.9.2.3	2.4.18.3 or 2.4.24.4	✓		C	per TM
Planarity	3.9.1.4	2.2.21	✓		C	per TM
Glass Transition Temperature (T_g)	3.9.1.5 3.9.2.4	2.4.24.4, 2.4.24.5, or 2.4.25	✓		C	per TM
CTE Above and Below T_g	3.9.1.6 3.9.2.5	2.4.24.5	✓		C	per TM
Chemical Requirements	3.10					
Flammability	3.10.1.1	UL 94	✓		C	per TM
Relative Thermal Index (RTI) ⁵	3.10.1.2	UL 796	✓		C	per TM
Electrical Requirements	3.11					
Dielectric Constant (Relative Permittivity and Range)	3.11.1.1	2.5.5.9		✓	B	per TM
Loss Tangent and Range	3.11.1.2	2.5.5.9		✓	B	per TM
Dielectric Strength	3.11.1.3	2.5.6.1		✓	B	per TM
Bulk or Volume Resistivity	3.11.2.1	2.5.17.2		✓	B	per TM
Environmental Requirements	3.12					
Surface Resistivity	3.12.1.1	2.5.17.1		✓	B	per TM
Volume Resistivity	3.12.1.2	2.5.17.1		✓	B	per TM
Moisture Resistance by Pressure Vessel Test	3.12.1.3 3.12.2.1	2.6.16.1		✓	B	per TM
Moisture and Water Absorption	3.12.1.4 3.12.2.2	2.6.2.1	✓		C	per TM

A = Lot basis

B = Every 12 months

C = One time for material qualification

For an explanation of frequency indicators, see 4.4.

5. RTI requirements can be exempt for applications intended for use in low voltage limited energy (LVLE) circuitry (see UL 796).



3.4.1.2 Frequency Each material (as outlined in the specification sheets) **shall** undergo qualification once. The material supplier upon demand **shall** provide certified data that the supplied material is qualified to this standard. Qualification retesting is not required unless agreed upon between end user and material supplier or as specified in Table 3-1.

3.4.1.3 Production Board Qualification Assessment of Materials Production board system qualification is the responsibility of the PCB fabricator and/or end user to confirm that the materials, production board system, and production process chosen is qualified for the appropriate application level. This qualification can use test vehicles from IPC-6016 or a substitute pattern agreed upon by the printed board fabricator and user, which are evaluated according to tests listed in Table 3-1.

3.4.2 Qualification Testing Dielectric Materials The specification sheets referenced herein are designed to provide the designer and end user with information that will allow selection of suitable materials for specific products. Definitions of characterization testing included in the specification sheet information but are not a requirement for routine conformance testing are explained in 3.8 through 3.12.

3.4.3 Qualification Testing of Conductive Materials The specification sheets referenced herein are designed to provide the designer and end user with information that

will allow selection of suitable materials for specific products. This section defines the characterization testing that is included in the specification sheet information but is not a requirement for routine conformance testing.

For solid metal conductive material, characterization testing such as 3.9.2.4 and 3.12.2.1 are not applicable. For applied conductive materials, (i.e., plated, vacuum deposited, conductive paste), material characterization in 3.9.2.1, 3.9.2.2, 3.9.2.3, 3.9.2.4, and 3.10.1.2 may not be applicable, depending on the specific material.

3.5 Verification of Material Supplier's Quality System

The verification of the material supplier's quality system may be conducted to reduce risk to the PCB fabricator. The verification can be accomplished via several means, including internal assessment, individual customer audit, and/or end user assessment.

3.6 Conflict In the event of conflict, the following order of precedence **shall** apply:

1. Purchase order as agreed upon between PCB fabricator and material supplier
2. Master drawing (see 6.1)
3. This specification (specification sheet takes precedence over the body of the text)
4. Applicable documents (see Section 2)

3.7 Materials The type of materials **shall** be specified as stated in 3.7.1 through 3.7.3.3. See Figure 3-1 for a layout of 3.7.

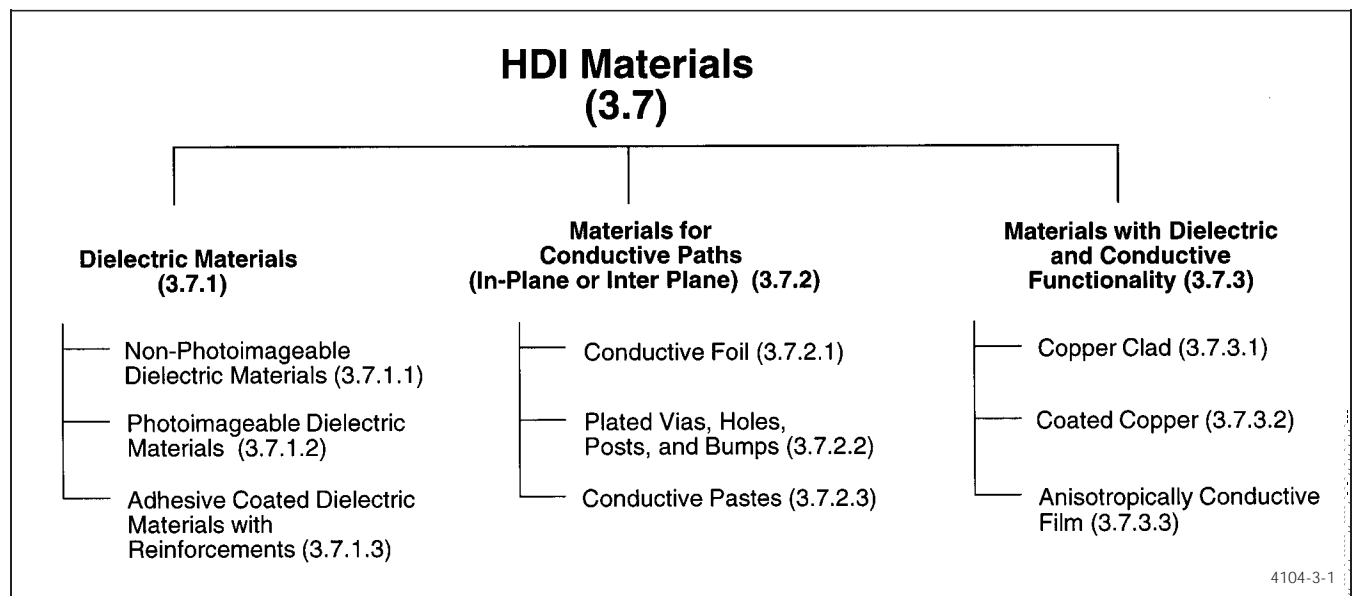


Figure 3-1 Layout of Materials Section

3.7.1 Dielectric Materials

3.7.1.1 Non-Photoimageable Dielectric Materials Non-photoimageable materials are typically supplied as a liquid, paste, or dry film non-reinforced dielectric, which is applied to the sub-composite to form an insulating layer in a build-up circuit at the PCB manufacturing location. These dielectrics are suitable for via formation by LASER or mechanical methods. Some of these materials are used to fill the core board through hole to achieve planarization.

Material chemistries for this application include epoxies, epoxy blends, polyester, polynorborenes, polyimides, etc.

3.7.1.2 Photoimageable Dielectric Materials Photoimageable materials are typically supplied as a liquid, paste, or dry film non-reinforced dielectric, which is applied to the sub-composite to form an insulating layer in a build-up circuit at the PCB manufacturing location. These dielectrics have the capability of forming vias by photographically defined processes. Some of these materials may also be used to fill the core board through hole to achieve planarization. Material chemistries for this application include epoxies, epoxy blends, polynorborenes, polyimides, etc.

3.7.1.3 Adhesive Coated Dielectric Materials with Reinforcements These materials act as an insulator and provide the bond-ply required to adhere copper foil to the surface of a sub-composite. Vias are formed utilizing methods such as plasma, LASER, or mechanical drilling. Materials available differ by reinforcement (i.e., woven glass, nonwoven glass, aramid, film, expanded PTFE, etc.) and chemistries involved (i.e., epoxies, polyimides, cyanate esters, acrylics, etc.).

3.7.2 Materials for Conductive Paths (In-Plane or Inter-Plane)

3.7.2.1 Conductive Foil Conductive foils are comprised of foil that is either laminated with dielectric, coated with dielectric, or used as stand alone and then laminated into the structure. Foil materials are mostly copper, although other metals are possible. For more information, see IPC-MF-150.

3.7.2.2 Plated Vias, Holes, Posts, and Bumps These materials include various applied conductive materials that are plated (electroless and electrolytic) in vias or as bumps or posts on top of other circuitry to make the electrical connection between layers. Plated materials are mostly copper, although other plating is possible.

3.7.2.3 Conductive Paste Conductive pastes are pastes applied into vias that are photoimaged, LASER ablated, plasma formed, or formed by other means in any of the dielectric materials in 3.7.1. Some of these materials may

be used to fill the core board through hole to achieve conduction and planarity. They differ by the material that is responsible for electrical conduction. They include silver particle loaded, other metal or metal-coated particles, transient liquid phase sintering compositions, organometallics, and conductive polymers.

3.7.3 Materials with Dielectric and Conductive Functionality

3.7.3.1 Copper Clad Copper clad materials have copper foil laminated on one or both sides of cured (c-stage) dielectric. The typical application uses single-side clad material where the copper clad is used as the outer layer and the c-stage is bonded to the sub-composite. Vias are formed utilizing methods such as plasma, LASER, or mechanical drilling. Materials available differ by reinforcement (woven glass, nonwoven glass, aramid, film, and expanded PTFE) and chemistries involved (epoxies, polyimides, cyanate esters, acrylics, liquid crystal polymers, etc.).

3.7.3.2 Coated Copper Coated copper materials are comprised of copper foil coated with a dielectric material that can be directly bonded to the sub-composite. They differ by whether they are wet processable or not. In wet processable coated copper, the vias are formed by acidic or alkaline etching, or the dielectric may be made etchable by photographic definition. In non-wet processable-coated copper materials, vias are formed utilizing methods such as plasma, LASER, or mechanical drilling. The materials coated are typically epoxy, polyimide, or acrylic.

3.7.3.3 Anisotropically Conductive Film These materials are conductive in the z-axis and are applied as bond-ply in between circuit layers to form the vertical electrical connection. They differ by the material (silver, nickel, alloy, or other metals or metal-coated particles) that is responsible for electrical conduction.

3.8 General Acceptability Materials in paste, sheet, roll, or liquid **shall** be considered acceptable if they meet the requirements of 3.8.1 through 3.8.4.2.1 or are as agreed upon between user and supplier.

3.8.1 Dielectric and Conductive Materials

3.8.1.1 General Acceptability of Dielectric Materials Dielectric material property qualification and conformance are required to be performed by the material supplier but may, by appropriate agreement, also be used as an incoming material inspection procedure by the PCB user. The tests the supplier **shall** perform to determine the properties of each material are outlined in 3.8.3.1, 3.8.4.1, 3.9.1, 3.10.1, 3.11.1, and 3.12.1. A summary of the tests is