

IPC J-STD-003C
Amendment 1
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JOINT INDUSTRY STANDARD

Solderability Tests for Printed Boards

Amendment 1



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- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

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- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

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Solderability Tests for Printed Boards

Global Replacements:

Replace “circuit board” with “printed board”

Replace “vendor” with “supplier”

Beginning with 1.3:

Replace “plated-through hole” with “PTH”

Replace “plated-through holes” with “PTHs”

Beginning with 1.3.2:

Replace “as agreed between user and supplier” with “AABUS”

1.1 Scope

Replace as follows:

1.1 Scope This standard prescribes test methods, defect definitions, and illustrations for assessing the solderability of printed wiring board surface conductors, attachment lands, and plated-through holes (PTHs). This standard is intended for use by both user and supplier.

This standard is not intended to verify the potential of successful processing at assembly or to evaluate design impact on wettability. This standard describes procedures or methods to determine the acceptable wettability of a surface finish. Wettability can be affected by handling, finish application, and environmental conditions.

1.4 Classification

Replace “specification” with “standard” in the final paragraph as follows:

This standard relies on input from the 4-14 plating process subcommittee and the 4500 series of printed board surface finish documents generated in that subcommittee to determine the durability rating potential for each specified finish. This document and the appropriate 4500 series document should be considered complimentary to one another.

1.5 Test Method Classification

Insert new first paragraph, 2nd sentence as follows:

This standard describes test methods by which the surface conductors, attachment lands, and PTHs may be evaluated for solderability. Edge Dip, Wave Solder, Surface Mount Simulation, and Wetting Balance testing can be used for both tin-lead (SnPb) and SAC 305 alloys. Other Pb-free alloys may be used for testing AABUS.

Replace within the last paragraph as follows:

The following tests are considered destructive tests. Tested printed boards should not be used in further production steps.

Table 1-1 Solderability Test Method Selection

Insert new rows "Solder Float Test – 'M' coupon" and replace appropriate Table 1-1 sections and notes as follows:

Test Method	Surface Finish	Pre-Conditioning Default	Alternative Conditioning	Applies to Surface Features	Plated Through Holes
Edge dip test	Pb-Containing	Steam exposure ^a	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes	NA
	All other	8 hours (3.4.2) ^b	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes	NA
Wave solder	Pb-Containing	Steam exposure ^a	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes (solder source side only)	Yes
	All other	8 hours (3.4.2) ^b	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes (solder source side only)	Yes
Surface mount simulation	Pb-Containing	Steam exposure ^a	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes	NA
	All other	8 hours (3.4.2) ^b	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes	NA
Solder float test ("S" coupon or referee coupon) (compliance to IPC-6010 series only)	Pb-Containing	NA	NA	NA	Yes
	All other	NA	NA	NA	Yes
Solder float test ("M" coupon or referee coupon) (compliance to IPC-6010 series only)	Pb-Containing	Steam exposure ^a	NA	Yes	NA
	All other	8 hours (3.4.2) ^b	NA	Yes	NA
Tests with Force Measurement Criteria (refer to 1.5.2)					
Wetting balance	Pb-Containing	Steam exposure ^a	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes	NA
	All other	8 hours (3.4.2) ^b	Reflow Simulation 2X (3.4.2) ^{b,c}	Yes	NA

The use of the preconditioning stressing **shall** be restricted to the following:

- Eight hours of steam exposure precondition for Pb-bearing surface finish requirements only. The requirements should be listed in the procurement documentation.
- PBs that are less than eight weeks older than the date code on the lot, unless AABUS. Pb-containing surface finishes are HASL and reflowed plated SnPb. All other surface finished currently include; ENIG, ENEPIG, I Ag, I Sn, OSP, Pb-Free HAL, Electroless Pd, Immersion Pd, Electrolytic NiAu, and Electroless Au.
- "Reflow Simulation 2X" means two excursions through the reflow oven using one of the profiles defined in IPC-TM-650, 2.6.27.

1.8 Coating Durability – SnPb Containing (HASL and Plated and Reflowed SnPb) Surface Finishes

Replace the first sentence as follows:

Shelf life criteria are applicable only to surface finishes that contain SnPb.

Table 1-2 Final Finish Conditioning/ Stress Testing for Category 3 Durability

Replace the table title and add note "a" as follows:

Table 1-2 Final Finish Conditioning/ Stress Testing for Category 3 Coating Durability^a

- "Reflow Simulation 2X" means two excursions through the reflow oven using one of the profiles defined in IPC-TM-650, 2.6.27.

1.9 Coating Durability – Non-SnPb Surface Finishes

Replace the 2nd paragraph as follows:

The robustness of the surface finish **shall** be defined in the appropriate IPC-4500 series document. It is noted that the 4-14 Plating Process Subcommittee usually specifies the surface finish for maximum coating durability and robustness as the default, with some exceptions. Stressing of surface finishes prior to solderability testing is used to provide a determination of robustness of the finish that may be used to evaluate the quality of a surface finish. Furthermore, stressing of the finish can help evaluate the likelihood for assembly related issues with multiple thermal excursions and/or complex assembly processes. It may also be used to compare the performance of similar surface finishes from different suppliers. Exposure to the stressing protocols is not intended to predict shelf life of a surface finish. It may be inferred that successful testing of a surface finish post stressing and stored according to the manufacturers recommendations should allow the surface finish to meet industry requirements for one year of shelf life unless otherwise stated in an appropriate IPC-4500 series document. Coating Durability A is considered the default condition.

Coating Durability B:

Add the following:

Coating Durability B: Intended for boards likely to experience multiple soldering processes and/or other process steps using SnPb or Pb-free assembly profiles when defined in the procurement documentation.

Insert Fahrenheit conversion as follows:

Following stressing in humidity and/or steam exposure as appropriate, the boards **shall** be baked for 1 hour at 105 °C [221 °F] prior to testing.

Requirement Post Stressing:

Delete letter “e”:

Requirement Post Stressing:

- a. **For the Edge Dip Test A:** Each and every feature to exhibit wetting with the minimum of 95% of each feature showing uniform smooth coverage. All holes **shall** show evidence of wetting.
- b. **For the Wave Solder Test:** All SMT pads on the wave side of the board and holes **shall** wet and fill and meet the requirements of the test.
- c. **For the Surface Mount Simulation Test:** Where paste is applied, there **shall** be evidence of at least 95% of each pad wetting.
- d. **For the Wetting Balance Test:** There **shall** be evidence of positive wetting with an allowable increase in wetting time of 2X that of the non-stressed samples. The final wetting force **shall** be at least 70% that of the non-stressed samples.