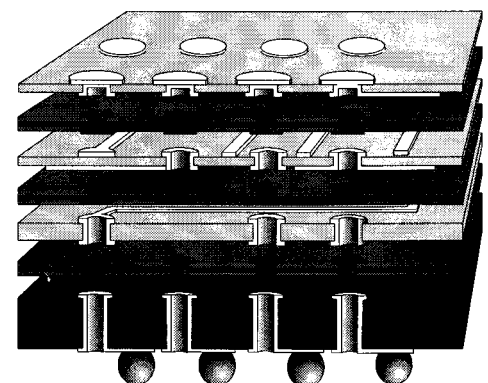
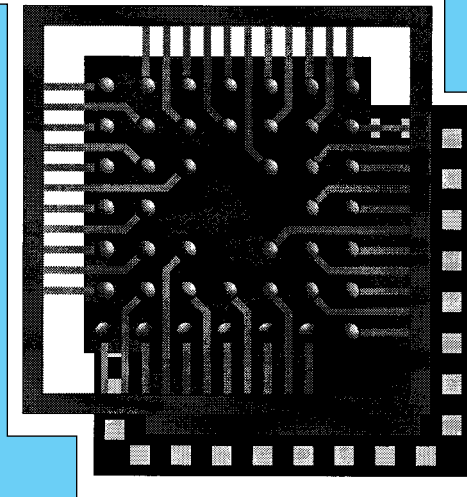
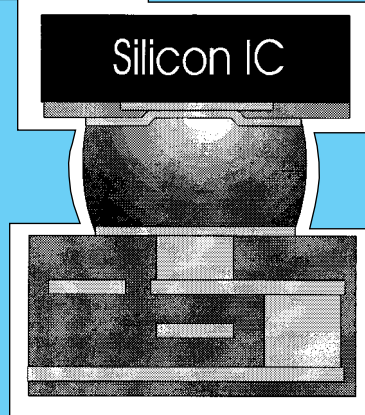
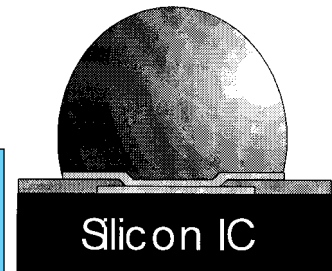
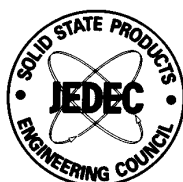


JOINT INDUSTRY STANDARD

IMPLEMENTATION OF FLIP CHIP AND CHIP SCALE TECHNOLOGY



COORDINATED BY THE SURFACE MOUNT COUNCIL



Material in this standard was voluntarily coordinated by the Surface Mount Council (SMC), and established by Technical Committees of IPC, EIA and JEDEC. Committee members of the three organizations contributed their time, knowledge and expertise to blend a cohesive report on the topic covered by this document. Representatives from Sematech and MCNC also participated and contributed to the development of this document. Proposals were sent to key individuals in each of the individual standard development organizations for consensus. Meetings were held to resolve differences or conflicts prior to documenting the information in the final released version.

The material contained herein is advisory and its use or adaptation is entirely voluntary. IPC, EIA and JEDEC disclaim all liability of any kind as to the use, application, or adaptation of this material. Users are also wholly responsible for protecting themselves against all claims or liabilities for patent infringement.

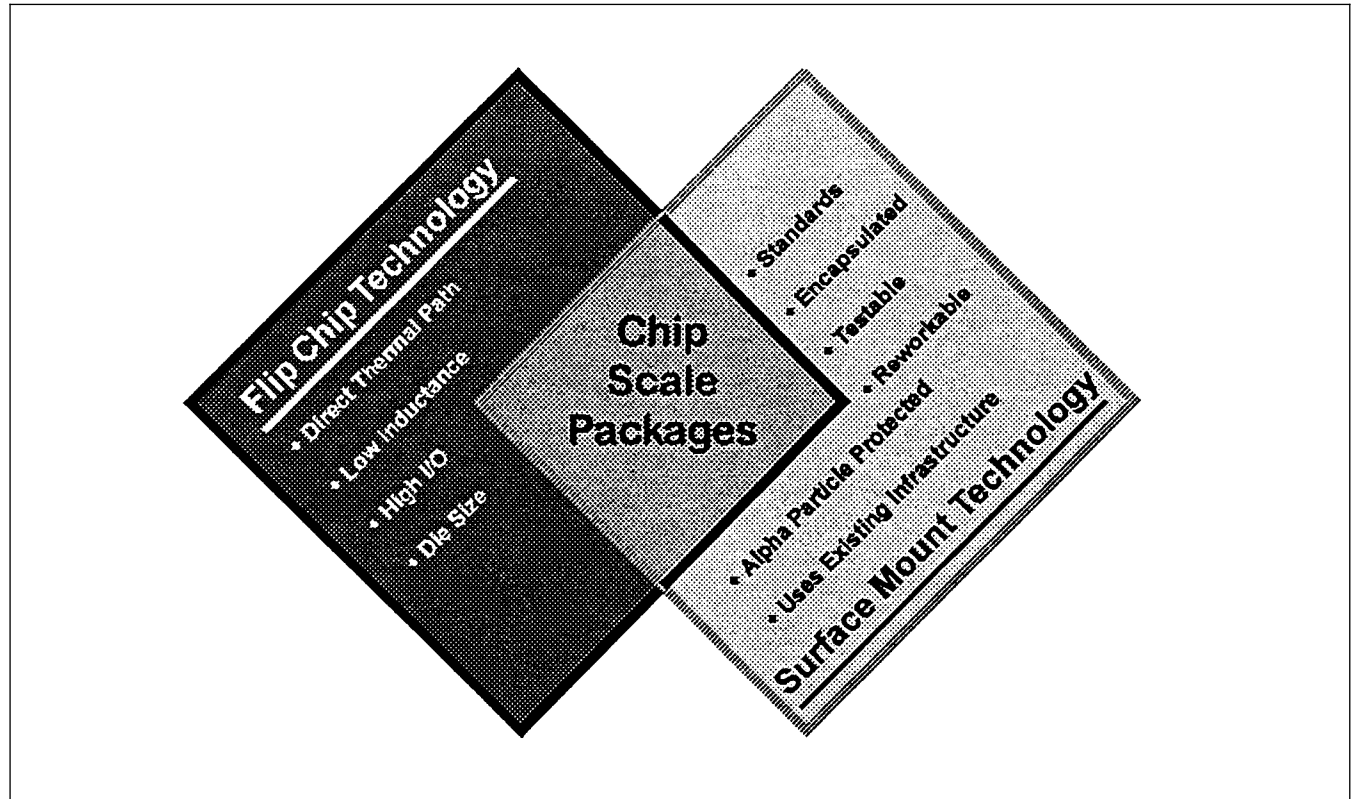
Comments Welcome

The J-STD-012 is intended to serve as a roadmap for flip chip and chip scale implementation.

In order to keep the document current, the Surface Mount Council welcomes comments from individuals reading the document, or implementing the suggested concepts.

Comments may be sent to the EIA, IPC or JEDEC. All comments will be organized and sent to representatives of the Ad Hoc Committee for a yearly review and updating procedures.

J-STD-012 IMPLEMENTATION OF FLIP CHIP AND CHIP SCALE TECHNOLOGY



About this Document

This document is intended to report on the work being done by a variety of organizations concerned with surface mounting of bare die in flip chip or chip scale configurations. The details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Section 10 of the document represents a listing of standards that are being developed, being updated, or need to be created in order to provide for the orderly implementation of flip chip or chip scale technology. Members of industry are invited to participate in the ongoing standardization process.

For additional information regarding material published herein or inquiries regarding the status of standardization activities, we urge you to contact the organization listed below.

IPC
**The Institute for Interconnecting
and Packaging Electronic Circuits**
2215 Sanders Road
Northbrook, IL 60062-6135
Telephone: (847) 509-9700
Fax: (847) 509-9798

EIA
Electronic Industries Association
2500 Wilson Blvd.
Arlington, VA 22201-3834
Telephone: (703) 907-7552
FAX: (703) 907-7501

JEDEC
**Joint Electron Device
Engineering Council**
2500 Wilson Blvd.
Arlington, VA 22201-3834
Telephone: (703) 907-7560
Fax: (703) 907-7501

Acknowledgment

In response to the need for a document covering flip chip and chip scale technology, J-STD-012 was developed. Because EIA, IPC, and JEDEC have members worldwide who participated in this effort, J-STD-012 represents a comprehensive report on the subject of flip chip and chip scale design rules. While the principal members of the Task Group are listed below, a special note of thanks goes to everyone who assisted in the development of this document.

Abbas I. Attarwala, Hewlett Packard
 Walt Ackerman, Universal
 Bernie Aronson, EIA
 Pamela Ashcraft, Delco Electronics
 Mark Baker, National Semiconductor
 Roger Benson, Grace Specialty Polymers
 Dieter Bergman, IPC
 Ruben Bergman, HDP User Group
 Rao Bonda, Motorola
 Kimera Cho, Rockwell International
 Dave Corisis, Micron Technology
 Richard Cooley, AMKOR Electronics
 Brian Conaghan, DuPont
 Ben Cranston, AT&T Bell Labs
 Philip Deane, MCNC
 Keith DeHaven, Motorola
 Werner Englemaier, Englemaier Associates
 Joe Fjelstad, Tessera
 Garry Green, Cypress Semi Conductor
 Bill Hargis, Coors Electronic Packaging Co.
 Matthew Heydinger, Hewlett-Packard
 Gary Hill, IBM
 John Jackson, Sematech
 Donald Johnson, Sandia National Labs
 William Kenyon, Global Center for
 Process Change

Mohan Kirloskar, Shinko
 Young Kwon, Philips Semiconductor
 Helen M. Low, Celestica
 Nick Lycoudes, Motorola
 Rob Lyn, Celestica (IBM Canada Sub.)
 Alan Lyons, AT&T Bell Laboratories
 Susan Mack, Delco Electronics
 Paul A. Magill, MCNC
 Phil Marcoux, Chip Scale Inc.
 Charles Martin, Hewlett Packard
 Mark McLeod, IBM
 Kevin Moody, Hewlett Packard
 Archie Mones, E.I. DuPont
 Charles Pagel, NSWC-CRANE
 Tze W. Poon, Sematech
 David Read, NIST
 Cathy Reber, Sandia National Labs
 Glenn Rinne, MCNC
 Ray Rinne, IBM
 Paul Roeder, Universal Instruments
 Paul Totta, IBM East Fishkill
 Iwona Turlik, Motorola
 Dan Ward, Delco Electronics
 David Wright, NSWC - Crane Division
 Frank S. Stein - Consultant
 James Young, Chip Scale Inc.

A special note of thanks goes to the representatives of MCNC, who hosted several of the meetings during which this document was developed. Also a word of appreciation to Bernie Aronson, EIA, and Joe Fjelstad, Tessera, for their participation in the special Ad Hoc Committee that assembled the input for this document.

The IPC is also grateful to representatives of IBM and Motorola, who provided information on design of flip chip assemblies for incorporation into this document.

Table of Contents

1 SCOPE	1	4.5.1	Final Metal Reticle Mask.....	30
1.1 Purpose.....	1	4.5.2	Passivation (Terminal Via) Reticle Mask and Plan	30
1.2 Categorization	1	4.5.3	Unit Cell Design.....	30
2 TECHNOLOGY OVERVIEW	1	4.5.4	Printed Board Land Pattern Design	30
2.1 History of Flip Chip	1	4.6	Electrical Design.....	30
2.1.1 Hybrid Thick Film Packages	3	4.6.1	Equivalent Circuitry.....	30
2.1.2 Hybrid Thin Film Packages.....	4	4.6.2	Final Metal Traces	31
2.1.3 Multilayer Ceramic Substrate (MLC)	4	4.6.3	Inductance and Capacitance	34
2.1.4 Thin Film on Multilayer Ceramic.....	5	4.6.4	High Frequency Performance.....	34
2.1.5 Thin Film on Organic Epoxy/Glass Laminate....	5	4.7	Thermal Design.....	34
2.1.6 Chip on Flexible Printed Board	5	4.7.1	Bump Interconnect Thermal Model.....	35
2.1.7 Thin Film on Silicon	5	5 MATERIAL PROPERTIES AND PROCESSES		37
2.1.8 Characteristics of Flip Chip Technology	6	5.1	Solder Bumping	37
2.2 Introduction to Chip Scale Packaging	7	5.1.1	Solder Evaporation	37
2.2.1 Chip Scale Grid Array Packages.....	9	5.1.2	Solder Electroplating	37
2.2.2 Peripheral Leaded Chip Scale Packages (CSP-P)	13	5.1.3	Solder Paste Deposition.....	38
2.2.3 Advantages and Disadvantages of Chip Scale Technology	14	5.1.4	Conductive Paste Method.....	38
3 APPLICATIONS OF FLIP CHIP AND CHIP SCALE	16	5.2	Conductive Adhesives.....	38
4.0 DESIGN CONSIDERATIONS	17	5.2.1	Design Issues	39
4.1 Chip Size Standardization	17	5.2.2	Anisotropic Adhesive Details	40
4.1.1 Bump Site Standards	17	5.3	Solder Bump Evaluation.....	40
4.1.2 Peripheral Lead Standards.....	18	5.4	Other Bumping Techniques and Materials	41
4.1.3 Package Size Standards	18	5.4.1	Board Process Attach.....	41
4.2 General Considerations for Flip Chips	18	5.4.2	Gold Bumping.....	41
4.2.1 Final Metal.....	18	5.4.3	Gold Bump Flip Chip.....	41
4.2.2 Passivation.....	18	5.4.4	Indium-Based Bumps	41
4.2.3 Pad Limiting Metals	19	5.4.5	Bump Transfer	41
4.2.4 Solder Bump	20	5.4.6	Stud Bumping (Ball Bonding)	42
4.2.5 Existing Chip Designs	21	5.5	Chip Materials.....	42
4.2.6 I/O Capability	21	5.6	Other Bumping Process Considerations.....	43
4.2.7 Alpha Particle Emissions (Soft Errors).....	22	5.6.1	Redistribution.....	43
4.2.8 Edge Seal Design.....	23	5.6.2	Electrostatic Discharge (ESD).....	43
4.3 General Consideration for Chip Scale	23	5.7	Handling, Shipping and Storage	43
4.3.1 Chip Scale Grid Arrays (CSP-A)	23	6 Mounting and Interconnection Structures		43
4.3.2 Peripheral Leaded Chip Scale Packages (CSP-P)	24	6.1	Background	44
4.4 Substrate Structure Standard Grid Evolution....	24	6.2	Mounting Structures General Considerations ...	45
4.4.1 Footprint Design	25	6.3	Interconnection Substrate Material Choices	48
4.4.2 Design Guide Checklist.....	25	6.3.1	Rigid Organic Substrates.....	48
4.4.3 Footprint Population	28	6.3.2	Flexible Laminates.....	49
4.5 Design Output Requirements	29	6.3.3	Inorganic Substrates.....	49
		6.4	Surface Finish Properties.....	50
		6.4.1	Chemical plating finishes (electrolytic and electroless).....	50
		6.4.2	Thick film metallic finishes.....	51

6.4.3	Sputtered (Thin Film) Conductive Finishes.....	51	9.3.2	Reliability Factors.....	74
6.4.4	Alternative Protective Coatings for Conductors	52	9.3.3	Event Related Failures.....	75
6.5	Substrate Constructions	52	9.4	DESIGN FOR RELIABILITY (DfR)	76
6.5.1	Rigid Printed Wiring Boards.....	52	9.4.1	Damage Mechanisms and Failure of Solder Attachments.....	76
6.5.2	Flexible Printed Wiring Boards.....	53	9.4.2	Reliability Prediction Modeling	78
6.6	Thermal Requirements.....	53	9.4.3	DfR-Process	82
7	ASSEMBLY PROCESSES	54	9.4.4	Validation and Qualification Tests.....	82
7.1	Substrate Preparation	54	9.4.5	Screening Procedures	83
7.2	Chip and Chip Scale Placement.....	54	10	STANDARDIZATION	83
7.3	Attachment Processes	54	10.1	Standards for Development	83
7.3.1	Attachment Process for Solder	54	10.2	Flip Chip Development and Performance Standards.....	84
7.3.2	Adhesive Interconnection	54	10.2.1	Flip Chip IC/Component Design	84
7.3.3	Thermocompression Bonding.....	55	10.2.2	Mechanical Outline Standards.....	84
7.4	Cleaning	55	10.2.3	Performance Requirements for Bumps	84
7.4.1	No-Clean Flip Chip Concepts and Processes ...	55	10.2.4	Physical Flip Chip Testing Requirements.....	84
7.4.2	Aqueous Flip Chip Cleaning Technology	55	10.2.5	Trays for Flip Chip (Shipping and Delivery) ...	84
7.5	Attachment Inspection	55	10.2.6	Configuration Management	85
7.6	Underfill (Flip Chip Encapsulation).....	56	10.3	Standard on Mounting of Substrate Design and Performance	85
7.7	Electrical Test.....	56	10.3.1	Design Standard for Flip Chip or Chip Scale Package Mounting	85
7.8	Rework	56	10.3.2	Qualification and Performance of Organic Mounting Structures intended for Flip Chip Mounting.....	85
8.0	Flip Chip Test and Burn-in Methodology.....	56	10.3.3	Qualification and Performance of Inorganic Mounting Structures Intended for Flip Chip Mounting.....	85
8.1	Known Good Die.....	57	10.3.4	Qualification, Quality Conformance, and In-process Test Methods used for Organic/ Inorganic Flip Chip Mounting Structures	85
8.1.1	IC Quality	57	10.4	Flip Chip/Substrate Assembly Design and Performance Standards	85
8.1.2	IC Reliability.....	58	10.4.1	Flip Chip Assembly Design	86
8.2	KGD Techniques for Flip Chip.....	59	10.4.2	Assembly Performance Requirements	86
8.2.1	IBM's R3.....	59	10.4.3	Assembly Test Methods.....	86
8.2.2	MCNC s Burn-in and Test Substrate (BATS)	59	10.4.4	Qualification and Performance of Rework and Repair of Flip Chip Assembly	86
8.2.3	IBM's Dendrite Temporary Chip Attach (TCA)12	60	10.4.5	Assembly Reliability.....	86
8.3	Known-Good Mounting and Interconnection Structure	60	10.5	Standards for Material Performance	87
8.3.1	Testing Techniques.....	61	10.5.1	Underfill Material Requirements.....	87
8.4	Product Verification	61	10.5.2	Passivation Material Requirements	87
8.4.1	Standard Test Access Port and Boundary Scan Architecture.....	61	10.5.3	Encapsulation Material Requirements.....	87
9	REQUIREMENTS FOR RELIABILITY	62	10.5.4	Adhesives Used for Flip Chip Assembly.....	87
9.1	Robustness of Products to Use	62	10.5.5	Flux for Flip Chip Mounting Applications.....	88
9.1.1	Chip Scale Package Robustness and Reliability	63	11	FUTURE NEEDS	88
9.2	Reliability Factors.....	63	11.1	Critical Factor: Manufacturing Infrastructure... ..	89
9.2.1	Wear Out Mechanisms.....	63	11.1.1	Materials.....	89
9.2.2	Solder Bump Mechanical Reliability	64	11.1.2	Equipment	89
9.2.3	Reliability Modeling.....	68			
9.3	Reliability Testing.....	71			
9.3.1	Wear-Out Mechanisms.....	74			

11.1.3	Design	89
11.2	Critical Factor: Bump Attachment and Bonding	90
11.2.1	Dimensional Control	90
11.2.2	Metallurgical Integrity	90
11.2.3	Cleanliness of Bumping Site	90
11.3	Critical Factor: Testing Scenarios	90
11.3.1	Critical Environmental Testing	90
11.3.2	Die Testing for KGD	90
11.3.3	Inspection and Process Control Assurance	91
11.4	Total Quality Management and Manufacturing (TQMM)	91

Figures

Figure 2-1	Basic Metallurgy/Glass Design for SLT Transistors	2
Figure 2-2	Chip Collapse and Edge Shorting Problem During Solder Reflow Joining and Two Solutions	2
Figure 2-3	Flip Chip with Silver Bump Stand-Off	2
Figure 2-4	Thick Film Glass Dam Preventing Solder Flow and Collapse in First C4 Application	2
Figure 2-5	Early IBM Hybrid Thick Film Module Mixing Copper Ball SMT Transistors and C4 Integrated Circuit. (12 mm)	3
Figure 2-6	Thin Film Chromium-Copper-Chromium on Ceramic (MC)	3
Figure 2-7	Cross-Section of Cofired Alumina Multilayer Ceramic Package	3
Figure 2-8	Full Area Array C4 Configuration Microprocessor with 762 Solder Bumps in a 29x29 Array.	4
Figure 2-9	Depopulated C4 Array on Chip	4
Figure 2-10	Area Array C4 Configuration (a) 11x11 Full Array with Cantilevered Silicon, (b) SEM View	5
Figure 2-11	Structure of Hybrid IC Using Solder Bump and Cross-Sections	6
Figure 2-12	Uncapped 50 mm Multi-Chip Module (MCM)	6
Figure 2-13	IBM Thermal Conduction Module with 100-130 Flip Chips and Hat with Piston Assemblies	6
Figure 2-14	Effect of TCE Mismatch on Solder Fatigue Life	7
Figure 2-15	AT&T Silicon-on-Silicon Packaging System	7
Figure 2-16	Cut-away of IBM Glass/Ceramic TCM with Polyimide/Thin Film Surface Redistribution Layer	8
Figure 2-17	C4 Life Extension by Use of Filled Epoxy Resins with Matching Expansivity (Hitachi)	8
Figure 2-18	IBM SLC Chip-on-Card Technology	9
Figure 2-19	Bridging the Gap	9
Figure 2-20	Chip Scale Grid Array Package (CSP-A)	9
Figure 2-21	Example of Chip Scale	10
Figure 2-22	Micro BGA	10

Figure 2-23	Mini BGA	11
Figure 2-24	SLICC Chip Scale Grid Array	11
Figure 2-25	Chip Scale Package	12
Figure 2-26	Resin Encapsulated LSI Chip with Bumps	12
Figure 2-27	Peripheral Area Array Converter	13
Figure 2-28	Cutaway View of an MSMT Packaged IC	14
Figure 2-29	MSMT Posts in Saw Lane	14
Figure 2-30	MSMT Posts in Bonding Pad Area	14
Figure 2-31	Cross-Sectional View of an MSMT Package ..	15
Figure 2-32	Close-up Photo of MSMT Posts, Encapsulant and Bottom of the Chip	15
Figure 2-33	Chip Scale Peripheral Package	15
Figure 4-1	Flip Chip Connection	17
Figure 4-2	Mechanical and Electrical Connections	17
Figure 4-3	Joined Chip with Chip Underfill	18
Figure 4-4	A Solder Bump Flip Chip Connection	18
Figure 4-5	Two Simple Chips, Showing Original Pad Locations and Rerouted Bumps	19
Figure 4-6	Redistribution of a Single Metal Layer Device	19
Figure 4-7	Passivation (Cross-Section)	19
Figure 4-8	Schematic Plan View of Bump	20
Figure 4-9	Example of Pad Limiting Metal	20
Figure 4-10	Initial C4 Bump	21
Figure 4-11	A C4 Bump After Reflow	21
Figure 4-12	Recommended DCA Grid Pitch (250 μ m Grid, 150 μ m Bumps)	21
Figure 4-13	Interconnect Density (Peripheral vs. Area Array)	22
Figure 4-14	Alpha Particle Emission Track and E/H Pairs ..	23
Figure 4-15	Distortion of Depletion by Alpha Particles	23
Figure 4-16	Chip Edge and Polyimide Seal	23
Figure 4-17	MSMT Post Configurations	24
Figure 4-18	Standard Grid Structure	25
Figure 4-19	Bump Footprint Planning	26
Figure 4-20	Alignment to Visual/Sensitive Chip Structures	27
Figure 4-21	Minimum Pitch from Bump to Passivation Seal ("A" - $\frac{1}{2}$ finished bump diameter, plus alignment to tolerances, plus desired minimum)	28
Figure 4-22	Redundant Footprint	29
Figure 4-23	Design Shrink Footprint	29
Figure 4-24	Signal and Power Distribution Position	30
Figure 4-25	Nested I/O Footprints	30
Figure 4-26	Typical Bump Passivation Reticle Mask Format	31
Figure 4-27	Product Unit Cell Plan (example)	31
Figure 4-28	Printed Board Flip Chip or Grid Array Land Patterns	32
Figure 4-29	MSMT Land Drawing and Dimensions	32
Figure 4-30	Bump Electrical Pad (Redistributed Chip)	33
Figure 4-31	Bump Equivalent Circuit (Redistributed Chip) ..	33

Figure 4-32	Final Metal Trace and Underlying Traces (Cross Section)	34
Figure 4-33	Thermal/Electrical Analogy	35
Figure 4-34	Bump Interconnect Equivalent Model.....	35
Figure 4-35	Thermal Paste Example	36
Figure 4-36	Approximate Thermal Model for Thermal Paste.....	36
Figure 4-37	Chip Underfill Example	36
Figure 4-38	Approximate Thermal Model for Chip Underfill	36
Figure 5-1	Photomicrograph of As-Plated Solder Pads....	37
Figure 5-2	Photomicrograph of Solder Bumps	38
Figure 5-3	An Example of Fine Line Stencil Printing.....	39
Figure 5-4	Gold Bumped IC Adhesively Attached to a Glass Substrate	42
Figure 5-5	Newly Developed Chip on Glass Technology.....	42
Figure 5-6	Schematic Cross-Sectional View of Connection for Chip on Glass	42
Figure 5-7	Redistribution of a Peripheral Pattern	43
Figure 5-8	ESD Path to Ground.....	43
Figure 6-1	Packaging Efficiency.....	44
Figure 6-2	Exploded View of a Substrate for Flip Chip or Chip Scale Applications.....	46
Figure 6-3	Wire Routing Ability of Different Design Rules for One and Two Sided PWBs.....	47
Figure 6-4	Conductor Routing Comparison	47
Figure 9-1	Chip Scale Package Lead Compliance.....	64
Figure 9-2	Fracture Due to Fatigue/Creep Interaction.....	67
Figure 9-3	Example of Solder Bump Fatigue Curves.....	67
Figure 9-4	Thermal Cycling Frequency Threshold vs. Temperature.....	68
Figure 9-5	Compliant Lead Alternative to Underfill.....	69
Figure 9-6	Lognormal Distribution of Thermal Cycle Failures	70
Figure 9-7	Effect of α on Reliability	71
Figure 9-8	Acceleration Factor Shift of Lognormal Distribution	72
Figure 9-9	Thermal Cycling Test Profile.....	73
Figure 9-10	Pre-Conditioning Thermal Profile.....	74
Figure 9-11	Depiction of the Effects of the Accumulating Fatigue Damage in Solder Joint Structure.....	77
Figure 10-1	Semiconductor Design.....	84
Figure 10-2	Mechanical Outlines	84
Figure 10-3	Bump Performance.....	84
Figure 10-4	Flip Chip and Chip Scale Test Methods.....	84
Figure 10-5	Flip Chip/Chip Scale Carrier Trays.....	84
Figure 10-6	Flip Chip/Chip Scale Configuration Management.....	85
Figure 10-7	Mounting Structures Design	85
Figure 10-8	Organic Mounting Structure Performance.....	85
Figure 10-9	Inorganic Mounting Structure Performance.....	86
Figure 10-10	Mounting Structure Test Methods.....	86
Figure 10-11	Assembly Design Configuration	86

Figure 10-12	Assembly Performance Requirements	86
Figure 10-13	Assembly Test Methods.....	87
Figure 10-14	Assembly Rework and Repair	87
Figure 10-15	Assembly Reliability.....	87
Figure 10-16	Underfill Material Performance	87
Figure 10-17	Passivation Material Performance.....	87
Figure 10-18	Encapsulation Material Performance.....	88
Figure 10-19	Flip Chip/Chip Scale Adhesives	88
Figure 10-20	Flux Qualification and Performance	88

Tables

Table 3-1	Commercial Flip Chip and Chip Scale Applications	16
Table 3-2	Comparative Table of Various Technologies for a 100 Lead 10x10 mm Die	16
Table 4-1	Commonly Used PLM Systems	20
Table 4-2	C4 Bump Diameter and Minimum Pitch Options	21
Table 4-3	Alpha Particle Emissions of Semiconductor Materials.....	22
Table 4-4	Chip Edge Seal Dimensions (Typical)	23
Table 4-5	Design rules for substrates for Chip Scale Technology	25
Table 4-6	Terminal Via and Final Metal Via Pitch.....	27
Table 4-7	Final Metal Signal Trace (30 μ m).....	34
Table 4-8	Final Metal Power Trace (60 μ m)	34
Table 4-9	Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip)	35
Table 4-10	Typical Bump (150 μ m) Thermal Resistances Multi-Layer Metal Chips	36
Table 6-1	Comparison of Selected Material Properties	48
Table 6-2	Inorganic Substrate Characteristics	50
Table 9-1	Product Categories and Use Environments.....	65
Table 9-2	Coefficients of Thermal Expansion	66
Table 9-3	Typical Heights (Joined).....	66
Table 9-4	Acceleration Factor Values for Example 1.....	71
Table 9-5	Representative Realistic Worse Case Use Environments for Surface Mounted Electronics and Recommended Accelerated Testing for Surface Mount Attachments by Most Common Use Categories.....	75

Implementation of Flip Chip and Chip Scale Technology

1 SCOPE

This document describes the implementation of flip chip and related chip scale semiconductor packaging technologies. The areas discussed include: design considerations, assembly processes, technology choices, application, and reliability data. Chip scale packaging variations include: flip chip, High Density Interconnect (HDI), Micro Ball Grid Array (μ BGA), Micro Surface Mount Technology (MSMT) and Slightly Larger than Integrated Circuit Carrier (SLICC).

1.1 Purpose

This document is intended to provide general information on implementing flip chip and chip scale technologies for creating single chip or multichip modules (MCM), IC cards, memory cards and very dense surface mount assemblies.

1.2 Categorization

Flip chip is categorized as versions of a tin-lead (SnPb) solder bump process, and alternative solutions that use other forms of chip bond site bumping.

Chip scale technology is categorized as semiconductor chip structures that have been made robust to facilitate ease of chip handling, testing and chip assembly. The chip scale technologies have common attributes of minimal size, no more than 1.2X the area of the original die size, and are direct surface mountable.

2 TECHNOLOGY OVERVIEW

Flip chip and chip scale technology relate to methods used to provide an efficient technique for interconnecting semiconductor die to a substrate. Over the years flip chip technology has grown in stature and expanded into the more generic area of chip scale technology. In addition, many new techniques for mounting bare die were also established. Today, enhancements of the semiconductor die, which ruggedize the product to facilitate ease of handling and testing, have established another level of packaging technology in which many companies can participate.

2.1 History of Flip Chip

Flip chip solder bump interconnection technology is over 30 years old. It was first conceived and developed in 1960-61 by IBM for the Solid Logic Technology (SLT) hybrid electronic circuitry in IBM's System 360 computers introduced in April 1964.

At that time, standard transistor packaging used hermeti-

cally sealed metal cans with glass sealed wires emerging from a header upon which the germanium or silicon chip was metallurgically backbonded. Manual thermocompression wire bonding to the chip was the common technique.

Although transistor technology was much more reliable than vacuum tube technology that preceded it, the packaging and interconnection technologies were weak. Faulty manual wire bonds, purple plague (gold-aluminum intermetallic formation), and aluminum corrosion of thin film interconnections on the chip, even in hermetic packages, were all reliability concerns. In addition, manufacturability and productivity were deficient.

SLT transistors and diodes were glass passivated at the wafer level to protect aluminum wiring from the environment. Glass frits of borosilicate glass were fused on the surface of transistor wafers after the aluminum wiring was formed. The glass film obviated the need for a hermetic enclosure because the transistor was sealed at the chip level.

Consistent with maintaining a hermetic seal was the idea of etching via holes in the glass where electrical connections were to be made, and hermetically resealing the holes with an overlapping, larger pad of metal films. The first film, typically chromium, was used to create a good bond to glass and aluminum.

Subsequent metal films, typically copper and gold, were deposited to provide wettability and solderability for a ball of metal alloy that was to be melted on the pad. Originally, the ball was an alloy of Au-Sn eutectic which melted at 360°C; therefore, the pad was called the ball-limiting metallurgy because the melted ball would not wet the glass beyond the area of the pad. Later the ball or bump became a solder bump with an embedded copper ball "stand-off," shown in figure 2-1.

The packaging concept required that thick film electrodes or wires be screened and fired on alumina substrates. Originally, the thick film was glass fritted Au-Pt paste; later it became Ag-Pd. The wiring was hot dip tinned with 90Pb-10Sn solder to improve conductance and to interconnect the active and passive components. For each transistor, three of the screened wires were to terminate in a spot that would be the mirror image of the chip bumps.

After each chip site was fluxed with a droplet of sticky water white rosin flux, the chip was picked up and placed on the solder coated electrodes face down or "flipped" compared to normal chip placement. Subsequently, the substrate was heated in a furnace to reflow the solder and

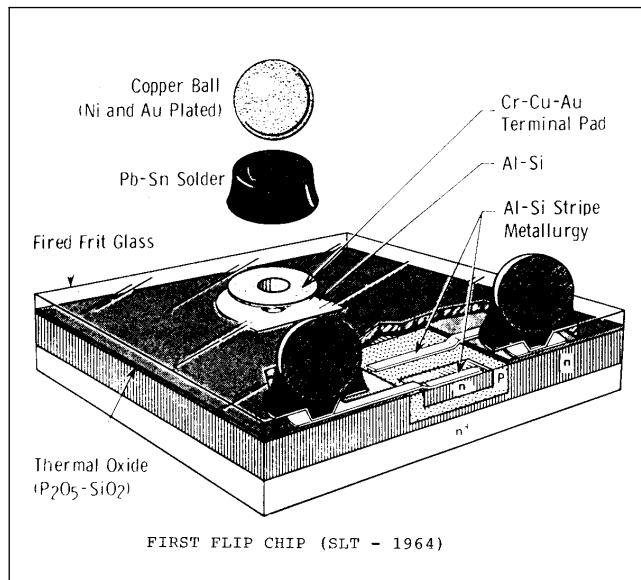


Figure 2-1 Basic Metallurgy/Glass Design for SLT Transistors

thereby reflow soldering the device bump asperities and joining the chip to the substrate.

However, there were problems with the original gold alloy balls in that they would alloy and melt with the high lead solder at a relatively low temperature (Pb-Au eutectic melts at 215°C). The ball would alloy and flow into the solder lands thereby “collapsing” and allowing solder to short to the raw edges of the chip (Figure 2-2). There were three solutions to the problem.

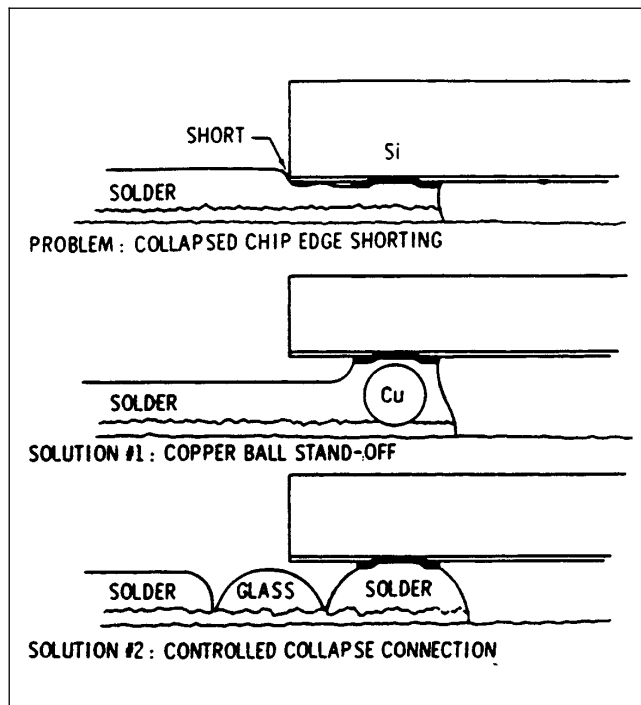


Figure 2-2 Chip Collapse and Edge Shorting Problem During Solder Reflow Joining and Two Solutions

The first was to embed copper balls in the solder bumps.

This positive stand-off solution was used for all of the SLT and SLT extension designs. The second solution, developed by Delco Electronics (General Motors) in the late 60s, was similar to embedding copper balls except that the design employed a rigid silver bump. The bump provided a positive stand-off and was attached to a thick film ceramic substrate by means of solder that was screen-printed onto the substrate, as shown in figure 2-3.

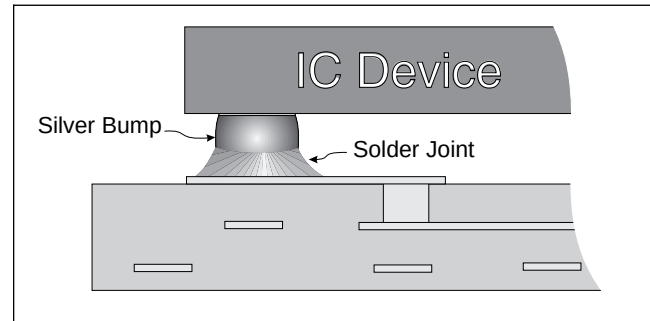


Figure 2-3 Flip Chip with Silver Bump Stand-Off

The third solution was to use a screened glass dam near the electrode tips to act as a “stop-off” to prevent the ball solder from flowing down the electrode. The silver-palladium paste under the glass provided sufficient conductivity for circuit continuity. By then the Ball Limiting Metallurgy (BLM) with a high-lead (Pb) solder system and a copper ball had proven to work well. Therefore, the ball was simply removed and the solder evaporation process extended to form pure solder bumps which were approximately 125µm high.

This system, shown in figure 2-4, became known as the controlled collapse chip connection (C⁴, or C4). For integrated circuit fabrication where the I/O count would grow from 3 pads to 20 or 30, the process for fabrication and the uniformity of C4 bumps was superior to previous IBM copper ball design.

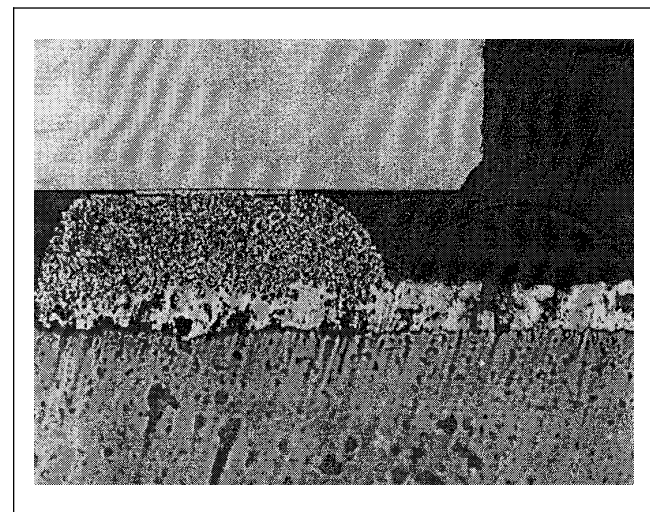


Figure 2-4 Thick Film Glass Dam Preventing Solder Flow and Collapse in First C4 Application

There was a long era of thick film hybrid technology from the early 60s to late 70s at IBM using thick film screened and tinned conductors and thick film trimmable resistors with flip chips. Discrete transistor and diode chips used copper ball solder bumps, while early integrated circuits had C4 solder balls. Sometimes both were mixed on the same substrates, shown in figure 2-5.

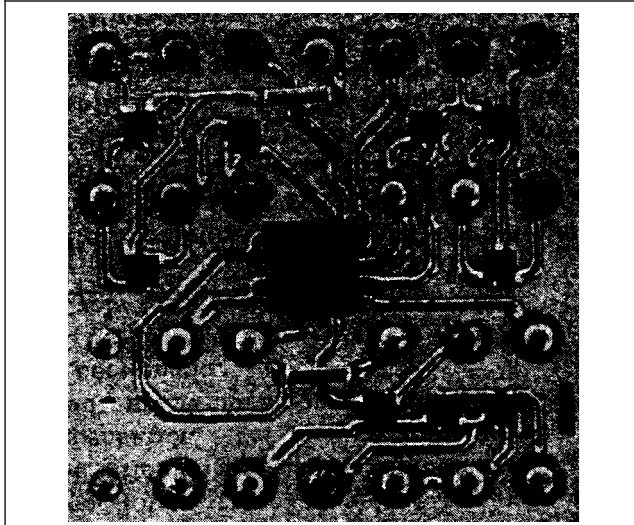


Figure 2-5 Early IBM Hybrid Thick Film Module Mixing Copper Ball SMT Transistors and C4 Integrated Circuit. (12 mm)

Contemporary with this, Delco Electronics' silver bumps did not require tinning of the conductors. By the mid 80s, Delco Electronics was using a reflowable indium-lead solder bump with alternative methods for controlling solderability on the substrate. This bump was compatible with low temperature solder processing without requiring deposition of solder on the substrate. Motorola's efforts in this time period included evaporated (and later electroplated) tin-lead bumps.

As the number of circuits on a chip and the number of interconnections on logic and memory IC's grew, it became necessary to increase the number of I/O pins on substrates. This led from 12.5 mm (0.5 inch) SLT substrates to 25 mm (1 inch) substrates of thin film metallized ceramic (MC). The thin film metallization was evaporated, later sputtered, Chromium-Copper-Chromium. The upper chromium film was left intact except at pin interconnect site heads and C4 finger tips. The chromium (or chromium oxide surface) then replaced the glass dam as "stop-off", shown in figure 2-6.

Later, using cofired multilayer alumina substrates, electrical connections were brought to the surface through a molybdenum stud-capped nickel/gold vias. Since solder does not wet to the alumina, the need for glass or chromium dams disappeared, as shown in figure 2-7.

Early integrated circuits had solder bumps around the perimeter of the chip because of concerns that the passiva-

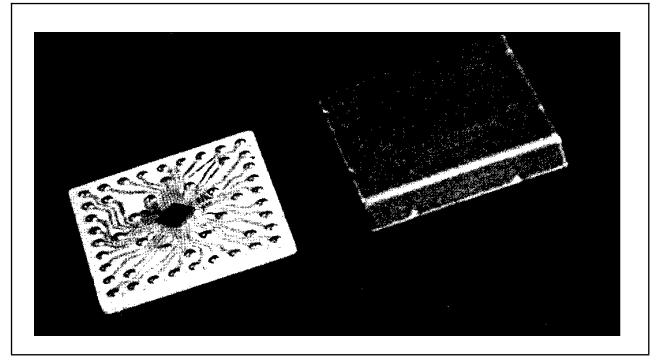


Figure 2-6 Thin Film Chromium-Copper-Chromium on Ceramic (MC)

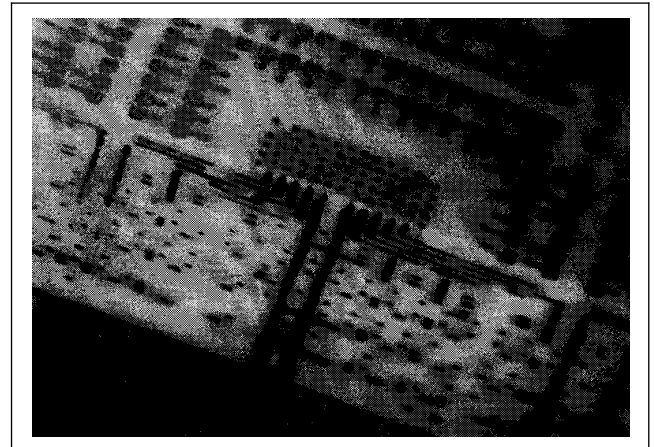


Figure 2-7 Cross-Section of Cofired Alumina Multilayer Ceramic Package

tion vias opening process or the bump stresses would affect underlying transistors. Later, it was discovered that there was no problem putting solder bumps directly over integrated circuits, transistors and diodes. This permitted the staggering of bumps around the perimeter with an occasional inboard power pad for single level substrates of thick or thin film designs. Thin film substrates enabled finer pitches and more escape channels between pads so that depopulated area arrays could be accommodated. Multilayer ceramic substrates with buried redistribution wires allowed full area arrays and higher I/O capability than TAB or wire bond peripheral connections, shown in figure 2-8.

2.1.1 Hybrid Thick Film Packages

Early solder bump flip chip packages used thick films of glass fritted precious metals tinned with 90% lead-10% tin solder. Cost reduction favored silver-palladium paste but reliability issues with silver caused later use of ternary pastes of silver-palladium-gold. A typical package, see figure 2-5, shows the bottom-side view of thick film resistors that were dynamically trimmable with abrasive jets and later with lasers.

Equally important to the elimination of hermetic packaging and manual wire bonding was the profound improvement in manufacturability of circuits. Glass passivation

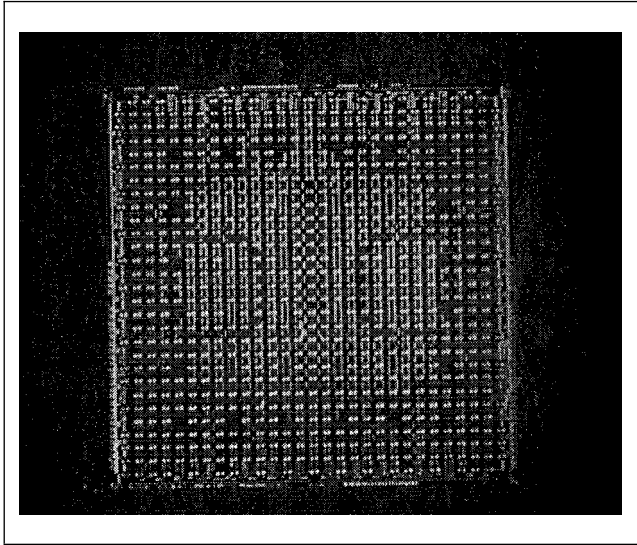


Figure 2-8 Full Area Array C4 Configuration Microprocessor with 762 Solder Bumps in a 29x29 Array.

and diode chips were so robust they could withstand random mechanical handling in vibratory bowl feeders. Testing and chip placement were highly automated, attaining process rates of 3 to 6 chips per second. Chip joining to substrates was done with thousands of solder joints being made in reflow furnaces simultaneously.

Low cost and high productivity were closely associated. Those factors along with the mechanical ruggedness made flip chip attractive to the automotive industry as well. General Motors (through Delco Electronics) became an early high volume user of hybrid flip chip technology for voltage regulators and ignition modules.

Completion of a thick film module typically required silicone gel around the chips to protect against moisture, a metal can for mechanical protection and RTV™ silicone rubber for a backseal.

Solder bump integrated circuit chips brought other changes. Fired frit glass films were replaced by sputtered SiO₂ films that were compressive in residual stress and lower in pinhole defect density. These films were ultimately good enough to support two and three levels of chip metallization.

As the number of circuits grew from three to four to tens of circuits, the number of I/O bumps on logic chips grew as did the demand for pins in the substrate. Interstitial pins were put in the pin grid array to increase the I/O count. Rent's rule was found to apply to logic chips as well as logic cards (empirical observations showed that card I/O terminal count is directly related to the number of logic circuits).

2.1.2 Hybrid Thin Film Packages

Due to the continued use of logic chips, large ceramic substrates were required. These were approximately 25 mm²

with higher pin capacity and grew in size as the need developed. Also, thick film screening was supplemented with thin film chromium-copper-chromium depositions (Metallized Ceramic or MC). These films were subtractively etched, using photolithographic processes, to form finer lines and pitches than their thick film counterparts (20 µm lines, 60 µm pitches, minimum).

Thin film processing maximized the wireability of the substrate and allowed more wires per channel between pins or C4 bumps. Subsequently, polyimide thin films were used in combination with metal thin films to allow a buried ground plane and a two level wiring capability with vias and cross-overs. [Metallized Ceramic with Polyimide (MCP)]

As the number of logic circuits on a chip continued to grow, the peripheral solder bump pad arrangement became a constraint to circuit count. It was soon discovered that solder bumps could be put over active circuits with no negative effect. Stresses from testing or joining were not transferred to active devices unlike other chip joining technologies such as wire bonding. This led to in-board solder bumps, at first peripherally because chip testers were best suited to such configurations, then in staggered multi-row peripheral patterns. Later, with MC and MCP capabilities to fan out the interconnection of arrays and new chip testers, patterns known as depopulated arrays were possible as shown in figure 2-9. Solder bumps over the active area greatly relieved the I/O constraint. Chips could be smaller or could accommodate a greater number of circuits, as the designer desired.

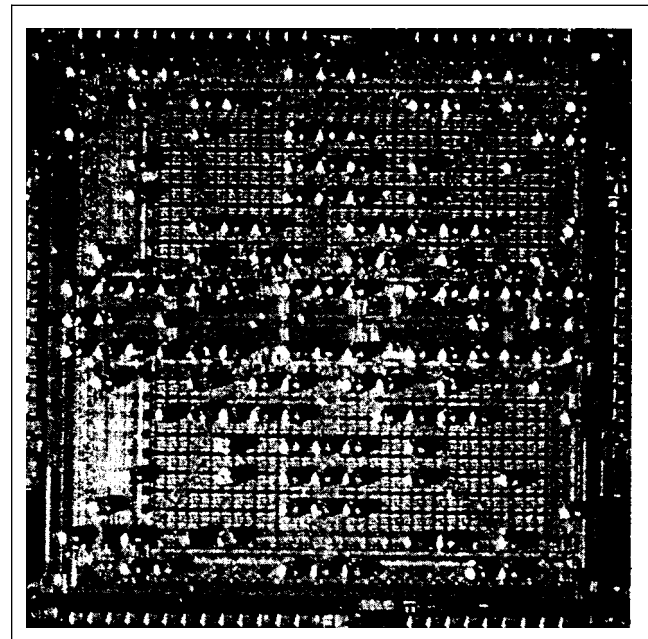


Figure 2-9 Depopulated C4 Array on Chip

2.1.3 Multilayer Ceramic Substrate (MLC)

A full area array C4 chip footprint required the high I/O redistribution capability of multilayer ceramic technology.

For example, the top five layers of green sheet in the cofired ceramic packages introduced by IBM in 1978 were necessary to fan out an 11x11 array of C4 pads, shown in figure 2-10.

The package body was alumina with glass binder and

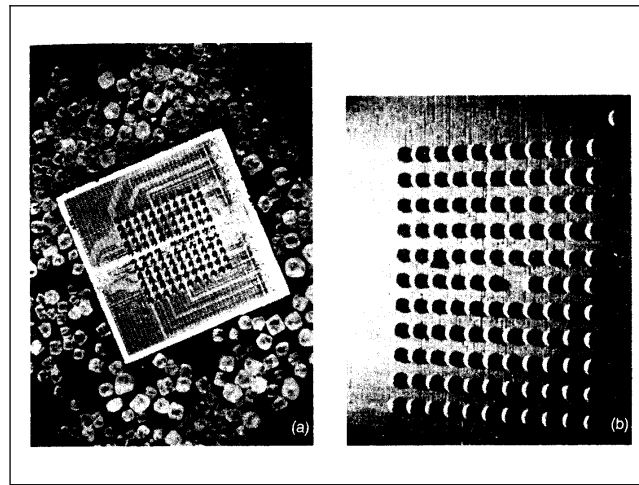


Figure 2-10 Area Array C4 Configuration (a) 11x11 Full Array with Cantilevered Silicon, (b) SEM View

molybdenum conductors. The surface finish of the molybdenum studs emerging from the top and bottom of the package was nickel and gold film for solderability and brazeability.

Other manufacturers, such as Hitachi and NTT, began to use flip chip and co-fired MLC not only for silicon chips but also for thin film flip chip resistors and capacitors as shown in figure 2-11. The module illustrated was for a telecommunications application.

Because of the coefficient of thermal expansion (CTE) mismatch in expansivity between alumina ($CTE=6 \text{ PPM}/^{\circ}\text{C}$) and silicon ($CTE=3 \text{ PPM}/^{\circ}\text{C}$) much of the silicon was cantilevered beyond the pad array to minimize distance from the neutral point (DNP), shown in figure 2-10. Chips had grown sufficiently large that the mismatch in expansion rate could plastically deform the most remote solder pads during thermal cycling. This caused fatigue fracture and electrical discontinuity of those pads in the corners.

Multilayer ceramic technology also allowed the use of Multiple Chips on the Module (MCM). Figure 2-12 shows an uncapped flip chip multichip module. Each chip had 120 I/O pads, supported a maximum of 704 available bipolar circuits and dissipated a maximum of 1.5 watts to an air cooled cap.

IBM developed a series of Thermal Conduction Modules (TCMs) starting in 1981 where the chip count on the substrate grew to 100-130. Each chip was backed by a spring loaded piston in a helium atmosphere and could dissipate 3 watts/chip, as shown in figure 2-13. The area array pads started as 11x11 arrays but grew to 17x17 arrays in subsequent models.

Improved thermal cycle solder joint performance, by reducing distance-to-neutral-point, was short lived as chip circuit density was growing rapidly and larger chips were imminent. The fatigue life vs. CTE relationship is shown in figure 2-14.

It is clearly shown that fatigue life is not a problem if the expansion rate of the chip could be matched with a silicon substrate (see figure 2-15) or a man-made substrate such as glass-ceramic (cordeirite-like) which matches silicon.

2.1.4 Thin Film on Multilayer Ceramic

The glass ceramic MLC substrate which IBM developed for System/390 also had a redistribution layer of thin film wiring on its surface to reduce the number of buried layers that would have been necessary for a 28x28 array of C4's (648 bumps) on each chip.

The heat dissipation through each piston was raised to a maximum of 28 watts using an oil heat transfer fluid in place of helium, see figure 2-16.

2.1.5 Thin Film on Organic Epoxy/Glass Laminate

Chip under fill development improved the solder joint reliability of flip chips by at least an order of magnitude by encapsulating the solder joints in filled epoxy, as shown in figure 2-17. The strain level is reduced and reliability is therefore extended. Chips can be mounted to a printed board as a surface mount component without a plastic or ceramic package. This technology is an example of Direct Chip Attach (DCA). Smaller, lighter, less expensive electronic applications therefore are attainable.

Another example of DCA is IBM's SLC technology. By using layers of photosensitive epoxy and copper thin film wiring on the epoxy glass laminate board surface, it is possible to create chip bonding sites that match solder bump footprints similar to ceramic packages, shown in figure 2-18. By pretinning the land pattern with tin lead (SnPb) eutectic, high-lead bumps can be attached to the substrate.

Application of chip underfill enhances reliability performance. Epoxy underfill reinforcement allows use of lower-compliance eutectic SnPb bumps, which eliminates the need to pretin or deposit solder on the substrate thereby reducing cost.

2.1.6 Chip on Flexible Printed Board

Chip on flex is another direct chip attach technology. Most flexible circuits are polyimide-based substrates with or without adhesives. This technology is used in static and dynamic applications. Viewed as a compliant substrate this DCA method is designed to reduce or eliminate the need for underfill.

2.1.7 Thin Film on Silicon

An AT&T developed process places flip chips into an alloy solder paste that has been printed onto a substrate.

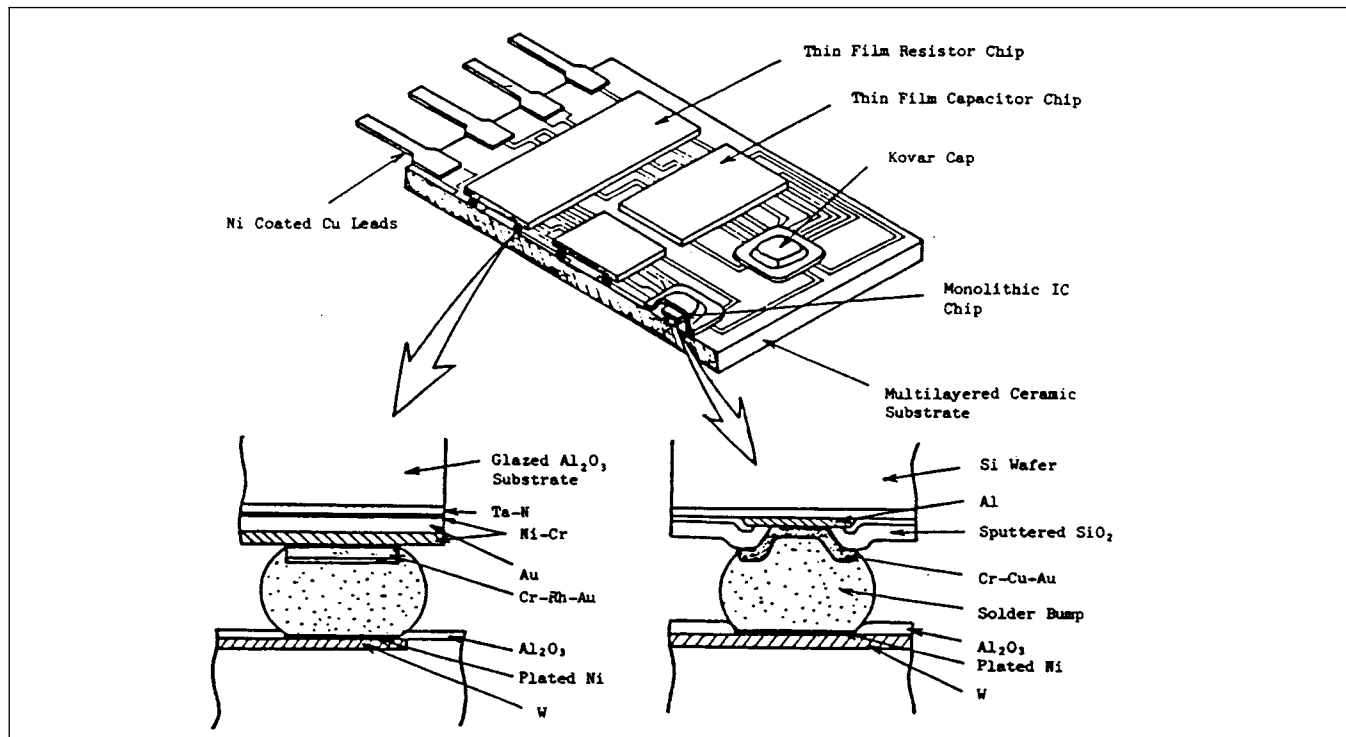


Figure 2-11 Structure of Hybrid IC Using Solder Bump and Cross-Sections

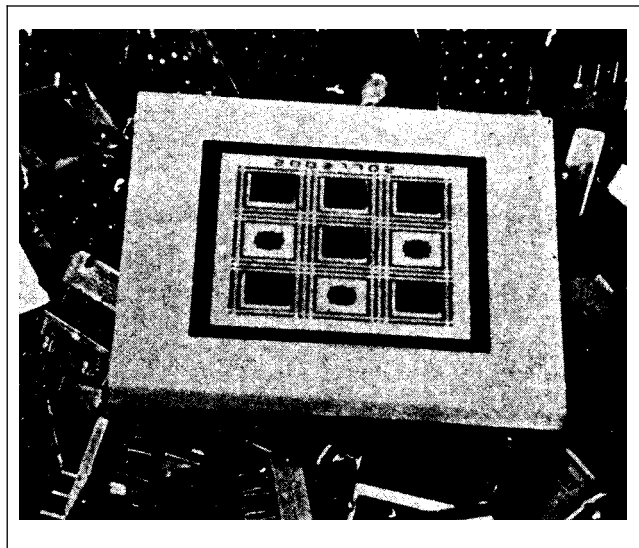


Figure 2-12 Uncapped 50 mm Multi-Chip Module (MCM)

interconnection MCM substrate. Both the die and substrate have matching patterns of solder wettable connection pads. The printing step deposits uniform volumes of solder paste on all the interconnection lands on the substrate in one step.

2.1.8 Characteristics of Flip Chip Technology

There are many advantages to the use of flip chip. Some of these are:

- Reliability without hermeticity at the chip level has been achieved successfully for many years through the use of glass, sputtered SiO_2 , CVD oxide or nitride, or polyimide passivation films on the face

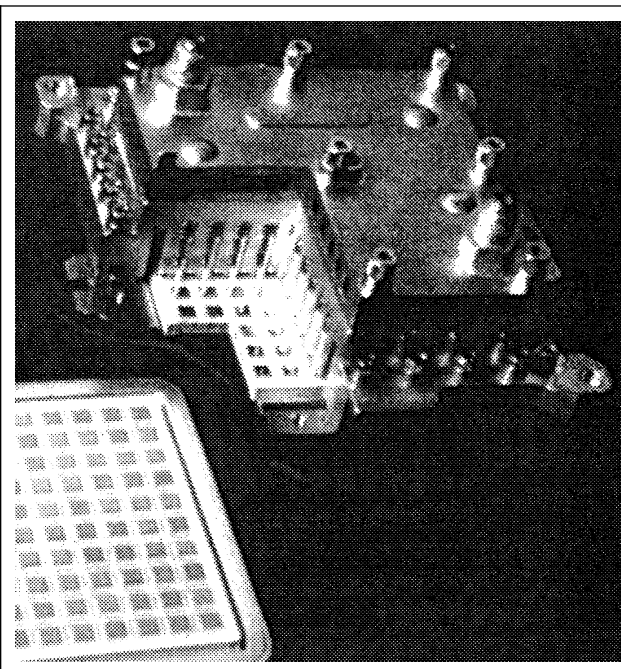


Figure 2-13 IBM Thermal Conduction Module with 100-130 Flip Chips and Hat with Piston Assemblies

of the chip.

- Rugged, high strength interconnections between chip and package make disturbance unlikely in severe mechanical environments of shock and vibration such as automotive, aircraft and space launch applications.
- The highest density of packaged circuit components

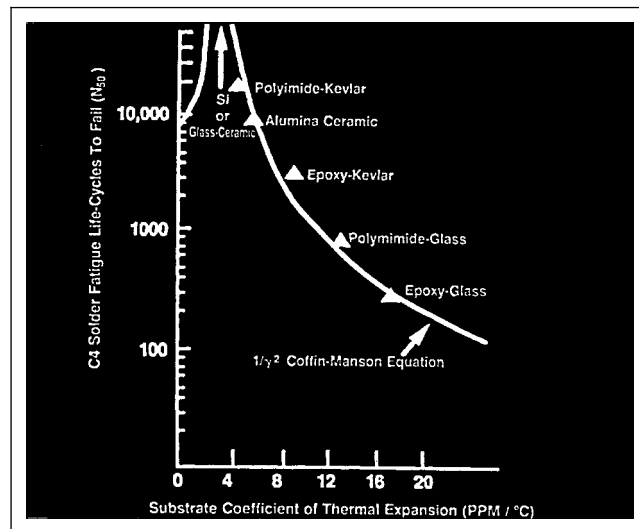


Figure 2-14 Effect of TCE Mismatch on Solder Fatigue Life

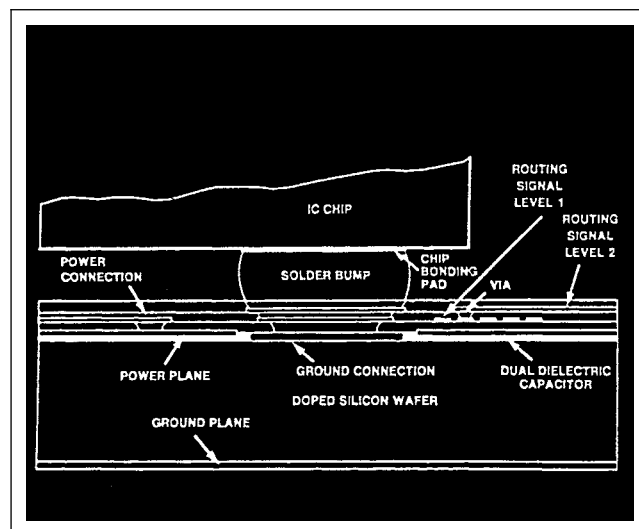


Figure 2-15 AT&T Silicon-on-Silicon Packaging System

achievable has been demonstrated with multichip modules of flip chips with area array interconnects on multilayer ceramic substrates.

- Self alignment of chips during reflow soldering due to surface tension forces in liquid solder allows chips to be placed relatively crudely (as much as 50% off of substrate lands). This allows thousands of joints to be made simultaneously in a reflow furnace.
- Photonic applications gain very high optical efficiency by attaining 1-2 μm overlay from solder bump self alignment, and therefore flip chips have found wide application in photonics.
- Excellent electrical properties with low capacitance, inductance and resistance exist, due to the short electrical paths enabling future application for high frequency circuitry.

- Proven field reliability is experienced in billions of shipped flip chip solder connections in a variety of packaging applications from thick film hybrids to cofired multilayer ceramic (MLC).
- Reliable replacement methodology is possible for multichip modules, which makes repair and engineering change possible and practicable.
- Low profile and small footprint enable very dense applications.
- Direct chip attach on organic rigid material and flex with lower melting temperature solders is SMT compatible and has successfully demonstrated opportunities for more consumer goods applications.

Flip chip packaging technology has some limitations. Users have determined some areas where flip chip technology does not apply. Some of the limitations and concerns are:

- The required infrastructure for manufacturing, testing and handling of flip chips can be an obstacle. Commitment to fixed footprints of bump patterns and matching substrates can be constraining.
- Availability and cost of flip chips from semiconductor vendors have been a problem, and contract bump facilities are in their infancy.
- CTE mismatch between silicon and substrate expansivity causes such limitations as thermal cycle fatigue failure of solder and thermal shock failure. Where possible the strain level in the solder may be greatly reduced by using underchip encapsulants and adhesives, but presently at the cost of throughput rework capability.
- Inability to optically inspect hidden area array bumps may be a consideration in the quality control of soldered interconnections. However, process optimization can eliminate the need for bump inspection.
- Heat dissipation (0.5-2 watts) is limited in flip chips without thermal enhancements.
- Alpha particle radiation from ordinary solder can cause soft error events.

2.2 Introduction to Chip Scale Packaging

Chip scale packaging or CSP is an emerging branch of semiconductor packaging that seeks to bridge the gap between flip chips and conventional surface mount packages. The technology is developing in response to some of the limitations of flip chip technology and to address the concerns and perceived risks associated with handling and assembling bare die while still maintaining most of the volumetric packaging and performance advantages that flip chip technology offers. See figure 2-19.

The terms chip scale package and CSP have become popular in

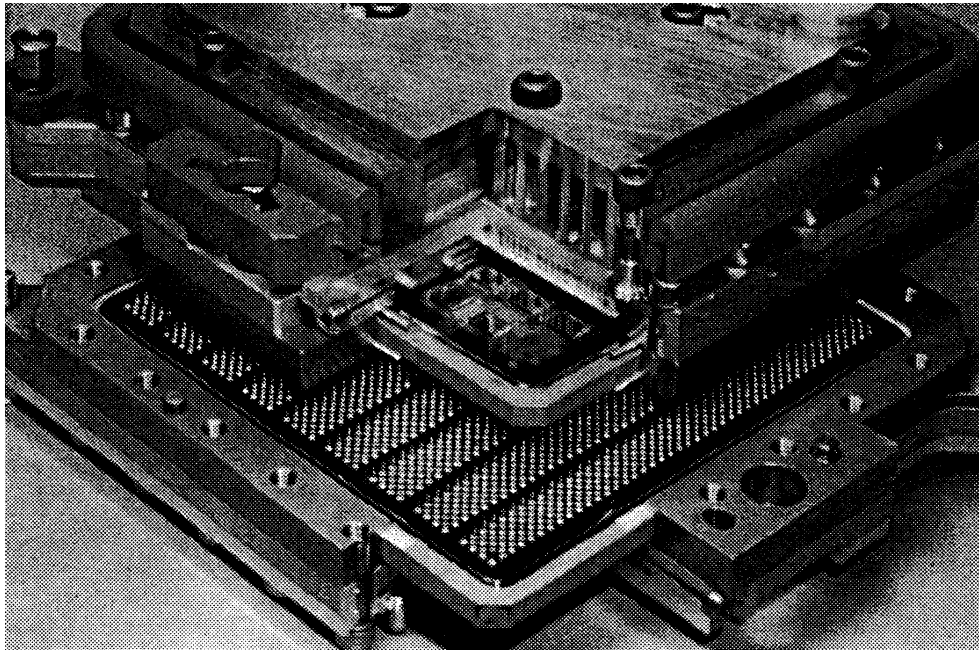


Figure 2-16 Cut-away of IBM Glass/Ceramic TCM with Polyimide/Thin Film Surface Redistribution Layer

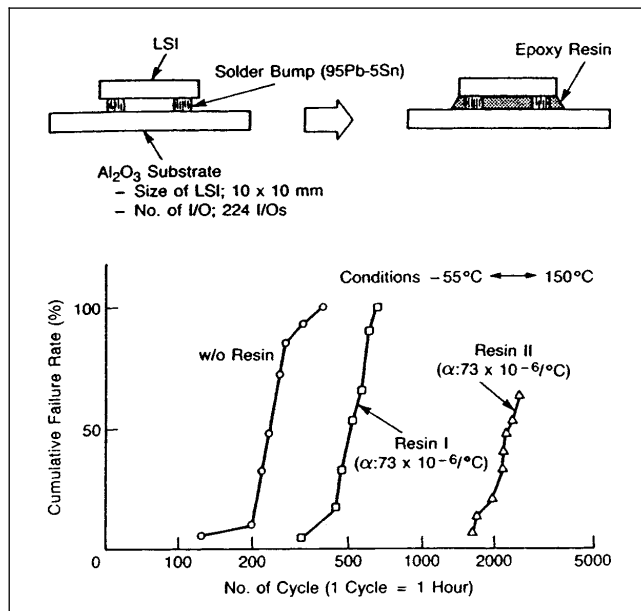


Figure 2-17 C4 Life Extension by Use of Filled Epoxy Resins with Matching Expansivity (Hitachi)

1994. The term was used in several presentations to indicate comparison of the economics of multichip modules vs. denser SMT assemblies using smaller surface mountable packages that were called CSPs. The conclusion was that CSP's were far more economical than MCMs.

Chip scale packages parallel standard surface mount packages in form factor, being found in both peripherally leaded and area array formats. As with their larger counterparts, chip scale packages are designed to facilitate test and burn-in of the semiconductor before committing them to the assembly process, thus effectively providing and

answer to the current problem of known good die (KGD). CSPs generally use the same assembly process as larger SMT packages. Presently there are a number of CSPs being developed, evaluated, or offered as solutions.

The original chip scale package was the beam lead package developed by AT&T in the 1960s. This package was proven very reliable and economical. However, it was viewed as more difficult to handle than the dual in-line package, or DIP.

The common advantage of these differing approaches is the ability to offer packaged chips that will facilitate movement toward smaller, lighter, high performance systems at lower cost, using the current SMT assembly infrastructure.

The need for smaller devices, the developments in flip chip bumping processes, and advancements in the packaging of microwave devices have lead to the development of chip scale package concepts. CSPs are extensions to the flip chip concept as the packaging of the chip provides robust handling and attachment without the need for additional materials, such as underfill epoxies.

Chip scale packages are available in two basic configurations;

1. Chip Scale Grid Array Packages (CSP-A)
2. Chip Scale Peripheral Leaded Packages (CSP-P)

Chip scale packages are attached to the PCB using the basic fine pitch surface mount technology assembly process. The fine pitch process starts by stenciling a thin layer of fine particle solder paste onto the PCB land areas. Next, the bumps, balls, or leads of the chip scale and other SMT packages are placed in contact with the solder paste. The assembly is heated in a controlled oven to reflow the solder.

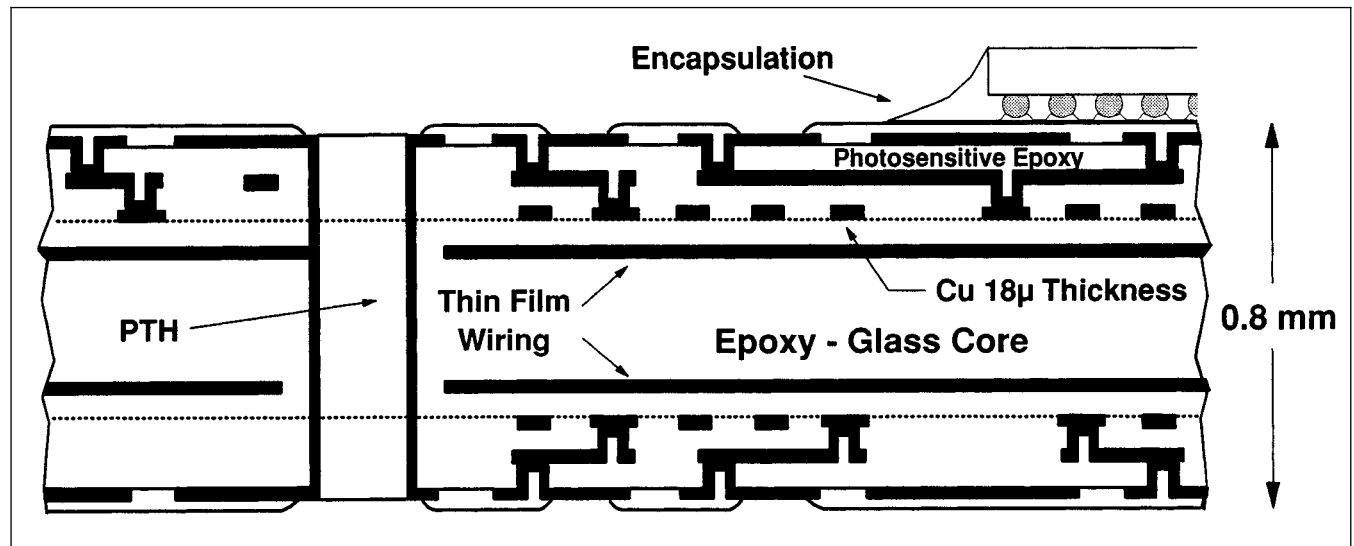


Figure 2-18 IBM SLC Chip-on-Card Technology

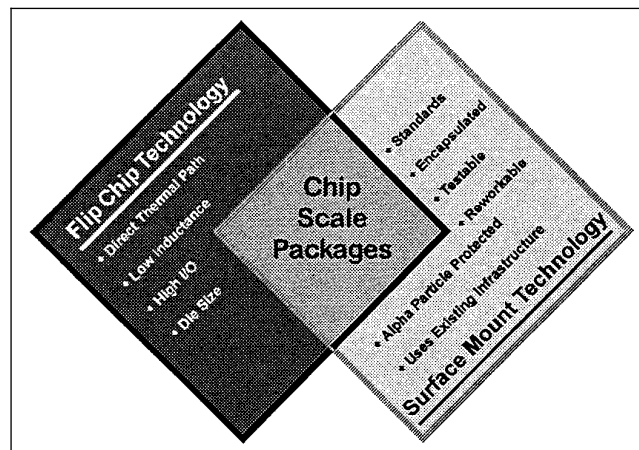


Figure 2-19 Bridging the Gap

above the melting temperature of the solder. The assembly is cleaned, if required. As with flip chip, an underfill epoxy may be injected under and around the chip scale devices to enhance their solder joint reliability, however, like conventional SMT, certain chip scale packages do not require the underfill epoxy. After curing the underfill epoxy, the assembly is tested.

2.2.1 Chip Scale Grid Array Packages

Chip Scale Grid Array Packages (CSP-A) are produced in different variations. These include the mini and micro ball grid arrays. These packages are similar in appearance to the larger Ball Grid Array or BGA packages. The pitch of the solder balls on BGAs is 1.0 to 1.5 mm; on CSP-As the pitch can be from 0.5 to 0.65 mm. The basic structure of a CSP-A is shown in figure 2-20. An example CSP-A is shown in figure 2-21.

In one chip scale array the chip is attached to an interposer that contains an interconnection method designed to translate bonding sites on the chip to a large array. The interposer is connected to solderable balls, posts or planar lands

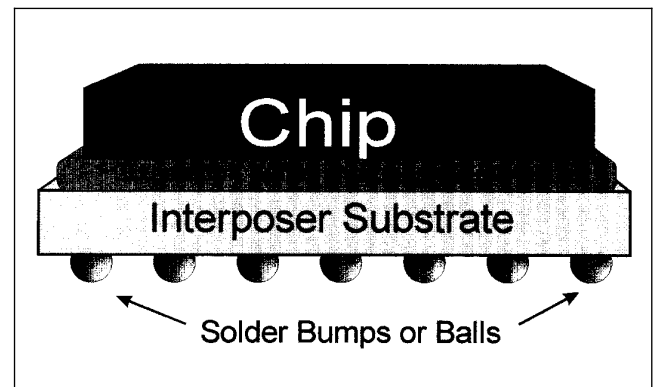


Figure 2-20 Chip Scale Grid Array Package (CSP-A)

on the bottom. The chip interconnection methods to the interposer include wire bonds, flip chip bumps and TAB style ribbon leads.

2.2.1.1 Micro BGA (μ BGA)

In constructing a micro BGA, a flexible circuit similar to a TAB circuit is attached to the surface of the IC by means of a semiconductor grade elastomer. This flexible circuit structure forms the basic interposer. Thin flexible ribbon like bond leads of metal such as gold, gold plated copper, gold plated nickel etch are then bonded directly to the gold or aluminum pads on the IC. (See figure 2-22). While the illustration shows a single metal layer construction, micro BGAs can and have been fabricated with two metal layers for power and/or ground distribution and controlled impedance designs for highest level performance.

The elastomer or compliant polymer layer serves to decouple the differential expansion of the silicon and from that of the interconnection substrate. This compliant layer together with the "S" shaped bond lead ribbon effectively decouple the devices from the strains of thermal expansion. The novelty is contained in the ability to create a compliant

Elements of a Chip Scale Array Package

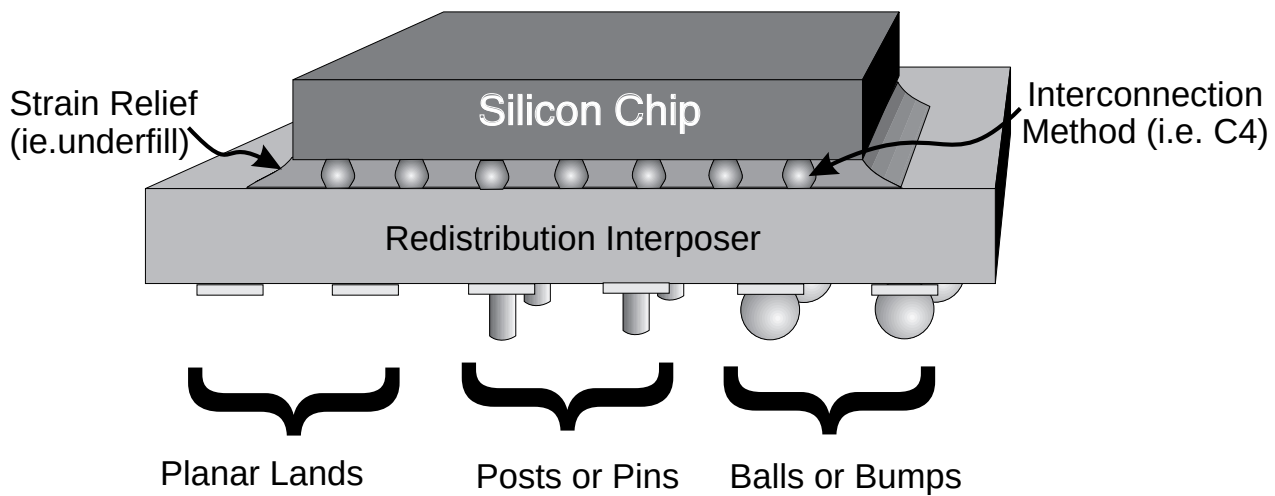


Figure 2-21 Example of Chip Scale

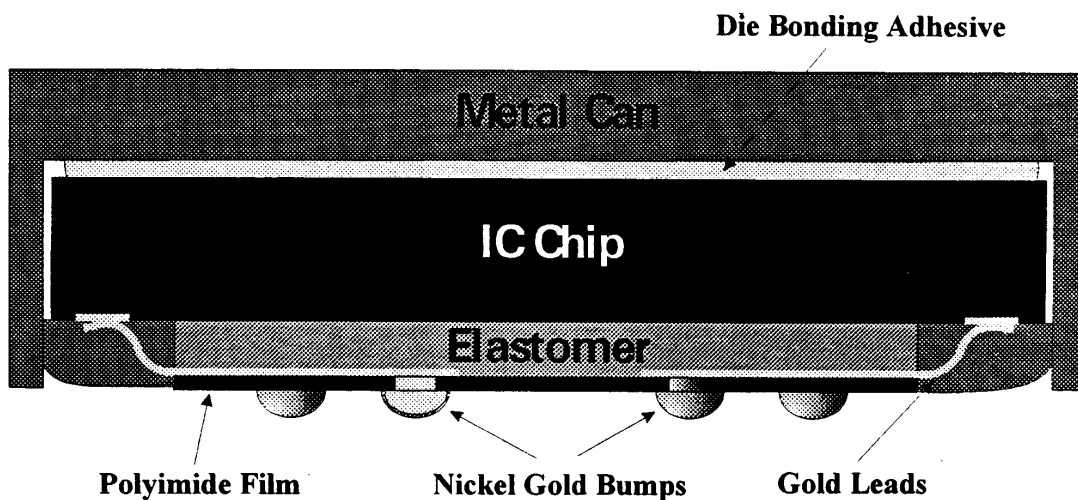


Figure 2-22 Micro BGA

packages that are compliant in X, Y, and Z direction, facilitating both test and assembly while enhancing reliability.

The package is interconnected to the substrate by means of either nickel-gold bumps or solder balls. The I/O grid pitch for the micro BGA are typically spaced at bump pitches which are increments of the international Electrotechnical Commission's Publication 97 recommended base pitch of 0.5 mm. Depending on the lead count and bump pitch, the micro BGA area can vary from die size to several times the chip area. Smaller chips may require a fan-in/out approach to layout due to the area required by the bumps.

Finally, the micro BGA is amenable to mass processing at the wafer level, thus making it possible to move the pack-

aging and assembly process to the end of the wafer fab process, affording a very low cost method of packaging ICs.

2.2.1.2 Mini BGA

The mini BGA is very similar to the flip chip described previously, but it utilizes different metals than flip chip (see figure 2-23)

The chip is coated with polyimide resin. Vias are etched into the resin to access the chip's bonding pads. Metal is deposited and patterned from the via to the polyimide surface. Solderable balls are attached to the via connection sites.

The lead count of the mini BGA is limited to the chip area.

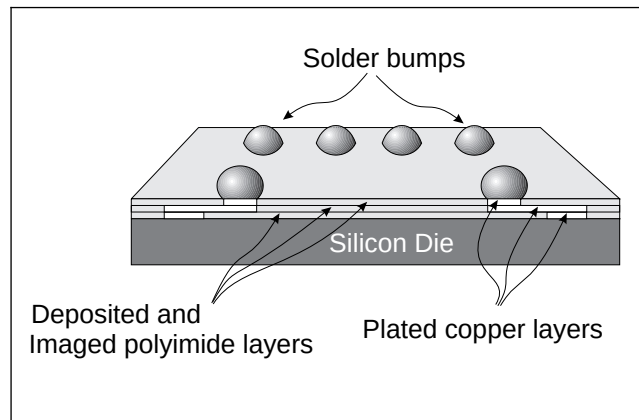


Figure 2-23 Mini BGA

and the assembly limits of the bump pitch.

2.2.1.3 SLICC

SLICC stands for Slightly Larger than IC Carrier. Its construction uses flip chip mounting on a rigid organic interposer to create the chip scale package with redistributed I/Os. An underfill epoxy is injected around and under the chip and the bumps. The purpose of the underfill is to constrain the CTE of the organic interposer so that it is close to the low CTE of the silicon chip. The interposer is connected to the PCB via solderable Cu-Ni balls.

As with the micro BGA, the SLICC area is dependent on the number and pitch of the balls. (See figure 2-24)

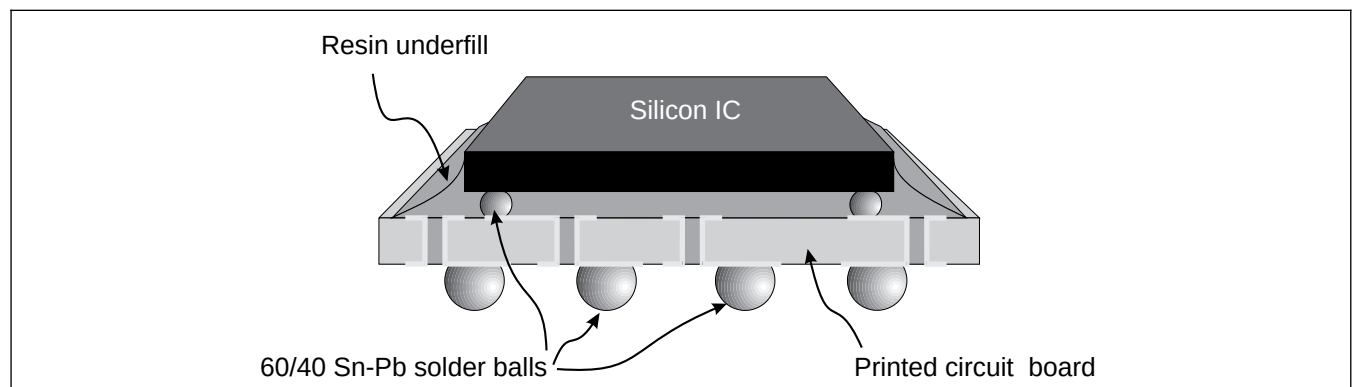


Figure 2-24 SLICC Chip Scale Grid Array

2.2.1.4 Chip Scale Package

A flip chip like package called a “CSP” has been reported. This CSP is constructed of an LSI semiconductor chip, a thin plastic resin and electrode bumps.

The package has neither leadframe nor any bonding wires (figure 2-25). The chip surface is insulated from the chip wiring pattern and conductor paths are redistributed on the face of the die and are electrically connected to external electrode bumps (figure 2-26). Since the internal/external pad locations can be adjusted by those wiring conductor patterns, this package does not impose any additional restrictions on LSI designers.

Several process improvements involving material selections and reliability studies have been executed in the package development.

2.2.1.5 Peripheral to Area Array Converter

The Peripheral to Area Array Converter (PAAC) technology provides standard peripheral array chip pad ICs with redistribution and voltage planes made from organic dielectrics and copper, for low resistivity, and an area array of solder bumps. The PAAC employs a thin film transfer process either at the wafer or bare die level. This allows for yield testing of the completed thin film add-on prior to transfer and minimizes IC exposure to processing. The solder bumps are simultaneously electroformed to make electrical contact from the IC chip pad to the redistribution lines and to produce the area array at the surface. The chip pad contact method is the photolithographic “Reach Through Via” (RTV) made by thin film patterning, dielectric etch and metal deposition processes. (See figure 2-27)

As few as one (simple fan-in redistribution wiring) and as many as four layers may be transferred in a single step. The more complex structure is comprised of intra-chip “net list” redistribution which translates and optimizes the chip I/O to the system interconnect requirements. This significantly reduces the wiring burden and resulting complexity and thereby cost in the inter-chip substrate.

Voltage layers provide for low inductance power supply

and impedance control of the interconnect line from the point of the output of the chip driver, to the substrate and into the receivers. An elastomeric mechanical buffer layer at the IC/PAAC interface enables reliability from thermal cycle induced solder connection fatigue failure due to chip and substrate CTE mismatch. A Multi-chip Module or Chip on Board system utilizing PAAC may be reworked by means of solder reflow of the failed IC die. PAAC high volume production costs for bare die transfer are estimated to be comparable to wire bonding. Wafer level transfer significantly reduces cost.

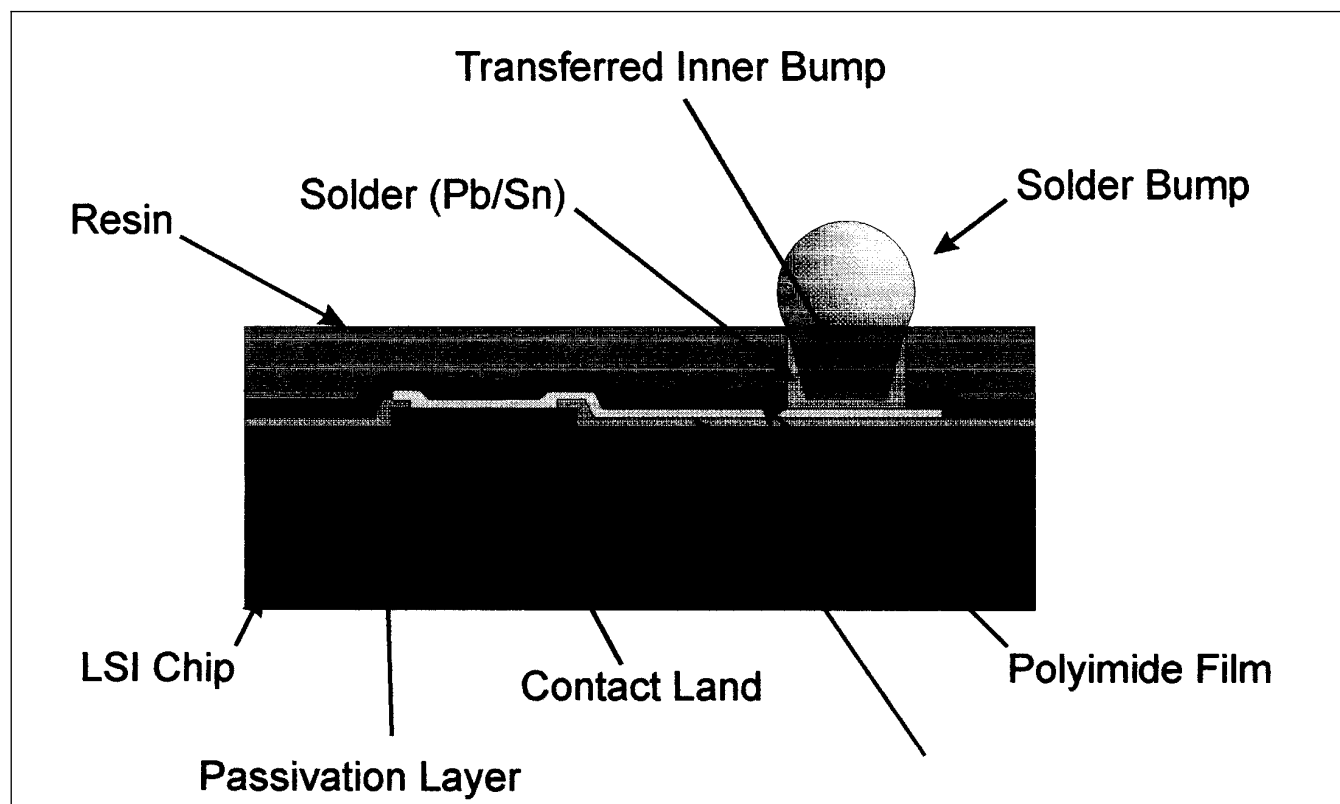


Figure 2-25 Chip Scale Package

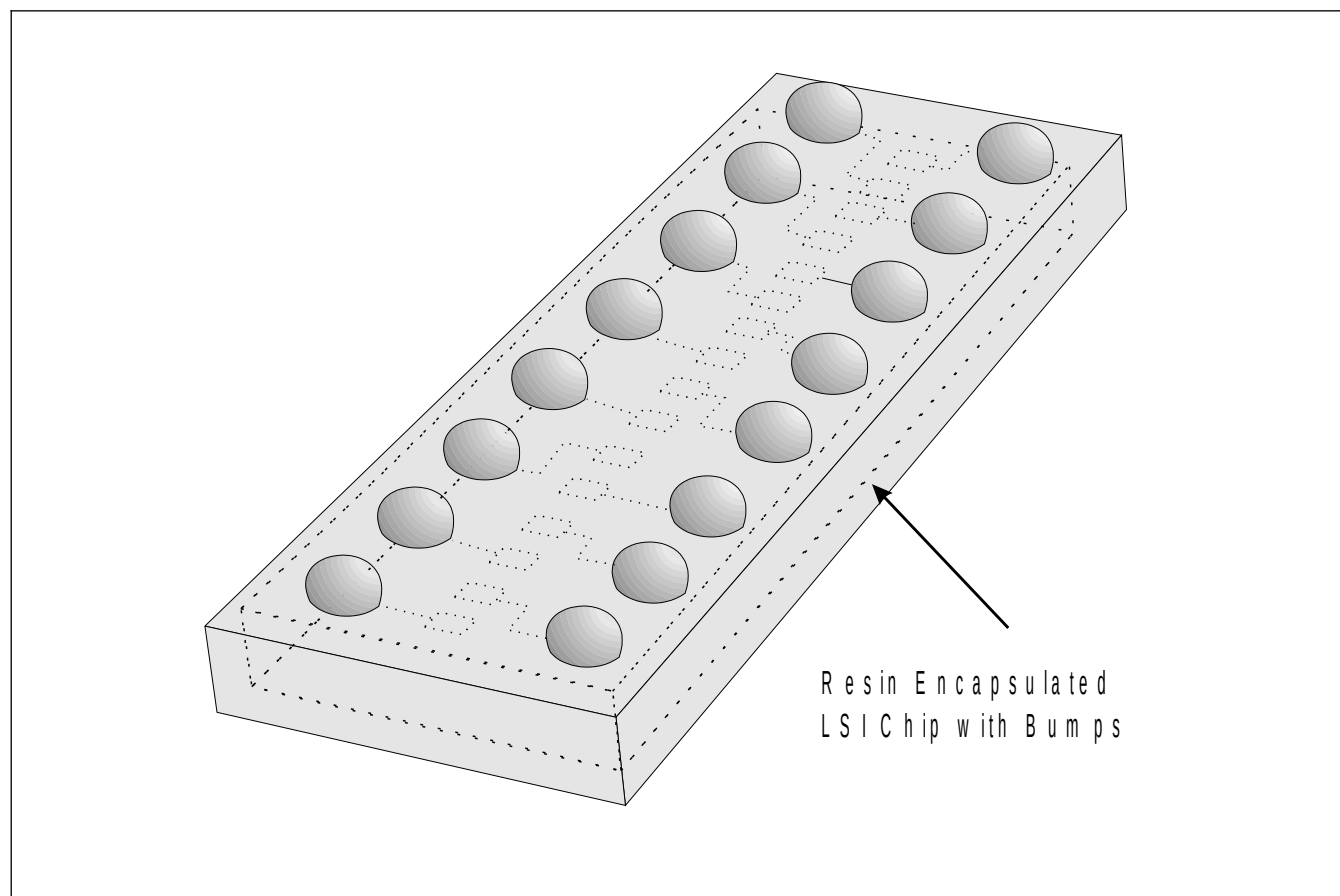


Figure 2-26 Resin Encapsulated LSI Chip with Bumps

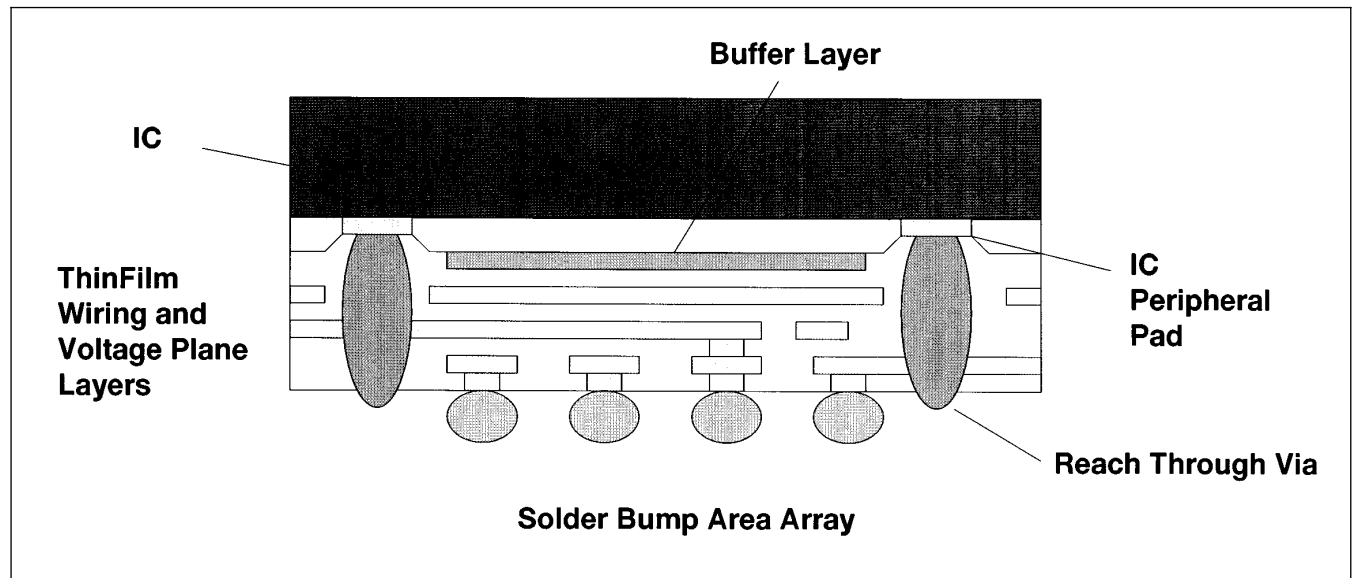


Figure 2-27 Peripheral Area Array Converter

2.2.2 Peripheral Ledged Chip Scale Packages (CSP-P)

Peripheral ledged chip scale packages are those that make use of, or replace the existing bonding pads on the semiconductor chip. TAB is one form of peripheral package and qualifies as a chip scale package if the TAB area is within the area defined for chip scale packages. (More information is available on TAB in the document SMC-TR-001 available from the IPC).

Beam lead technology is another chip scale peripheral approach that is still used for microwave devices.

New ideas for chip scale packages have developed. One of these is the Micro SMT or MSMT package. This package consists of metallized silicon or GaAs posts and metal beams. The chip, the posts, and the beams are encapsulated in an epoxy or similar compound.

2.2.2.1 Micro SMT or MSMT Package

The micro SMT or MSMT package evolved from the microwave industry as a replacement for the beam lead package. The MSMT package was invented in 1990. The chip scale grid array packages evolved from the combined concepts of flip chip and ball grid array technologies.

MSMT packages, like flip-chips, are created while the semiconductor chips reside in wafer form. Most chip scale grid arrays are attached to the chip after it has been singulated from the wafer.

The MSMT package is formed by micro-machining the semiconductor, while in wafer form to create posts. The micro-machining starts by depositing and patterning metal from the junction to the top of the post site, forming a beam. An encapsulant covers and protects the chip, posts, and beams. A cut away drawing of a MSMT packaged IC is shown in figure 2-28.

The post site may be in the saw lane, or where the bonding

pads reside. Locating the posts in the saw lane, illustrated in figure 2-29, adds silicon area to some devices, which may reduce cost savings, size reduction, and gross die per wafer. A more optimal application of the MSMT package is to design the post sites over the bonding pads, as illustrated in figure 2-30.

A cross-sectional view of an MSMT package is shown in figure 2-31, showing the use of a cap. For larger chips, a cap of silicon, glass or ceramic is placed on the epoxy and the wafer. This cap provides an additional heat removal path, and it helps to planarize the posts to within ± 3 microns of each other.

The wafer is thinned and flipped over and the remaining silicon that holds the post is etched away. Metals are deposited on the sides and bottom of the post. The solderable metals provide a low resistance path from the bottom of the post through the beam and to the chip.

MSMT posts are located on the periphery of the chip (see figure 2-32). They add little area to the chip. The primary lead count range covered by MSMT packages is from 2 to 100. Higher lead counts are limited primarily by the printed board fabrication and assembly pitch limitation rather than packaging limitations. MSMT posts for 2 to 100 leads are fabricated with areas of 0.1 mm square on 0.30 to 0.65 mm pitch. Package sizes depend on the chip size, but range from 1005 (1 mm by 0.5 mm) to 20 mm by 20 mm.

2.2.2.2 Chip Scale Peripheral Packages

Another form of CSP with peripheral leads has been developed using a planar lead frame. The lead frame provides the redistribution of the chip bonding sites from the corner to the peripheral.

The chip is wire bonded to the lead frame and is then encapsulated to protect the wiring and the chip.

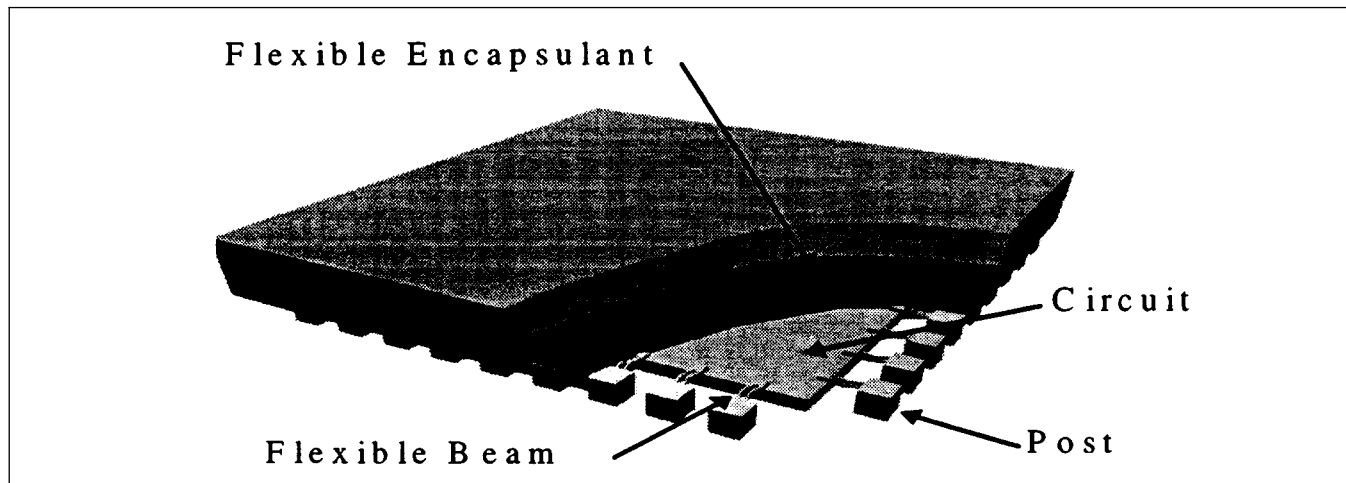


Figure 2-28 Cutaway View of an MSMT Packaged IC

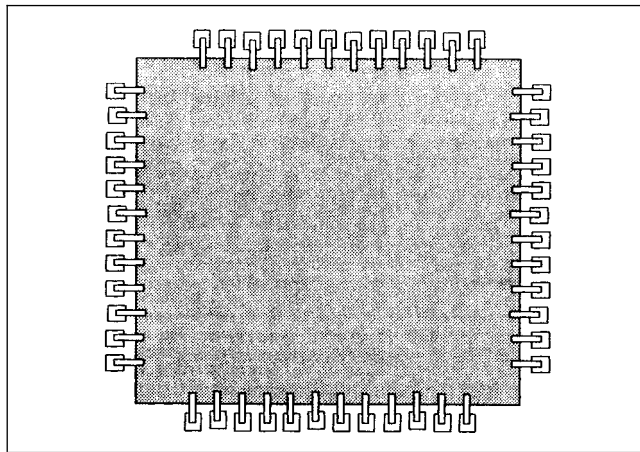


Figure 2-29 MSMT Posts in Saw Lane

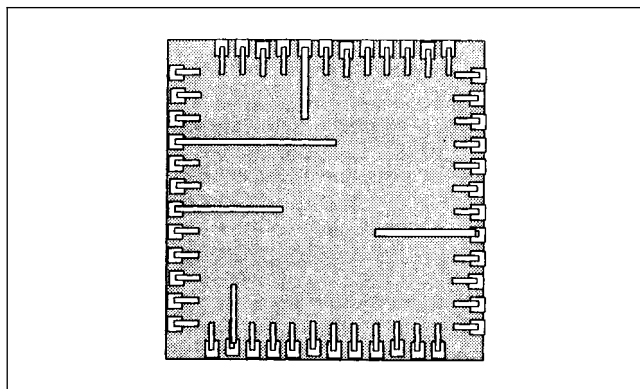


Figure 2-30 MSMT Posts in Bonding Pad Area

(see figure 2-33). As in many of the chip scale packages the back of the die is accessible for heat transfer.

2.2.3 Advantages and Disadvantages of Chip Scale Technology

There are many characteristics of flip chip and chip scale technology that need to be compared in order to select the most appropriate package technology. Advantages of flip chip has been stated in 2.1.8. Some of the advantages of chip scale are:

- Packaged semiconductors are very close to the size of unpackaged die
- Packaging the chips allows for easier handling, testing, and assembly than bare die or flip chips
- Chip scale packages assemble to PCBs without the need for additional materials, such as underfill epoxy and processes than currently used for SMT assembly
- Chip scale packages add minimal electrical and thermal parasitics
- Preliminary reliability data for several of the chip scale packages shows results matching current SMT package levels
- Some of the chip scale package technologies produce less expensive packages than conventional SMT packages

There are also several limitations and concerns with Chip Scale Packages. These include:

- Availability of most chip scale packages is very limited
- Reliability data for most technologies is preliminary
- Useability data for all chip scale packages is limited

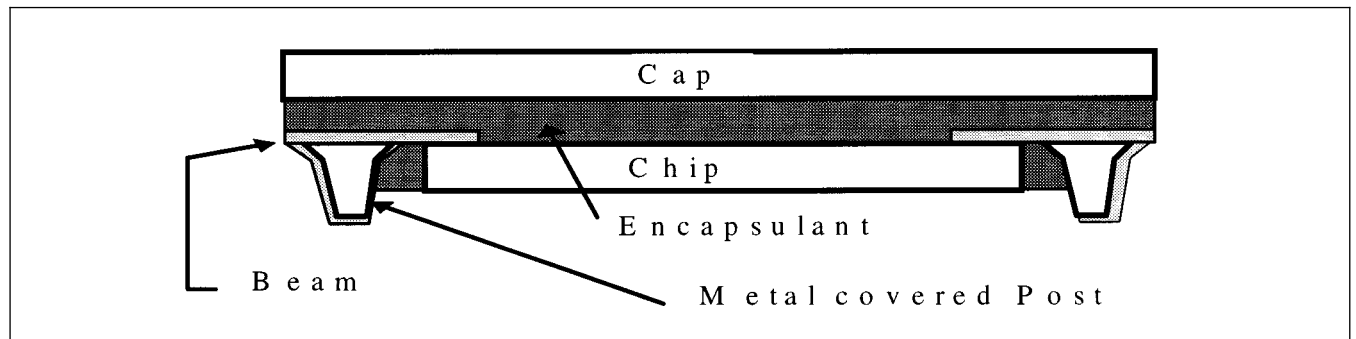


Figure 2-31 Cross-Sectional View of an MSMT Package

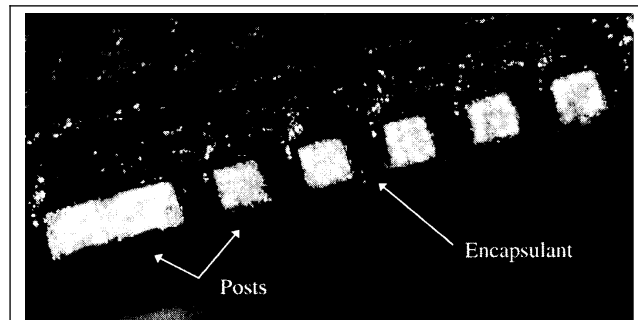


Figure 2-32 Close-up Photo of MSMT Posts, Encapsulant and Bottom of the Chip

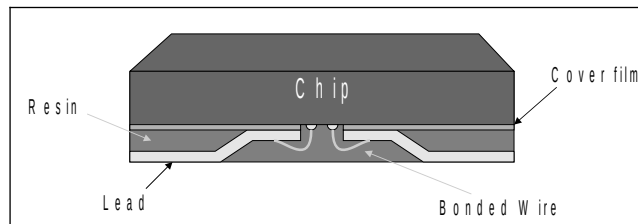


Figure 2-33 Chip Scale Peripheral Package

3 APPLICATIONS OF FLIP CHIP AND CHIP SCALE

Over the years there have been many applications of flip chip technology. Chip scale technology is now becoming a viable solution for those companies that prefer a more ruggedized approach to bare chip mounting. Table 3-1 illustrates some of the applications for flip chips.

Table 3-2 provides a comparison of different commonly used technologies including flip chip, micro-BGA and MSMT. Section 4 provides more detailed descriptions of each of the cited chip scale technologies.

Table 3-1 Commercial Flip Chip and Chip Scale Applications

Application or Market	Bump Type				Number of I/O's	Organic Substrates	Bonding Method
	Material	Fabrication Method	Layout	Pitch μm			
Automotive	SnPb on Cu InPb	Electroplate, print	Peripheral Array	250- 400	10-100	Ceramic	Mass reflow
Computer	SnPb	Evaporate, Electroplate	Array	210-250	500+	Ceramic	Mass reflow
LEDs, MCMs	Au, SnPb	Plate	Peripheral Array	63.5-100	110-126	Glass, silicon	mass reflow UV cure resin
IC Cards	SnPb	Electroplate	Peripheral	140-160	100	Laminate	Mass reflow
Computers, Telecom. (cellular) IC Cards	SnPb	Evaporate Electroplate	Array	250	300-500	Laminate	Mass reflow
Telecommunications including pagers	SnPb	Lift-off evaporation	Peripheral	200	20-40	Ceramic Laminate	Mass reflow
		Print	Array	150-200	8-40	Silicon	Mass reflow
		Plate or Evaporate	Array	225-350	84-400	Laminate, ceramic	Mass reflow
Power amplifier for cordless phone	Au	Electroplate	Array, peripheral	Varies	<20	Ceramic	Thermocomp. bond
Watch Module	SnPb on Cu	Electroplate, Print	Peripheral	200	13-60 (15 typ)	Laminate	Compression bond
LCD	Au or Au-plated	Plating	Peripheral	216	10-20	Glass	Conductive adhesive
LCDs (camcorder view finder/pocket TV	Au	Stud bump bond	Peripheral	100-140	110-126	Glass	Conductive adhesive
Military (FPA)	In	Electroplate	Array	100	4096	3D Si stack	Reflow
Military	In, Au, SnPb	Evaporate	Array	50-120	100-262, 144	Si, saph. cer.	Cold weld
Military LCD	Au	Microballs (LETI-proc.)	Peripheral	50-100	100-200	Si, glass	Hot gas

Note: Quite often conductive adhesives are used to connect bumped chips to various substrates .

Table 3-2 Comparative Table of Various Technologies for a 100 Lead 10x10 mm Die

Package Parameter	Bare Die (with wire bonds and pads)	Flip-chip	0.3QFP	μBGA	MSMT
Pitch, mm	0.15	0.25	0.30	0.50	0.30
Footprint Area, mm^2	125	120	785	150	110
Package/Chip Area	1	1	6.30	1.20	0.90
Height, mm	0.4 to 0.6	0.5 to 0.7	1.4 mm	0.84	0.5 with cap 0.3 without
Inductance nH (circuit length)	1-2 (0.75 mm wire)	0.1-0.2 (0.5 mm bump)	1 to 7 (0.7 to 3 mm wire and lead)	0.5-2.1 (1 mm bump)	0.1 to 0.2 (0.5 mm post and bridge)
Capacitance pF	0.2	0.03	0.5-1	0.05-0.2	0.02 to 0.03
PCB Attachment	wire bond & epoxy die attach encapsulant	solder & underfill epoxy	solder	solder	solder

4.0 DESIGN CONSIDERATIONS

Flip chip technology began as an interconnection technology developed by IBM during the 1960's as an alternative to manual wire bonding. In this methodology the chip is attached to circuitry facing the substrate. Solder bumps are deposited onto a wettable chip pad that connects to matching wettable substrate lands as shown in figure 4-1.

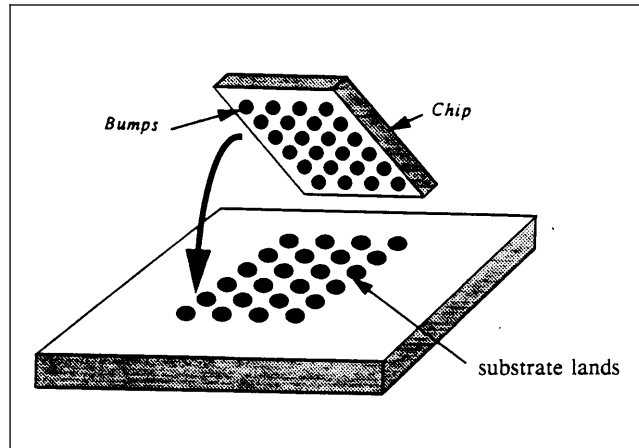


Figure 4-1 Flip Chip Connection

Flipped chips are aligned to corresponding substrate metal patterns. Interconnections are formed by reflowing the solder bumps as shown in figure 4-2 simultaneously forming the electrical and mechanical connections. The joining process is self-aligning, i.e., the wetting action of the solder will align the chip bumped pattern to the corresponding substrate lands. This action compensates for chip-to-substrate misalignment incurred during chip placement.

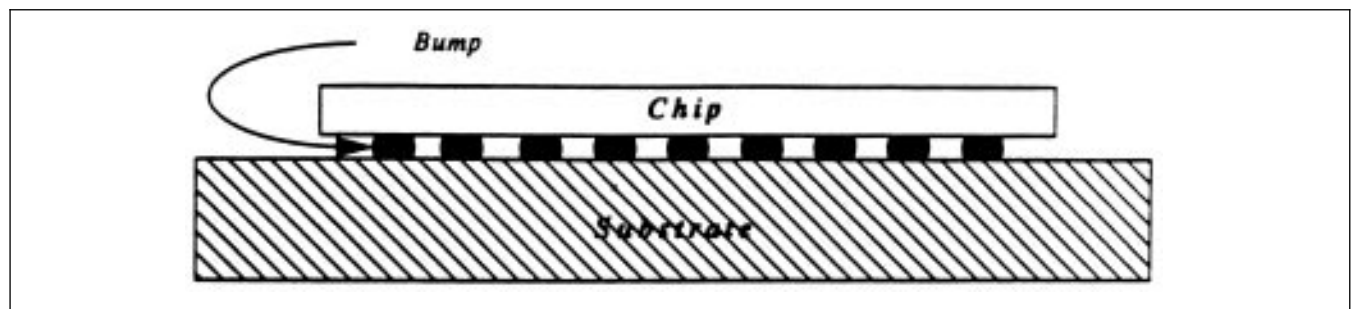


Figure 4-2 Mechanical and Electrical Connections

An added feature of the flip chip process is the potential to rework. Several techniques exist that allow the removal and replacement of chips without scrapping the chip or substrate. Depending on substrate material, rework can be performed numerous times without degrading the quality or reliability provided that the mounting substrate can tolerate the rework temperatures.

Injection of chip underfill, as illustrated in figure 4-3, improves reliability most notably in cases of high mechanical stress. It should be noted that currently any rework must be performed prior to the application of chip underfill.

An alternate joining technology to reflowable bump flip chip is one that has low melting solder bumps attached directly to a printed board. The bump on the semiconductor die is not reflowed, instead the lower melting solder on the printed board wets the bump on the die to form the interconnect.

4.1 Chip Size Standardization

Standardizing the size of semiconductor chips may appear to be counter to the objectives of the chip designer and supplier. Many chip suppliers rely on the ability to shrink the size of a chip as it matures. This results in more good chips per wafer. This strategy is sound if the chip is the dominant cost item for the product.

Today many products are dominated by packaging, as opposed to chip cost. Prime examples are discrete diodes and transistors, low lead count logic devices and general purpose analog chips. These products benefit from the cost reduction and performance improvements possible with chip scale packaging.

Chip suppliers and their customers will benefit if when converting their die to chip scale packages they adhere to area size standards. These standards are established by the EIA/JEDEC JC-11 Committee. The committee develops standards for outlines for semi-conductor devices as their counterpart in the EIA Committee develops standards for passives.

Accepting chip size standards will reduce the need for many different tape stocks for the tape and reel packaging

of these devices. Standards will also allow users multiple sources for the same device.

4.1.1 Bump Site Standards

The chip scale bump grid array packages give chip designers significant freedom to choose the bump location and the signal type transmitted on the bump. Chip suppliers should observe standards for grid pitch, bump size, and bump location.

Optical assemblers will use placement machines that will place the package based on the edge dimensions. This is because the machine can't see the bump locations.

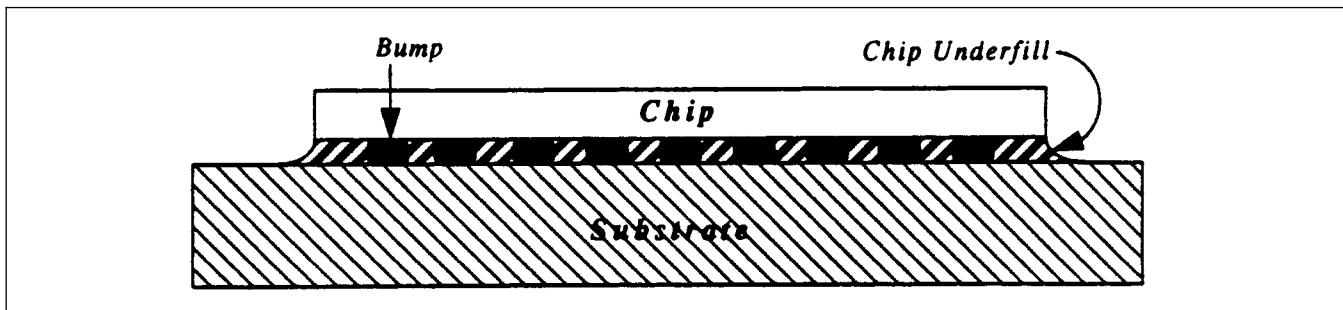


Figure 4-3 Joined Chip with Chip Underfill

placement accuracy and assembly yield will depend on the assumed location of the bumps relative to the distance from the edge of the package and the bump grid.

4.1.2 Peripheral Lead Standards

The lead pitch standards for peripheral lead chip scale packages, such as MSMT should follow the existing standards set by the JEDEC JC-11 Committee. Applicable pitch standards are 0.2 mm, 0.3 mm, 0.4 mm, 0.5 mm, 0.63 mm, 0.65 mm. Refer to JEDEC publication JEP-95 for detailed dimensions.

4.1.3 Package Size Standards

The use of package sizes and tolerances as published by JEDEC in the JEP-95 publication is highly recommended. For smaller sizes, such as those applicable to MSMT and other packages, the use of the size dimensions published in the EIA publication PDP-100 is recommended. However, be sure to refer to the suppliers package drawings in all cases where there may be deviations.

4.2 General Considerations for Flip Chips

Flip chip technology encompasses preparation of the chip surface, deposition and shaping of the bumps and joining the bumped chips to a substrate. The main physical attributes consist of four primary components. These are:

- Final Metal
- Passivation
- Metals/Under Bump Metals
- Bump

Each component plays a key role and all components work together to form the appropriate connection as shown in figure 4-4. The design of the bump, the land pattern, and the fabrication are essential to forming a strong, reliable and high performance interconnect.

4.2.1 Final Metal

Final Metal is the top layer of metallization (typically aluminum) on a chip. It may be the first layer or the fourth of n^{th} depending on the device complexity. The solder bump connects downward through the Final Metal to the chip. All electrical paths to and from the chip travel through the Final Metal.

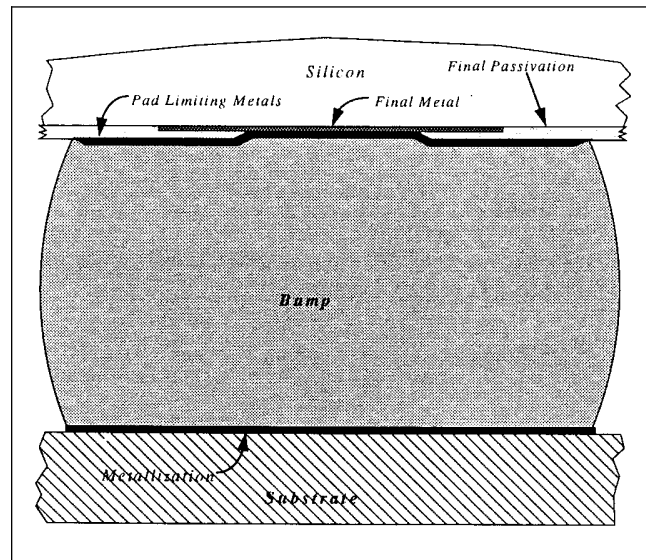


Figure 4-4 A Solder Bump Flip Chip Connection

Redistribution, illustrated in figure 4-5, is the relocation of original terminal locations to preferred bump sites. This requires a new metal layer that becomes final metal as illustrated in figure 4-6.

4.2.2 Passivation

Passivation consists of a layer of protective films that coat the Final Metal and chip. These films can vary with semiconductor technology, e.g., CMOS, bipolar, BiCMOS, etc. and with the wafer fabrication facility. These films are deposited and imaged with standard wafer processing techniques.

There are many types of passivation in practice, some of which are silicon nitride, silicon oxy-nitride, spin-on-glass, polyimide, and sputtered SiO_2 . Figure 4-7 illustrates passivation for a CMOS product showing cured polyimide covering inorganic chip passivation. It must be noted that sidewall profile is critical.

The cross-section of passivation shown in figure 4-7. Polyimide is recessed from the chip passivation because the same mask is used to pattern the chip and the passivation layer plus different processing is used for each layer.

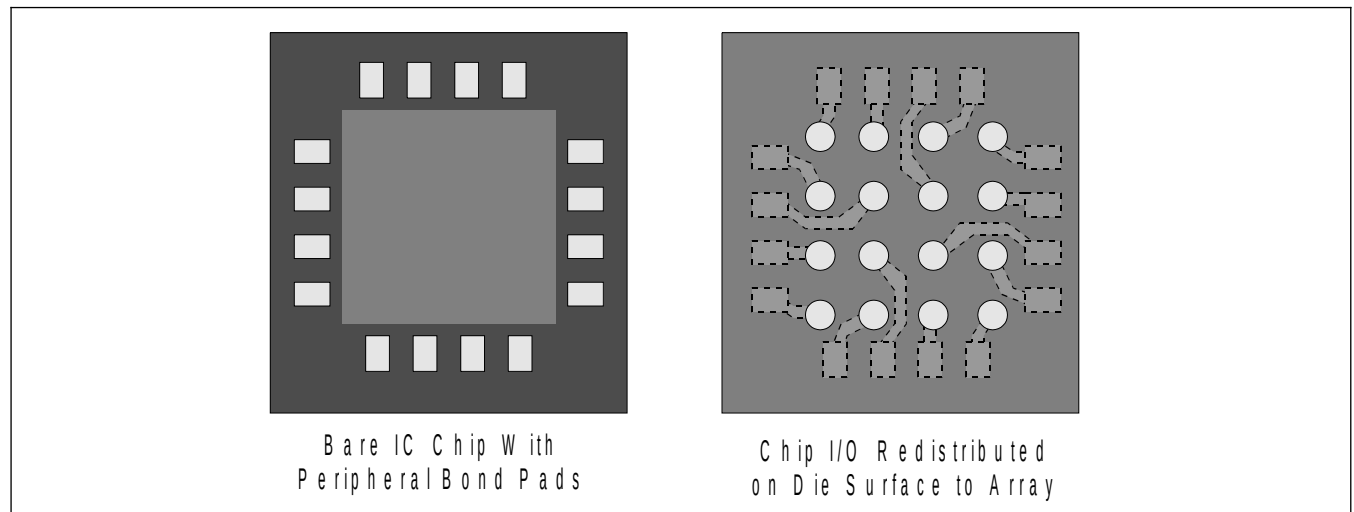


Figure 4-5 Two Simple Chips, Showing Original Pad Locations and Rerouted Bumps

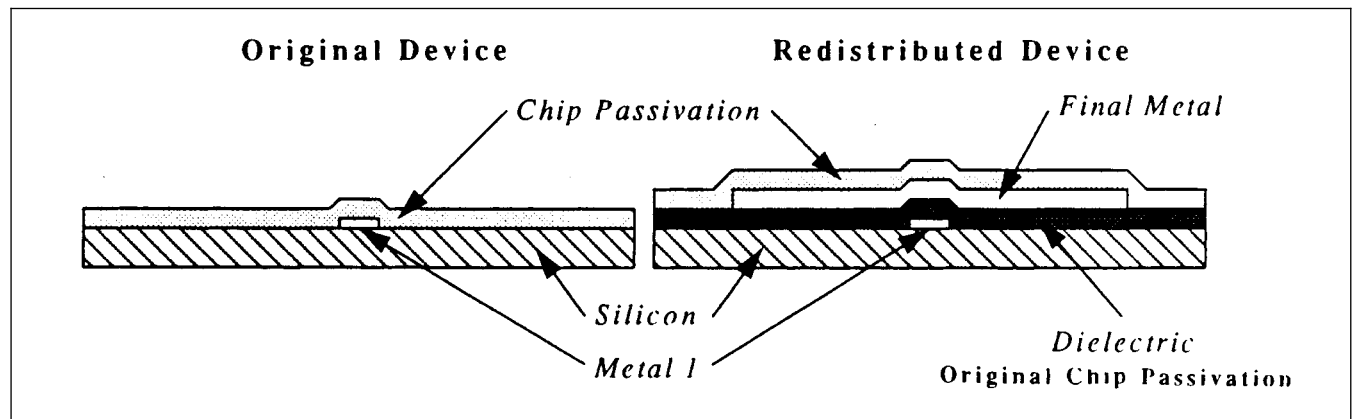


Figure 4-6 Redistribution of a Single Metal Layer Device

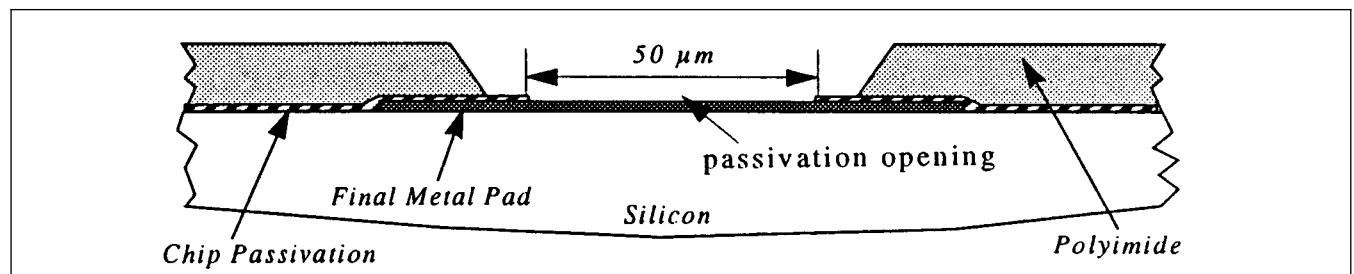


Figure 4-7 Passivation (Cross-Section)

Chip passivation provides moisture, ionic and physical protection to the chip, adhesion, and electrical insulation to the pad limiting metal.

Openings in the passivation are centered over the Final Metal pads to allow contact of the pad limiting metal (PLM) to the Final Metal pad as shown in figure 4-8.

4.2.3 Pad Limiting Metals

The Pad Limiting Metal (PLM) is a solder wettable terminal metallurgy that defines the size and area of a soldered connection, limits the flow of the solder bump, and provides adhesion and contact to chip wiring. Requirements of the PLM are:

- Low electrical contact resistance
- Good adhesion to passivation and aluminum
- Reliable diffusion barrier
- A wettable metal
- Good adhesion between PLM layers
- Protection of final metal from the environment

Table 4-1 shows some commonly used PLM systems for each of the desired properties.

PLM systems are deposited after oxide removal of the final metal. Common deposition methods include evaporation and sputtering. Figure 4-9 shows an example of pad limiting metals.

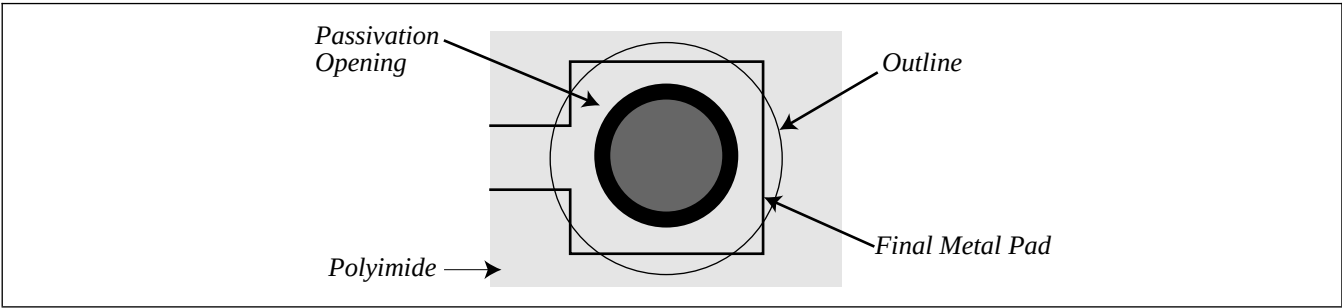


Figure 4-8 Schematic Plan View of Bump

Table 4-1 Commonly Used PLM Systems

Characteristic	Pad Limiting Metal Combinations				
Adhesion	Ti	Al	Cr/Cu	TiW	TiW
Diffusion	Pd	Ni	Cr	TiW	TiW
Wettability	Au	Cu	Cu	Au	Cu
Oxide Preventor	—	—	Au	—	Au

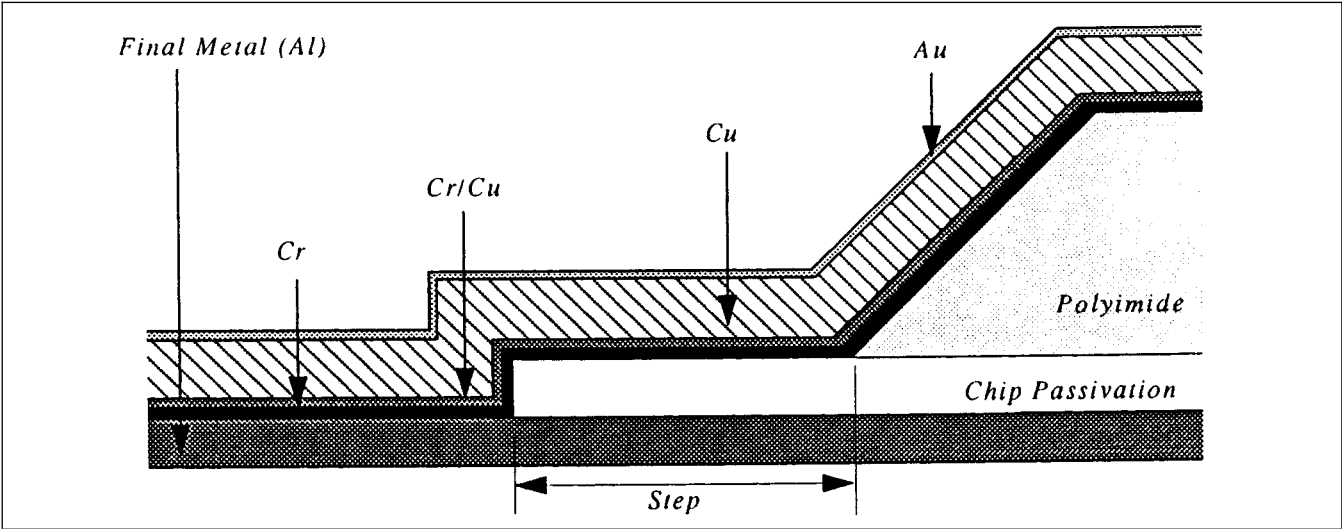


Figure 4-9 Example of Pad Limiting Metal

The IBM process requires a sputter clean to prepare the Final Metal. Chrome is deposited as a barrier and adhesion promoter to the aluminum and polyimide. Next, copper and chrome are co-deposited to enhance inter-metal adhesion. Then a thick layer of copper is deposited as the primary wetting surface for the bump. This is followed by a flash of gold to inhibit copper oxidation.

4.2.4 Solder Bump

The solder bump forms the electrical and mechanical bridge between the chip and next level assembly. It absorbs the stress between the chip and next level of assembly caused by variations in their relative thermal expansion rates.

The solder composition of the flip chip bumps varies according to required mechanical and thermal properties. Common bump compositions include:

- 90 PbSn

- 97 PbSn
- 63 SnPb
- 50 InPb
- 95 PbSn

In addition, conductive polymer bumps are also used. With the IBM process, an evaporated shadow mask or bump mask is used to define the solder bumps. Once the bumps are deposited, the Bump Mask is removed, and the bump resembles a truncated cone as depicted in figure 4-10. A subsequent non-oxidizing reflow process yields the final round C4 Bump illustrated in figure 4-11.

Electrodeposition offers a wider range of SnPb composition than evaporation, and thus offers greater control over mechanical and thermal properties. Electrodeposition also produces smaller diameter bumps and is more difficult to control uniformity.

A variety of solder paste compositions can be screen printed. Delco Electronics printed InPb which contains

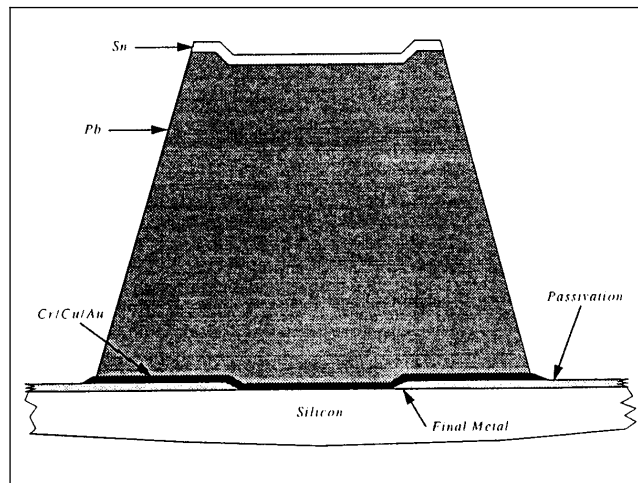


Figure 4-10 Initial C4 Bump

lower processing temperatures and provides improved compliance and fatigue life.

Common bump diameters and minimum pitches are shown in Table 4-2. Minimum pitch requirements are based on radial distances (center to center) between bumps. Bump diameters are measured at the widest point of the ball.

Table 4-2 C4 Bump Diameter and Minimum Pitch Options

Deposition Types	Diameter (μm)	Minimum Pitch (μm)
(A) Evaporation or Electrodeposition	150 μ	300/350
	125	250
	100	225
(B) Screen Printing	200	375
	150	250*
	125	200*

*peripheral only

It should be noted that 250 μm pitch is the most commonly used for the evaporative and electrodeposited bump process, due to its ease of manufacture and smaller pitch capability; 225 m pitch is used for very high interconnect density applications. Generally the larger bumps provide improved reliability.

Today, for flip chip applications, minimum pitch requirements are larger to account for printed board wiring capabilities. An example of typical DCA bump design is shown in figure 4-12.

4.2.5 Existing Chip Designs

To take complete advantage of flip chip technology, the chip designer must comprehend substrate and system requirements. However, the bumping process may be implemented on existing chips without circuitry redesign. An advantage of wafer fabrication is that wafers can be built to the point where they can be split for bumping, or packaging.

If the existing perimeter wirebond or TAB pads do not vio-

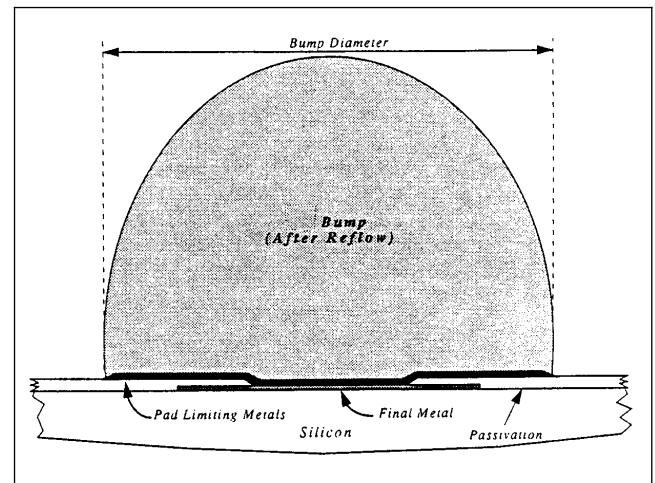
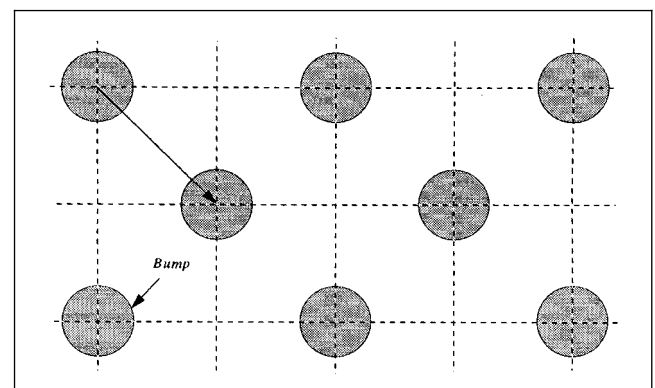


Figure 4-11 A C4 Bump After Reflow

Figure 4-12 Recommended DCA Grid Pitch (250 μm Grid, 150 μm Bumps)

late the minimum bumping ground rules for pitch and location, bumps can be located on or near these existing sites. If the existing perimeter pads violate the minimum ground rules, an extra layer of redistribution metal (final metal covered with additional passivation) will be required.

In either case, a wire bond or TAB chip can be converted to a bumped or posted chip. This is appealing to those trying to implement flip chip or reduce module to package area but cannot afford the time and/or cost to design of a new chip.

4.2.6 I/O Capability

With the chip bumping process nearly the entire chip surface can be utilized for interconnect pad locations. In fact, over 2500 bumps on a chip has been demonstrated and chips with over 1500 bumps are in production.

Chip bumping enables increased interconnect density. Signal, clock and power connections can be placed almost anywhere on the chip and redundancy means distributions can be optimized for minimum noise and skew, current density and line length. Additionally, on-chip wiring can be reduced since the z-axis escapes are available where needed.

Figure 4-13 compares single row wire bond and bump chips. Each chip is 8 mm square. Wire bond pad size is 76 μm with pads on 100 μm centers. Bump size is 100 μm bumps on a 230 μm center. In this example, interconnect density is increased over 2.4X using bumping technology.

ticle track as shown in figure 4-15.

Many materials used in semiconductor packaging emit low levels of alpha particles. This is illustrated in table 4-3.

Emission rates vary for solder and chip underfill depending

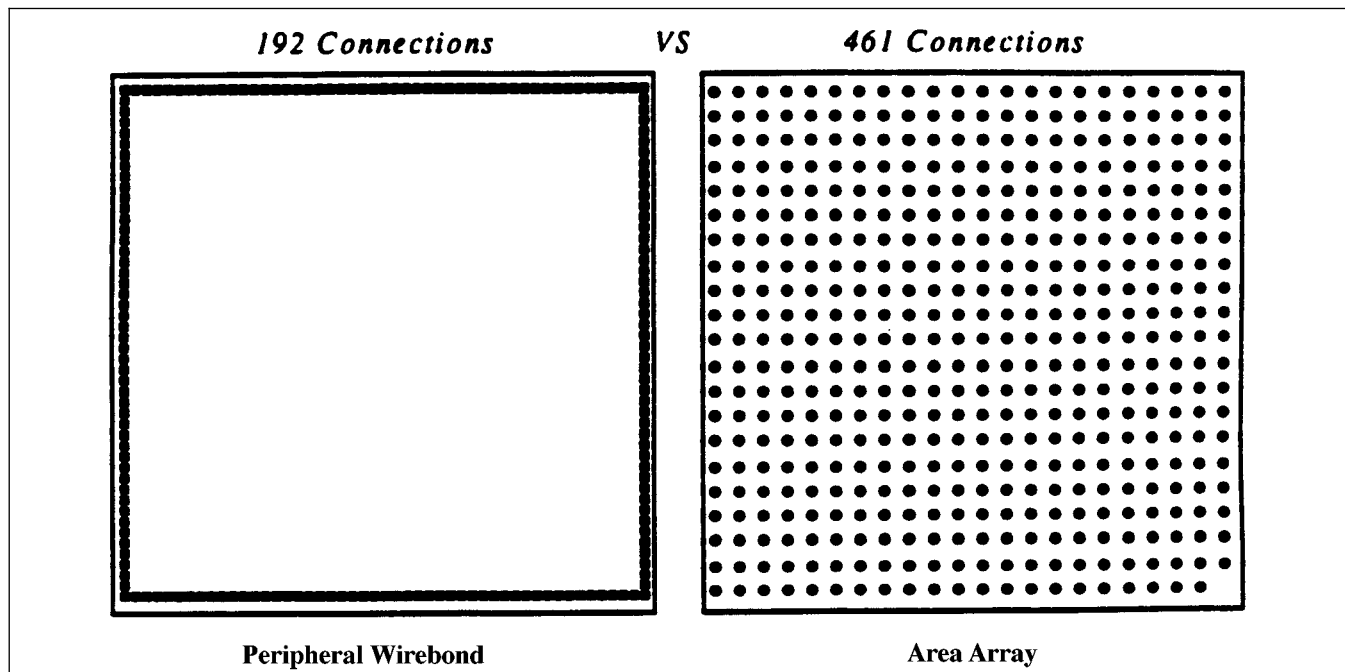


Figure 4-13 Interconnect Density (Peripheral vs. Area Array)

4.2.7 Alpha Particle Emissions (Soft Errors)

Alpha particles may cause soft errors in semiconductor devices. Circuit sensitivity to alpha particle emissions and the allowed soft error rate must be clearly understood for each chip design.

Lead contains traces of thorium and daughter elements, e.g., polonium, which emit alpha particles. Circuits resistant to soft errors are designed to withstand alpha particle emission energies.

Circuits sensitive to soft errors are DRAMs, closely followed by SRAMs and some flip-flop circuitry. Sensitivity increases as chip geometries shrink and device (node) critical charge diminishes.

The primary concern of the particle emission is the energy that can be imparted to the device circuitry. This is quantified and illustrated in figure 4-14.

- Alpha Particle = He nucleus = 2 protons + 2 neutrons
- Up to 8.8 MeV of kinetic energy
- Energy converted to electron/hole pairs (3.6 eV per E/H Pair)
- Highest charge density near end of emission track.

The resulting effect of an alpha particle can be a distortion of the depletion region's electric field near the alpha par-

Table 4-3 Alpha Particle Emissions of Semiconductor Materials

Material	Activity [$\text{a}/(\text{cm}^2\text{-hr})$]
High Lead Solder (3/97)	0.05 - 10.0
Alumina	0.1
Chip Underfill (cured)	0.002 - 0.020
Plastic	0.04
Silicon Wafer	<0.004

on the material source. Certain solders may emit a higher rate of alpha particles relative to other materials. These emissions may not be a problem depending on the device circuitry, sensitivity and the allowable soft error rate.

If sensitive circuits are present, their proximity to a bump, the bump diameter, the chip structure, and the alpha activity rate must be considered in order to estimate the soft error rate.

Because distance and materials attenuate alpha particles, emission effects are localized to a bump. Hence, only the bump near the sensitive circuits warrants concern. The total number of bumps on a chip does not necessarily increase or decrease the risk to a sensitive circuit. Consequently, chips utilizing bump solder must meet Guide 2 as shown in 4.4.2.

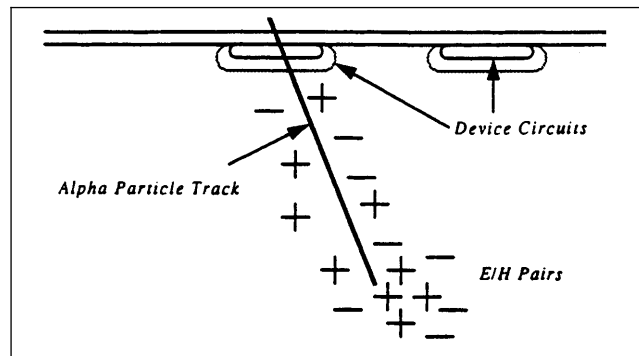


Figure 4-14 Alpha Particle Emission Track and E/H Pairs

4.2.8 Edge Seal Design

The chip edge seal is typically associated with CMOS devices. Edge seal considerations resulting from passivation and Final Metal design must meet existing chip design rules. Other than noted, solder bumps do not alter or supersede any existing chip design rules for chip edge closure.

Table 4-4 defines the typical dimensions for chip edge seal. As illustrated in figure 4-16, the polyimide seal is drawn back from the chip edge seal. The cross-sectional view of these chip edge enclosures relates to those detailed dimensions shown in Table 4-3.

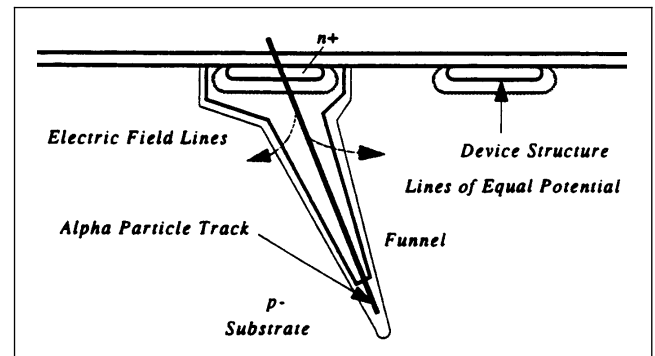


Figure 4-15 Distortion of Depletion by Alpha Particles

scribe is a ratio required by the particular wafer fabrication. Although the same reticle/mask is used for the chip passivation and polyimide layers, due to etch bias, the polyimide edge seal is recessed by 7µm (typical).

4.3 General Consideration for Chip Scale

Developments in flip chip bumping processes have lead to the development of concepts identified as Chip Scale interconnection. Chip Scale Packages are extensions of that concept that have been enhanced to provide more robust attachment technology.

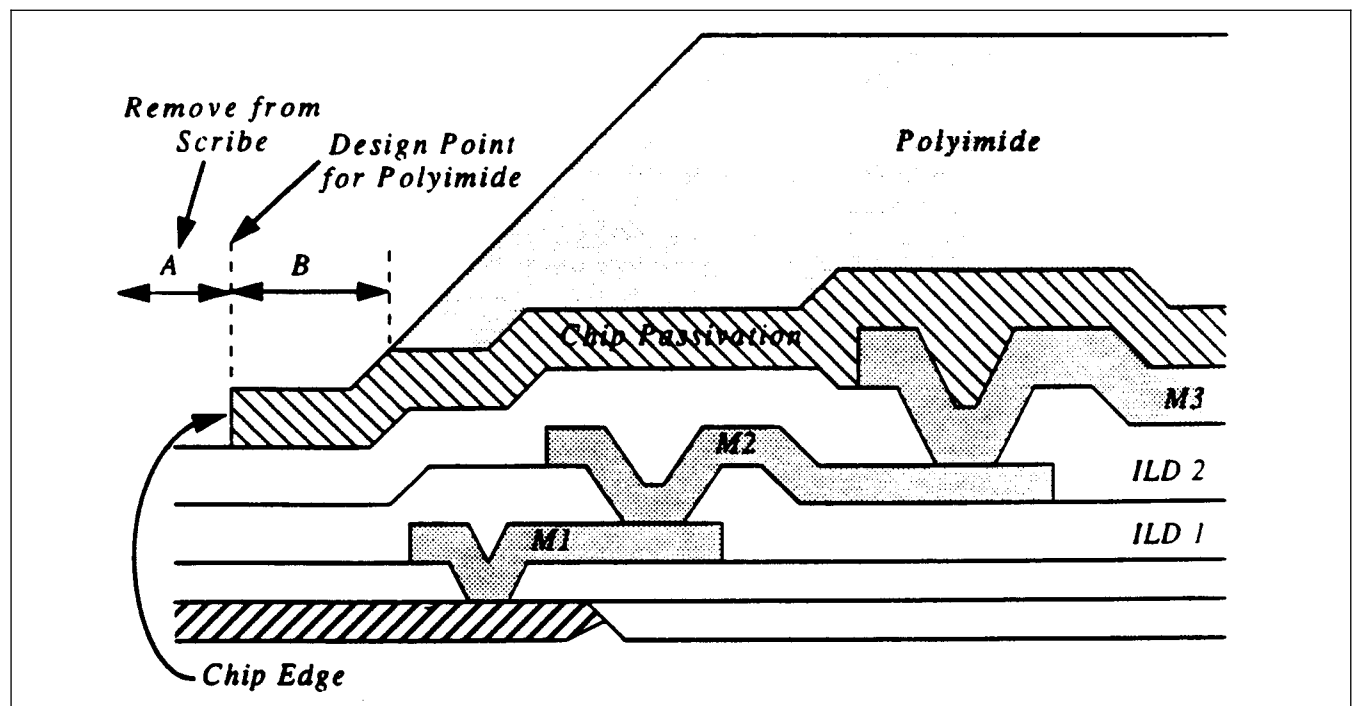


Figure 4-16 Chip Edge and Polyimide Seal

Table 4-4 Chip Edge Seal Dimensions (Typical)

Description	Dimension	Width
Chip Passivation Edge Seal	A	A.R
Polyimide Edge Seal	B	7 µm

It should be noted that edge seal design width to the kerf/

4.3.1 Chip Scale Grid Arrays (CSP-A)

Chip Scale Grid Arrays are produced by a few different fabrication methods.

The CSP-A configurations developed to date include:

- Micro BGAs
- Mini BGAs



Documents

Document Sharing Hub

- SLICC
- Other chip scale packages

Each has its unique method of manufacture, however, most of the devices contain an interconnection method for the chip on the top side in an array format similar to flip chip.

In the case of μ BGA and SLICC a flexible or rigid interposer serves at the redistribution dielectric. In the case of mini BGA and CSPs the dielectric is a polyimide which is deposited on the active part of the chip.

4.3.2 Peripheral Leaded Chip Scale Packages (CSP-P)

One of the new chip scale package types is the Micro SMT (MSMT). This package consists of metallized silicon posts and metal beams. The chip is encapsulated in an epoxy or similar compound. A second CSP-S is the system that uses a lead frame described in 2.2.2.2.

The major difference between the two peripheral packaging systems is that the MSMT is accomplished at the wafer level.

The MSMT process utilizes four mask steps that are applied to the wafer after the bondable metal is complete and covered with a passivation, such as silicon nitride or silicon dioxide. The process sequence, including the mask steps is:

1. Deposit the Beam metals
2. Mask the Beam metal to form the Beams
3. Apply the top trench mask and etch the trench
4. Apply epoxy and centrifuge
5. Apply cap, if required
6. Thin wafer and cap
7. Mask the bottom Post forming trench and etch the trench
8. Deposit Post metal
9. Mask the Post metal
10. Singulate the chips

To summarize the masks used to form an MSMT package, the masks include:

1. The Beam mask
2. Top trench mask
3. Bottom Post forming mask
4. Post metal mask

The Posts of the MSMT package can be designed in a variety of configurations. These include face-wrapped, inside-wrapped, side wrapped, and non-wrapped posts. The wrap style determines the silicon area needed to fabricate the post as shown in figure 4-17.

4.4 Substrate Structure Standard Grid Evolution

More recent entries into the arena of substrates designed to meet the demanding requirements of flip chip and chip scale technologies appear well suited to the task. These

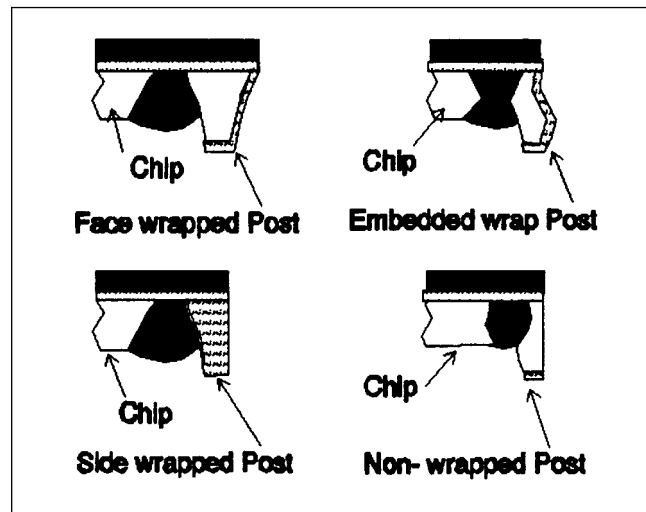


Figure 4-17 MSMT Post Configurations

technologies allow for the construction of shortest path routing for the IC device. Typically based on the concept of standard grids, laminated substrates will allow for the production of inexpensive, high performance systems.

These technologies are fundamentally elegant in concept and are predicated on the notion that standard grids will be required to create economically tomorrow's most advanced systems. The grid pitch that appears most attractive is the one forwarded by the International Electrotechnical Commission (IEC) in their Publication 97.

The pertinent citation from the IEC publication is as follows:

5.0 Preferred Grid System

- 5.1 For positioning connections on a printed circuit board, a grid with a nominal spacing in the two directions of 0.5 mm shall be used.
- 5.2 Where a grid with a nominal spacing of 0.5 mm is not adequate, a grid with a nominal spacing in the two directions of 0.05 mm shall be used.

This seemingly simple standard will ultimately prove to be extremely important because it facilitates implementation of common grid systems that will be necessary for future high performance systems. This was recognized by the IEEE's Computer Society Technical Committee on Packaging. The committee appointed a special task force in the fall of 1990 "to seek early consensus on the need to standardize MCM sizes and to propose some possible sizes." The task force recommended 0.5 mm center lines for peripherally leaded packages and PGA standards for area array packages.

Thus IEC-97 with a base pitch of 0.5 mm with a subdivision of 0.05 mm would replace the familiar 0.100", 0.050", 0.025", and 0.005" grid that has been outdated by the wholesale move to metric based measurement systems for electronics. A common grid will facilitate common design

Table 4-5 Design rules for substrates for Chip Scale Technology

Feature	0.5 mm Grid (2 lines between pads)	1.0 mm Grid (2 lines between pads)	1.5 mm Grid (2 lines between pads)
Line Width (L)	50 μm (0.002")	125 μm (0.005")	200 μm (0.008")
Space (Line to Line) (S)	75 μm (0.003")	175 μm (0.007")	300 μm (0.012")
Space (Line to Pad) (SC)	50 μm (0.002")	125 μm (0.005")	200 μm (0.008")
Hole Size (H)	125 μm (0.005")	200 μm (0.008")	250 μm (0.010")
Pad Size (P)	225 μm (0.009")	326 μm (0.013")	400 μm (0.016")
Wire Routability	40 cm/cm ² (100 in/in ²)	20 cm/cm ² (50 in/in ²)	13 cm/cm ² (33 in/in ²)

rules for routing. Table 4-5 illustrates the design rule concept.

An example of a structure that supports the standard grid concept is shown in the figure 4-18. The use of interposers and substrates designed on a common grid allows for the construction of substrates that can offer "Manhattan routing" of signals. This eliminates the need for redistribution wiring, which normally consumes large amounts of valuable board real estate while limiting higher performance opportunities.

4.4.1 Footprint Design

A flip chip or chip scale footprint design is the arrangement of bumps on the chip surface. When laying out the array of bumps, forethought and planning are required. Bump footprints can be arranged in peripheral, array, or interstitial array formats. Examples of these are shown in figure 4-19.

The size and population of the bumps affects the attachment reliability. The use of the design guide checklist shown in 4.4.2 will minimize reliability problems.

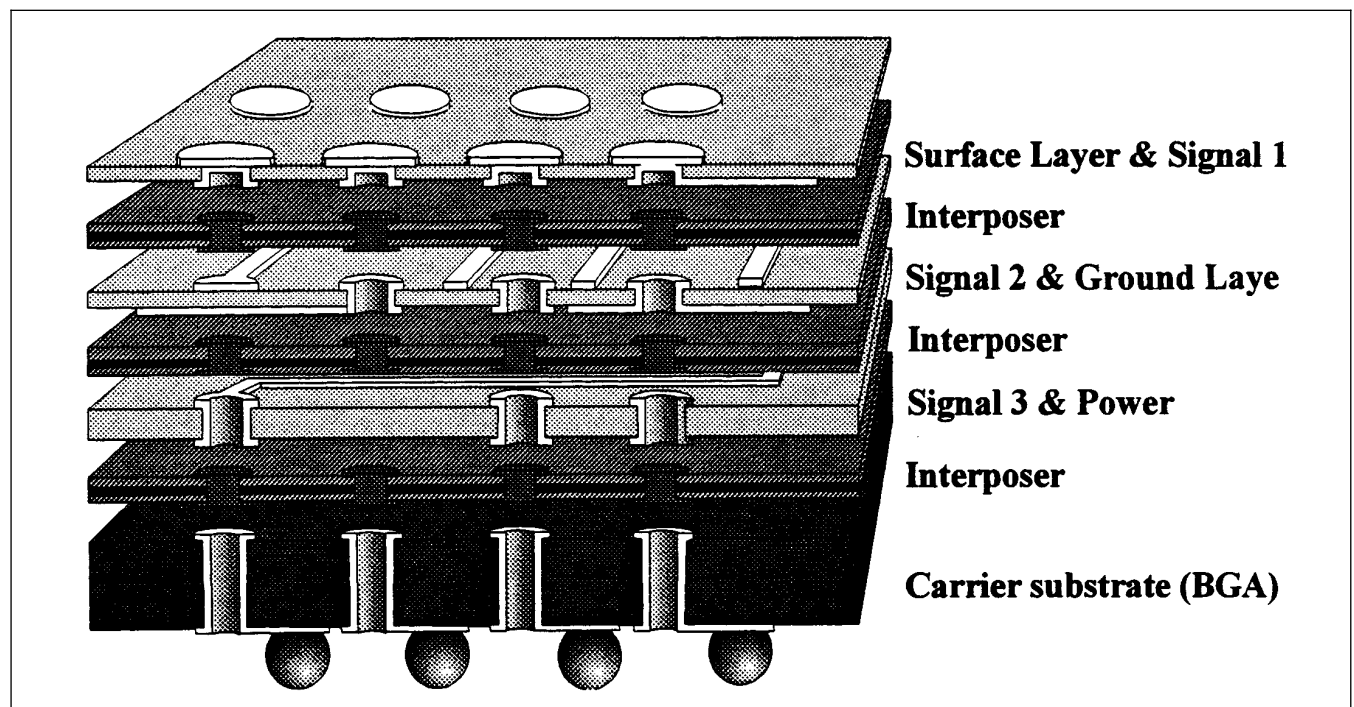


Figure 4-18 Standard Grid Structure

In the illustrated format the interposer joins the innerlayers and interconnects them in a single step process. Because the inner layers are thin, the plated through-holes have very small aspect ratios for plating and are relatively easy to produce. These innerlayers can then be electrically tested before committing them to the finally assembled laminate stack, thus providing greater assurance of a high yield.

4.4.2 Design Guide Checklist

Various design guidelines are applicable in the development of the chip, the CSP, or the attachment process. The guidelines in some instances relate directly to the chip manufacturing conditions. In other instances they also apply to chip scale I/Os. In any event, the guidelines are for very specific reasons and designers should consider the following issues:

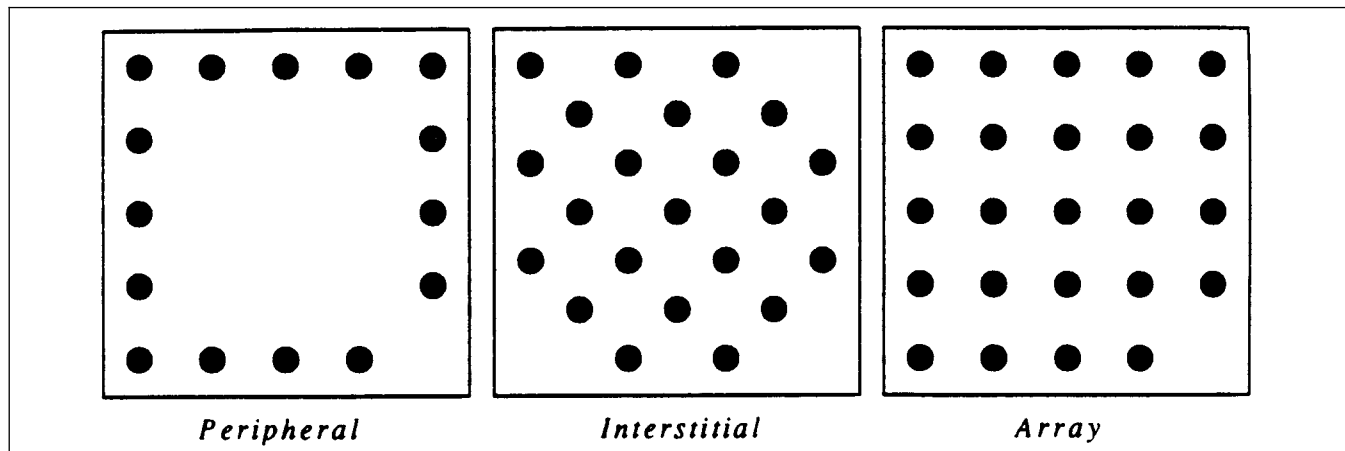


Figure 4-19 Bump Footprint Planning

Guide 1 Operating temperature must be considered when determining interconnect reliability. Devices with underfill may operate reliably at higher temperature than devices without.

Reason Solder creep at elevated temperatures is not well characterized. Applications will require evaluation and testing at operating temperature to determine expected interconnect reliability. There are five basic thermal and mechanical factors that affect solder bump fatigue. These are:

- Strain
- Thermal Activation
- Thermal cycling frequency
- Bump footprint
- Chip underfill (once underfilled, the performance of the underfill is the key, not the solder)

Guide 2 Solder and other alpha emitting materials must be kept an appropriate distance from alpha particle sensitive chip circuitry. For example, a separation of 150 μm is required between C4 bumps (97 PbSn) and sensitive circuitry on polyimide passivated devices.

Reason Alpha particle emission rate of various materials may be too high for reliable operation of alpha sensitive chip circuitry within close proximity. Measures such as thicker passivations or metal shields can mitigate the effects of proximity.

Guide 3 Redistribution designs must minimize the inductance and resistance to reduce sensitivity to ESD.

Reason Increased inductance and resistance of the redistribution line reduces the effectiveness of ESD circuits.

Guide 4 Maximum current should be modeled for the interconnect system used.

Reason Current density and therefore reliability, varies with materials, construction, cross-sectional area, operating temperature, etc.

Guide 5 Designs should conform to all applicable chip design and wafer fab specifications.

Reason Design for manufacturability.

Guide 6 The bump footprint cannot be symmetrical with respect to the X or Y axis unless there are other features to define orientation.

Reason To identify chip orientation for subsequent processing.

Guide 7 At least two bumps are required on each edge of a chip positioned near the chip corner. Dummy Bumps can be used to satisfy this requirement.

Reason Needed for visual inspection and mechanical support of the chip required during joining to maintain parallelism to the substrate.

Guide 8 It is recommended that bump diameters conform to the mandates of the chosen bump pitch to assure reliable connection without risking shorting between bumps. Some desirable bump sizes are 100, 125, 150, and 250 μm .

Reason Conforming with individual suppliers' processes and anticipated industry standards (e.g., ANSI, JEDEC, etc.)

Guide 9 Some minimum number of bumps may be required for manufacturability and reliability.

Reason To withstand dynamic and steady state mechanical forces.

Guide 10 In most applications only one bump diameter per chip/wafer should be used.

Reason Varying bump diameter may impair chip attach. Specialized applications for multiple bump sizes per chip/wafer do exist.

Guide 11 The minimum bump pitch should be held at 250 μm , if possible to facilitate the production of standardized substrates. (Multiple minimum pitches will cause confusion).

Reason Minimum pitches prevent bump to bump, bump-to-trace, and trace-to-trace shorting and provide the distance needed to effectively clean chip joining flux (if applicable).

Guide 12 Location of bumps near areas requiring visual recognition will depend on final bump size as illustrated in figure 4-20.

Guide 16 The edge of the PLM as patterned should not transect an underlying step feature such as a via edge. The importance of this guideline increases with increasing step height and slope.

Reason Pad limiting larger metal can cause stresses when positioned over irregular surfaces.

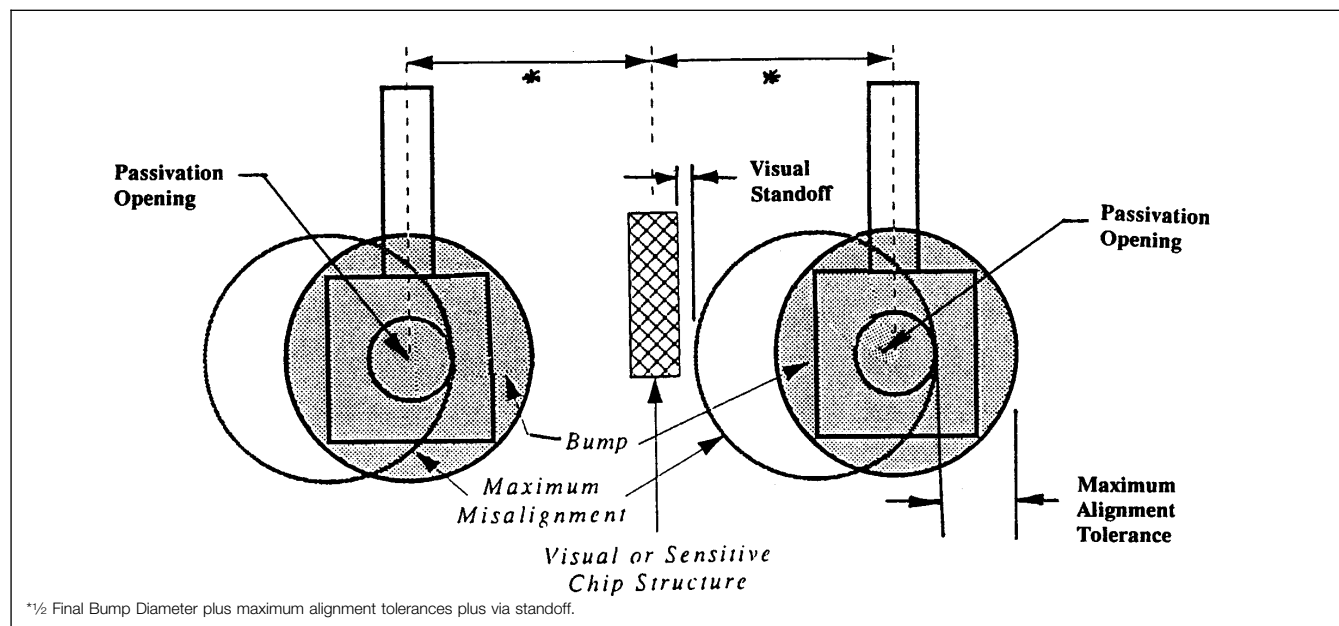


Figure 4-20 Alignment to Visual/Sensitive Chip Structures

Reason Allows for alignment tolerance such that misaligned bumps do not block or cover areas needed for visual or optical recognition.

Guide 13 The minimum distance from the center of the passivation opening to the passivation seal at the edge of the chip is 1/2 the final bump diameter, plus the maximum alignment tolerance, plus the desired minimum standoff between bump and chip seal. (figure 4-21)

Reason Minimum pitch required for Bump alignment tolerance.

Guide 14 Every bump must be connected to a corresponding substrate metal pad.

Reason Metallurgical attachment of every bump to both chip and substrate is required for flip chip interconnect integrity.

Guide 15 Vias under final metal wiring must be spaced away from the edges of the passivation opening. Examples of minimum spacing values used by IBM and Motorola are shown in table 4-6.

Reason Intersection of the edge of the passivation opening with the underlying via topography results in steep features which are difficult to cover with PLM metallurgy and may induce stress related defects.

Guide 17 Practical test cell bumps should be identical to bumps on product die.

Reason To provide correlation between test cell bumps and active product bumps.

Table 4-6 Terminal Via and Final Metal Via Pitch

Descriptions	Size	Tolerance
Passivation Opening Dimensions	50 μm	$\pm 1 \mu\text{m}$
Passivation Opening Edge vs Stacked Wiring Via	2 μm	Minimum
Passivation opening edge Vs. Common Wiring Via	10 μm	Minimum

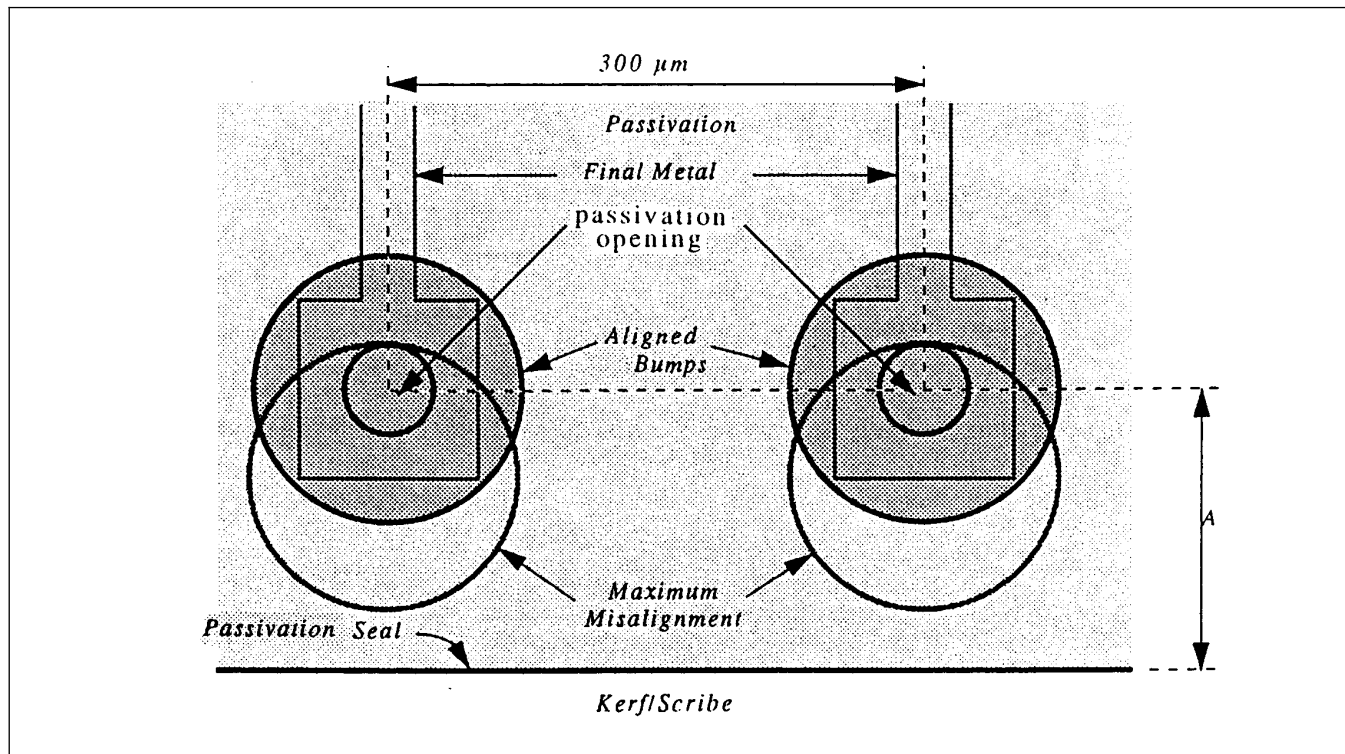


Figure 4-21 Minimum Pitch from Bump to Passivation Seal ("A"-½ finished bump diameter, plus alignment to tolerances, plus desired minimum)

4.4.3 Footprint Population

The number of bumps needed varies with electrical, thermal, and mechanical requirements. Besides electrical connections, bumps may be included for heat dissipation, mechanical support (outriggers, chip orientation, or future design migration).

Each application has its own unique characteristics. This makes it impossible to establish a general methodology for footprint population; however, there are various strategies that can be employed depending on the application.

The following are some examples of several footprint population design issues and suggested approaches for solving them.

4.4.3.1 Redundant Bumps

Redundant bumps are designed for power and critical signals. The chip area will support a larger footprint but the resulting distance from the neutral point (DNP) may negatively impact reliability. In this approach the outermost rows of bumps join chips and endure the most stress. As the DNP increases, the stress in the outer rows increases. By placing redundant bumps in the outer rows and critical bumps in the inner rows, if bumps in the outer rows fail, chip functionality will not be compromised. Include a sufficient number of redundant bumps to allow for potential loss. Figure 4-22 shows how this might be accomplished.

An alternative and supplemental solution would be to use chip underfill after the chip is attached to a substrate. This

might be necessary if the DNP is sufficiently large. This does not involve additional wafer level processing.

4.4.3.2 Chips That Will Incur Design Shrinks

Designing a footprint for chips that incur design shrinks requires additional considerations.

The approach for this chip design is to locate the critical bumps in the chip's interior. Use outer rows for redundant and mechanical bumps. When the shrink occurs, the outer, less essential rows will be lost, but the critical bumps will not be affected. As the chip shrinks so does the DNP - making the loss of redundant and mechanical bumps less of an issue. This is illustrated in figure 4-23.

It should be noted that with this approach, the package is not affected by the bump footprint as the critical connections do not change. Redundant connections to the package simply become open pins. Caution should be exercised when the chip area shrinks so that the bump footprint does not shrink. In addition, provision must be made for orientation and alignment of the shrunk die.

4.4.3.3 I/O Drivers on the Periphery

Some chip designs require that the I/O drivers are on the periphery with other circuits internal to the chip. Redundant connections for power and signals are desired.

When using the approach that positions I/O drivers on the chip periphery, shorter interconnection lengths are always desirable in order to minimize parasitic effects. Bumps