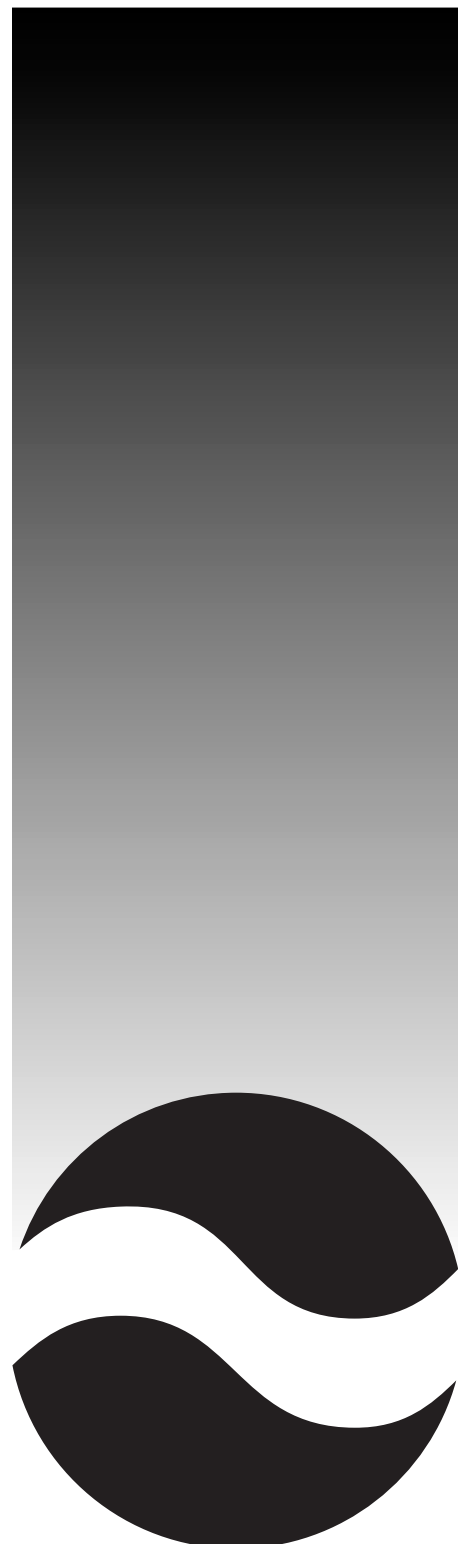


IPC/EIA J-STD-032
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JOINT INDUSTRY STANDARD

Performance
Standard for
Ball Grid
Array Balls



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Performance Standard for Ball Grid Array Balls

About This Document

This document is intended to report on the work being done by several organizations concerned with the design of bare die in flip chip or chip scale configurations. Details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade associations or societies any comments or observations regarding details published in this document, or ideas for additional details that would serve the industry.

Users of this standard are encouraged to participate in the development of future revisions.

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Members of the EIA Soldering Technology Committee (STC) and the IPC Device Manufacturers Interface Committee (A-10) have worked together to develop this document.

We would like to thank them for their dedication to this effort. Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Flip Chip Task Group are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the EIA and IPC extend their gratitude.

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