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ELECTRONICS INDUSTRIES

IPC-MC-790

Guidelines for Multichip Module Technology Utilization

IPC-MC-790

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A standard developed by IPC

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Guidelines for Multichip Module Technology Utilization

Developed by the IPC Multichip Module Subcommittee of the Hybrid and Related Technologies Committee of IPC

About this document

This document published by IPC is for informational purposes and can serve as a baseline for selecting an appropriate MCM technology. It is not intended to be a standard and in fact, this document is expected to evolve with significant technological developments.

This document reports on work which has been done by a variety of individuals and organizations concerned with increasing system performance and reliability through multichip module technology. You, as the reader, are invited to review the content of this document and communicate your comments and ideas for additional details that may serve the industry to the appropriate trade associations or technical societies. In this way, the infrastructure necessary to implement this new philosophy for packaging will make its way forward.

Thanks to Chairman Phil Marcoux, ISHM and IPC are in the process of a detailed update program. It is expected that the result of this effort will culminate in a hardbound version that will provide an excellent reference tool. IPC will also consider future review of the MC-790 as more information becomes available. You are invited to participate in any of the revision or update processes.

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Foreword

The developments over the past 8–10 years reflected in this document have resulted in a variety of new materials, structures, and interconnect methodologies. This “smorgas-bord” of MCM technology is shown in Figure F–1. The selection of the elements that make up a structure to meet the systems level needs initially appears to be a difficult problem in the current environment. However, the choices available should be viewed as part of the beauty of this technology.

Initially, system requirements should be developed on a hierarchal basis. A simple high-level breakdown of a system is shown in Figure F–2. System requirements for cost, reliability and performance must be clearly understood in the context of the application and system environment. In this way, requirements are logically developed and an understanding of their interrelationships can be inferred or modeled.

The complexity of an MCM structure demands the development of requirements for the structure from system level considerations. The next step is to work with system partitioning concepts that make sense in terms of system cost and performance. For example, the designer should question whether it makes sense to use single chip packaging,

manufacture a single module on a 10.2 cm [4 in] substrate, or four modules on a 5.1 cm [2 in] substrate. Perhaps the answer is the latter when cost is compared to performance requirements for the system. This process of system partitioning may require an iteration or two following the initial technology selection in order to develop accurate costs as the process of developing a module-based system progresses.

Following the development of system requirements and partitioning, a specific module can be synthesized which meets the systems needs through a balancing of module attributes related to cost, performance, and reliability. At this point, IPC-MC-790 can become a useful tool in understanding the various module options and the relationship of these attributes to a potential structure. This is done through the use of comparisons of interconnect and substrate properties, manufacturing costs and other criteria for MCM-L, MCM-D, and MCM-C as defined in section 1 of the document. Table F–1 shows these various module attributes and their relative weights for these general categories.

The selection of a general category is initially made through comparing system requirements to module attributes. This should be done in a quantitative fashion

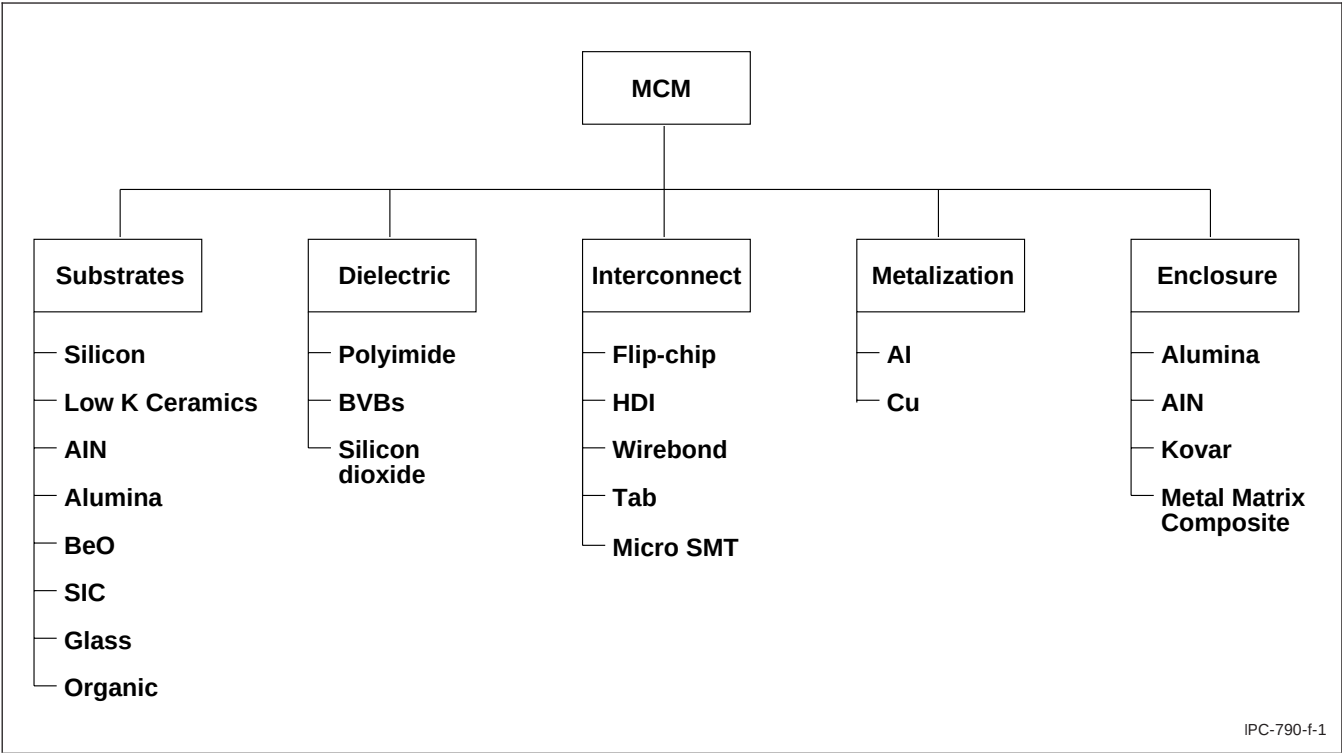


Figure F–1 MCM options

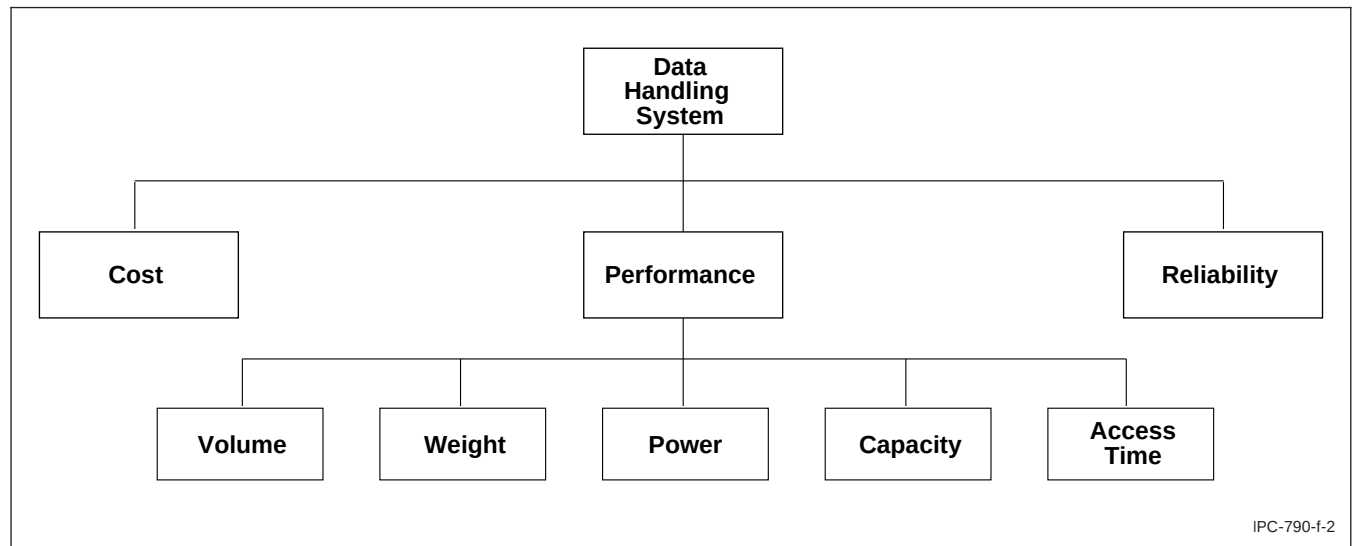


Figure F-2 Electronic system packaging hierarchy

Table F-1 Multichip Module Parameter Complexities

Parameter	Thick-film MCM-Circuits	Thin-film MCM-D circuits	MCM-L circuits
Performance	Medium	High	Medium
Design flexibility, digital	Medium	High	Medium
Analog	High	High	Low
Plastics	Low	Low	Medium
Power dissipation	High	High	Low
Frequency limit	Medium	High	Medium
Voltage Swing	Medium	Medium	Low
Size	Small	Smallest	Small
Package density	Medium	High	Medium
Reliability	High	High	High
Circuit development time (prior to prototype)	1- 2 month	2-3 month	1 month
1:1 design transfer from bench	Yes	Yes	Yes
Turnaround time for design change	2 weeks	4 weeks	2 weeks
Part cost, low quantity	High	Impractical	Medium
High quantity	Medium	Medium	Low
Cost of developing one circuit	Medium	High	Low
Capital outlay	Low	Medium	Low
Production setup and tooling costs	Low	Medium	Low

Section One

Technology Overview

1.0 INTRODUCTION

Electronic packaging continues to focus on the ever increasing need for higher electrical speed and higher interconnection density. In existing packaging concepts using printed board assemblies and individually packaged integrated circuits, performance may be sacrificed because of the signal path length needed to interconnect the semiconductors contained in the various packages.

In contrast to the above, improvements in speed, reliability, and density accompany the use of unpackaged integrated circuit chips on fine line interconnection substrates. A functional, packaged module exhibiting these attributes will be called a "Multichip Module" (MCM), and is the subject of this document. A variety of materials and techniques may be employed in creating an MCM. In section 2.0, various approaches are categorized, and the reader is led through a decision-making process to assist in the selection of the proper MCM technology for a given set of technical requirements. Later sections provide detailed information regarding each technology type.

The balance of this introduction discusses the drivers toward use of MCM's, and the type of problems which may be resolved via MCM technology. The following key point should be assimilated: total cost is minimized when the best technological choice is made for packaging and interconnection.

There is an important drive to increase density in order to make the product smaller. Space restrictions exist in end-use environments ranging from aircraft to laptop computers and hand-held TVs. Another driver is the potential cost reduction available from reduction in material usage, or even from less real estate being employed, as may be the case in telephone exchanges. Table 1-1 shows MCM selection according to various market segments.

The heart of electronic performance capability is the integrated circuit and the increasing levels of integration being achieved. To capitalize on IC capability, we have already seen the move to surface mount packages with fine pitch I/O. For the same reason, direct attach, such as TAB, Flip-Chip, and Chip-On-Board, are also becoming important interconnection techniques.

Observations indicate that when single I/C chip mounting is used, a trend exists toward one package per 6.45 sq. cm. [1 sq. in] of substrate compared to 0.2 to 0.5 per 6.45 per sq. cm. [1 sq. in] for packaged I/Cs. Under these circumstances, the I/O count of the package becomes the major determinant of the interconnect density required. Figure 1-1 shows just how these individual IC chip I/Os are expected to increase.

While not totally separate from the density considerations, the issue of system speed presents some major challenges

Table 1-1 Characterization of Selected MCM Market Segments

Segment	Drivers	Personality	Price Elasticity
Electronic T&M	Precision	Industrial	Moderate
Logic Analysis	Precision, Miniaturization	Industrial	High
Global Positioning & Surveillance	Miniaturization Miniaturization	Military Commercial	Moderate High
Communications Satellites	Miniaturization	Commercial	Low
Telephone	Miniaturization	Commercial	Very High
Smart Sensors Weapons Systems Automotive Control Robotics	Miniaturization Miniaturization Miniaturization	Military Consumer Industrial	Moderate, Low Very High Moderate
Computing Systems Strategic/Tactical Mgmt. Info. Sys. Scientific Models	Speed Speed Speed	Military Commercial Industrial Academic Government	Low Moderate Low
Image Processing	Speed, Miniaturization	Industrial	Moderate
Engineering Workstations	Speed	Industrial	Very High
Laptops/Notebooks	Miniaturization	Consumer	Very High

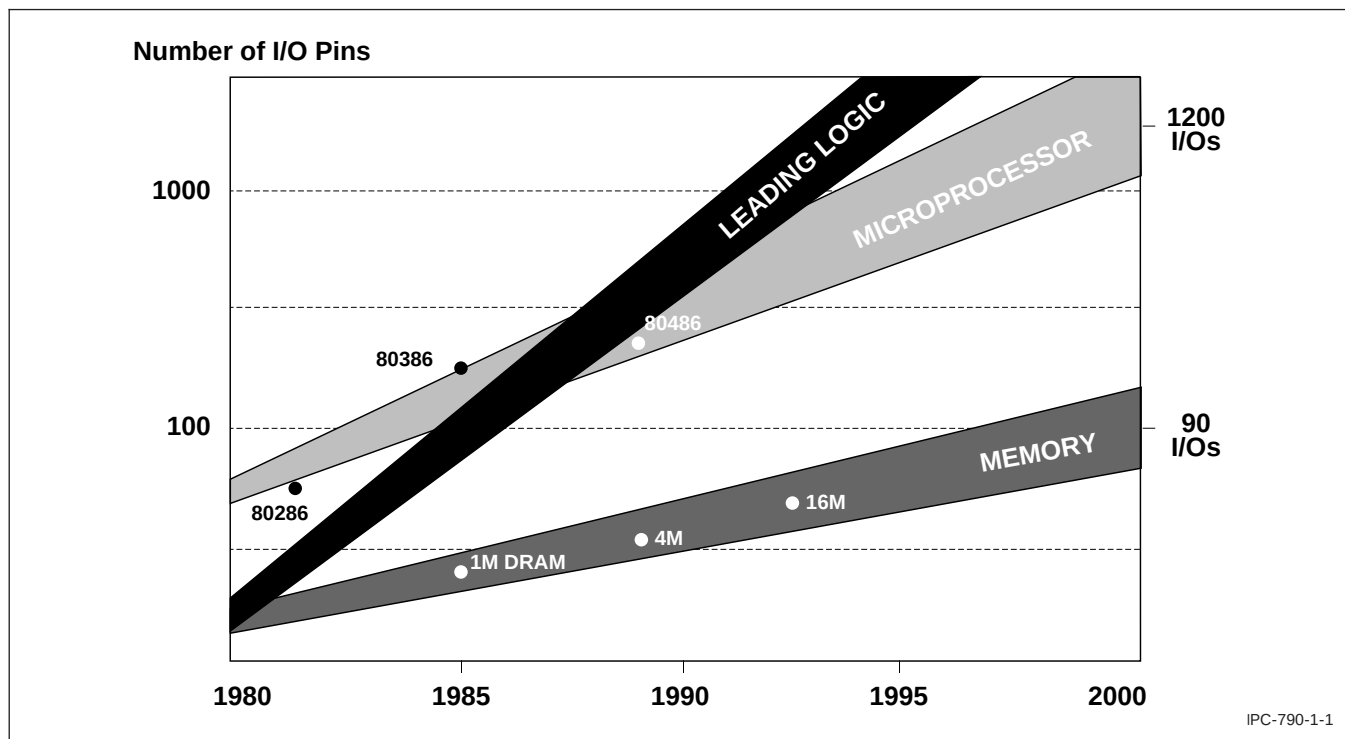


Figure 1-1 Typical pin count per integrated circuit

to interconnect structures. Figure 1-2 shows a forecast of how clock frequencies will develop during the early part of the 1990s: note the increasing proportion of systems with operating frequencies at a level where the electrical performance of the interconnect becomes critical.

As new generations of electronic products emerge, they surpass the capability of existing packaging and interconnection technology and infrastructure. This movement is occurring at all levels: at the IC, at the IC package, at the hybrid, the board, the connector, and even the cable which ties all the systems together. Interconnection density becomes the measure of successfully managing performance and interconnect requirements.

Interconnect substrate capability continues to be challenged by the combined effects of two interrelated movements: 1) use of digital circuitry at the expense of analog circuitry; and 2) continued technical progress in semiconductor processing, which enables production of denser IC devices having progressively higher interconnection demands.

The gap between printed boards and semiconductor technology (wafer scale integration) is greater than one order of magnitude in interconnection density capability, although the development of "fine-pitch" printed boards and assembly technology has narrowed the gap somewhat.

Comparison of technology capability is presented in Figure 1-3. This generalized plot approximately relates price and density for a wide variety of interconnect technologies, and deserves additional discussion. Along the vertical (Y) axis, price information is normalized to cost-per-square-inch of interconnect substrate. The variable along the horizontal

(X) axis is interconnect density, which is defined as total possible wiring trace length of all signal layers, per square inch of substrate. Present practice, substantiated by several empirical studies, indicates that actual wiring efficiency is approximately 50% of theoretical. The plotting scale for both axes is logarithmic. Certain areas of the graph are annotated to indicate the price/density relationship for selected technologies. The technologies covered range from single sided printed boards (low cost, low density capability) in the lower left hand corner of the plot, to ICs, multichip modules, and wafer scale integration (high cost, high density capability) in the upper right hand corner.

In addition, some trend lines have been inserted in the figure to indicate price history and anticipated future trends. In the mid 80s, the prices of substrates were increasing as the square of the interconnection density. But, the plot also shows that, in response to an "experience curve" and general market dynamics, the Price/Density relationship is constantly changing. As a result, it is expected that at some future time, arbitrarily marked in the plot as the "1992 price line," substrate prices will increase only linearly with density. There are indications that when such a pricing state is reached sometime in the future the interconnections at higher density levels may be more economical than low density interconnects.

The previous plots and discussion indicate a void in interconnection density capability between present printed wiring board technology and wafer scale integration. All viable efforts at filling this void utilize unpackaged integrated circuits. This avoids the space in

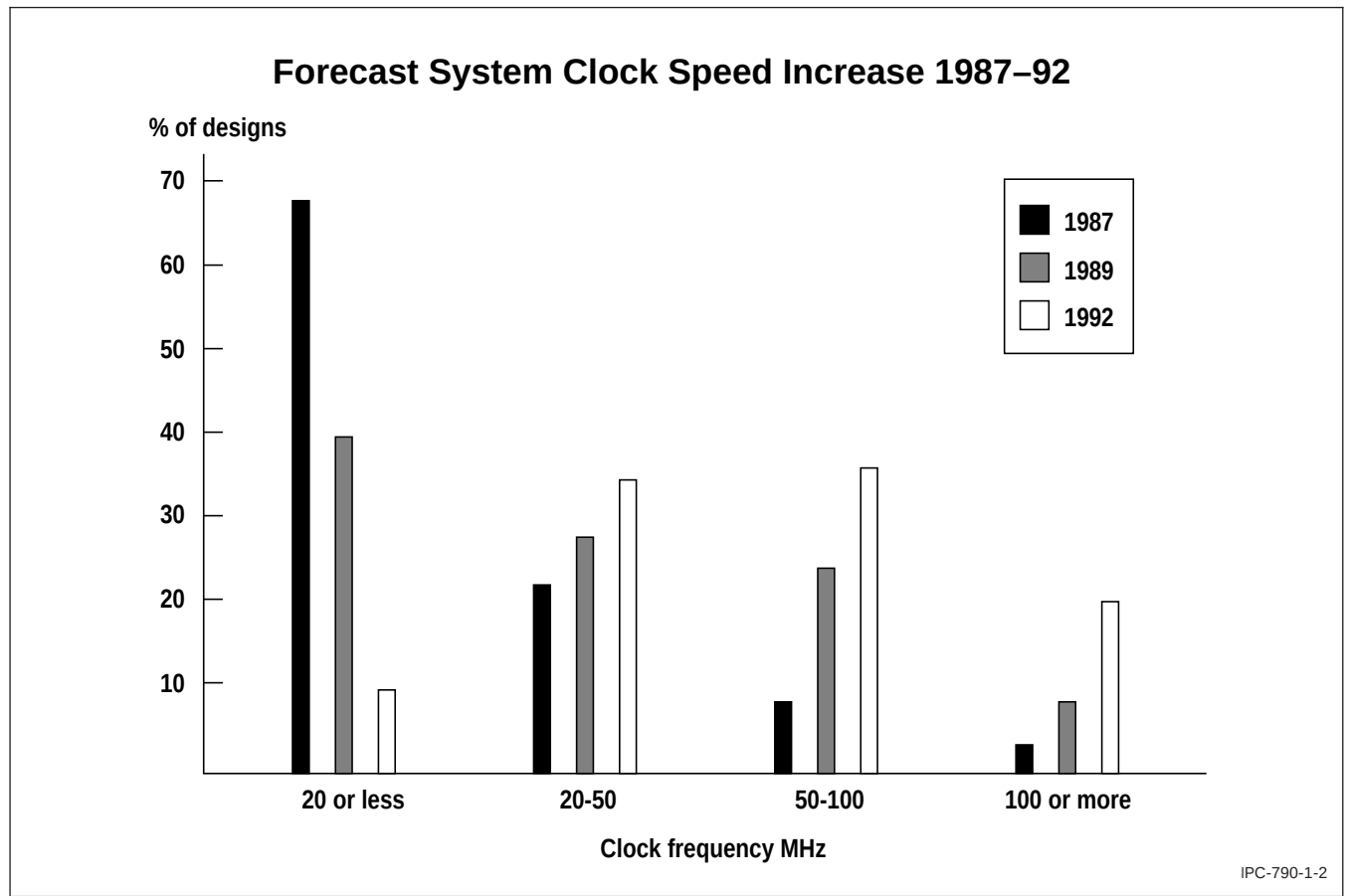


Figure 1–2 Forecast system clock speed increase 1987–92

fanout and relatively bulky leads which accompany single chip packages. The acronym “MULTICHIP MODULE” is appropriate for all technical approaches for 1) interconnecting multiple bare integrated circuits for efficient operation, and for 2) interfacing to the outside world through a “next level assembly”. With this as background, a multichip module may be defined as follows:

“LOGICAL FUNCTIONAL BLOCKS GROUPED TO MAXIMIZE INTERCONNECT WITHIN A COMPACT ASSEMBLY, YET MINIMIZE INTERCONNECT TO THE NEXT LEVEL.”

Technologists have emphasized the applicability of Rent’s rule, which relates IC chip I/O count to the number of functions on the chip. However, the use of Rent’s rule for multichip modules or wafer scale integration is not appropriate. Consider, for example, a television. If all the electronics required for the TV’s operation were contained in one MCM, only a few I/O would be required, including 1) power cord, 2) antenna, 3) video signal out, 4) audio signal out, 5) adjustment controls (e.g., on-off-volume). Other examples include the personal computer, cellular phone, camcorder, etc. Proper utilization of MCM technology should reduce the need for fine-pitch package I/O.

If careful attention is paid to technical/design issues in combination with achievement of interconnection “density matching,” many benefits may be realized, including the following:

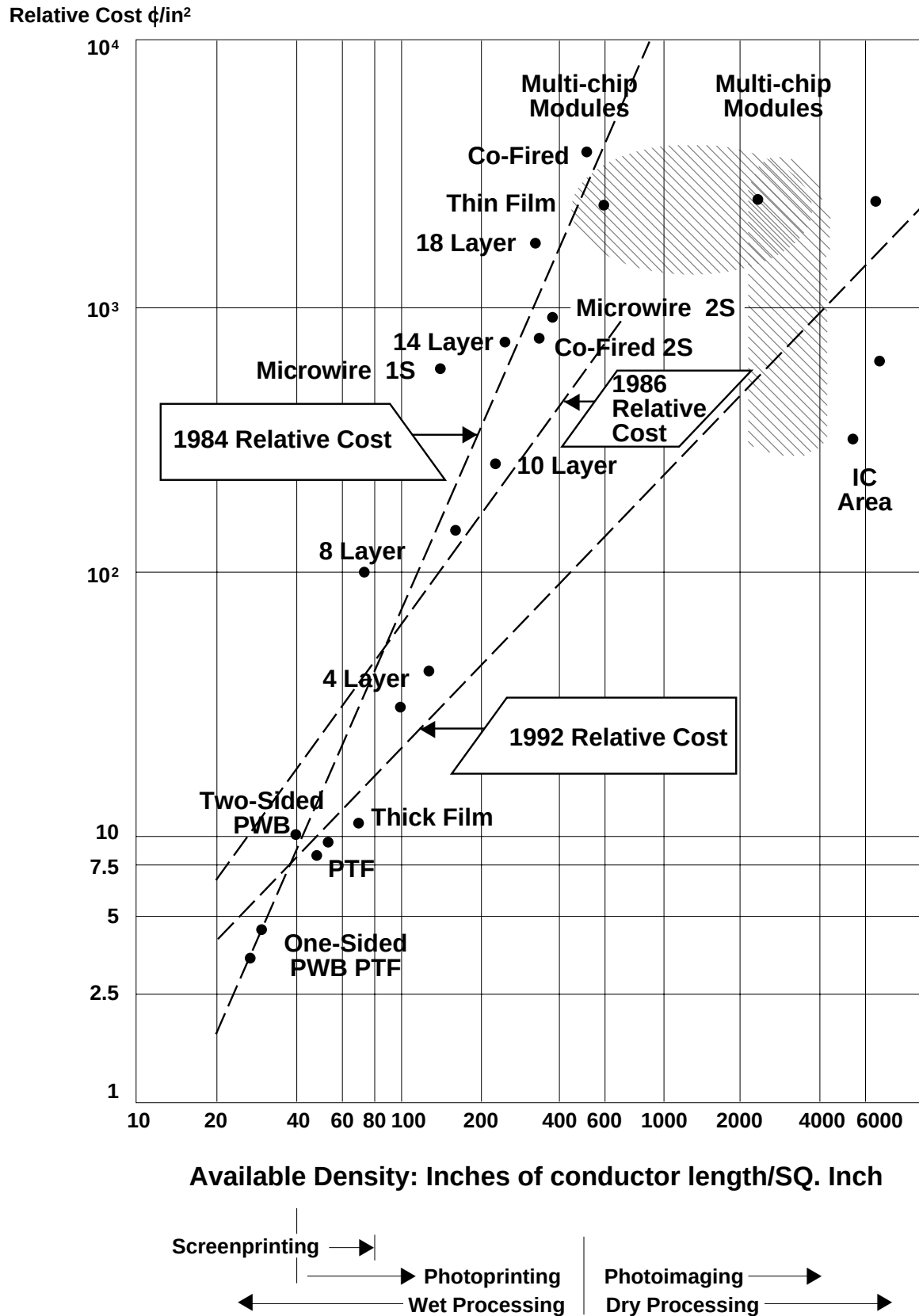
- Reduced electrical losses, resulting in improved speed capability; fewer components (as might be needed for decoupling).
- Lowest cost for the required performance.
- Reduced size and weight.
- Potential for reduced I/O.

It is important to recognize that several forms of multichip technology have been in existence for a number of years, and new approaches have been introduced recently. Among these are the following:

- Thick film hybrid microelectronics
- Thin film hybrid microelectronics
- Co-fired multilayer ceramic module
- Chip-on-board (COB)
- Silicon-on-silicon
- Wafer-scale integration

Their relative position on a density capability plot is shown in Figure 1–4.

1.1 Multichip Module Classification Traditionally, the differences among printed board assemblies, hybrid circuits



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Figure 1-3 Price/density relationships



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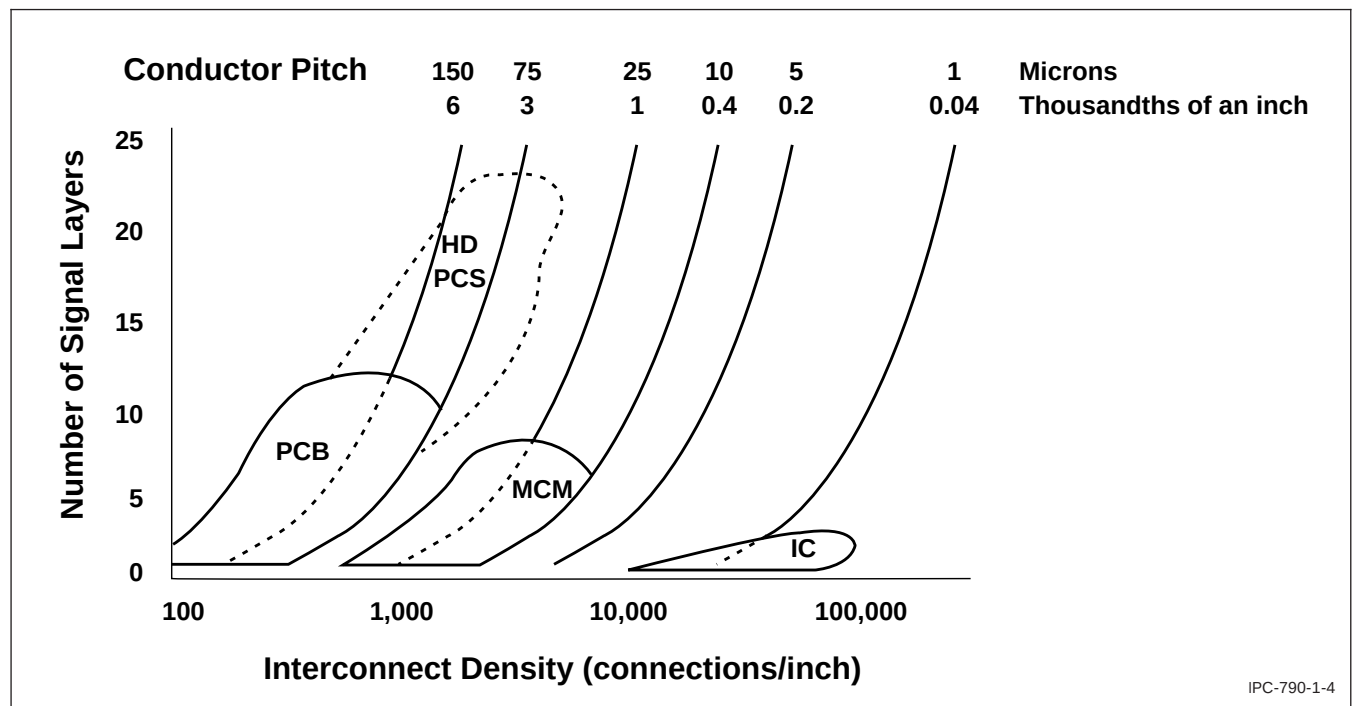


Figure 1-4 Interconnection density vs. line technology

and integrated circuits have been related to substrate materials being used, i.e. organics, ceramics and silicones, respectively. However, using the substrate material as a determining factor no longer seems to be appropriate, due to the wide range of material combinations now being used in the electronics packaging and interconnection industry.

Thus, if substrate materials are not considered, it may be possible to define new categories of electronic circuit assemblies in accordance to the dielectric materials used to separate conductive interconnection layers.

In an attempt to characterize multichip modules, it is generally agreed that multichip technology cannot be defined on complexity alone. In addition multichip module definitions should not mix co-fired ceramic with reinforced organic or other deposited unreinforced low dielectric technologies.

Since many of the assembly techniques for components on multichip modules are similar or identical the characterization concepts lead to using the mounting substrate as a method for determining the complexity, manufacturability, and some of the performance of the multichip module in its environment.

Multichip modules, as the name implies, are intended to mount bare I/C die. Although the majority of the components are unpackaged, I/C's and other components may be included in the multichip module. The attachment techniques are:

- Passive component chips: Reflow solder or conductive adhesive
- Unpackaged Active I/C's: Wire bond, TAB, or Flip-Chip

- Packaged Active I/C's: Reflow solder or conductive adhesive

In order to provide multichip module characterization, three categories of multichip modules have been established. These are:

- Multichip Module Type C (Ceramic Dielectric)
- Multichip Module Type D (Deposited, Unreinforced low Dielectric)
- Multichip Module Type L (Laminated, Reinforced organic Dielectric)

The subsequent paragraphs identify some additional details, while Table 1-2 summarizes some of the attributes of the three classifications.

1.1.1 Multichip Module C Multichip modules identified by the letter C normally are constructed of ceramic or glass ceramic alternatives. These materials have a dielectric constant that is ≥ 5 . Performance of the MCM-C considers the dielectric properties between single planes or between single planes and ground planes. The materials act as both the dielectric and the supporting plane for the components. Conductors are usually a fireable metal material such as tungsten, molybdenum, and the screenable frit metal thick film conductors of gold, silver, palladium and copper. When these materials are used to form the conductors, the conductor width is < 0.15 mm Vias necessary during the interconnecting process are formed during the conductor screen printing. The vias are usually the same materials as the conductor.

For most Multichip C applications, the number of active devices is greater than the passive components.

1.1.2 Multichip Module D Multichip Modules identified by the letter D are normally constructed using unreinforced dielectric materials that are adjacent to the signal plane. The dimensional stability of this type of module is determined by the underlying substrate which is usually made of ceramic, silicon, copper, glass-reinforced laminate, or other metal or metal composites.

The dielectric materials normally have a dielectric constant of <5 . The additive dielectrics may be deposited on the substrate or may be deposited on a metal platen and peeled off to be reapplied elsewhere in fresh situations.

Conductors are sputtered or plated. The materials may be aluminum, copper, or gold. Photolithography is used to provide the imaging of the conductor patterns.

Vias may be formed during the conductor deposition/plating processes. When deposition and plating are used in combination, the vias are plated after conductor deposition.

1.1.3 Multichip Module L Multichip Modules identified by the letter L use laminated printed board fabrication technology. Laminated layers may be reinforced or unreinforced and consist of such resin materials as epoxies, polyimides, or acrylics, reinforced with fiberglass, quartz, Kevlar, etc.

Conductors are almost always copper. These are deposited additively or are generated as part of the printed board subtractive process.

Vias are copper, electrolessly plated initially, followed by additional electrodeposition. When the MCM-L requires control of the coefficient of thermal expansion, lamination techniques use materials that have low CTE such as copper-invar-copper.

1.1.4 Multiple Module Attributes The general characteristics of the three multichip module classifications are compared in Table 1–2. The table provides a general overview. The main purpose of the document is to describe the details for decision making on which module type best suits the application. These details are described in section 3 on design. Producibility issues are described in sections 4 through 7. Testing and acceptance are covered in sections 9 and 10.

1.2 Materials Data Since dielectric and base materials properties form the major attributes of multichip modules, their properties should be well understood. Table 1–3 indicates the properties of some of the most used material in multichip module construction.

The expansion characteristics are key items related to the coefficient of expansion mismatch between the chip and the base material of the MCM. This becomes extremely critical when the chip is bonded to the substrate for thermal

performance. Figure 1–5 shows graphically the change in the thermal expansion characteristics of different materials while Figure 1–6 provides a graphic presentation of their thermal conductivity properties.

1.3 Advantages and Disadvantages of Multichip Modules The design of a multichip module structure starts with the decision to use direct chip attachment interconnection to the multichip module interconnection structure. That decision is based on the advantages and disadvantages of the chip assembly technique as well as the performance achieved by packaging bare chips closer together.

The principal advantages of MCM's are higher density and higher speed performance. In addition, potential advantages include:

- Lower cost (in high volume)
- Lighter weight
- Smaller packages
- Lower “Z” dimension profile (thinner packages)
- Shorter circuit paths (faster switching speed)
- Improved impedance control
- Reduced number of interconnection levels in the overall system (fewer solder joints)
- Shorter turnaround time for prototypes and production

The disadvantages include:

- Specialized capital equipment required
- Unprotected integrated circuit chip handling techniques required
- Chip encapsulation and metallurgy must be carefully selected to meet environmental and mechanical requirements
- User/vendor relationship required for acquisition of fully tested, uncased integrated circuit chips
- For chip and wire, the total number of chips per assembly might be limited by the expected burn-in yield per chip
- CAD tools may need to be modified to accommodate chip-on-board
- Component reliability, availability, and yield
- Difficulty of test prior to assembly
- Lack of standardized I/C layout and pad placement
- Repairability/socketability

1.4 Design Cycle The system specification will identify several factors influencing the selection or determination of design criteria. The environment in which the system must operate, system size, weight, reliability, power, and signal sources and levels should be specified by the system specification. In addition, manufactured item cost, life-cycle cost, and cost-versus-performance criteria should be available from the systems design activity. System reliability

Table 1-2 Multichip Interconnect Attributes by Classification Multichip Modules

Parameter	MCM-C		MCM-D		MCM-L
	Co-fired Ceramic	Low-K Ceramic	Silicon	on ceramic, Metal Substrates	Low-K Dielectrics Printed Boards
Line Density Cent. Per Square Cent. Per Layer	20	40	400	200	100
Min. Line Width Range, Microns	125-200	125- 200	10-25	15-100	50-100
Min. Spacing Range, Microns	125-375	125-375	10-30	35-75	100- 300
Dielectric Const. of Substrate	9	5	8	8- 16	3.0-5.5
Diel. Constant of Diel. Layers	9	5	3- 6	3-6	3.0-5.5
Pinout: Per cm ² Peripheral	15-60 1600-6400	15-60 1600-6400	8-30 800-2300	8-30 800-2300	15-30 1600-3200
Number of Years Commercially Avail.	>10	>5	5	5	>20
Terminating Resistors	Built-in Acceptable	Built-in Possible	Difficult	Built-in Possible or Surface Mounted	Built-in Poss. or Surface Mounted
Power Distribution Capacitors	Surface Mounted	Surface Mounted	Can have depletion layer, dual dielectric layer, or high capacitance layers	High capacitance layer or surface- mounted	Surface Mounted

Table 1-3 General Multichip Material Properties

Material	Glass Transition Temperature	XY Coefficient of Thermal Expansion	Thermal Conductivity	XY Tensile Modulus	Dielectric Constant	Volume Resistivity	Surface Resistivity	Moisture Absorption
<i>Unit of measure</i>	(°C)	(PPM/°C) (note 4)	(W/M°C)	(PSI x 10 ⁶)	(At 1 MHz)	(Ohms/cm)	(Ohms)	(Percent)
Epoxy Fiberglass	125	13-18	0.16	2.5	4.8	10 ¹²	10 ¹³	0.10
Polyimide Fiberglass	250	12-16	0.35	2.8	4.8	10 ¹⁴	10 ¹³	0.35
Epoxy Aramid Fiber	125	6-8	0.12	4.4	3.9	10 ¹⁶	10 ¹⁶	0.85
Polyimide Aramid Fiber	250	3-7	0.15	4.0	3.6	10 ¹²	10 ¹²	1.50
Polyimide Quartz	250	6-8	0.30		4.0	10 ⁹	10 ⁸	0.50
Fiberglass/Teflon	75	20	0.26	0.2	2.3	10 ¹⁰	10 ¹¹	1.10
Thermoplastic Resin	190	25-30		3-4	10 ¹⁷	10 ¹³	NA	
Alumina-Beryllia	NA	5-7 21.0	44.0	8.0	10 ¹⁴			
Aluminum (6061 T-6)	NA	23.6	200	10	NA	10 ⁶		NA
Copper (CDA101)	NA	17.3	400	17	NA	10 ⁶		
Copper-Clad Invar	NA	3-6	150XY/20Z	17-22	NA	10 ⁶		NA
Copper-Clad Molybdenum 13%/74%/13%	NA	5.7	209XY/161Z	43.5	NA	10 ⁶	—	NA
Copper-Clad Molybdenum 20%/60%/20%	NA	6.9	244XY/195Z	41	NA	10 ⁶	—	NA
Graphite (P-100)	160	-1.15	110XY/1.1Z	37	NA			
Graphite (P-75)	160	-0.97	40XY/72	25	NA			

Notes:

- These materials can be tailored to provide a wide variety of material properties based on resins, core materials, core thickness, and processing methods.
- The X and Y expansion is controlled by the core material and only the Z axis is free to expand unrestrained. Where the T_g will be the same as the reinforced resin system used.
- When used, a compliant layer will conform to the CTE of the base material and to the ceramic component, therefore reducing the strain between the component and P&I structure.
- Figures are below glass transition temperature, are dependent of method of measurement and percentage of resin content.

NA = Not Applicable

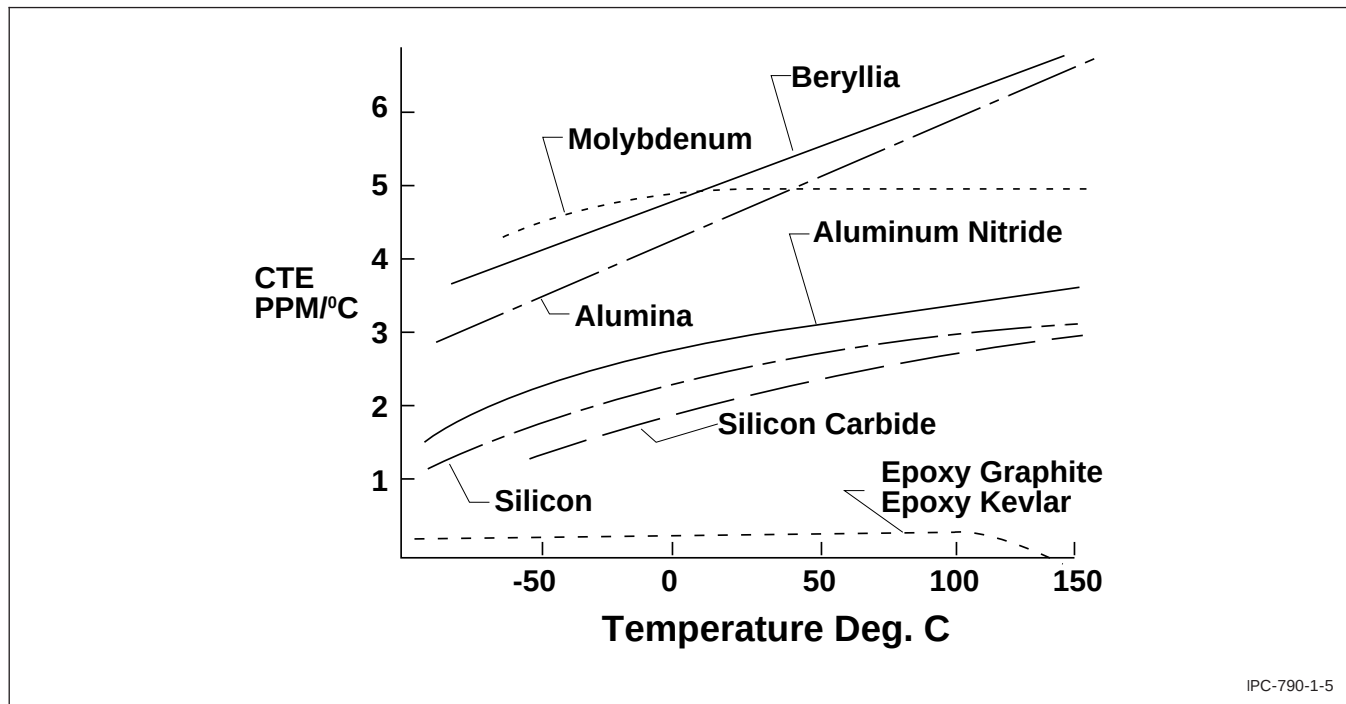


Figure 1-5 Expansion of Packaging Materials

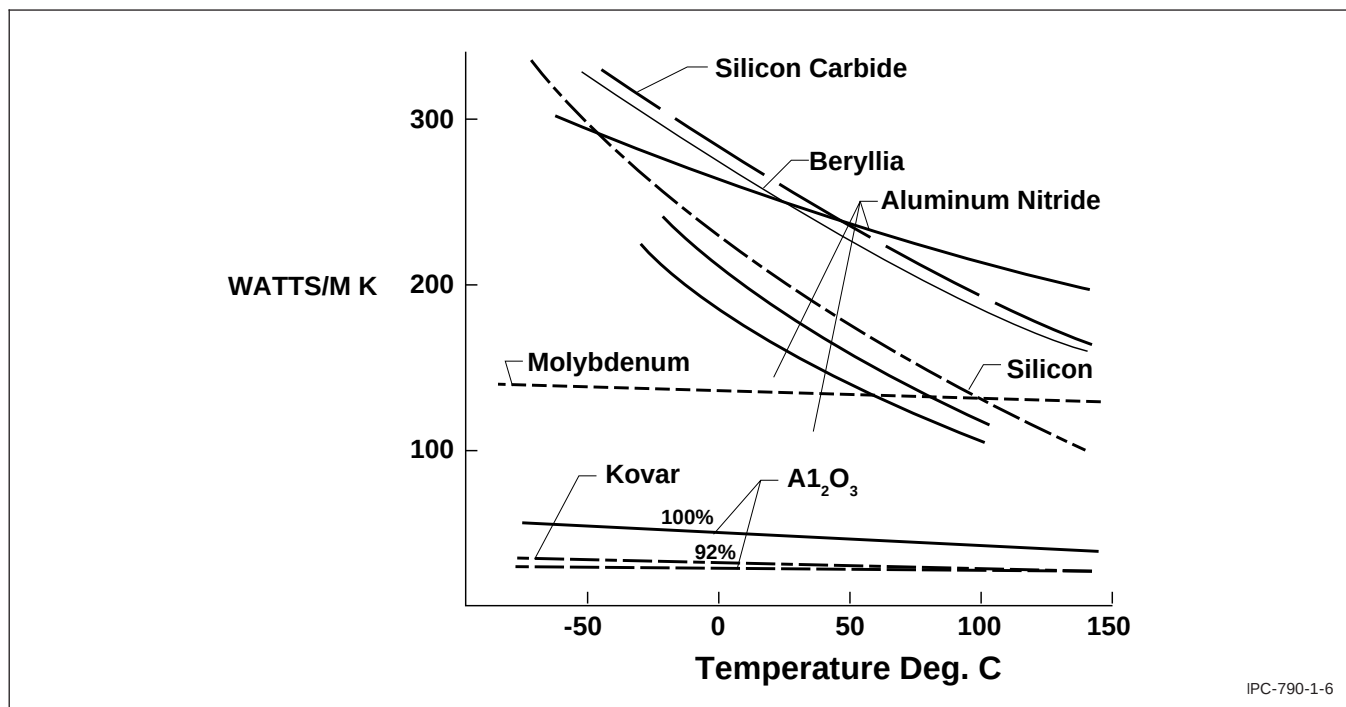


Figure 1-6 Conductivity of Packaging Materials

may include a schematic diagram or may be limited to block diagrams indicating simple functions and signal flow information. In either case, the system must be partitioned to reliable circuit functions. For some types of multichip modules (MCMs), the maximum number of chips per module could be a consideration.

The environmental requirements during storage, shipment and use of the MCM assembly could easily dictate the substrate, joining method and/or type of encapsulant used.

The power handling capabilities of MCM structures often require the consideration of thermal enhancements (thermal vias, etc.), if the power to be dissipated is more than 1/2 to

1 watt per chip, depending on the density of chips on a substrate and the type of substrate material employed.

Table 1–4 defines nine end use environments that should be considered during the design cycle. The table indicates the minimum and maximum temperatures that an equipment might see, however, the delta difference in actual operation may be somewhat less.

1.4.1 Cost Drivers The price of the equipment to be designed is based on material cost, equipment available, facilities, those parts which must be subcontracted, labor rates, overhead cost, percent of profit, delivery, quantities, and level of complexity, Figure 1–3.

When the design task is initially proposed estimates are forecasted. After starting the design it should then be re-estimated to adjust for any changes in conceptual approaches from the proposal.

Relative cost comparisons of multichip modules and custom integrated circuits should not be done on a function-to-function basis, but should consider the total cost impact on the complete electronic system. In order to have a realistic cost evaluation one should compare a standard printed board assembly techniques to MCM designs having less complex printed board assemblies.

Also, volume or quantity consideration should be applied to any cost trade-off. Custom devices may prove to be the most effective for very large quantities, but due to the

higher nonrecurring costs of large scale integration (LSI) circuits, they may not be cost effective for low volume systems.

1.4.2 Component Availability Component availability is the biggest obstacle to implementing multichip modules. Great care and planning must be used when selecting an I/C and its vendor. Component definition and count will affect module size because of topological considerations. Layout restriction associated with alternate process design rule and performance-related criteria developed in the breadboard stage must also be considered. If required, the custom development of a semiconductor function or package may affect the project schedule.

1.4.3 Reliability Considerations Reliability considerations for a multichip module are complex. Users expecting MCMs to meet the same reliability requirements as packaged components are unrealistic since the individual I/C chips, especially bare, are not thoroughly tested and preconditioned prior to assembly. In normal PC assembly, the individually packaged I/Cs are tested, conditioned and warranted. The use of TAB, encapsulation, and chip testing provide the potential to achieve reliability comparable to the PC level of assembly.

1.4.4 Make or Buy One of the options available to management is to subcontract the packaging effort, or a portion of it. Another option, if personnel availability is a problem,

**Table 1–4 End Use Environments
Worst-Case Use Environments**

Use Category	T_{min} °C	T_{max} °C	ΔT^1 °C	t_p hrs	Cycles/year	Years of Service
1 CONSUMER	0	+60	35	12	365	1-3
2 COMPUTERS	+15	+60	20	2	1460	~ 5
3 TELECOM	–40	+85	35	12	365	7-20
4 COMMERCIAL AIRCRAFT	–55	+95	20	12	365	~ 20
5 INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	–55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	~ 10
6 MILITARY GROUND & SHIP	–55	+95	40 &60	12 12	100 265	~ 10
7 SPACE leo geo	–269	+95	3 to 100	1 12	8760 365	5-30
8 MILITARY AVIONICS a b c	–55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	~ 10
9 AUTOMOTIVE UNDER HOOD	–55	+125	60 &100 &140	1 1 2	1000 300 40	~ 5

& = in addition

1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT ; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, T , is not the difference between the possible minimum, T , and maximum, $min T$, operational temperature extremes; T is typically max significantly less.



is to bring in contract employees to supplement the existing staff. Equipment can be rented, and facilities leased. The important point is to identify any problems at the early stages of the design effort when decisions can be made in a non-crisis atmosphere.

1.5 Assembly Options Several multichip module assembly options exist. These include:

- Single-sided/Double-sided
- Cavity Structures
- Stacked Structures
- Embedded Structures

1.5.1 Single- and Double-Sided A single-sided module has conductors on one side only while a double-sided module has components and traces placed on both sides. Single- or double-sided boards generally provide a fan-out pattern from the bonding lands to the package I/O points. They are best for low to medium conductor routing density applications.

1.5.2 Cavity Structures Many module designs use a cavity with I/O pads on more than one level. The cavity protects the chip from handling damage while the multiple pad levels increase I/O density. For I/O densities which surpasses 100 pin counts, a cavity structure is recommended. Like blind vias, cavities may be difficult to achieve in multilayer structures. Double-sided PWBs can be fabricated with cavities by a routing technique.

1.5.3 Stacked Structures Stacked structures are multiple I/Cs or other components stacked on top of each other. The stacked components may be interconnected by wire bonds, deposited metal, or TAB or beam leads, as shown in Figure 1-7. Components are insulated by dielectric materials that are part of a component or applied separately.

1.5.4 Embedded Structures. I/C chips and other components are attached to a heat sink and surrounded by a resin that provides the attachment and dielectric. The interconnections are then deposited simultaneously to the resin surface and the component land sites.

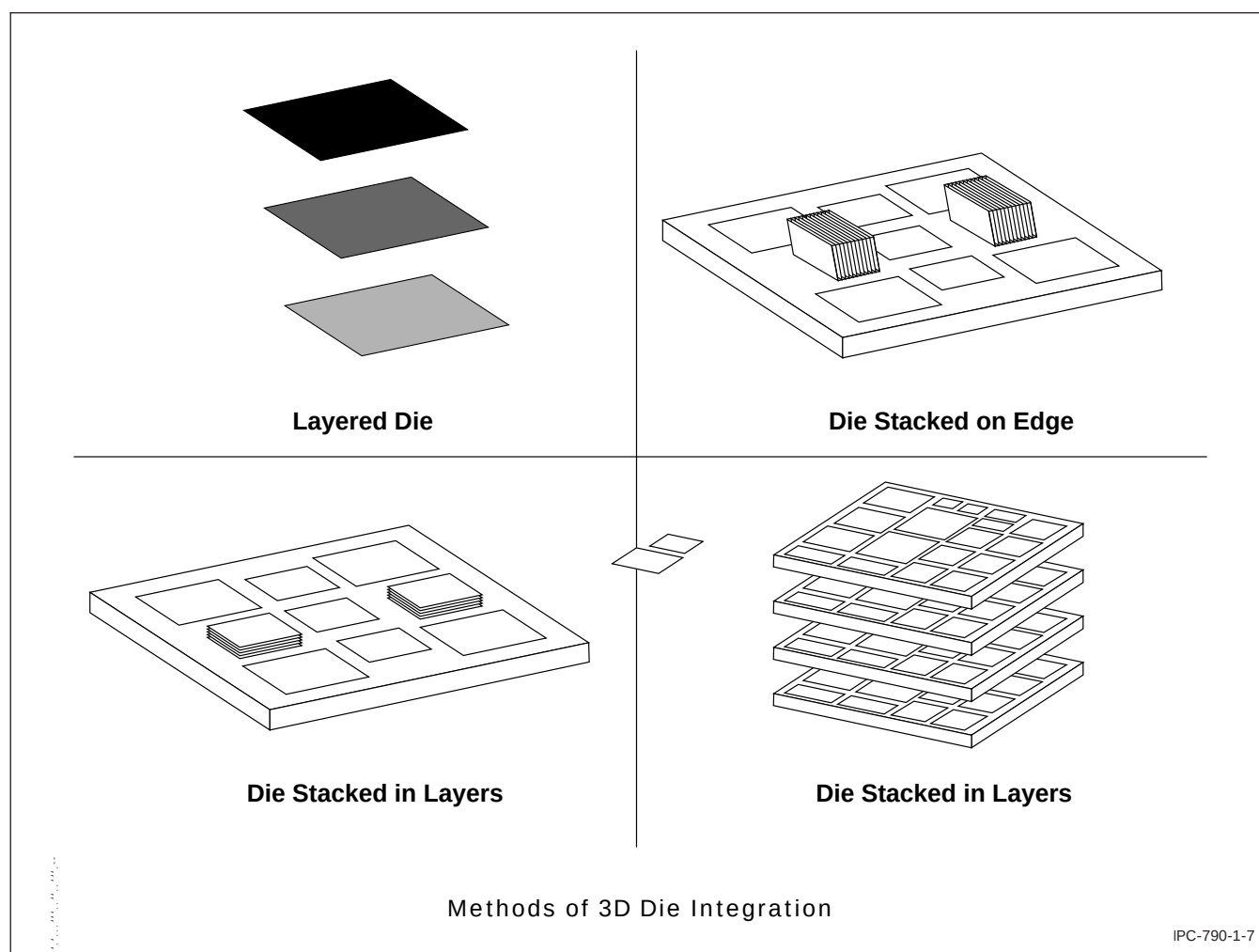


Figure 1-7 Methods of 3D die integration

- If fine conductors are necessary, limit them to the areas of necessity, enlarging conductors as more space becomes available, providing that electrical performance is not affected.
- Balance plated areas on front and back of design. A ground plane on one side with a few isolated conductors on the opposite side is difficult to manufacture. If possible, add nonfunctional cross hatched areas to large empty areas.
- If selective plating is desired for bonding areas, make certain bussing is accommodated, such that all areas can conveniently make contact with the board periphery.

1.6 Substrate (Interconnect Carrier) The physical carrier for the interconnect, the “substrate,” may be a separate entity. In several cases, such as the printed wiring board (MCM of type “L”), the dielectric is, or becomes the substrate. In other cases, such as MCM type “D,” the thin film circuitry requires an external substrate.

1.6.1 Selection of Substrate Material Topics include discussion of TCE, thermal conductivity, material stiffness. Materials to be discussed include aluminum nitride, BeO, alumina, metal matrix composites, Si, Cu/In/Mo laminates, SiN, SiC, and FR4. For MCM type “L,” the selection of an appropriate board substrate material depends a great deal on the cost trade-offs associated with the end product applications and the type of assembly technology being employed.

If cost is paramount in a high volume application, localized charring at die sites on conventional epoxy (FR-4) and composite (CEM) substrates as a result of thermocompression gold ball bonding is often tolerated. Fortunately, applications which select flexible wiring and molded thermoplastic board materials can withstand the thermosonic bonding temperatures (150–200°C). These special applications, however, introduce other considerations such as the ability during fabrication to achieve and to repeat, with precision, small features for placement, attachment and wire bonding. Printed board structures can be made from one of several organic, resin systems. The most common resins are FR-4 (Epoxy), FR-4 BT (Bismaleimide - Triazine - Epoxy, GPY (Polyimide) and blends of these resins.

FR-4, Epoxy, has a glass transition temperature between 110°C and 140°C. Wire bonding may be difficult above this temperature. However, the thickness and hardness of the nickel plating could allow bonding at the most commonly used thermosonic bonding temperature. Aluminum ultrasonic bonding at room temperature can avoid any high temperature processing on FR-4, but it is slower than thermosonic bonding.

Compared to FR-4, BT (Bismaleimide-Triazine Epoxy) offers improved temperature performance, enhanced reliability and excellent wire bondability at moderately higher

cost. BT has a glass transition temperature of 180°C, which is acceptable for all standard wire bonding processes. The maximum operating temperature for BT is 150°C, which makes it a material of choice for assemblies utilizing thermosonic gold ball bonding.

Polyimide printed wiring boards have still higher temperature performance properties with a glass transition temperature of 260°C. Polyimide offers advantages for extreme operating environments.

1.6.2 Substrate Design Substrate design of an MCM follows the same procedures of a pcb for SMT or FPT. The use of multiple layers is very common. Connection between layers of the interconnect substrate may vary with the fabrication technology which will dictate the via hole size and location. Bonding pad locations are determined by the chips pinout and bonding method (TAB, wire, bump) and for the feature size capability of the interconnect technology. Chip to chip spacing is determined primarily by the placement method (auto vs manual), the test method (in circuit vs system), and the need for inspectability and repairability. For heat sensitive devices, chip spacing may be determined by the heat flow patterns and the distance required to avoid proximity heating.

CAD system software for MCM-D substrate is now becoming available. This offers a combination of the features available in printed wiring and ASIC CAD software.

1.7 Thermal Issue For MCM type “L,” the IC chip is typically mounted to the printed wiring board package with silver filled epoxy that provides electrical contact to the back of the chip and a low thermal resistance at the interface. Since the chip is attached to a printed wiring board substrate whose thermal conductivity is approximately 1/65 that of ceramic, the printed wiring board package must contain built-in designs that will enhance the thermal characteristics of the material. The thermal enhancements may consist of large unbroken copper planes under the die attach area to spread the heat dissipated by the chip as well as plated-through holes that connect these planes and shunt the epoxy material. The plated-through holes act as thermal vias and for best results should be placed within the die attach area connecting it to an outer copper plane where a heatsink may be mounted. An alternate method, but less effective, is using blind vias (see Figure 1–8) to connect two or more heat spreading planes.

The effectiveness of thermal shunting is directly proportional to the number and size of the plated-through holes in the die attachment area as expressed by the following approximation:

Thermal Shunt Efficiency (0%) = $100 \sqrt{A_{da} + C_{DN}}$

Where:

A_{da} = Total die attach area in²



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D = Plated through hole diameter, inch

N = Number of plated through holes within die attach area

C = 7°C inch (for thermal conductivities of $K_{cu} = 10.1$ watts/ $^{\circ}\text{C inch}$)

$K_{pwb} = 0.0066$ watts/ $^{\circ}\text{C inch}$

The above relationship does not take into consideration the additional thermal enhancement of the silver filled epoxy

that may fill the plated-through holes during the die attach process. It is recommended that the plated-through holes have an aspect ratio of approximately 5:1 (board thickness to via diameter) and be located on 1.9 mm [0.75 in] centers. Reliability tests have shown that the assembled chip in the printed wiring board package is not adversely affected by the plated-through holes in the die attach area when subjected to a temperature humidity bias (THB) environment of 85°C & 85% RH.

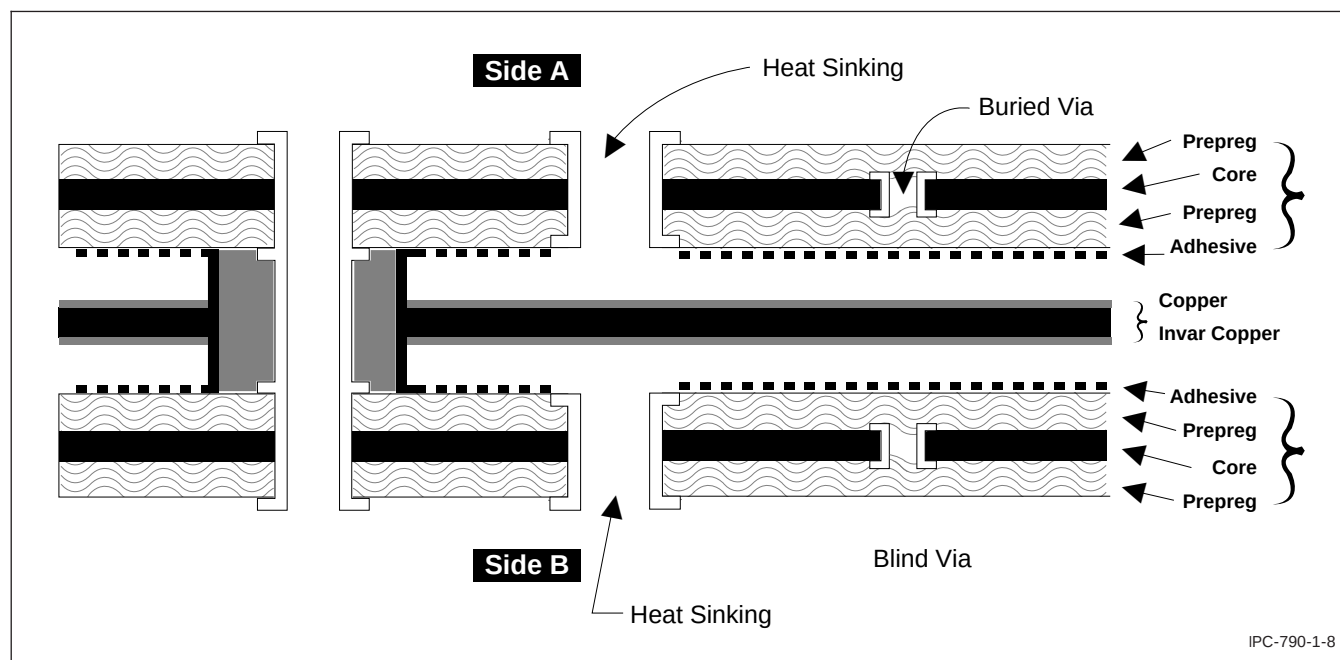


Figure 1-8 Eight-Layer MCM-L

using one of several systems- engineering decision-making tools. Such tools include Quality Function Deployment (QFD), which uses matrix manipulations to direct the designer into identifying the most important module attributes needed to meet the system requirements and can quantitatively compare various module concepts in terms of these requirements. The use of QFD requirements is explored in several of the basic system engineering references.

Additionally, an Analytical Hierarchy Process (AHP) can be extremely useful in comparing system requirements to attributes of various options for a particular module architecture. AHP uses a pair-wise comparison process to rank the most important module architectures with respect to a

particular system requirement, such as cost or performance. This allows an intelligent selection of a packaging architecture which can fulfill the system requirements in the most efficient manner. AHP is a well known systems-engineering tool, and is available in the open literature and through various relatively simple analysis packages.

In summary, the complexity of modern packaging systems demands a quantitative decision-making approach to developing a package architecture. This allows selection of a module which will successfully fulfill systems performance needs in the most cost effective manner while assuring high reliability. IPC-MC-790 can serve as a useful tool in implementing this approach.



Section Two

Multichip Module

General Design Considerations

2.0 INTRODUCTION

The success or failure of a multichip module design depends on many interrelated considerations. From an end-product usage standpoint, the impact on the design by the following typical parameters should be considered.

- Equipment environmental conditions, such as ambient temperature, heat generated by the components, ventilation, shock and vibration.
- If the module is to be maintainable and repairable, consideration must be given to chip density, the selection of coating materials, and placement for accessibility.
- Testing/fault location requirements that might affect placement, conductor routing, connector contact assignments, etc.
- Process allowances such as etch factor compensation for conductor widths, spacings, bonding site, fabrication, etc.
- Manufacturing limitations such as minimum etched features minimum plating thickness, module shape and size, etc.
- Assembly technology used, such as wire bonding, flip chip, TAB, etc.
- Materials selection.
- Producibility of the multichip module as it pertains to manufacturing equipment limitations.

2.1 Materials The primary concern with materials is the effect that one material may have upon another material within a multichip module. Materials in a module should be carefully analyzed to determine whether the proposed design is susceptible to failure mechanisms.

Nonconforming materials can result in failure of the circuit due to one or more of the following conditions:

- Metal
- Corrosion or oxidation
- Ionic contamination
- Improper adhesion
- Intermetallic formation
- Drastic differences in thermal coefficients of expansion

2.1.1 Substrates The substrate is the mechanical base and electrical insulating material used in multichip module fabrication. The material properties of the substrate affect the processes used in the fabrication of the multichip module and affect the inherent reliability of the final circuit.

Important factors in selecting a substrate for high reliability are dielectric strength, thermal conductivity, thermal coefficient of expansion, camber, surface finish, and materials compatibility.

The majority of MCM-C and MCM-D multichip module substrates used in fabrication are produced from ceramic materials such as alumina, or beryllia. More exotic substrate materials such as quartz, oxidized silicon, and sapphire are often used for high-frequency circuits. Where larger sizes and higher strength is required, for MCM-D, coated metal substrates are used.

For MCM-L applications, rigid or flexible polymer substrates with or without reinforcement are used.

2.1.2 Conductive Materials The conductor, analogous to the wire in older technologies, is fabricated from material of very low resistivity and is used to advance the signal (information to be processed or used) to the desired location with minimal signal loss.

2.1.2.1 Thin-Film Metallizations Thin-film conductors are typically gold or aluminum. The choice of metallization systems is limited from any given multichip module supplier because of the significant capital and development costs.

Gold is the primary thin-film conductor material. This material is deposited by means of vapor deposition, by evaporation, and by sputtering. The deposited film is electroplated to increase its conductivity. Generally, a final thickness of from 0.0025 mm to 0.005 mm [0.0001–0.0002 in] of gold is necessary for circuit conductivity and wire bonding.

Aluminum, copper, and palladium are alternative conductor materials used in thin-film applications. These materials are employed primarily by semiconductor houses, as their use is more specialized. The primary reasons for using these alternative conductor films are cost, conductivity, and metallurgical compatibility.

2.1.2.2 Thick-Film Metallizations Thick-film conductors are typically silver, gold, and alloys of these materials with either platinum or palladium. Glass frits and other additives are used which will affect the electrical characteristics of these materials. Copper- and nickel-based, thick-film pastes are emerging as a newer low-cost, thick-film conductor.

Thick Film is used in multichip technology where density is not a factor. Since the technology is well established,

entry into multichip module implementation is somewhat easier and independent suppliers of mounting substrates are more readily available. Typical usages are listed below:

- A. Gold (Au) conductors are used where high conductivity combined with long-term reliability are required.
- B. Platinum gold (PtAu) conductors are used where soldering is the only viable means of component attachment.
- C. Palladium gold (PdAu) is limited to use in those areas discussed under PtAu and where cost is to be kept as low as possible. PdAu is a relatively low cost alternative to PtAu.
- D. Silver (Ag) is used primarily in commercial applications where low cost is essential. Typical applications are in microcircuit displays and polymeric composites, adhesives, and sealants.
- E. Platinum silver (PtAg) is used where soldering of components is employed. Its application is limited presently to nonmilitary applications.
- F. Palladium silver (PdAg) is a low-cost solderable conductor designed for good solder-leach resistance.
- G. Palladium platinum silver (PdPtAg) is a ternary metal composition which attempts to reduce the silver migration that has limited the utilization of silver-bearing inks in military applications. It provides a solderable conductor with good solder-leach resistance.
- H. Copper (Cu) was developed primarily to reduce cost associated with conductors of noble metals. The use of this material must be carefully evaluated, as the processes and equipment required employ tighter controls than those associated with noble metals.
- I. Nickel (Ni) is another low-cost substitute for noble metals. It finds its greatest use in display applications.
- J. Tungsten molybdenum, manganese (W/MoMn) materials require reducing atmospheres. The firing conditions require considerably greater controls which are generally not available in small laboratories. The inks are not readily available.

2.1.2.3 Metallic Foil/Film Conductors may be formed in metallic foils or films bonded to a substrate by selective etching. The more common usages are listed below:

- A. Copper foil. Two types of copper foil are available, rolled annealed and electrodeposited (ED). For rigid substrates, electrodeposited is most commonly used and is available in thickness as low as 0.004 mm [0.0002 in]. Flexible materials normally use rolled annealed copper with a minimum thickness of approximately 0.018 mm [0.0007 in].

- B. Copper Film. Copper film is applied to the substrate by an additive electroplating process and has a normal minimum thickness of 0.005 mm [0.0002 in].
- C. Other Foils or Films. Foils or films of nickel, Kovar, aluminum, etc. may be used when special requirements dictate.

2.1.2.4 Metallic Platings and Coatings Conductors may be formed by selective deposition or application of metallic foils or coatings. The more common usages are given below:

- A. Electroless Copper. Copper is deposited on selected areas (including through-holes when required) by a chemical process and may be built up to the desired thickness.
- B. Electrodeposited Copper. Copper is applied to selected areas (including through-holes when required) by electrodeposition from several different electrolytes and may be built up to the desired thickness.
- C. Gold Plating. A variety of gold platings are available for deposition on substrates. These include 24k soft gold, 23+k hard gold (using cobalt, nickel or iron as a hardener), and a number of low (14k–18k) karat golds. Minimum thickness is approximately 0.0008 mm [0.00003 in].
- D. Nickel Plating. Nickel plating may be used to provide an “anvil” effect under gold plate, as a barrier plate to prevent diffusion of copper into gold, or as a bonding surface for direct attachment.
- E. Tin/Lead Plating. This deposit with a composition of approximately 60% tin, 40% lead may be selectively deposited to provide either an etch resist, a directly solderable surface, or both. After deposition, it is generally fused to provide a true solder alloy and to extend shelf life of the product.
- F. Solder Coating. Solder coating is selectively applied by immersing the substrate in molten solder and removing the excess by blowing hot, pressurized air, oil or vapors over the surface of the substrate in a specially designed machine.

2.1.2.5 Polymer Conductors Polymer conductors are typically silver-filled, thermosetting plastics. The metal loading determines the conduction of the system and ranges from 50×10^3 ohms to 2 ohms per square. This family of products is screen printed and cured at from 150 to 175°C for 30 to 60 minutes in a convection oven or, for 10 to 20 minutes under an infrared heat source. Polymer conductors are used in various low-cost circuit designs such as the interconnect of LED displays or adding new circuitry to existing etched copper printed wiring boards.

2.1.2.6 Conductor System Attributes Typical attributes for both thick- and thin- film conductors are listed in Table 2–1.



Table 2-1 Conductor System Attributes

Thick Films	Die Bondability Methods			Wire Bondability		Solderability	Solder Leach Resistance	Corrosion Resistance
	Eutectic	Solder	Organic	Gold	Aluminum			
Au	Good	Poor	Excellent	Excellent	Good	Poor	Poor	Excellent
PtAu	NG	Good	Excellent	Fair to Poor	Fair	Excellent	Good	Excellent
PdAu	NG	Fair	Excellent	Fair to Poor	Fair	Good	Good	Excellent
Ag	NG	Good	Excellent	Good	NG	Good	Poor	NG
PtAg		Good	Excellent	Good	NG	Good	Good	Good
PdAg		Good	Excellent	Good	Good	Good	Good	Good
PdPtAg		Good	Excellent	Good	Good	Good	Good	Good
Cu	NG	Good	Excellent	NG	Fair	Excellent	Excellent	Poor
Ni	NG	NG	Excellent	NG	NG	NG	Excellent	Excellent
Polymeric	NG	NG	Excellent	NG	NG	NG	NG	Good
W/MoMn	NG	NG	Excellent	NG	NG	NG	NG	Good
Thin Films								
Au	Good	NG	Excellent	Excellent	Excellent	Poor (with Ni undercoat OK)	Poor	Excellent
Cu	NG	Good	Excellent	NG	NG	Excellent	Excellent	Poor
Pd	NG	NG	Excellent	NG	NG	NG	NG	Excellent
Ag	NG	NG	Excellent	NG	NG	NG	NG	Poor
Platings								
Au	Good		Excellent	Excellent	Good	Poor	Poor	Excellent
Cu	NG	Good	Excellent	NG	Fair	Excellent	Excellent	Poor
Ni	NG	NG	Excellent	NG	NG	NG	Excellent	Excellent
Pb/Sn	NG	Excellent				Excellent		

2.1.3 Resistive Materials A variety of characteristics are provided by materials that impede signal flow in a circuit, and these entities are considered separately as passive elements in the circuitry. Typical attributes for both thick- and thin-film resistors are listed in Table 2-2.

2.1.3.1 Ceramic Thick-film Resistors Ceramic thick-film resistors are available with sheet resistivities in a range from a very few ohms/square to high megohms/square. The resistivity is controlled by varying the metal-to-glass content which causes large variations in all mechanical and physical properties. Their usage is limited mainly to MCM-C.

Temperature coefficients as low as 50 ppm/°C are readily achievable in the mid-range of from 100 ohms/square to 100 Kohms/square. In the extended ranges, TCRs of 100 ppm/°C are available in resistors as low as 10 ohms/square and as high as 1 Megohm/square.

2.1.3.2 Polymer Thick-Film Resistors A variety of filled organic materials used for polymer thick-film resistors are available. They typically are cured at relatively low temperatures of from 100 to 200°C, and are used with MCM-D and MCM-L.

An important advantage of these materials is their use on a variety of low-melting temperature substrate materials. However, stability is a disadvantage.

2.1.3.3 Thin-Film Resistors A wide variety of film materials are used for thin-film resistors used for both MCM-C and MCM-D. Elemental metals, alloy, and metal/dielectric mixtures have been widely used to provide films with sheet resistivity values ranging from 10 to 2000 ohms/square. Processes involve the use of evaporation and/or sputtering vacuum techniques.

Typical materials used are nickel-chromium (NiCr) and tantalum nitride. Chromium disilicide and tantalum are less typical thin-film resistor materials.

2.1.4 Dielectric Materials Dielectric compositions are playing an increasingly important role in the multichip module technology and will probably continue to do so. The first dielectric compositions used were sealing glasses that served to cover other circuit elements and protect them from attack by atmosphere and other processes. Since the start, the use of dielectrics has spread until the sealing functions are secondary to the more directly functional capacitor, crossover, and multilayer uses.

Table 2-2 Film Resistor Characteristics

Parameter	Units	Thick Film		Thin Film	
		Ceramic	Polymer	Ni-Cr	Tantalum Nitride
Resistivity Range	Ohms/Sq	1-1000 M	10-100K	10-300	5-500
Temperature Coefficient of Resistance	PPM/°C	±50-300	±250-1000	±0-50	±40
TCR Tracking	PPM	10	50	1	1
Power Handling Capacity	Watts/in ²	≤100	25	≤100	40
Thermal Stability (150°C/1000 hrs.)	%ΔR	≤±0.25	≤±2	≤±0.1	≤±0.2
Voltage Coefficient of Resistance	PPM/V	0.5-5	25-100	0	1
High Voltage Stability	%ΔR	≤±0.5	≤±2	≤±1	≤±1
Noise	dB	-35 to +20	0 to +35	<-30	<-10
Trim Stability	%ΔR	≤±0.25	≤±2	≤±0.01	≤±0.01
Load Life 25°C-1000 hrs (rated power)	%ΔR	≤±0.25	≤±3	0.1	≤±0.1
Aging Stability 25°C/50% RH/1000 hrs.	%ΔR	≤±0.25	≤±2	≤±0.1	≤±0.1
Conductor Compatibility	—	Au, Ag, Cu, PdAg, PtAg	Au, Ag	Au, Cu, Al	Au, Cu, Al

For MCM-C dielectric compositions are now firmly established in three important classes of film compositions: resistors, conductors, and dielectrics. The three types of dielectric compositions are crossover and multilayer compositions, capacitor compositions, and sealing or encapsulating compositions.

Table 2-3 lists typical properties of film dielectrics.

2.1.4.1 Thin-Film Dielectrics For MCM-D, thin film dielectrics such as silicon oxide, boron nitride, and silicon nitride are most commonly used, typically for dielectric isolation between layers and as a protective overcoat. Their dielectric constants are low and their uses limited.

2.1.4.2 Organic Dielectrics For MCM-L, rigid polymer materials such as epoxy or polyimide resins reinforced with

fiberglass, aramid or quartz cloth, and non-reinforced polyvinyl or polyimide films are commonly used as a substrate, for dielectric isolation between layers, and as a protective overcoat.

2.1.5 Solder and Flux Table 2-4 lists important characteristics of the typical alloy combinations.

2.1.5.1 Solder Solders are low melting point metal alloys. Soft solders are those whose liquidus is below 315°C. Typical examples of “soft solders” are AuSn, AuGe, SnPb, PbSnAg, SnAg, and PbIn alloys.

Solders are generally encountered in four forms: preforms, bulk, paste and spheres (bumps). Bulk solder is typically used in a solder pot. The substrate is dipped into the pot.

Table 2-3 Dielectric Comparisons

Parameter	Units	Glass Ceramic	Thin Film	Polymer Film
Insulation Resistance Range	ohms	<10 ¹¹	<10 ¹⁰	<10 ⁷
Dielectric Constant Range @ 1 kHz	—	8-14	NA	4-6
Dissipation Factor Range	%	<3.5	NA	<5
Voltage Breakdown Range	Volts/mil	0.002 in film <500	≤100	low
Temperature Coefficient of Capacitance	PPM/°C	<250	NA	NA
Hermeticity	—	excellent	fair	poor
Thermal coefficient of Expansion Range	—	96% Al ₂ O ₃	99% Al ₂ O ₃	high
Conductor Compatibility	—	PtAu, Au	Au	Cu, Ag
Resistor Compatibility	—	good	good	good
Capacitor Value Range (practical)	pF	≤1000	small	small
Trimability	—	abrasive	no	abrasive

Table 2-4 Typical Solder Systems

Alloy	Thermal Conductivity W/m-k	Coefficient of Expansion ppm/°C	Tensile Strength MPa	Shear Strength MPa	Electrical Conductivity % IACS	Melting Range	
						Solidus Deg. °C	Liquidus Deg. °C
Sn96	—	29.3	36.3-57.6	32.1	12.6	221	221
Sn63	50.6	24.7	35.4-42.2	28.5	11.5-11.9	183	183
Sn62	—	27.0	31.0-59	27.6—37.9	14.0	179	179
Sn60	50-65	23.9	18.6-28.0	24.133	11.5	183	191
Sn50	46.5	23.4	—	24.2	10.9	—	—
Sn10	36.0	28.0	—	—	8.2	268	290
Sn5	35.5	28.7	—	—	—	308	312
Sb5	—	—	—	—	10.9-11.9	235	240
Ag1.5	—	—	38.5	21.0	—	309	309
Ag2.5	—	—	26.5	17.9	—	304	304
Ag5.5	—	—	—	—	—	304	380
AuSn	251	16.0	198	185	4.8	280	280
AuSi	293 (94.1-5.9)	10-12.9	255-304	—	—	—	—
AuGe	—	13.0	23.3	22.0	6.0	356	356
PbIn50	—	26.3	32.2	18.5	5.1-6.0	180	210
SnIn50	—	—	—	—	11.7	117	125
AgIn90	—	—	—	—	22.1	141	237
PbIn25	—	—	—	—	4.6	226	264

Then with the metallization wetted with solder, the add-on components are positioned and the solder reflowed.

- A. Temperature Considerations—In electronic assemblies, temperature is a critical parameter. Some assemblies require a minimum temperature at which the solder is still solid; others require a maximum temperature during soldering. In the former the solidus temperature of the alloy is critical, but in the latter the liquidus is most important.

However, neither the solidus nor the liquidus of an alloy are the actual soldering temperatures. A temperature gradient of 30 to 75°C is required over the melting point for good wetting action. The lower rise (30°C) applies to lower melting point alloys. As a rule the alloys in the tin-lead family require about 50°C over the liquidus.

Once the temperature range for an assembly has been set, it is possible to narrow the selection to a group of alloys falling into this category.

- B. Freezing Range—Eutectic alloys have a defined and narrow freezing range. The noneutectic alloys have a “pasty range” within which the solder gradually freezes over a wide temperature range, and during cooling, crystals of the solid solder are mixed with liquid solder.

Assembly movement during the freezing period, can result in a cold solder joint. A cold joint has doubtful quality and could become a fractured joint. Therefore, it is vital that the alloy’s pasty range and the method of application be considered when selecting the material.

- C. Mechanical Properties—For structural design, the alloy’s mechanical properties must be related to the base metal’s mechanical properties. It is important that all stress concentrations be eliminated from the solder fillet.

- D. Electrical Properties—Solder-joint shape and the alloy’s resistivity affect current-carrying capacity and voltage drop. These characteristics can always be matched to those required in the circuit.

- E. Proper Joint Design—The solder joint must be designed with due consideration for its electrical and mechanical properties. For example, the bulk solder strength, including a small safety factor, should be considered for calculation purposes.

In most cases the base metal goes into metallurgical solution in the solder alloy and a mechanism called “solution strengthening” increases the solder strength in the joint area. However, since this is not uniform throughout the joint, it should not be accountable for the added strength it imparts to the solder.

The spacing between the surfaces is important.

Maximum strength can be obtained with a space between 0.05 mm and 0.13 mm [002 and 0.005 in], with the optimum around 0.08 mm [0.003 in]. When the clearance between the surfaces is less than 0.025 mm [0.001 in], the flux and the absorbed air present before the bond formation do not have adequate exit space. This interferes with the joint formation.

When the distance between the surfaces is too large, capillary forces no longer help draw the solder between the surfaces. In this situation voids or gaps can exist.

Solder paste is solder in a screen-printable form that may be printed onto the desired pads and subsequently reflowed.

Solder preforms are normally made from flux-cored solder, and are provided in a variety of shapes, such as rings, ovals, squares, etc., which can be preplaced at the point of soldering prior to application of heat.

2.1.5.2 Flux The choice of base metal dictates both the type of flux required and its use. If the flux is not suitable for the assembly, the base metal must be changed or its surface modified. This can be done by pretinning or plating to allow the use of a more suitable flux.

The effect of flux on circuit components is a very important consideration. Solder pastes generally contain the necessary flux. However, flux must be applied with bulk soldering and in some cases, with preforms. (Steps to remove the flux and its residue must be taken into account when processing the circuit.)

2.1.6 Adhesives While organic adhesives are primarily used to attach devices to substrates and fulfill the bonding requirements, they may also be used to provide thermal and/or electrical conductivity. The materials selected for these purposes must be compatible with temperature-sensitive components.

When a series assembly approach is used (i.e., the sequential attachment of substrates, devices, and covers) a temperature hierarchy must be established. Also, both the mechanical and environmental characteristics of organic adhesives must be adequate to fulfill hybrid and system requirements. Therefore, long-term outgassing products, ionic contaminants, and electrical properties must all be characterized with regard to the reliability and functional requirements of the circuit. Some critical adhesive properties are shown in Table 2-5.

2.1.6.1 Suitability The properties of adhesives that are important in determining their suitability for use in the assembly of hybrid microcircuits include the following:

- A. **Electrical**—Stable electrical properties must be maintained over wide ranges of temperature and humidity, for example, insulating adhesives should maintain a volume resistivity greater than 10^{14} ohm-cm in the dry condition.
- B. **Handling Convenience**—From the standpoint of both economy and user convenience, factors such as storage life, storage conditions, pot life, whether the adhesive is a single-component or two-component system, and whether or not the adhesive is available premixed, frozen, and/or in a ready-to-use tube will influence selection.
- C. **Ease of Application**—Adhesives must be capable of being applied in controlled amounts and thicknesses, and also must give void-free bonds. Insufficient thickness can result in electrical breakdown, while excessive amounts can result in stresses during temperature cycling.
- D. **Flow During Cure**—Excessive flow must be prevented during cure to avoid the coating of adjacent areas that must subsequently be soldered, the bridging of conductor lines, and possibly electrolytic corrosion.
- E. **Outgassing**—Both the release of condensable volatiles during cure, and the continued outgassing after cure are undesirable, as outgassed constituents can absorb onto electronic components and possibly degrade properties.
- F. **Ionic Content**—Adhesives must not contain water-extractable ionic constituents, such as Cl or Na⁺, that will promote corrosion or electrical leakage between conductors.
- G. **Solvent Resistance**—The degradation of bond strength, or the leaching of adhesive components, must not be caused by solvents used in cleaning electronic components, modules, or subsystems.
- H. **Corrosivity**—Adhesives must not be innately chemically corrosive or electrolytically corrosive to the metallization system(s) with which they are used.
- I. **Flexibility**—The adhesives must be sufficiently pliable to relieve mechanical stresses between thermally mismatched materials in order to avoid warping or cracking of the substrates and components.
- J. **Repairability**—It is desirable that the adhesive bond be fracturable at some reasonable temperature and with minimal mechanical force to avoid, during rework, the damaging of any metallization(s) or the breaking of the substrate.
- K. **Hydrolytic Stability**—The adhesive must not chemically degrade (i.e., revert back to a liquid) upon its exposure to high temperature and humidity for long periods of time.
- L. **Thermal Stability**—The adhesive must not decompose at temperatures of subsequent process steps, either in module fabrication or system assembly. It should also be stable in the range of product performance requirements, typically -65 to +150°C.
- M. **Bond Strength**—The adhesive must have adequate bond strength at maximum use temperature, after exposure to commonly used solvents, high humidity, and extended aging.



Table 2-5 Properties of Adhesives

Material	Tensile Strength MPa	Shear Strength MPa	Elastic Modulus Gpa	Hardness	Conductivity W/m-k	Coefficient of Expansion ppm/°C	Resistivity ohm-m	Dielectric Constant @ 1MHz
Silicone	10.3	—	2.21	20-90A	6.4-13 15 7.5	262	10^{13} - 10^{15}	2.9-4.0
Urethane	5.5-55	15.5	.172-34.5	10A-80D	1.9-8 4.6	90-450	3×10^8	5.9-8.5
Acrylic	12.4-13.8	—	.69-10.34	40-90A	—	—	7×10^{11}	—
Epoxy Silicone	—	11.7	—	—	—	—	—	—
Epoxy Novolac	55-82.7	26.2	2.76-3.45	—	—	13 16	10^{13} - 10^{16}	3.4-3.6
Epoxy Bisphenol A	43-85	—	2.7-3.3	106RM	—	14 16	10^{14} - 10^{16}	3.2-3.8
Epoxy Elec. Cond.	3.4-34	—	—	—	.17-1.5	—	10^{-6}	—
Polyimide Modified	—	—	0.275	—	—	73	—	—
Polyimide	—	16.5	3.0	—	—	50	—	—
Epoxy Polyimide	—	41	—	—	—	—	10^{12}	—
Epoxy Polyurethane	34	—	—	—	—	—	—	—

2.1.7 Bonding Wires (Chip-and-Wire Assembly) Gold or aluminum wire bonds are used to interconnect the semi-conductors and ICs to the MCM network and to the I/O pins. The wires are bonded from the chip to a metallized bonding pad that is connected to the circuitry or the I/O pins.

The gold wires are typically alloyed with small amounts of beryllium or copper to control grain growth during bonding. The aluminum wires are typically alloyed with approximately 1% silicon.

The following factors will influence the choice of wire bonding materials and equipment:

- Maximum processing temperature, including rework.
- Size of bond sites on the semiconductor or I/C (0.025 mm [0.001 in] diameter wire thermosonic ball bonding requires pad sizes greater than 0.064 mm square [0.0025 in]).
- Substrate conductor materials.
- Final operating and nonoperating environment.
- The geometry of the MCM package which may restrict bonding tool access.

2.1.8 Tape Automated Bonding (TAB) Materials The TAB interconnect system is based on a polyester or polyimide tape with an interconnect conductor pattern etched in copper foil bonded to the tape. Gold bumps are applied for subsequent thermocompression bonding.

2.1.9 Beam Ledged Components Some components are available with thin leads deposited onto the chip terminations, such as IC bonding pads. These beams create relatively large metal areas that can be welded onto land areas on the substrate when the chip is mounted upside down. Typical beam lead metals are gold or aluminum.

2.1.10 Micro SMT Integrated Circuit Packages A new IC package for MCM and high frequency applications uses semiconductors that are iso-tropically etched to expose the semiconductor, plated beam leads, and conducting silicon pillars attached to the beams. The top portion of the semiconductor and the beams are covered by a conformal plastic coating that is spun on the semiconductor while it is still part of the wafer.

2.2 Components The parts selection process for hybrids requires considerations beyond those for conventional printed wiring components. As a rule, increasing the frequency of operation will require closer attention to devices that must be attached directly to the substrate. These elements are generally divided into two types, i.e., active and passive. The active components are virtually always preselected by the circuit-design engineer and appear on the substrate as an add-on chip, while the passive components can be an integral part of the thick- and/or thin-film deposition or add-on chips.

Active devices are semiconductor chips such as diodes, transistors, and monolithic integrated circuits. The die is the most common configuration for the active device assembly, and in the unleaded, unbumped, chip form requires wire bonding from the chip to the substrate.

Beam-lead devices have preprocessed leads protruding past the die edges to facilitate component attachment to the substrate in a face-down condition.

Flip-chip devices have been processed to provide a solder bump to enable the device to be mounted face down on a mounting pad pattern on the substrate.

2.2.1 Integrated Circuits (Active Devices) Each manufacturer's die and topography is different from that of other manufacturers. Therefore, die bonding patterns and chip sizes from different manufacturers should be examined.

optimize part selection. (Caution: It is easy to design with the smallest possible component, but if the source becomes nonexistent or delivery is not within limits of the program, hybrid layout may be in jeopardy.)

2.2.1.1 Substrate Electrical Potential Many integrated circuit substrates perform an integral role toward providing proper performance of the device. Depending upon the type of device, the substrate may be required to float or to be tied to the most negative potential.

2.2.1.2 Electrical Limitations Unlike packaged devices, extensive testing cannot be performed on components that are in the die form. Thus, circuit designs that require low-current/voltage offsets, AC responses, or temperature responses might not function because of the inability to select (test) the die with probe testing. The testing of die components is generally limited to DC parameters at 25°C or in some instances at elevated temperatures.

2.2.1.3 Visual Inspection Although only limited testing can be accomplished in the unpackaged state, 100% visual inspection to MIL-STD-883 can and should be performed.

2.2.1.4 Confidence Testing A sample quantity of selected devices may be packaged and evaluated through test and burn-in. While this will not indicate exactly how the remaining die will perform, it will serve as an indication of the electrical performance and the possible yield level that can be expected during further use of the device in a hybrid. It will also help to identify defective lots.

2.2.2 Transistors/Diodes (Active Devices) The same considerations apply to discrete semi-conductors that apply to integrated circuits. However, in addition, there are the further implications of diode polarity and die attachment.

2.2.3 Passive Devices Passive devices are those other than integrated circuits or semiconductor devices (such as capacitors, resistors, inductors, thermistors, etc.) that are procured as separately manufactured components. They can also be integrally deposited on the substrate.

Passive devices typically require fewer electrical connections than do active devices. When passive devices have been separately manufactured, there are two major methods of mounting: (1) using a nonconductive adhesive and wire bonding the electrical connection, and (2) using either conductive adhesives or solder (solder will require a higher temperature than the adhesive, but may be processed faster).

The attachment method must be determined prior to specifying the termination material used on the passive device.

2.2.3.1 Capacitors In most cases, add-on chip capacitors are employed in multichip modules due to the fact that

optimum characteristics are usually achieved by unique material systems, fabrication techniques, and geometries.

Chip-capacitor devices are available in silicon, ceramic wafer, multilayer ceramic, or ribbon lead configurations in a wide range of capacitances, voltage ratings, and dielectric materials.

The use of variable-value capacitors is discouraged since they present mounting problems and are not readily available for MCM usage.

2.2.3.2 Resistors Resistor choice is based upon a number of electrical, thermal, and processing capability considerations.

Resistors are available in standard values and tolerances from a size of 1.0 mm x 0.5 mm x 0.25 mm [0.04 x 0.02 x 0.01 in] (RC-0402) at 0.1 W dissipation capability to increased dimensions in proportion to higher power dissipation capabilities.

Tantalum nitride and nickel-chromium chip resistors are available in a wide variety of networks or discrete values. Thin-film resistors can be obtained in several configurations with sizes from 0.43 mm x 0.43 mm x 0.28 mm [0.105 x 0.110 x 0.65 in] for a single-value resistor. Some configurations include several different values on a larger chip.

2.2.3.3 Inductors Although an inductor is not usually a part of a multichip module, when required the primary concern is its physical size, as height restrictions of the multichip module will limit the type and range of inductors that can be used. Miniature wirewound inductors are available in sizes of 2.67 mm x 2.79 mm x 1.65 mm in a range of from 0.01 to 10,000 microhenries in standard values.

The etched thin-film spiral or the screened thick-film spiral have been used for inductors to some degree, but they are limited in terms of quality factor ("Q") and inductance range.

2.2.4 Derating Unlike packaged devices, the MCM thermal environment must be calculated/measured for each application, since packaging density/mounting will determine the thermal rise of the device.

In addition, each particular family of devices has its own unique derating considerations. Thermal and electrical derating guidelines for integrated circuits, semiconductors, capacitors, resistors, and inductors are summarized in Table 2-6.

Failure rates of all components are an exponential function of temperature. Thus the extent of the thermal analysis is a key element in the credibility of predicted reliability. As a minimum effort, the designer should insure that the maximum allowable junction temperature and the maximum

Table 2-6 Derating Guidelines

Substrate Part Types	Maximum Rated Derating Factor				Operating Junction Temperature (Tj ¹)	
	Power ¹ Stress		Voltage/Current Stress			
	Design Goal (%)	Absolute Maximum (%)	Design Goal (%)	Absolute Maximum (%)	Design Goal Hot Spot (°C Allowable)	Absolute Maximum Hot Spot (°C Rated)
Resistor, Thick/Thin Film	25	50		80	N/A	N/A
Resistor, Film Chip	50	80		80	N/A	N/A
2 Capacitor, Ceramic Film Chip	N/A	N/A	50	80	N/A	N/A
2 Capacitor, Tantalum Film Chip	N/A	N/A	50	80	N/A	N/A
Inductor, Film Chip	—	—	—	60 I _{AVE} 80 I _F	110	125
Diode, Chip (general purpose, zener, microwave)	—	—	—	60 PIV 60 I _F 60 I _{ZM}	110	135
Transistor, Chip (bipolar & FET)	—	—	—	60 V _{CEO} 60 V _{EBO} 60 V _{GS} 60 V _{GD} 60 I _C 60 I _B 60 I _G	110	135
Integrated Circuits Digital Bipolar	—	—	—	75 FAN-OUT 75 I _{SINK}	95	110
Digital MOS (CMOS)	—	—	—	75 FAN-OUT 75 I _{SINK} 75 I _S	85	110
Linear	—	90 PSV	—	75 I _L	95	115
Bipolar TTL Memories	—	—	—	75 I _L	105	125
MOS Memories, Static or Dynamic	—	—	—	75 I _S	95- s Static 85-Dynamic	105-Static 100-Dynamic

1. For repetitive pulse applications, determine the average power (P_{AVE}) as follows:

$$P_{ave} = E / R \times t/T$$

where:

E²/R = peak power

t = pulse duration

T = duty cycle

2. Voltages must never be applied in reverse of the normal polarization of a polarized capacitor.
3. Maximum junction temperature ratings for all semiconductors and integrated circuits are assumed to be greater than or equal to the maximum operating temperature required of the device.

4. Legend

FAN-OUT Number of input loads driven

FET Field effects transistors

I_{AVE} Average current

I_B Base current

I_C Collector current

I_F Forward current

I_G Gate current

I_L Load current

I_S Source current

I_{SINK} Sink current

I_{ZM} Zener (maximum) current

PIV Peak inverse voltage

PSV Power supply voltage

TTL Transistor-Transistor logic

V_{CEO} Collector-to-emitter voltage with base open

V_{DIF} Differential input voltage (defined as applied input voltage swing vs. manufacturer's specified input swing)

V_{EBO} Emitter-to-base voltage with collector open

V_{GD} Gate-to-drain voltage

V_{GS} Gate-to-source voltage

V_{PK} Peak voltage

V_S Voltage supply



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allowable hot-spot temperature have not been exceeded as based on the calculated power dissipation of the unit.

2.3 Multichip Module Design Layout The first step in the design process is to determine the appropriate component mounting substrate, component selection, and interconnection technology that will be required to meet the end use environment conditions as established in Table 1-4. A cross-functional engineering team should review the relative applicability of major design characteristics of each MCM type and compare these to the performance required.

As with any technology, the consistent utilization of absolute workable minimum values will result in reduced circuit yields. When any design/layout guideline is established, these data should be given: the absolute minimum to be used only with approval, the suggested minimum, and if applicable, the maximum dimension.

2.3.1 Layout The initial diagram should show all components in their relative positions as they will appear in the final layout. This drawing or sketch is usually termed the "preliminary layout." The inputs to the layout process should include special component positioning requirements if there is interaction among the components that will affect overall circuit performance.

2.3.2 Computer-Aided Design (CAD) The state-of-the-art in the application of CAD systems to the design of multichip modules is such that the term interactive graphics (IG) more properly applies. Since IG is truly computer-aided, and will ultimately develop into true CAD, the broader term "CAD" will be liberally applied herein.

In making the decision concerning the use of CAD in the design cycle, the designer should carefully consider potential savings in design and manufacturing. By the early entering of the design into a digital database, the MCM designer can in many cases reduce production costs by the application of computer-aided manufacturing (CAM) techniques. Some examples include the following:

- The automatic preparation of programs and data for laser trimmers,
- The use of automatic chip-placement machines,
- The use of automatic wire bonders,
- The use of digital test equipment,
- MCM Geometry,
- Drilling and pick-and-place,
- Hole or via preparation,
- Photo tooling
- CAD systems can accommodate virtually any grid with its origin at any point. The grid size and its origin can be changed during the design cycle. In addition, the grid can be turned on and off as desired. The grid should be

selected to accommodate the smallest dimension as required.

- CAD design rules should conform to those detailed for the manual design of MCM circuitry. The designer should devote special attention to features such as arcs, circles, and fillets because of their difficulty to implement using cut-and-peel techniques.
- Some CAD systems have automatic design rules checking features that automatically check for adherence to design rules such as minimum spacing minimum line width, and minimum overlap. When available, this CAD feature should be used prior to photoplotting.
- At this point the entire design consists of two CAD data files: (1) the schematic or electrical description, and (2) the layout with additional documentation features. Any changes can be easily accomplished in the data base using specialized CAD features and then generating a new set of drawings and phototools with pen and photoplotters.

2.3.3 Conductor Layout Rules The following are general design/layout rules regarding multichip modules. Individual rules regarding individual processes used by manufacturers should be generated.

2.3.3.1 Type of Operation The type of assembly operation, e.g., soldering, wire bonding, epoxy attachment, etc., must be considered before choosing the appropriate conductive method.

2.3.3.2 Conductor Width Determine the absolute minimum conductor width (either thick- or thin-film) which can be accommodated.

2.3.3.3 Conductor Length Conductors, when run for long distances, can add sufficient resistance to the circuit to alter its final operating characteristics.

2.3.3.4 Conductor Spacing High-frequency operations can be detrimentally affected by the gap (spacing) between conductors, particularly when the conductor traces run parallel for long distances. This parameter can assume such importance as to determine the usable technology (thick- or thin-film) that can be used to fabricate a circuit.

2.3.4 Conductive Pattern Capabilities Comparison The following comprises a head-to-head comparison and in depth analysis of the three technologies, thick film for MCM-C, thin film for MCM-D, and plated and etched/plated for MCM-L. This is a guideline prepared to help those in the technology as a starting point for their own design rules.

- A. Metallization pattern resolution. MCM-D designs offer finer metallization pattern resolution than do MCM-C or MCM-D.



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- B. Conductor Width and spacing.
- MCM-C conductor lines (usually deposited on 96% Al_2O_3) are 0.25 mm [0.01 in] preferred minimum width and 0.13 [0.005 in] mm in space limited areas.
 - MCM-D conductor lines (usually deposited on 99.5% Al_2O_3) are 0.13 mm [0.005 in] preferred minimum width and 0.06 mm [0.002 in] in space limited areas.
 - MCM-L conductor lines (usually etched or electrodeposited) are 0.1 mm [0.004 in] preferred minimum width and 0.05 mm [0.002 in] in space limited areas.
- C. Resistor Size
- Thick film resistor widths are 1.02 mm [0.04 in] preferred minimum, and 0.76 mm [0.03 in] in space limited areas.
 - Thin film resistors on Al_2O_3 are 0.06 mm [0.002 in] minimum width.
 - Thin film resistors on silicon or polished ceramic are 0.025 mm [0.001 in] preferred minimum width and 0.013 mm [0.0005 in] in space limited areas.
 - Some thin film resistor chip suppliers use resistor line widths of 0.008 mm [0.0003 in] and 0.005 mm [0.0002 in] for special high resistor value applications.

2.3.4.1 Basic Thick Film Technology (For MCM-C) The thick film technology used in type C multichip modules involves the following parameters.

- Substrates. Thick film technology is primarily cermet, using ceramic, or glass ceramic materials.
- Conductors. Conductor materials are typically created from screenable frits of gold, silver, palladium, or copper. Tungsten and molybdenum may also be used.
- Resistors
 - Resistors in the 1K to 10K range have the best Temperature Coefficient of Resistance (TCR) and load-life stability. TCR's of 50 ppm/°C and 0.1% stabilities after load-life stressing are commonplace. The stability of high and low resistor pastes deteriorates exponentially as shown in Figure 2-1.

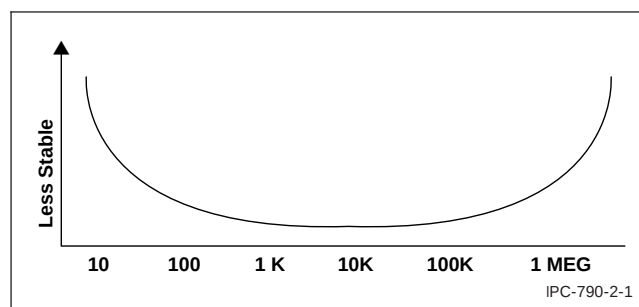


Figure 2-1 Resistor paste stability

- Resistors below 10 ohms are made with great difficulty, as are resistors above 10 megohms.
- Cermet resistors are voltage variable. The Voltage Coefficient of Resistance (VCR) is dependent on the resistor geometry and ink formulation. The range of VCR can be from 3 to 10 PPM/V. High VCR causes odd order harmonic distortion and cross-modulation in signal circuits.

2.3.4.2 Basic Thin Film Technology (for MCM-D) When considering the design and use of the thin-film technology, the following parameters should be considered.

- Substrates. Thermal considerations, size constraints, capacitance, assembly considerations, and cost influence the choice of substrate materials, e.g., alumina (ceramic), oxidized silicon, glass, sapphire, beryllia, etc.
- Conductor Material. Either aluminum, gold, or sometimes copper is usually chosen for the thin-film conductor material depending on the type of bonding equipment to be used, whether or not a monometallic system is desired. Thickness of conductors is always above 0.6 microns since wire bonding becomes difficult or impossible at or below this thickness. Thicker films of 3 microns or more are used where necessary for microwave circuits.
- Resistors. A wide variety of film materials are used for thin-film resistors. Elemental metals, alloys, and metal/dielectric mixtures have been widely used to provide films with sheet resistivity values ranging from 10 to 2000 ohms per square. Processes involve the use of evaporation and/or sputtering vacuum techniques.

Typical materials used are nickel-chromium (NiCr) and tantalum nitride. Chromium disilicide and tantalum are less typical thin-film resistor materials.

- Resistor Cost Comparisons. The factors most influencing costs are:
 - Tolerance
 - Density: Number and value of resistors on a given network
 - Substrate: Beryllia only; all others equal but higher than thick film
 - TCR: if zero wanted
 - Circuit size (yield) and ratios
 - Visual inspection
 - Stability greater than 0.1% R (+150 20 @ 1000 hrs.)
 Those that do not usually affect costs or have a minimal impact are:
 - Resistor film
 - Conductor film: unless very thick layers are desired
 - Noise: comes with the film
 - Stability down to 0.1% R
 - Substrate

e. Advantages and Disadvantages. Thin film technology has some constraints different from thick film, and some advantages. One of the basic constraints is that the available sheet resistance of resistor material is in the range of 100 to 200 ohms/square. A consequence of this is that very small (less than 10 ohms) and very large (over 100 K ohms) resistors take up a lot of real estate. The main advantages of thin film resistors are their load life stability, low noise and predictable TCR.

2.3.4.3 Multilayer Technology All three designs offer a multilayer conductor capability. The number of layers in thick film designs range from 1 to greater than 5. For MCM-L, the number of layers may range from 1 to 20 or more. The multilayer capability offsets the wide line restrictions with high component and interconnect densities.

True multilayer designs consist of full layers or blankets of dielectric between adjacent layers of interconnect metallization. Layer-to-layer interconnection of the metal layers is made by vias (window openings), or, for MCM-L, with plated-through holes through the dielectric layers.

- Conductor Routing (MCM-C)

- Avoid running one conductor which is parallel to another conductor directly beneath it for long distances.
- There should be an overlap where a top and bottom conductor connect.
- Avoid running the conductor over the edge of multiple dielectric layers.
- If necessary to run conductors over the edge of a single dielectric layer, the spacing and "stagger stepping" should avoid shorting due to the spreading effect.
- It is recommended that a minimum of conductor levels be used since processing yields will be affected by each additional layer.
- Provide test points for continuity checking between conductor levels.

- Conductors Routing (MCM-L)

- Avoid running one conductor which is parallel to another conductor directly beneath it for long distances.
- Keep length of conductor between two lands at a minimum.
- Conductors which are straight lines and run in X, Y, or 45 degree directions are preferred to aid computerized documentation for mechanized or automated layouts.
- All conductors that change direction, where the included angle is less than 90 degrees should have their internal and external corners rounded.

e. It is recommended that a minimum of conductor levels be used since processing yields will be affected by each additional layer.

- Vias (MCM-D) The selection of via design will depend on the specific layout of the adjacent conductor levels. vias may be square, rectangular or round. It is recommended that a minimum dimension of 0.25 mm [0.01 in] width, length and diameter be followed since processing yields are affected using smaller dimensions.

Various via designs are as follows:

- Via window smaller than bottom conductor but larger than top conductor.
 - Via window larger than bottom conductor but smaller than top conductor.
 - Via window larger than both top and bottom conductor.
- Vias (MCM-L) The selection of hole (via) design will depend on the specific layout and space requirements. Plated-through vias may be blind (exposed on only one outer surface), buried internally with no external exposure, or through the entire substrate with exposure on both outer surfaces. It is recommended that a minimum dimension of 0.25 mm [0.01 in] width, length and diameter be followed since processing yields are affected using smaller dimensions.
 - Power/Ground Planes (MCM-C) In a typical multilayer design, a combination power/ground plane is screened directly on the substrate. Vias for the power and ground connections are often made larger than the vias for signal interconnection because the power and ground connection vias carry more power and they traverse more layers. Above this are alternate layers of dielectric and interconnect metallization.
 - Power/Ground Planes (MCM-L). Power/ground planes are etched and laminated as an integral part of the multilayer structure between dielectric layers and interconnections are made to the signal layers by plated-through vias.
 - Bonding Lands (MCM-C and MCM-D). The top layer contains all device I/O bonding lands and the substrate I/O lands. If space permits, this layer may also contain some interconnections. Metallization lands are provided for physical attachment of the integrated circuit chips. These lands are normally connected to ground or a voltage supply. Six metallization layers are generally considered to be a reasonable maximum. The base metal in coated metal-core substrates may be utilized as a ground plane that is contacted by printing a circuit directly over a via through the coating.
 - Bonding Lands (MCM-L). Bonding lands on MCM-L circuits are normally produced by selective etching of the surface copper during the manufacturing process and are connected to vias by additional electrodeposited copper on the land surface and through the via.

electrical continuity from the bonding surface to all necessary internal layer lands and circuitry.

- Resistors for Multilayer Applications. The following specific details apply to the use of resistors in multilayer MCMs.

- Resistors may be printed on the dielectric.
- Dielectric should not be printed over a thick film resistor.

Some multilayer designs for circuits containing resistors use:

- Ceramic chip resistors.
- Thick film resistors located outboard of multilayer section on the same substrate.
- Thick film resistor printed on dielectric (top level).

Note: Resistor material should be selected such that the material is able to withstand curing temperatures of the dielectric material, especially in the case of MCM-D dielectrics.

2.3.5 Technology Capability The technology capability within a hybrid fabrication company can be identified as being one or more of the following:

- Thick-film circuit fabrication (MCM-C)
- Thin-film circuit fabrication (MCM-D)
- Clad organic (polymer) (MCM-L)
- Assembly of packaged and unpackaged components
- Encapsulation
- Interconnection
- Packaging

Note: The thick film technology (A) can also be used with MCM-L (C).

The practical application of the elements that go into making a multichip module do impose some restrictions. In an attempt to avoid some of the conflicts and perhaps unnecessary iterations that may occur between the conceptual phase and/or system design and the completion of a dependable, economical, functioning circuit/system, the following checklist of processes and materials is included to provide the designer with knowledge of the limitations and restrictions imposed by in-house process and fabrication restrictions. These discussions should be used as a guide to establish a working relationship between design and manufacturing at the earliest possible time frame to insure that the design, as submitted for fabrication, has incorporated all of the cost effective operation, equipment and materials available plus proven methods being utilized by the selected facility.

2.3.5.1 MCM-C Substrate Fabrication The design of ceramic (alumina, beryllia, etc.) substrates for multichip modules is largely dictated by the application. However, designers should be generally aware of ceramic technology in order to avoid unnecessary and costly design errors. Most ceramic substrates for electronic applications are manufactured by either a dry pressing or tape casting process. In the former, the part is formed by compacting a powder in a specially designed tool or die. Sharp corners should be eliminated by designing chamfers or radii at the corners. Holes may be pressed in the part, but are subject to shrinkage tolerances listed below. The dry pressing process best lends itself to high volume production, but the process is confined to substrates of limited area-to-thickness ratio.

Parts formed by tape casting are punched in the desired shape from a flexible “green” (prefired) tape and fired. The tape is produced by drying a slurry cast on a moving belt. The advantage of the tape process is that it permits the manufacture of substrates with large area-to-thickness ratios. Typically, suppliers are able to provide substrates up to 100 mm square [3.9 in] in area with thicknesses of less than 1.2 mm [0.05 in].

Regardless of the forming method utilized, all ceramics shrink when fired. Therefore, as-fired dimensional tolerances are a function of shrinkage control. Typical as-fired dimensions are shown in Table 2-7.⁸

Table 2-7 Ceramic As-Fired Dimensions

Dimension/Feature	Tolerance
Dimensional tolerances, mm	±1% 0.08 mm [0.003 in] max.
Thickness	±2% 0.08 mm [0.03 mm] max.
Holes, dimension and location	±1% 0.13 mm [0.005 in] max
Flatness and parallelism	0.10 mm/ mm 0.05 mm TIR max

Parts with more stringent dimensional tolerances can be manufactured, but they generally require expensive machining. Typical machined tolerances are listed in Table 2-8.⁹

Table 2-8 Dimensional Tolerance

Dimension	Tolerance
Length, Width	±0.025 mm
Diameters (OD)	0.025 mm
Hole Diameters	±0.025 mm
Hole Locations	±0.13 mm
Radii	±0.13 mm
Angles	±1°
Flatness (TIR)	0.025 mm
Parallelism (TIR)	0.025 mm



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Ceramic substrate has a characteristic microstructure and alumina or beryllia supplied by one manufacturer will very probably have a different average grain size and surface finish than that produced by another manufacturer. Since these characteristics may have an effect on the effectiveness of the planned metallization, they should be carefully specified.

2.3.5.2 MCM-D Substrate Fabrication The choice of substrate for the Type D multichip modules, as in the case of MCM-C, is largely dictated by application. Since the thin-film circuitry is normally applied to unreinforced dielectric materials, an underlying substrate is usually required for dimensional stability. These may be ceramic, silicon, copper, other metal or metal composites, or coated metal cores.

Coated metal-core substrates are formed by coating a metal stamping (steel, copper-clad Invar, Inconel, copper, etc.) with an electronic grade coating fired at about 800°C. The stamping can have holes, cutouts, notches, bends, etc. By using “coining tools,” holes and edges may be fully insulated from the base metal by the coating. Tolerances are as for ceramic substrates except for a meniscus around holes (minimum diameter 1.0 mm) and along edges.

2.3.5.3 MCM-L Substrate Fabrication The substrates for type L Multichip modules are fabricated by laminated printed board technology. Specific materials used will be dictated by application, but will normally consist of a laminated structure of resin reinforced with woven or mat material and clad with copper of varying thickness on one or both sides. Unlike MCM-C or MCM-D, where the conductors are normally applied to the substrate by sputtering or screening after its fabrication, the copper conductors on MCM-L are etched or deposited as an integral part of the substrate manufacturing process.

Resins most commonly used are epoxy, polyimide, polyester, or polytetrafluorethylene with a reinforcing cloth or mat structure of materials such as paper, glass, aramid, or quartz.

Single sided printed boards are produced by masking the desired conductor configuration with an etch resist either by photoimaging, silk screening, or electrodeposition of a 60/40 composition tin/lead deposit. The unwanted copper is removed by etching, component or communication holes are drilled as needed, and the part is machined to final configuration.

Double-sided boards are produced by a more detailed process, using the following steps:

- a. Drill all holes to be plated-through, approximately 0.13 mm [0.005 in] larger than desired final diameter.
- b. Chemically process board to provide a thin film of electroless copper over all surfaces and through the drilled holes.

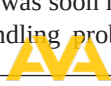
- c. Print negative plating resist image of the desired circuit configuration by photoimaging or silk screening, leaving the circuitry bare.
- d. Electrodeposit copper on the exposed circuit areas and through the drilled holes.
- e. Electrodeposit 60/40 tin/lead on exposed conductor areas and through the drilled and copper plated holes.
- f. Remove the plating resist image and etch off the copper in the non-circuit area.
- g. Machine to final configuration.

The multilayer process utilizes all of the above steps, after the following procedures have been accomplished:

- a. Print a positive circuit image of each individual layer of circuitry on a separate single-sided panel or one side of a double-sided panel by photoimaging or silk screening. Thin laminates with copper on both sides may be used for two layers.
- b. Etch off the copper in the non-circuit areas.
- c. Laminate the layers together into a homogeneous structure, using as bonding plies, thin sheets of appropriate cloth coated with the same resin used in the layer laminate material and partially cured. The individual layers of circuitry are keyed to tooling holes to assure proper registration of internal circuitry and lands, and the bonding takes place under sufficient heat and pressure to complete the cure on the resin in the bonding plies and form the finished multilayer structure.
- d. After hole drilling is complete, the bare holes are subjected to chemical and/or mechanical treatment to clean the hole walls and assure good electrical contact between the exposed internal copper lands and the plated-through copper.

Minimum thickness is approximately 0.05 mm [0.002 in] (for a single ply laminate with 1/4 oz. (9 µm) copper. Because of the capability of the process to produce multilayer boards of up to 20 layers or more, maximum thickness becomes a matter of design needs and package limitations. Thickness tolerances range from 0.05 mm [0.002 in] to 15% of nominal thickness.

Outline configurations are typically toleranced to 0.13 mm [0.005 in], although tighter tolerances can be achieved at the expense of higher cost and reduced yield.

2.4 Packaging and Higher-Level Assembly Historically, through chip and wire assembly techniques, the microelectronic industry moved in the direction of ultraminiaturization to increase packing density at the next level, to increase reliability and to ultimately reduce cost. However, a cost effective crossover point was soon reached where the small size of chips led to handling problems.  **Documents**

then had to be put in larger packages and “chip-size factor” was somewhat negated. Today, semiconductor technology has reached a level of sophistication where chip sizes are getting larger and the partitioning of circuits is more easily accomplished. Thus, many discrete components are attached to alumina substrates which are then put into a next level packaging form, e.g., into DIPs, flatpacks, TO-cans, etc.

2.4.1 Environmental Considerations Environmental considerations should be an integral part of package selection and design as the MCM packaging protects the microcircuits from the outside world. Some of the important factors which must be considered and which interact with each other are discussed below.

The presence of moisture, in the form of water vapor, has been a source of many problems in electronic equipment. Its effect in multichip modules may be displayed by several failure modes: (1) the growth of metallic dendrites, (2) metal migration, and (3) intermetallic formations, caused by the presence of bias and moisture, that completely alter and eventually destroy the MCM circuits.

Certain types of materials, such as tin and silver, are more active than others in the metal migration problem. Electrical bias conditions and elevated temperatures can accelerate the formation of these faults.

Ionic contamination, usually negatively-charged elements such as those in the halogen series, are found to be serious problems in hybrid microcircuits. Therefore, both the basic design of the hybrid microcircuit and the processing materials and methods employed should be given adequate consideration in order to keep these problems managed and controlled.

2.4.1.1 Hermeticity When specifying packaging to be used, the permissible leak rate should be considered in relation to the intended use. A long-term mission in a vacuum would impose different requirements than short-term usage. Also, moisture that might be tolerated at operating temperatures of 100°C might not be tolerable in a -10°C environment.

2.4.1.2 Corona Package shape and construction can be critical for corona sensitive devices and must also be considered in light of hermeticity requirements.

For circuits that are susceptible to corona problems, the change in internal package atmosphere during the operational life of the device must be considered, as a very small leak rate can cause significant changes over an extended lifetime.

2.4.1.3 Shock and Vibration The expected shock and vibration environment must be evaluated with respect to its effect on the integrity of the package's hermeticity, corona sensitivity, and the transmission of stresses to the MCM substrate.

2.4.1.4 Thermal Considerations Power dissipation has a major influence on circuit partitioning and ultimate package size. Also, all material and component operating capabilities are limited by inherent maximum operating temperatures, above which their performance may either degrade seriously or catastrophic failure may occur. With semiconductors, this temperature is usually specified in terms of a maximum junction temperature. For other components, the maximum body temperatures and hot-spot temperatures are commonly used as the figures of merit.

In any case the maximum operating temperature of an electronic material or component is a direct result of the electrical power dissipated in the element associated with the component. All components, especially resistors and active devices, will dissipate heat in the performance of their normal electrical function. Therefore, the problem is to remove the heat as quickly as possible to prevent temperature rises within the heat-generating elements.

A thick substrate is used for best heat transfer and distribu-

Table 2-9 Typical Materials Thermal Conductivity

Material	Thermal Conductivity W/°C/mm
Silicon	58.4
Kovar	9.1
Molybdenum Tab	99.1
Alumina (Al ₂ O ₃)	17.5
2 3 Beryllia (BeO)	139.7
Conductive Epoxy	1.02
Epoxy Preform	0.25
AuSi Eutectic Bond	144.8
AuSn Solder	114.3

tion unless it is to be bonded to a heat sink, in which case the thinnest possible substrate should be used.

The substrate area required for a given electronic circuit is greatly dependent upon power levels of components. Thus, low power level circuitry can be packaged more densely than power circuits.

The use of some first approximation “rules-of-thumb” for the number of devices (chips) that can be accommodated with a given technology in various package sizes would provide a starting point, together with the thermal considerations, for deciding if the given circuitry needs to be partitioned. Another deciding factor in partitioning is the input/output (I/O) requirements of the circuitry.

Select materials with good thermal conductivity. Table 2-9 is a useful guide for material selection.¹⁰

2.4.1.5 Radiation The effects of external electromagnetic and nuclear radiation must be considered in terms of the expected environment, the transmission of the radiation

through the package to the device, and the secondary radiation produced in the package materials by incident primary radiation.

2.4.1.6 Long-Term Stress and Corrosion The exposure of the package to long-term hostile environments may eventually lead to a failure in package integrity. Therefore, the package selection process should consider these aspects of intended usage, especially the effect of current applied in the presence of these conditions.

2.4.1.7 Higher-Level Assembly The environments experienced during actual assembly operations must also be considered. In particular, temperature and stress conditions must be considered, including those caused by lead bending, and the use of cleaning solvents and conformal coating.

2.4.2 Package Considerations When choosing a package, it is best to consider the use of an industry standard package, provided that it is compatible with the system constraints. In using a standard package, the costs are usually minimized. A further consideration might be whether for a given design situation it is necessary to package at all.

2.4.2.1 Pin Assignment Only pinout locations that are absolutely critical to the system's electrical performance should be preassigned. Otherwise, the pinouts should not be preassigned, but their assignment should be left to the discretion of the layout specialist.

2.4.2.2 Standard Packages A wide range of packages are available. These include welded-metal packages, epoxy-and-glass-sealed ceramic packages, and plastic types. The choice of package type is based upon mechanical and environmental requirements and manufacturing considerations.

ISHM has developed industry standards for a set of package sizes for both metal and ceramic packages. These are published as SP-008-M and SP-008-C respectively.

2.4.2.3 Lead Type A factor in package selection is the type of leads available. For reflow soldering, planar leads would be the best choice. For wave soldering, plug-in leads would be required.

2.4.2.4 Radiation (Internal) Certain package materials have been shown to be low level emitters of radiation (usually alpha particles). Care should be taken when choosing a package to ensure that such a package is not used with devices that are sensitive to this kind of radiation (i.e., large scale RAMs, etc.).

2.4.3 Reliability Evaluations The basis for a reliability prediction should begin by examining the system partitioning. Math models can be so formulated from block dia-

grams to derive probability of operational success that is consistent with contractual constraints. The achieving of the desired reliability, and the elimination of single-point failures, may impose constraints on the circuit partitioning decision.

Reliability prediction techniques should be employed as a part of major tradeoff studies. These prediction calculations should employ applicable baseline failure rates for piece parts. The adherence to derating guidelines will help to minimize the need to adjust failure rates for the stress conditions imposed by application and environment.

2.4.3.1 Single-Point Failures It is necessary to minimize the possibility of failure of the end items due to the failure of a single component. Therefore, particular attention should be given to tradeoffs that provide isolation, filtering, or overstress protection.

2.4.3.2 Worst-Case Analysis A worst-case analysis should be performed of both electrical and environmental conditions.

2.4.3.3 Failure Mode and Effects Analysis (FMEA) The FMEA defines the various failure states that can exist at a defined system (or subsystem) interface level. A typical FMEA at the MCM level is the examination of each input/output power termination and the immediate interface components to define the possible failure modes and subsequent effects on the module itself and on higher-tier circuitry.

2.4.4 Test Requirements Multichip modules should be designed in a way that facilitates testing and failure diagnosis. Therefore, unused pins should be used to bring out test points. Also, if heat sinking during test is required, this should be specified.

Troubleshooting and testing should be accomplished by documentation that shows pinouts, unused pins, component reference designators, nominal values, and tolerances.

Test pins or points should be provided and designated wherever needed.

Particular attention should be paid to areas where active trimming is required. The layout should be such that the test probes do not shadow a trimming laser beam. Also, some precautions should be taken to help prevent the laser beam and ambient light from causing spurious photocurrents in active devices.

2.4.5 Qualification Typical qualification procedures for the testing of multichip modules should include (but not necessarily be limited to) the following from MIL-STD-883:

- Thermal Shock
- Moisture Resistance



- Steady State Life
- Salt Corrosion (when appropriate)
- Shock and Vibration
- Constant Acceleration
- Thermal Fatigue (temperature and power cycling)

These procedures assist in achieving a level of quality and reliability commensurate with the intended application. They must be used in conjunction with other documentation, such as MIL-H-38354 and the applicable detail specification, to establish the requirements which are needed to achieve prescribed levels of quality and reliability.

2.4.6 Assembly Techniques The manner in which the multichip module is assembled will affect the loss in the electrical performance of the circuit, as well as provide an upper limit to the operating frequency.

Impedance matching and high current circuits often require ribbon interconnections in lieu of wire. Bond wire/ribbon lengths need to be kept at a minimum in order to minimize parasitic inductances that can mask device characteristics.

The graph in Figure 2-2 shows the relationship between inductance and wire length for various diameter wires and a ribbon. As can be seen from the graph, large diameter wires and ribbons allow device operation at higher frequencies.

The problem with inductance can be minimized by using alternate chip attachment techniques, such as beam-lead, flip chip or TAB.

If solder-mounting techniques are used, attention must be paid to the difference in the rates of thermal expansion of the materials joined, as voids in solder connections, that may be acceptable at lower frequencies, must be minimized in microwave applications to minimize circuit losses. Solder voids in the substrate/package interface must also be minimized in order to maintain ground plane integrity.

The testing of substrates prior to placement in packages can be facilitated by mounting substrates on carrier plates.

2.5 Electrical Design Guidelines

- Distribute power sources as evenly as possible over the substrate surface to reduce hot spots and to maintain a uniform thermal profile.
- Locate the highest-power sources over or near heat sinks.
- Do not locate high-power sources near substrate corners or edges unless heat sinking is provided in that vicinity.
- Design power resistors as large as possible and assure that sufficient area will be maintained after adjustment.

- High-heat dissipating components should be attached to the substrate in such a manner as to provide the lowest possible thermal resistance between the components and the substrate.
- Components should not be attached over other heat dissipating elements, i.e., chip capacitors over thick-film resistors.
- For best thermal performance, make the junction between a backside-mounted semiconductor chip and the substrate with a material of low thermal resistance that is as thin as possible, and provide a uniform contact area that is free from voids. (In this regard a knowledge of process capability is critical. If the worst-case die attachment wettability is 50%, base heat transfer calculations on the reduced area.)
- When wire leads or pins are attached to a substrate, try and adhere to the following rules: (1) make leads or pins as short as possible, (2) select a pin material of high thermal conductivity and a pin size with the maximum possible cross-sectional area, (3) use as many leads as possible, and (4) locate heat sources as near to the pins as possible.
- In final packaging, you should, (1) select a package configuration that will provide the best thermal conductivity for a specific application, (2) provide a good thermal conduction path between the substrate and the package case, and (3) avoid air spaces in the thermal conductivity path if possible. Plastics with high thermal conductivity can be used to fill voids and improve heat transfer.

2.5.1 Heat Dissipation Calculations The rise in temperature of each component can be estimated using a model of thermal resistance and power dissipation in which the temperature rise is calculated as,

$$T = R \times P$$

Where:

T = temperature rise of the device above the hybrid case (degrees C)

R = total thermal resistance between the device and the hybrid case (degrees C/W)

P = power dissipated in the device (W)

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and MCM case (see Figure 2-3). Thus,

$$RT = R_1 + R_2 + R_3 + R_4 + R_5$$

Where:

RT = total thermal resistance from the top of the device to the bottom of the hybrid case.

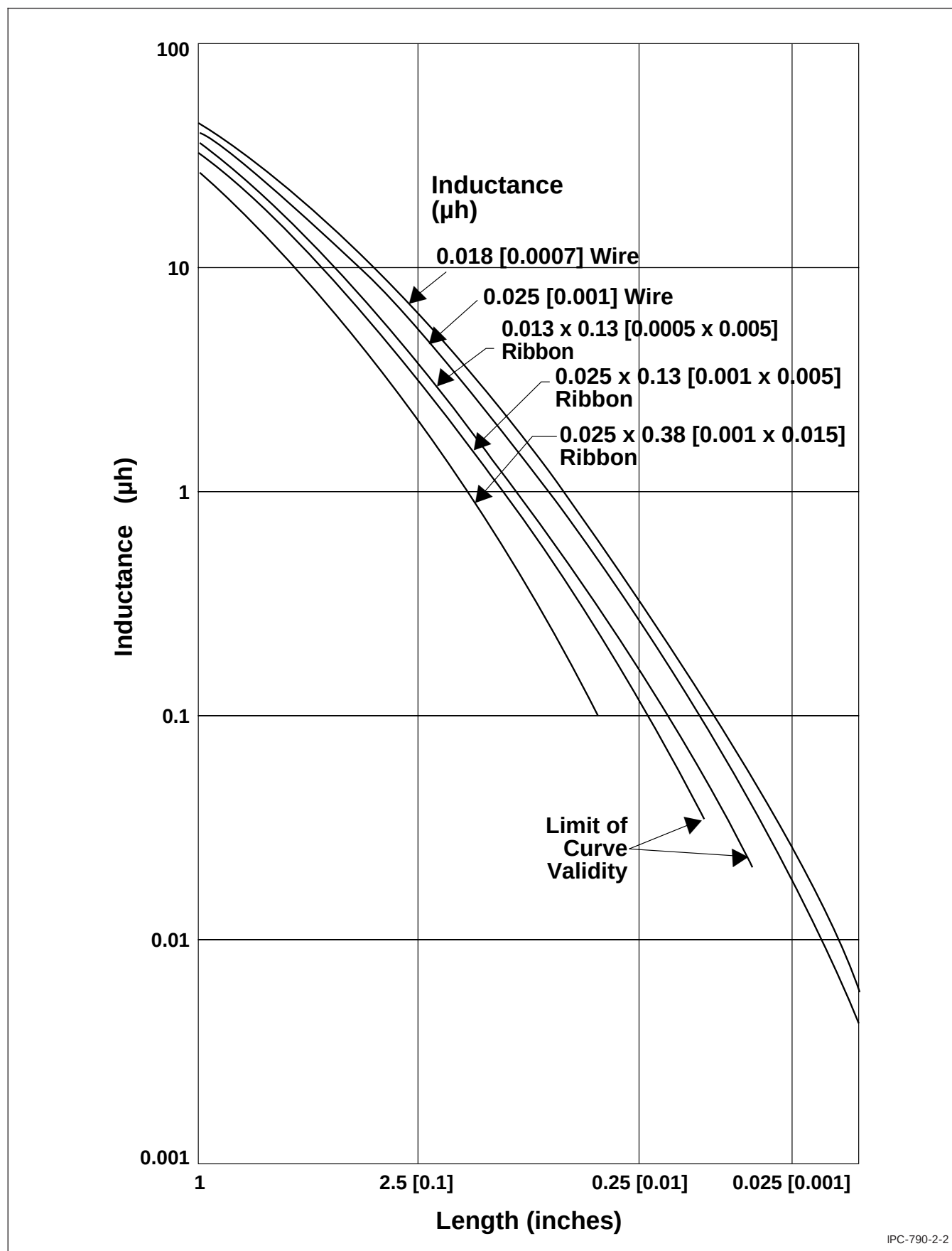


Figure 2-2 Inductance/wire length relationships



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