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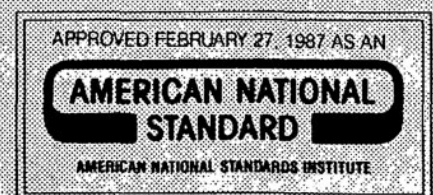
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Performance Specification for Rigid Multilayer Printed Boards



A STANDARD DEVELOPED BY THE INSTITUTE FOR INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS



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Performance Specification For Rigid Multilayer Printed Boards

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A STANDARD DEVELOPED BY THE
PERFORMANCE AND RELIABILITY SUBCOMMITTEE OF
THE RIGID PRINTED BOARD COMMITTEE OF
THE INSTITUTE FOR
INTERCONNECTING AND PACKAGING ELECTRONIC CIRCUITS.

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Performance Specification for Rigid Multilayer Printed Boards

1.0 Scope

1.1 Scope. This specification covers qualification and performance of rigid multilayer printed boards with plated-through holes. Circuitry may be bare copper, metallic overlaid or coated, unfused, fused, leveled etc.

1.2 Purpose. The purpose of this specification is to provide classes of requirements for performance/acceptance of multilayer printed boards for industry and government use, (excluding multilayer flexible and rigid-flex products).

1.3 Classifications. This specification recognizes that the multilayer printed boards will be subject to classifications by intended end item use. Towards this end, three general classes have been established to reflect progressive increases in sophistication, functional performance requirements and testing inspection frequency. It should also be recognized that there may be an overlap of equipment between classes. The user has the responsibility to determine the class, into which this product belongs. The three classes are defined below:

Class 1—Consumer Products

Includes TV sets, toys, entertainment electronics and non-critical consumer or industrial control devices. Boards in this class are suitable for applications where cosmetic imperfections are not of importance and the major requirement is function of the completed circuit.

Class 2—General Industry

Includes computers, communication equipment, sophisticated business machines, instruments and certain non-critical military applications. Boards in this class are suitable for high performance commercial and industrial products in which extended life is required but for which uninterrupted service is not critical. Certain cosmetic imperfections are allowed.

Class 3—High Reliability

Includes those equipments where continued performance is critical, equipment downtime cannot be tolerated or the equipment is a life support item. Boards of this class are suitable for applications where high levels of assurance are required and uninterrupted service is essential.

Requirements in this specification have been separated so that the performance of the multilayer printed board products may be tested to any one of the three classes. The use of one class for a specific attribute does not mean that all other attributes must meet that same class. Selection should be based on minimum need, however, cross-over between

classes requires complete definition of test requirements in the procurement document.

Note: Unless otherwise specified, military electronic equipment shall be Class 3. Printed boards furnished under this specification for military usage shall be fabricated by a supplier who has been certified by inspection in accordance with paragraph 4.4 and 4.5.

1.4 Dimensions and Tolerances. All dimensions and tolerances specified herein are applicable only to the end product. Dimensions are expressed in millimeters. Inches, shown in brackets [], are not direct conversions in order to provide usable numbers. Users are cautioned to employ a single system and not intermix metric and inch-based equivalents. Reference information is shown in parentheses ().

2.0 Applicable Documents

The following documents of the issue in effect on the date of issuance of this specification, form a part of this specification to the extent specified herein. Subsequent issues of or amendments to these documents shall become part of this specification unless otherwise stated.

2.1 IPC¹

IPC-T-50 Terms and Definitions

IPC-L-108 Specification for Thin Laminates, Metal Clad, Primarily for High-Temperature Multilayer Printed Boards.

IPC-L-109 Specification for Glass Cloth, Resin Preimpregnated (B Stage) for High Temperature Multilayer Printed Boards.

IPC-L-112 Standard for Foil Clad, Polymeric, Composite Laminate

IPC-L-115 Specification for Thin Laminates for Extended High Temperature Multilayer Printed Board (Polyimide)

IPC-L-125 Specification for Plastic Sheet, Laminated, Metal-Clad for High Frequency Interconnections (Microwave) Printed Boards

IPC-L-130 Specification for Thin Laminates, Metal Clad Primarily for General-Purpose Multilayer Printed Boards.

IPC-CF-150 Copper Foil for Printed Wiring Applications

IPC-FC-233 Specification for Flexible Adhesive Bonding Films

IPC-D-300 Printed Wiring Board Dimensions and Tolerances.

1. Institute for Interconnecting and Packaging Electronic Circuits, 7380 N. Lincoln Avenue, Lincolnwood, Illinois 60466.



IPC-D-325 End Product Documentation for Printed Boards

IPC-A-600 Acceptability for Printed Wiring Boards.

IPC-TM-650 Test Method Manual²

2.1.1 Microsectioning

2.3.15 Purity Copper Foil

2.3.38 Inspection Test for Organic Contaminants on Printed Wiring Boards and Assembly Surfaces

2.3.39 Identification of Residual Organic Non-Ionic Contaminant(s) on Printed Wiring Board and Assembly Surfaces

2.4.1 Adhesion, Plating

2.4.21 Terminal Pull Strength, Rigid Printed Wiring

2.4.22 Bow and Twist, Rigid Printed Wiring Materials

2.4.36 Rework Simulation

2.5.7 Dielectric Withstand Voltage, Printed Wiring Material

2.5.16 Shorts, Internal Multilayer Printed Wiring

2.6.3 Moisture and Insulation Resistance, Rigid, Rigid-Flex and Flex Printed Wiring Boards

2.6.4 Outgassing, Multilayer Printed Wiring

2.6.6 Temperature Cycling, Printed Wiring Boards

2.6.7 Thermal Shock and Continuity, Flexible Printed Wiring

IPC-S-804 Solderability Test Methods for Printed Boards

IPC-SF-818 General Requirements for Electronic Soldering Fluxes

IPC-CC-830 Qualification and Performance of Electrical Insulating Compounds for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Soldermask) for Printed Boards

IPC-D-949 Design Standard for Rigid Multilayer Printed Boards

IPC-100043-3 Master Drawing: IPC Multilayer Qualification Specimen

2.2 Military³

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-T-10727 Tin Plating, Electrodeposited or Hot Oil Dipped, for Ferrous and Nonferrous Metals

MIL-P-13949 General Specification for Plastic Sheet, Laminated Metal Clad (for Printed Wiring)

MIL-C-14550 Copper Plating (Electrodeposited)

MIL-G-45204 Gold Plating, Electrodeposited

MIL-I-45208 Inspection System Requirements

MIL-P-55110 Printed Wiring Boards, General Specification for

MIL-P-81728 Plating, Tin-Lead (Electrodeposited)

2.3 Federal³

QQ-N-290 Nickel Plating

QQ-S-571 Solder, Lead Alloy, Tin Lead & Tin Alloy, Flux Cored Ribbon and Wire, and Solid Form

3.0 Requirements

3.1 General. Multilayer printed boards furnished under this specification shall meet or exceed all the requirements of the specific class of this specification for which the order was made. Design features and coupon configuration shall be per IPC-D-949. Boards which must meet other special requirements beyond those specified in Section 3 will be as specified by the procurement document.

Boards furnished under this specification shall be as specified by the master drawing. They shall be fabricated from panels that include sufficient coupons (plus spares) to facilitate the testing requirement of the class to which the boards were produced. Test coupons used to verify registration and plating integrity shall be arranged so that they are within 6-13 mm [0.25-0.50 inch] of the production board. Board apportionment to panels shall be such that coupons and location is representative of the board panel processing and that the location integrity of the coupons to board images shall be verified. Unless otherwise specified, the test coupons shall be identified by lot and/or by board serial number when the boards are serialized and shall be packaged with the appropriate board(s).

Boards furnished under this specification shall be processed in such a manner as to be uniform in quality and be free from defects in excess of those allowed in this specification.

3.1.1 Master Drawing. The master drawing shall be prepared in accordance with IPC-D-325 and shall establish the size and shape of the multilayer board, the size and location of all holes therein, and the shape or arrangement of both conductive and nonconductive patterns or elements. Any and all pattern features not controlled by the hole sizes and locations shall be dimensioned either specifically or by notes.

If this specification is referenced on the master drawing, any permanent exceptions or deviations required shall be documented thereon.

3.1.2 Production Master. The printed board manufacturer or user, if the user provides the master, shall be responsible for the accuracy of the production master. Verification of compatibility with the master drawing and patterns and the specific manufacturing facilities and processes used are the responsibility of the manufacturer.

2. For convenience, all IPC-TM-650 Test Methods referenced herein are reprinted at the end of this standard.

3. To obtain documents, write Naval Publications & Forms Center, 5801 Tabor Road, Philadelphia, PA 19120.



The manufacturer shall insure that the end product board meets the requirements of this specification. When specified on the procurement document or master drawing, the position of the appropriate test patterns on the production master shall not be changed.

3.2 Terms and Definitions Terms and definitions shall be in accordance with IPC-T-50 and as defined below. Terms with an asterisk (*) are direct excerpts from IPC-T-50, and are repeated here for convenience.

3.2.1 Multilayer Printed Boards.* The general term for completely processed printed circuit or printed wiring configurations consisting of alternate layers of conductive patterns and insulating materials bonded together, with conductive patterns in more than two layers and with the conductive patterns interconnected as required. The term includes both flexible and rigid multilayer boards.

3.2.2 Qualification Testing. Testing performed to demonstrate the vendor's ability to meet all of the requirements of the specification invoked by the user.

3.2.3 Quality Conformance Inspection. Inspection and tests intended to demonstrate that the product being manufactured meets or exceeds the requirements of the performance document invoked.

3.2.4 Production Board. Any printed board manufactured in accordance with master drawings, applicable specifications and procurement requirements.

***3.2.5 Test Coupon.** A portion of the quality conformance test circuitry used for a specific acceptance test or group of related tests.

3.3 Conflict. In the event of conflict, the following order of precedence shall apply:

1. Purchase Order and/or Contract
2. Master Drawing (See 3.1.1)
3. This Specification
4. Applicable Documents (See 2.0)

3.4 Vendor Qualification and Performance. When required, vendors of printed boards to this specification shall be qualified per paragraph 4.4 and as specified by the user, for the class of product represented by the qualification sample. Qualification to a class of this specification is considered evidence of qualification to any lower class(es), i.e., qualification to Class 3 is extended to cover Class 1 and Class 2. Qualification to MIL-P-55110 type 3 may be used as evidence of qualification to this specification for all classes. Qualification with one material to a specific class does not qualify the board manufacturer for other materials, except that those materials as indicated in MIL-P-13949 may be grouped as follows: GF qualification can cover types GE, GB, and GH; GR can cover GP; GY can cover GT and GX; GX can cover GT; but GI covers only that material.

The multilayer printed boards furnished under this specification shall as a minimum meet the requirements of paragraph 4.5 and the master drawing.

3.5 Materials. All materials used in construction of the printed boards shall comply with applicable specifications and the master drawing. The user has the responsibility to specify on the master drawing materials capable of meeting the requirements of this specification and end item use. When possible, material call-out information shall be reviewed with the vendor so as to obtain concurrence that the part will meet the requirements of this specification and if necessary, to update the master drawing accordingly.

If no materials are specified, then the vendor has the responsibility to meet the requirements of this specification. Agreement or approval by the user of vendor selected materials shall not be construed as a guarantee of acceptance of the finished end item.

3.5.1 Rigid Metal Clad Laminates. Rigid reinforced metal clad laminates shall be in accordance with Table 1 or as specified on the master drawing. The type and copper thickness shall be as specified on the master drawing. For Class 3, the minimum base material thickness shall be 0.05 mm [0.002 inch] per core thickness plus sufficient pre-preg and or adhesive to provide for a minimum dielectric layer thickness of 0.09 mm [0.0035 inch] separation between consecutive conductive layers to meet the necessary dielectric thickness requirements.

Table 1. Rigid Metal Clad Laminates

Material	Specification
Laminate as applicable	MIL-P-13949
High temperature laminate	IPC-L-108 IPC-L-115
Composite material	IPC-L-112
High frequency	IPC-L-125

3.5.2 Preimpregnated Bonding Material (Prepreg). Pre-impregnated bonding material (B-Stage) shall be specified on the master drawing and shall be in accordance with MIL-P-13949 and IPC-L-109. Prepreg shall be selected to be compatible with the rigid metal clad laminates.

3.5.3 Bonding Material. The material used to adhere external heat sinks or stiffeners to the printed board shall be in accordance with Table 2.

Table 2. Bonding Materials

Material	Specification
Prepreg as applicable	MIL-P-13949
High temperature prepreg	IPC-L-109
Flexible adhesive bonding film	IPC-FC-233
Other	As Specified

3.5.4 Copper Foil. Copper foil shall be in accordance with IPC-CF-150. Thickness and type of treatment shall be specified on the master drawing.

3.5.5 Metallic Platings and Coatings. The circuit finish shall be one or a combination of the following plating materials as specified on the master drawing. Thickness of platings/coatings shall be in accordance with 3.10.2.1.

3.5.5.1 Electroless Deposition. Electroless copper deposition shall be of sufficient quality for subsequent electrodeposition processes.

3.5.5.2 Copper. All electrodeposited copper plating shall be in accordance with MIL-C-14550 or as specified on the master drawing. For Class 3, when tested as specified in IPC-TM-650-2.3.15 the purity of deposited copper shall be no less than 99.5%.

3.5.5.3 Tin-Lead. Tin-lead plating shall be in accordance with MIL-P-81728 and shall be 50% to 70% tin, with the balance being lead. Thickness of tin-lead plating shall be as specified in paragraph 3.10.2.1 and shall be applicable prior to fusing. Fusing is required for Class 3 board. Fusing shall be specified on the master drawing as required for other classes.

3.5.5.4 Nickel. Low stress nickel plating shall be in accordance with QQ-N-290. Class and type shall be as specified on the master drawing.

3.5.5.5 Gold. Gold plating shall be in accordance with MIL-G-45204. Class and type shall be as specified on the master drawing. For Class 3 boards, gold plating shall be Type II, class 1.

3.5.5.6 Tin. Tin plating shall be in accordance with MIL-T-10727 Type I (electrodeposited) or Type II (hot dipped).

3.5.5.7 Solder Coating. Solder used to apply a solder coating shall be applied by hand or machine and shall conform to Type Sn60, Sn62, or Sn63 of QQ-S-571. Use of solder compositions other than those specified above shall be specified on the master drawing.

3.5.5.8 Other Finishes. Under certain conditions, other depositions may be used provided they are specified on the master drawing.

3.5.6 Protective Coatings

3.5.6.1 Polymer Coating (Solder Mask). When permanent solder mask coating is specified on the master drawing, it shall be a polymer coating conforming to IPC-SM-840. The specific class of solder mask per IPC-SM-840 shall match or exceed the class requirement of the product on which the solder mask is applied.

3.5.6.2 Electrical Insulating Compound. When electrical insulating compound (conformal coating) is specified on the master drawing, it shall conform to the requirements of IPC-CC-830. The specific class of conformal coating per IPC-CC-830 shall match the class requirement of the product on which the conformal coating is applied.

3.5.7 Fusing Fluids & Fluxes. Fusing fluids and fluxes used in solder application shall be in accordance with IPC-SF-818 and meet the requirements of paragraph 3.5.

3.5.8 Marking Inks. Marking inks used shall be permanent, non-nutrient and nonconductive polymer inks, shall meet the requirements of paragraph 3.5 and be specified on the master drawing. Marking inks may be applied to a board or to a label applied to the board. The label should be a polyimide film with acrylic pressure sensitive and must withstand fluxes, cleaning, solvents, soldering and coatings encountered in later manufacturing processes.

3.6 Design. The design and construction shall be in accordance with the master drawing, and the rigid-flex design specification IPC-D-949. Dimensions and tolerances used on multilayer printed boards shall be in accordance with IPC-D-300 except as otherwise specified.

3.6.1 Locating Holes. Tooling holes within the board periphery may be added by the manufacturer when permitted by the user. Such holes (usually used to control dimensional movement) shall be considered as cutouts and subject to the same spacing requirements as specified on the master drawing.

3.7 Visual Requirements. Class 1 boards when examined in accordance with 4.6.1 shall be of uniform quality and any defects shall not impact form, fit or function.

Class 2 and 3 boards when examined in accordance with 4.6.1 shall conform to the following paragraphs.

3.7.1 Edges. Burrs, nicks, or haloing along the edges of the board shall be acceptable provided the penetration does not reduce the edge spacing specified on the master drawing by more than 50%. If no requirement is specified on the master drawing, the penetration shall not exceed 2.5 mm [0.100 inch].

3.7.2 Laminate. Surface and subsurface imperfections are not desirable but are permitted provided they meet the requirements specified in Table 3.

3.7.3 Plated-Through Hole Voids. Boards shall have no voids in excess of that allowed by Table 4. There shall be no circumferential voids. For Class 2, the maximum size of any void shall not exceed 5% of the hole length in any direction, or 10% of the surface area of the barrel.

3.7.4 Marking. Unless otherwise specified, each individual board, each qualification board, each set of quality conformance test circuit strips (as opposed to each individual coupon), shall be marked in accordance with the master drawing.

Table 3. Laminate Visual Requirements

Class 1		
Uniform quality Defects that do not impact form, fit or function can be allowed. Must meet drawing for all attributes. (Specific notes or references to requirements shown in Class 2 or 3 may be used.)	Uniform quality Defects only as allowed by specification. Must meet drawing for all attributes. Edges may allow burrs, nicks, and haloing provided the penetration does not reduce the edge spacing more than 50 percent of the edge spacing specified or shown on the master drawing. If not specified it shall not exceed 2.5 mm [0.100 inch]. Measling and crazing acceptability limits shall be per IPC-A-600. Foreign inclusions shall be allowed when they are clear or translucent, or: are located at least 0.25 mm [0.010 inch] from the nearest conductor; if located between conductors and there is more than 50 percent of the space remaining; the longest dimension is no greater than 0.8 mm [0.032 inch] in non-circuitry areas; and there are no more than two inclusions per side of the circuit board. Surface imperfections (such as haloing, scratches, pits, dents, etc.) shall be acceptable providing the imperfection meet the following: - The laminate fiber may be cut, disturbed, or exposed if it meets b. and d. below and does not exceed 0.5 mm [0.002 inch] in depth. - The imperfection does not bridge between conductors. - Weave texture is not a defect and may bridge conductors. - The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimums. Laminate surface microvoids shall be allowed if their longest dimension does not exceed 0.8 mm [0.032 inch], they do not bridge conductors, they do not occur more than 10 per 645 sq. mm [1 sq. inch], their total area does not exceed 5% of each side of the board and the finished printed wiring board is conformally coated or solder masked over the microvoids. Subsurface imperfections (laminates). When examined in accordance with 4.6.1, subsurface imperfections (such as haloing, etc.) shall be acceptable providing the imperfections meet the following: - Imperfection is nonconductive. - Does not bridge more than 25% of the distance between conductors or plated-through holes and no more than 1% of the board area on each side shall be affected. - At least the specified minimum spacing from the nearest conductor. - Does not propagate as a result of testing (such as bond strength, rework simulation, thermal stress, or thermal shock). Subsurface spots shall be permitted when they are clear or translucent; known to be weave texture other than delamination, disbonding, or measling; isolated white spots which are at least 0.25 mm [0.010 inch] from the nearest conductor; white spots which do not propagate as a result of any soldering operation; (gelation particles are acceptable regardless of location); isolated opaque spots which are at least 0.25 mm [0.010 inch] from the nearest conductor.	Uniform quality Defects only as allowed by specification. Must meet drawing for all attributes. Edges may allow burrs, nicks, and haloing provided the penetration does not reduce the edge spacing more than 50 percent of the edge spacing specified or shown on the master drawing. If not specified it shall not exceed 2.5 mm [0.100 inch]. Measling and crazing acceptability limits shall be per IPC-A-600. Foreign inclusions shall be allowed when they are clear or translucent, or: are located at least 0.25 mm [0.010 inch] from the nearest conductor; if located between conductors and there is more than 50 percent of the space remaining; the longest dimension is no greater than 0.8 mm [0.032 inch] in non-circuitry areas; and there are no more than two inclusions per side of the circuit board. Surface imperfections (such as haloing, scratches, pits, dents, etc.) shall be acceptable providing the imperfection meet the following: - The laminate fiber shall not be cut, disturbed, or exposed. - The imperfection does not bridge between conductors. - Weave texture is not a defect and may bridge conductors. - The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimums. Laminate surface microvoids shall be allowed if their longest dimension does not exceed 0.8 mm [0.032 inch], they do not bridge conductors, they do not occur more than 10 per 645 sq. mm [1 sq. inch], their total area does not exceed 1% of each side of the board and the finished printed wiring board is conformally coated or solder masked over the microvoids. Subsurface imperfections (laminates). When examined in accordance with 4.6.1, subsurface imperfections (such as haloing, etc.) shall be acceptable providing the imperfections meet the following: - Imperfection is nonconductive. - Does not bridge more than 25% of the distance between conductors or plated-through holes and no more than 1% of the board area on each side shall be affected. - At least the specified minimum spacing from the nearest conductor. - Does not propagate as a result of testing (such as bond strength, rework simulation, thermal stress, or thermal shock). Subsurface spots shall be permitted when they are clear or translucent; known to be weave texture other than delamination, disbonding, or measling; isolated white spots which are at least 0.25 mm [0.010 inch] from the nearest conductor; white spots which do not propagate as a result of any soldering operation; (gelation particles are acceptable regardless of location); isolated opaque spots which are at least 0.25 mm [0.010 inch] from the nearest conductor.

ing, with the date and manufacturer's code. The marking shall be produced by the same process as used in producing the conductive pattern, or by use of a non-conductive permanent fungistatic ink or paint (see paragraph 3.5.8), or by electrical pencil marking on a metallic area provided for marking purposes. Conductive marking shall not reduce the spacing requirements. All markings shall be compatible with materials and parts legible for all tests, and in no case effect board performance.

Table 4. Plating Voids-Visual Examination

Class 1	Class 2	Class 3
Maintain electrical function	Three voids allowed per hole in no more than 5% of the total number of holes	None

3.7.5 Solderability. After conditioning in accordance with 4.6.1.1, the surface shall exhibit proper wetting, and shall meet the requirements of Table 5. There shall be no separation or other forms of degradation of the conductive pattern. Hole solderability shall exhibit proper wetting of the wall of the plated-through hole and associated land.

3.7.6 Workmanship. Printed boards shall be processed in such a manner as to be uniform in quality and show no evidence of dirt, foreign matter, oil, fingerprints, flux residue,

extraneous copper, and other contaminants that effect life or serviceability. Printed boards shall be free of defects in excess of those allowed in this specification. There shall be no evidence of any lifting or separating of platings from the surface of the conductive pattern, or of the conductor from the base laminate in excess of that allowed. There shall be no slivers of solder or plating on the surface of the printed board.

3.8 Dimensional Requirements. Finished printed boards shall be examined in accordance with paragraph 4.6.2 and shall meet the dimensional requirements specified on the master drawing and shall conform to the following paragraphs.

3.8.1 Hole Pattern Accuracy. The accuracy of the hole pattern on the printed board shall be as specified on the master drawing.

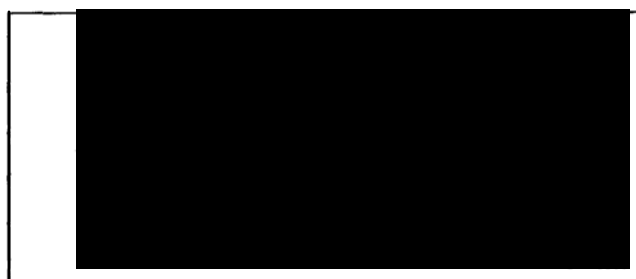


Figure 1. Breakout of 90° and 20% conductor width reduction.

Table 5. Solder Coverage By Class

Class 1		Class 2		Class 3	
Surface (Visual)	Hole (Microsection)	Surface (Visual)	Hole (Microsection)	Surface (Visual)	Hole (Microsection)
Any lack of solder shall not affect form, fit or function.	All holes show evidence of wetting.	80%	All holes show evidence of wetting.	95%	All holes show evidence of wetting.

Table 6. Minimum External Annular Rings

Characteristic	Class 1	Class 2	Class 3
Plated-through holes	Breakout of hole from land is allowed provided form, fit or function are not affected.	90° breakout of hole from land is allowed provided the land conductor junction is not reduced more than 20% of the minimum conductor width specified on the engineering drawing (see Figure 1) or the production master nominal. The conductor junction should never be less than 0.05 mm [0.002 in.].	Unless otherwise specified on the master drawing, the minimum annular ring shall not be less than 0.05 mm [0.002 in.] except at the conductor which shall not be less than 0.13 mm [0.005 in.]. The minimum external annular ring may have 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas is acceptable.
Unsupported holes	No breakout at conductor junction.	No breakout allowed.	Unless otherwise specified on the master drawing, the minimum annular ring shall not be less than 0.38 mm [0.015 in.]. The minimum external annular ring may have a 20% reduction of the minimum annular ring in isolated areas due to defects such as pits, dents, nicks, pinholes or splay in the annular ring of isolated areas is acceptable.

3.8.2 Front to Back Registration. When evaluated in accordance with 4.6.2.1, registration must not allow violation of annular ring requirements as defined in 3.8.3, nor the tolerance relationship of the edge card contacts, as specified on the master drawing.

3.8.2.1 Internal Layer to Layer Registration (Nondestructive). Special registration test coupons may be designed into the board or panel in accordance with IPC-D-949, or they may be added to the panel by the vendor to enhance testability. To be usable for acceptance purposes, special registration coupons must relate the actual grid location of each circuit layer to all other layers and to the hole pattern accuracy attained (see paragraph 3.8.1) in each printed board. When examined in accordance with paragraph 4.6.2.2, internal layer registration shall meet the requirements of Tables 18, 19 and 20.

3.8.2.2 Internal Layer to Layer Registration (Destructive). When no special registration coupons are incorporated, internal layer to layer registration shall be examined during construction integrity examinations (see paragraph 3.10).

3.8.3 Annular Ring (External). When examined in accordance with paragraph 4.6.2.3, the minimum external annular ring shall meet the requirements of Table 6.

3.8.3.1 Solder Mask on Land. Solder mask misregistration is permitted, however, it shall leave a minimum solderable annular ring for a supported hole of 0.13 mm [0.005 inch] for at least 360° for Class 3, and 270° for Class 1 and 2. For an unsupported hole the minimum solderable annular ring shall be 0.25 mm [0.010 inch] for at least 360° for Class 3, and 270° for Class 1 and 2.

3.8.4 Conductor Width. Minimum allowable end product conductor width shall be as defined on the master drawing. Reductions in conductor width or thickness shall be in accordance with the requirements of Table 7, or as specified on the master drawing.

3.8.5 Conductor Spacing. Unless otherwise specified on the master drawing the minimum spacing between conductors, or conductors to lands shall not be less than 0.13 mm [0.005 inch]; for internal conductors 0.10 mm [0.004 inch]. Minimum spacing between conductor and the edge of board shall be specified on the master drawing and be in accordance with IPC-D-949. Random extraneous copper spurs are allowed provided they do not reduce conductor spacing more than specified in Table 8.

3.8.6 Bow and Twist. When examined in accordance with paragraph 4.6.2.4 the entire portion of the specimen or production board shall meet the requirements of Table 9, or as specified on the master drawing. For automated assembly and surface mounting operations, more stringent requirements may be necessary.

Table 9. Bow and Twist Maximums

Class 1	Class 2	Class 3
2%	1.5%	1.0%

3.8.6.1 Edge Board Contact Bow (Rigid Section Only). When printed edge board contacts are specified on the printed boards, the maximum allowable bow in the connector area shall meet the requirements of Table 10 when evaluated in accordance with paragraph 4.6.2.4. For automated assembly and surface mounting operations, more stringent requirements may be necessary.

Table 10. Board Contact Bow Maximums

Class 1	Class 2	Class 3
2%	1.5%	1%

3.8.7 Edge Board Contact—Junction of Gold Plate to Solder Finish or Solder Mask. Exposed copper/plating overlap between the solder finish and gold plate or solder mask and gold plating shall meet the requirements of Table 11. Where exposed copper/plating is allowed, discoloration in the "Permissible Zone" is permitted.

Table 11. Gap Allowed Between Gold Plating and Solder or Solder Mask

Class 1	Class 2	Class 3
+ 0.020 + (0.50)	+ 0.005 + (0.13)	+ 0.000 to -0.005 + (0.00) to -(0.13)

Note: Positive values indicate maximum exposed copper/plating gap permitted. Negative values indicate minimum overlap of the gold by the solder mask or lack of exposed copper/plating.

Table 7. Allowed Conductor Width Reductions

Class 1	Class 2	Class 3
Local reductions may be allowed based upon agreement between user and vendor.	Any combination of edge roughness, nicks, pinholes and scratches exposing base material shall not reduce the conductor width by more than 30% of the value specified on the master drawing. There shall be no occurrence greater than 25 mm [1 inch].	Any combination of edge roughness, nicks, pinholes and scratches exposing base material shall not reduce the conductor width by more than 20% of the value specified on the master drawing. There shall be no occurrence greater than 13 mm [0.5 inch].

Table 8. Conductor Spacing Reduction

Class 1	Class 2	Class 3
A 30% reduction in minimum conductor spacing is allowable in isolated areas due to conductor material edge roughness, copper spikes, etc.	A 30% reduction in minimum conductor spacing is allowable in isolated areas due to conductor material edge roughness, copper spikes, etc.	Spacing dimensions no less than 80% of the nominal spacing shown on the master drawing shall apply between: (a) any two conductors, (b) a conductor and any metallic item including electrically conductive designations, (c) a conductor or metallic item and the edge of a hole, and (d) a conductor and the edge of the part.



3.8.8 Other Dimensional Requirements. Other dimensional requirements are evaluated during construction integrity evaluations performed in paragraph 3.10. These include:

Plating and coating thickness	3.10.2.1
Internal conductor thickness	3.10.2.2
Conductor edge outgrowth	3.10.2.3
Conductor undercut	3.10.2.4
Internal layer registration	3.10.2.5
Minimum internal annular ring	3.10.2.6
Minimum internal lateral spacing	3.10.2.7
Minimum dielectric spacing	3.10.2.8
Solder mask thickness	3.10.2.9

3.9 Physical Requirements. Multilayer printed boards shall meet the physical requirements specified in the following paragraphs.

3.9.1 Plating Adhesion. When tested in accordance with paragraph 4.6.3.1 there shall be no evidence of any portion of the protective plating or the conductor pattern foil being removed, as shown by particles of the plating or pattern foil adhering to the tape. If overhanging metal breaks off (slivers) and adheres to the tape, it is evidence of overhang, or slivers, but not of plating adhesion failure.

3.9.2 Solder Mask Cure and Adhesion. When evaluated in accordance with 4.6.3.2, the cured solder mask coating shall not exhibit tackiness, blistering or delamination. The maximum percentage of cured solder mask lifting from the surface of the base material or conductors of the printed board shall be in accordance with Table 12.

3.10 Construction Integrity. Multilayer printed boards shall meet construction integrity requirements specified in the following paragraphs.

Table 12. Solder Mask Adhesion

Material	Maximum Percentage of Lifting		
	Class 1	Class 2	Class 3
Bare copper	10	5	0
Gold or Nickel	25	10	5
Tin-lead plating	25	10	10
Reflowed tin-lead	50	50	10
Base laminate	10	5	0

lowing paragraphs. Construction integrity shall be evaluated through microsectioning techniques on a standard test specimen in accordance with paragraph 4.6.4. Specimens shall be inspected in accordance with 4.6.4.1. Dimensional requirements only possible through the use in microsectioning techniques (see paragraph 3.8.8) are also defined in this section.

3.10.1 Plated-Through Hole Integrity Prior to Stress. When evaluated in microsection in accordance with paragraph 4.6.4, finished printed boards, supporting coupons, and qualification test specimens shall meet the requirements of paragraphs 3.10.1.1 through 3.10.1.4.

3.10.1.1 Plating Integrity (as produced). Plating integrity shall meet the requirements detailed in Table 13. In addition, there shall be no plating cracks or interplane separation.

3.10.1.2 Laminate Integrity. Laminate integrity requirements for the as produced plated-through hole shall be in accordance with Table 14. In addition, there shall be no delamination or voids in excess of 0.75 mm [0.003 inch] for Class 3 products. Laminate voids or delamination allowed on Class 1 and 2 products shall be as agreed to between user and vendor.

Table 13. Plating Through Hole Integrity Prior to Stress

Property	Class 1	Class 2	Class 3
Plating voids	Maintain electrical function.	Not to exist on both sides of hole in same plane. Not to extend full length of hole.	None allowed. ¹
Plating folds/inclusions	Must be enclosed and accumulated thickness meets minimum thickness.	Must be enclosed and accumulated thickness meets minimum thickness.	Must be enclosed and accumulated thickness meets minimum thickness.
Burrs and nodules	Allowed if part lead can be inserted.	Allowed if minimum hole diameter met.	Allowed if minimum hole diameter met.
Glass fiber protrusion	Allowed if part lead can be inserted.	Allowed if minimum hole diameter met.	Allowed if minimum hole diameter met.
Wicking	0.125 mm (0.005 in.) and maintain electrical function.	0.10 mm (0.004 in.) maximum.	0.08 mm (0.003 in.) maximum.
Nail-heading	As long as does not affect form, fit or function.	1½ x internal conductor thickness.	1½ x internal conductor thickness.

1. If any are found, 100% of lot shall be visually inspected per 3.7.3.

Table 14. Laminate Integrity

Property	Class 1	Class 2	Class 3
Resin recession	As agreed upon between manufacturer and user.	As agreed upon between manufacturer and user.	40% of the hole wall prior to thermal testing—not evaluated after thermal testing.

3.10.1.3 Etchback or Smear Removal. When specified on the master drawing, printed boards shall be etched back for the lateral removal of resin and/or glass fibers from the internal holes prior to plating. The etchback shall be between 0.005 mm [0.0002 inch] to 0.08 mm [0.003 inch] with a preferred depth of 0.01 mm [0.0005 inch]. Wicking may extend an additional 0.08 mm [0.003 inch] provided it has no detrimental effect on the function of the printed board. Shadowing is permitted on one side of each land. When no etchback is specified on the drawing and the board fabricator elects to use etchback, the vendor shall verify with the user, that etchback can be accomplished without degrading end item use. Smear removal shall not etchback greater than 0.03 mm [0.001 inch].

3.10.1.4 Negative Etchback. Negative etchback is not desirable, however if present shall not exceed the limitations detailed in Table 15.

Table 15. Negative Etchback

Class 1	Class 2	Class 3
0.08 mm [0.003 in.] max	0.04 mm [0.0015 in.] max	Allowed up to 0.013 mm [0.0005 inch] provided etchback is not specified on the master drawing.

3.10.1.5 Lifted Lands (prior to stress testing). There shall be no lifted lands in the "as received" microsection specimen. "As received" meaning after fusing, but prior to thermal stress testing or rework simulation. (See paragraph 3.11.)

3.10.2 Additional Dimensional Evaluations. When evaluated in microsection in accordance with paragraph 4.6.4 and inspected in accordance with 4.6.4.1, finished printed boards, supporting coupons and qualification test specimens shall meet the additional dimensional requirements detailed in the following paragraphs.

3.10.2.1 Plating/Coating Thickness. Plating/coating thicknesses, when evaluated in accordance with 4.6.4.2 or suitable electronic measuring equipment, shall meet the requirement of Table 16 or as specified on the master drawing. Tin-lead plating thickness measurements shall be made prior to fusing. After tin-lead plating is fused, no measurement of plating thickness is required, but solderability testing in accordance with IPC-S-804 and visual inspection of copper coverage shall be performed. Tin-lead coverage does not apply to vertical conductor edges. Nodules or rough plating shall not reduce the hole diameter below its minimum limits as defined on the master drawing. Solder coating shall meet solderability requirements.

3.10.2.2 Minimum Inner Layer Conductor Thickness. The minimum inner layer conductor thickness after processing shall be in accordance with Table 17.

**Table 16. Minimum Surface*
Plating/Coating Thickness Requirements**

Plating	Class 1	Class 2	Class 3
Gold	0.00075 mm [0.00003]	0.00075 mm [0.00003]	0.0012 mm [0.00005]
Nickel	0.0025 mm [0.0001]	0.005 mm [0.0002]	0.005 mm [0.0002]
Copper*	0.012 mm [0.0005]	0.025 mm [0.0010]	0.025 mm [0.0010]
Tin	0.00075 mm [0.00003]	0.0012 mm [0.00005]	0.0025 mm [0.0001]
Tin-Lead	0.0025 mm [0.0001]	0.005 mm [0.0002]	0.0075 mm [0.0003]
Solder†	Coverage	0.005 mm [0.0002]	0.0075 mm [0.0003]

*Plating thickness applies to surface and in the hole for copper.

†Measured at the crest.

**Table 17. Minimum Inner Layer Conductor Thickness
After Processing**

Copper Thickness	Class 1	Class 2	Class 3
0.5 oz. cu.	0.012 mm [0.0005]	0.012 mm [0.0005]	— ¹
1.0 oz. cu.	0.025 mm [0.0010]	0.025 mm [0.0010]	0.025 mm [0.0010]
2.0 oz. cu.	0.058 mm [0.0023]	0.058 mm [0.0023]	0.058 mm [0.0023]

1. 0.5 oz. copper is not allowed on Class 3 boards unless it is over plated to 0.025 mm [0.0010] final thickness.

3.10.2.3 Conductor Edge Outgrowth. There shall be no outgrowth on the conductor edges plated with tin-lead, and fused or solder coated. The maximum permissible outgrowth on conductors plated with other than the above metal shall be 0.025 mm [0.001 inch]. (See Figure 2.)

3.10.2.4 Undercutting. Undercutting at each edge of the conductor shall not exceed 1 times the total thickness for Class 2 and 3 and 1½ times the total thickness for Class 1 of the copper foil and plated copper or 10% of the conductor width, whichever is smaller, as shown in Figure 2. For fine line circuitry a percentage of undercut shall be agreed upon between supplier and user.

3.10.2.5 Layer to Layer Registration (destructive). Microsection of plated-through holes shall be used to determine layer to layer registration if nondestructive methods were not used. Registration shall meet the requirements of Tables 18, 19 and 20 and Figure 4 when examined in accordance with the requirements of paragraph 4.6.4.3. Class 1 shall meet form, fit and function.

3.10.2.6 Annular Ring (Internal). The minimum annular ring for functional internal lands shall be in accordance with Table 18 and Figure 3.

3.10.2.7 Thermal Plane. The minimum lateral spacing between adjacent conductive surfaces, non functional lands and/or plated-through holes, and the thermal plane, shall be the minimum specified in Table 19.

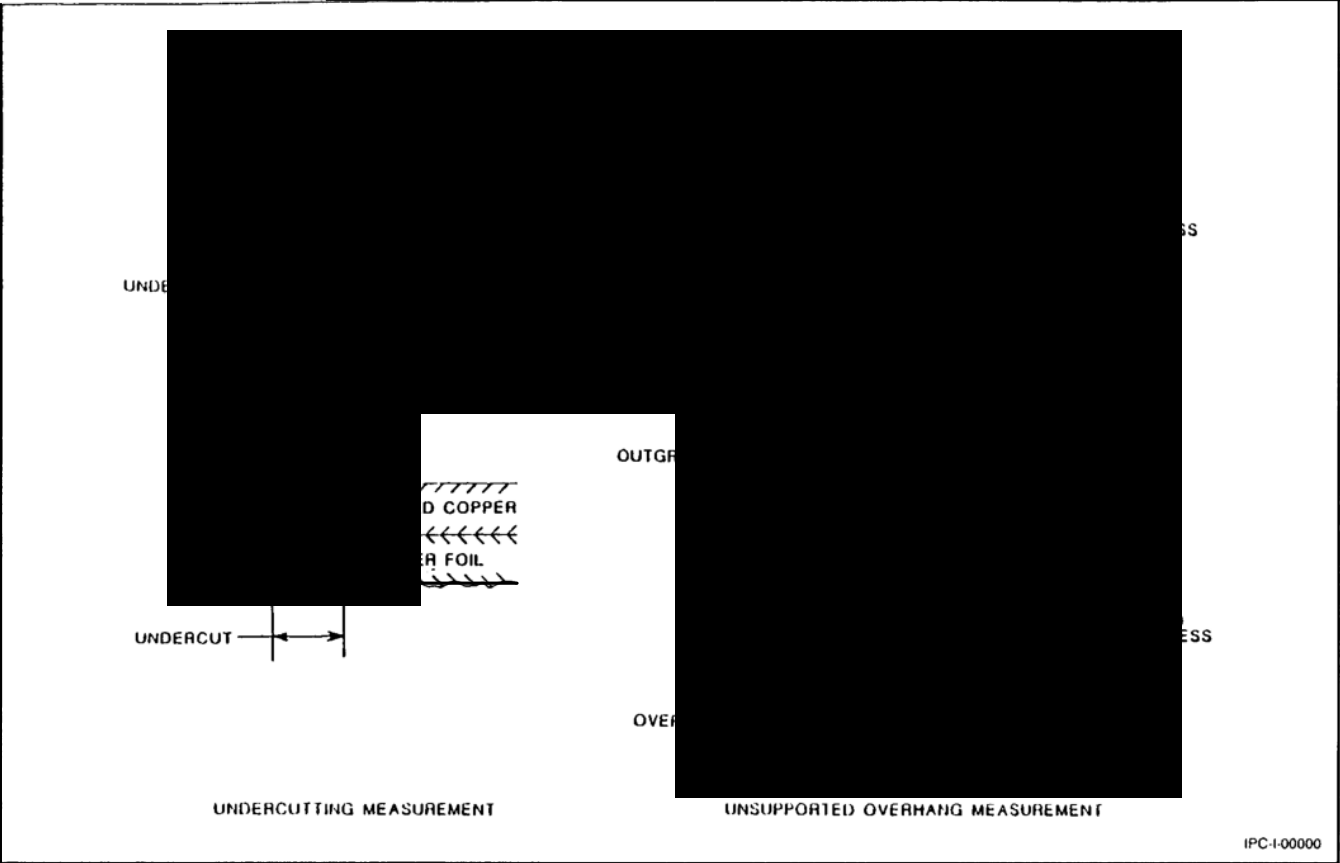


Figure 2. Undercut and outgrowth.

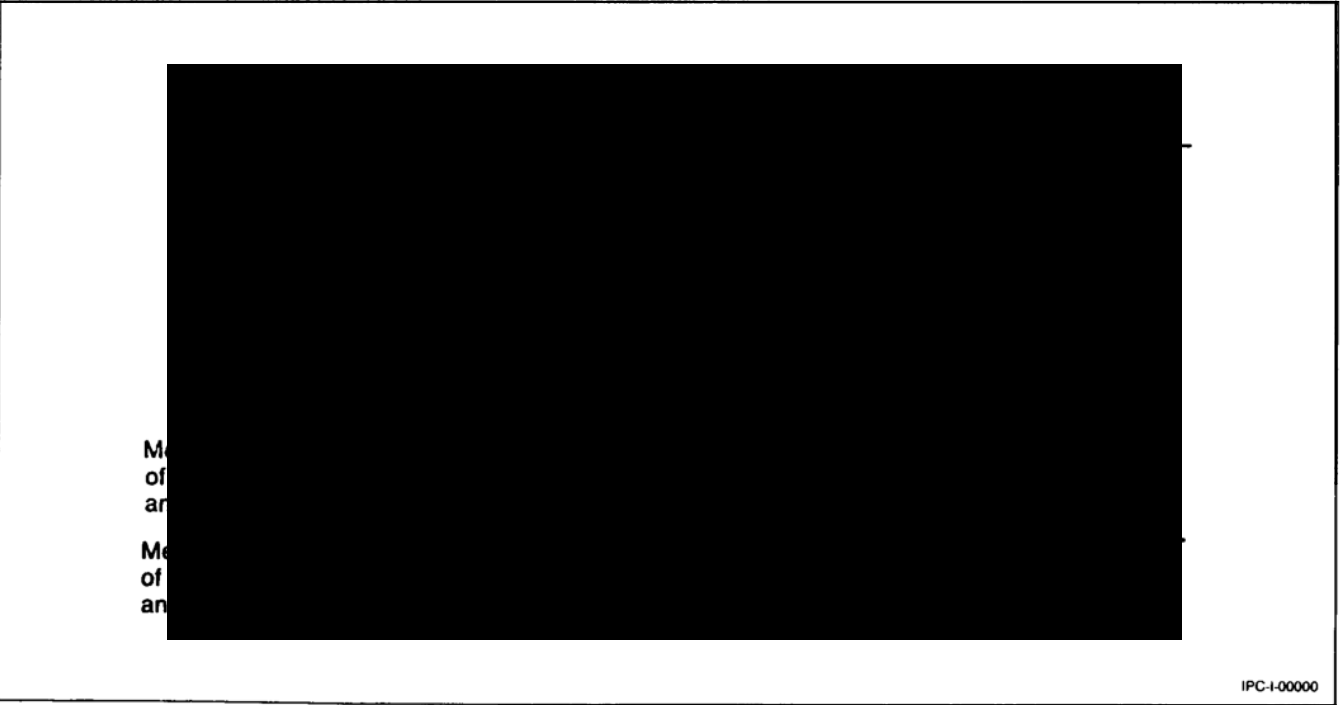


Figure 3. Layer to layer registration and annular ring measurement.

Table 18. Minimum Annular Ring Internal

Class 1	Class 2	Class 3
Breakout allowed per Figure 5.	Hole to pad tangency	0.05 mm [0.002 in.]

Table 19. Minimum Lateral Spacing to Thermal Planes

Class 1	Class 2	Class 3
0.05 mm [0.002 in.]	0.08 mm [0.003 in.]	0.1 mm [0.004 in.]

Table 20. Dielectric Spacing

Property	Class 1	Class 2	Class 3
Dielectric separation (minimum rigid area)	0.05 mm [0.002 in.]	0.076 mm [0.003 in.]	0.09 mm [0.0035 in.]

3.10.2.8 Dielectric Spacing. The minimum dielectric spacing shall be as detailed on the master drawing or Table 20.

3.10.2.9 Solder Mask Thickness. Solder mask thickness shall be in accordance with the master drawing. See IPC-SM-840.

3.11 Plated-Through Holes After Stress. Supporting coupons of finished printed boards and qualification test specimens shall be stressed in accordance with 4.6.5 and meet the requirements of the following paragraphs.

3.11.1 Thermal Stress (Solder Float). Prior to thermal stress testing, specimens require special conditioning (see paragraph 4.6.5.1). Specimens shall be thermal stressed in accordance with paragraph 4.6.5.1. Following stress, specimens shall be microsectioned in accordance with 4.6.4, inspected in accordance with 4.6.4.1 and shall meet the requirements of Table 21 and Figure 4.

Laminate voids greater than 0.08 mm [0.003 inch] outside the thermal zone A (see Figure 4) shall be cause for rejection for Class 2 and Class 3.

3.11.2 Rework Simulation. Printed boards or test coupons shall be stressed in accordance with paragraph 4.6.5.2. Fol-

lowing stress, specimens shall be microsectioned in accordance with 4.6.4, inspected in accordance with 4.6.4.1 and shall meet the requirements of Table 21, Figure 4 and 3.11.3.

3.11.3 Lifted Lands (After Stress Testing). When printed board test specimens (which have been subjected to thermal stress or rework simulation) are evaluated in accordance with paragraph 4.6.4 and 4.6.4.1, the maximum allowance of lifted lands from the base material to the outer lower edge of the land shall be 0.08 mm [0.003 inch] on both sides of the hole. There shall be a minimum of 50% of the land bonded on each side of the hole (see Figure 6). Increase in board thickness may affect land lifting.

3.12 Electrical Requirements. Printed boards shall meet the electrical requirements specified in the following paragraphs when tested in accordance with the test methods defined in paragraph 4.6.6.

3.12.1 Dielectric Withstand Voltage. When printed boards are evaluated in accordance with paragraph 4.6.6.1 they shall meet the requirements of Table 22, without flashover, sparkover or breakdown between conductor to conductor or conductor to lands.

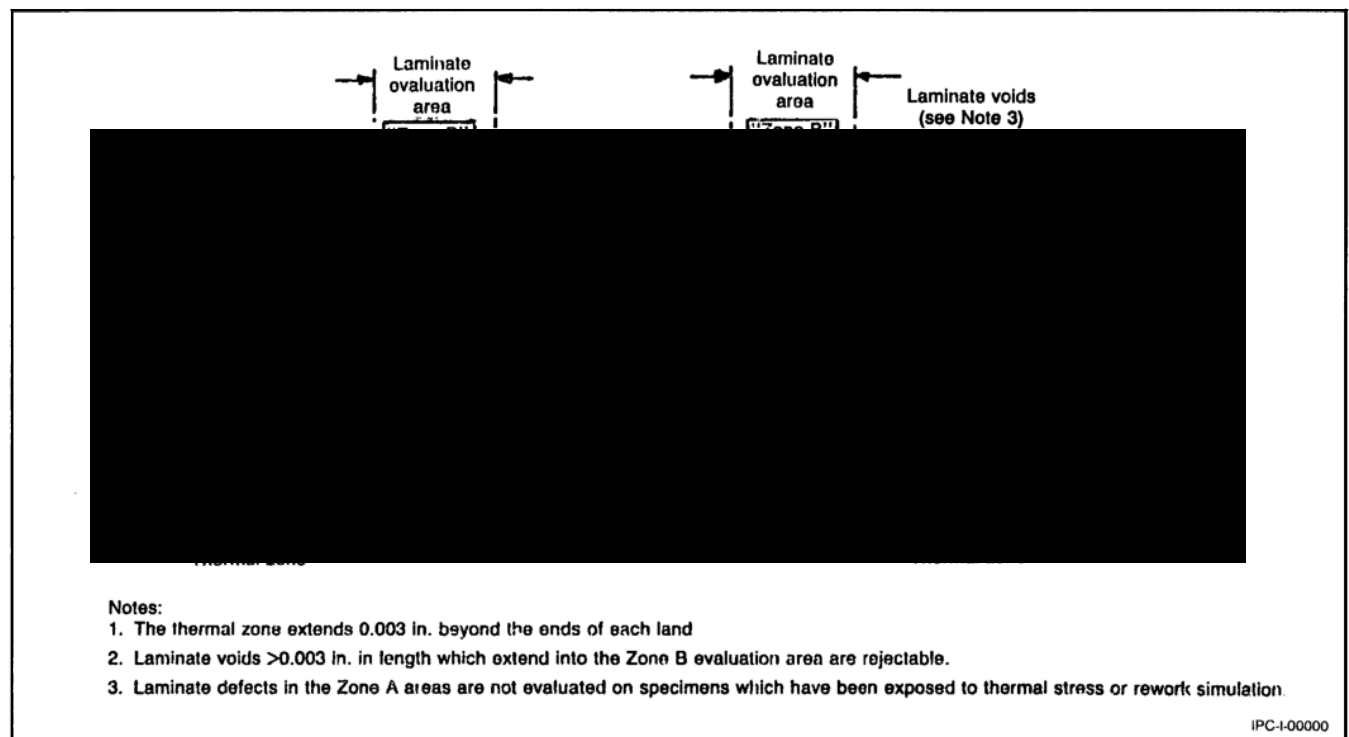


Figure 4. Typical microsection evaluation specimen (three plated-through holes).

Table 21. Plating Through Hole Integrity After Stress

Property	Class 1	Class 2	Class 3
Interplane separation (separation between internal lands and through hole plating)	Allowed on only one side of hole wall at each land location.	None allowed.	None allowed.
Inner foil cracks ¹	Allowed on only one side of hole provided it does not extend through foil thickness.	Allowed on only one side of hole provided it does not extend through land thickness.	None allowed.
External foil cracks ¹	Allowed provided it does not extend through plating—"A" and "B" cracks allowed.	Allowed provided it does not extend through plating—"A" and "B" cracks allowed.	"A" cracks allowed only.
Barrel cracks ¹	Allowed provided it does not extend through plating.	Allowed provided it does not extend through plating.	None allowed.
Hole wall pullaway	Acceptable provided dimensional and plating requirements are met. No interplane separations allowed.	Acceptable provided dimensional and plating requirements are met. No interplane separations allowed.	Acceptable provided dimensional and plating requirements are met. No interplane separations allowed.
Lifted lands after thermal stress or rework simulation.	As agreed to by user and vendor.	0.12 mm [0.005 in.]	0.08 mm [0.003 in.]
Plating voids	Maintain electrical function. No circumferential boards.	None allowed. If any are found, lot must be 100% inspected per 3.7.3.	None allowed. If any are found, lot must be 100% inspected per 3.7.3.

1. Copper Crack Definition: see Figure 5

"A" crack = A crack in the external foil.

"B" crack = A crack that does not completely break plating (minimum plating remains).

"C" crack = A crack in the internal foil.

"D" crack = A corner crack—complete break in foil and plating.

"E" crack = A barrel crack in plating only.

"F" crack = A corner crack in the plating only.

IN PLATING ONLY

IN PLATING ONLY

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Figure 5. Crack definition.

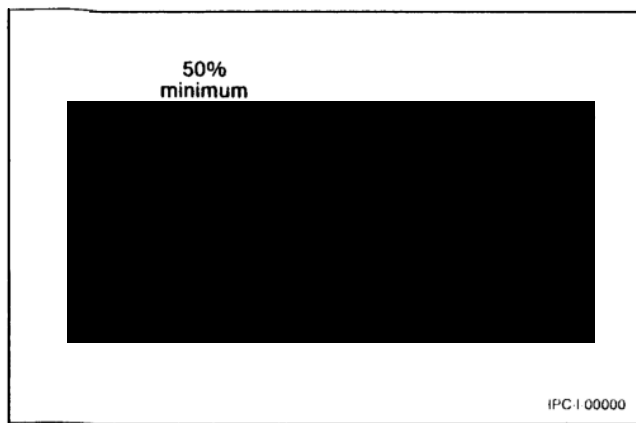


Figure 6. Lifted land.

Table 22. Dielectric Withstanding Test Voltages

	Class 1	Class 2	Class 3
Voltage	No requirement	500 Vdc	1000 Vdc
Time	—	30 sec	30 sec

3.12.2 Circuitry

3.12.2.1 Circuitry Continuity (Qualification). When printed boards are tested in accordance with paragraph 4.6.6.2 there shall be no open circuits whose resistance exceeds 0.5 ohms.

3.12.2.2 Circuit Continuity (Production). When printed boards are tested in accordance with paragraph 4.6.6.3 there shall be no open circuits whose resistance exceeds 5 ohms.

3.12.2.3 Circuit Shorts. When printed boards are tested in accordance with paragraph 4.6.6.4 the resistance between mutually isolated conductors shall be greater than: for class 1, 2 megohms; for class 2, 15 megohms, and for class 3, 100 megohms.

3.12.3 Circuit/Plated-Through Shorts to Metal Substrate. When printed boards with metal core substrates or test specimens are tested in accordance with paragraph 4.6.6.5, the board shall be capable of withstanding 500 volts (DC) between circuitry/plated-through holes and the metal core substrates. There shall be no flashover or dielectric breakdown.

3.12.4 Insulation Resistance. When printed boards or specimens are tested in accordance with paragraph 4.6.6.6, the insulation resistance shall be no less than that shown in Table 23.

Table 23. Insulation Resistance

	Class 1	Class 2	Class 3
As received.	Maintain electrical function.	500 megohms	500 megohms
After exposure to moisture.	Maintain electrical function.	100 megohms	500 megohms

3.12.4.1 Additional Insulation Resistance Requirements. Additional insulation resistance requirements are detailed after environmental exposure to moisture (see paragraph 3.13.1).

3.13 Environmental. Boards shall meet the environmental requirements specified in the following paragraphs when tested in accordance with the test methods specified in paragraph 4.6.7.

3.13.1 Moisture. When test coupons are stressed and evaluated in accordance with paragraph 4.6.7.1 the specimen shall not exhibit blistering, measing or delamination in excess of that shown in Table 3; or bow in excess of that allowed in 3.8.6.

When tested for insulation resistance in accordance with 4.6.7.1, the coupon shall meet the minimum requirements shown in Table 23 (at 500 volts DC).

When printed boards incorporate a coated metal core substrate, the insulation material used for hole fill dielectric shall provide an insulation resistance between the thermal plane (metal core substrate) and insulated plated-through holes greater than 100 megohms.

3.13.2 Outgassing. When specified, the printed board shall be free of materials, such as trapped plating solutions and uncured adhesive layers known to cause contamination. When tested in accordance with 4.6.7.2, the degree of outgassing shall not result in a weight loss of more than 0.1%.

3.13.3 Thermal Shock. When required, specimens shall be thermal shock tested in accordance with 4.6.7.3 using laminate operation as specified in IPC-D-949. The specimen shall meet the circuitry requirements of 3.12.2.2. In addition, for Class 3, a resistance measurement shall be made at the high temperature of the first and 100th cycle. A change of 10% or more shall be considered a reject.

3.13.4 Cleanliness. When tested in accordance with 4.6.7.4 and 4.6.7.5 and evaluated in accordance with 3.13.4.1 and 3.13.4.2. Printed boards shall be within the allowable limits of ionic and other contaminants. When a printed board requires a permanent solder mask coating, the uncoated boards shall be within the allowable limits of ionic and other contaminants prior to the application of solder mask coating.

3.13.4.1 Ionic (resistivity of solvent extract). When non-coated printed boards are tested in accordance with 4.6.7.4 the resistivity shall be not less than 2×10^6 ohm-cm. Equivalent test methods may be used in lieu of the method specified in 4.6.7.4, however, it shall be determined that the alternate method is demonstrated to have equal or better sensitivity and employ solvents with the ability to dissolve flux residue or other contaminants as does the alcohol-water solution specified in 4.6.7.4.