



ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES

IPC-SM-780

Component Packaging and Interconnecting with Emphasis on Surface Mounting

ANSI/IPC-SM-780

July 1988

A guideline developed by IPC

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Developed by the Technical Committees of IPC

APPROVED MARCH 31, 1988 BY



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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Advanced Packaging Guidelines Subcommittee of the IPC Advanced Packaging Committee are shown below, it is not possible to include all of those who assisted in the evolution of this Guidelines. To each of them, the members of the IPC extend their gratitude.

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A special note of thanks to the key members of the working group that met several times during the development of this standard and prepared the material reviewed by the committee and the IPC membership: Steven Kandybowski, *Amp, Inc.*; Colin MacKay, *Microelectronics & Computer*; Werner Engelmaier, *AT&T Bell Laboratories*; Harvey Walters-dorf, *Thomas & Betts*; Gerry Ginsberg, *Component Data Associates*; Jerry Holly, *Tektronix*; Terry Kingston, *Texas Instruments*

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Guidelines for Component Packaging and Interconnection with Emphasis on Surface Mounting

1.0 INTRODUCTION

Today's advanced electronic designs combine miniaturization and weight savings with high performance and low power consumption. To achieve all this, electronic assemblers often use surface mount technology, either alone or in combination with other sophisticated attachment processes.

This document examines key issues in advanced packaging techniques. These guidelines provide information on what type of parts are available, the techniques and processes necessary for their proper use, possible advantages, disadvantages or problems, how to start implementation, and where to find additional information. Since no one technology will provide all of the answers, the guidelines establish criteria for intermixing the processes, and define the necessary steps for producing quality electronic equipment. When other specific documents are cited, they should be reviewed for the current requirements. Where appropriate, sections from other IPC documents have been excerpted.

1.1 Scope This document provides guidelines for surface mounting electronic parts, and for intermixing surface and through-the-board mounting techniques. In addition, it describes the types of materials and interconnection substrates necessary for sophisticated electronic assemblies.

1.2 Purpose This document is intended to aid the designer in designing a manufacturable product by providing information on processing and on various types of substrate and joining materials.

The substrate physical and electrical characteristics and their compatibility for surface mounting are discussed. Land pattern designs, solder joint configurations, rework, and repair are also covered.

Adherence to the guidelines set forth in this document will generally assure adequate reliability for the majority of applications; however, more rigid requirements may be appropriate for more critical applications.

1.3 Classification When appropriate, this guideline will refer to three classes of component mounting complexity which reflect progressive increases in sophistication of tooling, assembly and joining techniques, and cost. These classes are as follows:

- A) Simple assembly techniques for through-the-board component mounting;
- B) Moderate assembly techniques for surface component mounting

- C) Complex assembly techniques for intermixing through-the-board and surface mounting on the same assembly.

Classification of component mounting complexity should not be confused with the performance classification of end-item use, as referenced in other IPC documents, which refers to Class 1) consumer products, Class 2) general industrial and Class 3) high reliability equipment types.

In addition to component mounting classification, a type designation may be specified for components mounted on one or both sides of the packaging and interconnecting structure:

Type 1 Components mounted on one side only;

Type 2 Components on both sides.

Type 2 is limited to only class B or C assemblies. Class and type designations help establish communication between design, manufacturing and assembly disciplines, as well as identify the precision and processing steps needed to assemble the board.

Any component mounting class and type may be applied to any of the end-product equipment classifications. For example, a consumer product designed to meet Class 1 requirements could have component mounting complexity Class A, B or C with components on either one or both sides of the board (Type 1 or 2).

1.4 Terms and Definitions The definition of terms used herein shall be in accordance with IPC-T-50 and the following: **Note:** Any definition denoted with an asterisk (*) is a reprint of the definition in IPC-T-50.

1.4.1 *Castellations Recessed metallized features on the edges of a chip carrier which interconnect conducting surfaces or planes within or on the chip carrier.

1.4.2 *Chip Carrier A low-profile rectangular component package, usually square, whose semiconductor chip cavity or mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package.

1.4.3 *Coefficient of Thermal Expansion Mismatch (Δ CTE) The difference between the coefficients of thermal expansion of two components, i.e., the difference in linear thermal expansion per unit change in temperature. (This term is not to be confused with Thermal Expansion Mismatch.)

1.4.4 Component A separable part of a printed board assembly which performs a circuit function (e.g., a resistor, capacitor, transistor, etc.)

1.4.5 *Component Mounting Site A location on a P&I structure, consisting of a land pattern and conductor fan-out to additional lands for testing or vias, used for mounting a single component.

1.4.6 *Constraining Core An internal supporting plane in a packaging and interconnecting structure, used to alter the P&I structure coefficient of thermal expansion.

1.4.7 *Double-Sided Assembly A packaging and interconnecting structure with components mounted on both the primary and secondary side.

1.4.8 *Dual In-Line Package (DIP) A component which terminates in two straight, parallel rows of pins or lead wires.

1.4.9 *Flat Pack A component with two straight rows of leads (normally on 0.050 inch centers) which are parallel to the component body.

1.4.10 *Footprint (See preferred term **Land Pattern**)

1.4.11 *Grid An orthogonal network of two sets of parallel equidistant lines used for locating points on a printed board.

1.4.12 Integrated Circuit (IC) An assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate, which performs an electronic circuit function.

1.4.13 *Land Pattern A combination of lands intended for the mounting, interconnection and testing of a particular component.

1.4.14 Leadless Chip Carrier A chip carrier whose external connections consist of leads around and down the sides of the package.

1.4.15 Leadless Chip Carrier A chip carrier whose external connections consist of metallized terminations.

1.4.16 *Mixed Mounting Technology A component mounting technology that uses both through-hole and surface-mounting technologies on the same P&I structure.

1.4.17 *Packaging and Interconnecting Structure (P&IS) The generic term for a completely processed combination of substrates, metal planes or constraining cores, and interconnection wiring, used for mounting components.

1.4.18 *Primary Side That side of the packaging and interconnecting structure closest to layer number one. (Also called the component side in through-hole component mounting technology.)

1.4.19 *Secondary Side That side of the packaging and interconnecting structure farthest from layer number one. (Also called the solder side in through-hole component mounting technology.)

1.4.20 Single In-Line Package (SIP) A component which terminates in one straight row of pins and lead wires.

1.4.21 *Single-Sided Assembly A packaging and interconnecting structure with components mounted only on the primary side.

1.4.22 *Supporting Plane A planar structure that is a part of a packaging and interconnecting structure and provides mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics. (It may be either internal or external to the packaging and interconnecting structure.)

1.4.23 *Surface Mounting The electrical connection of components to the surface of a conductive pattern without component lead holes.

1.4.24 *Thermal Expansion Mismatch The absolute difference in thermal expansion of two components, usually a component and a packaging and interconnecting structure, due to the influence of heat dissipation of an operating circuit and/or to changes in ambient temperature. (This term is not to be confused with Coefficient of Thermal Expansion Mismatch).

1.4.25 *Via Hole A plated-through hole used as a through connection, into which no component lead or other reinforcing material is inserted.

• **Blind Via** A plated-through hole connected to either the primary side or secondary side and one or more internal layers of a multilayer packaging and interconnecting structure.

• **Buried Via** A plated-through hole connected to neither the primary side nor the secondary side of a multilayer packaging and interconnecting structure; i.e., it connects only internal layers.

• **Tented Via** A blind or through via whose exposed surface(s) is fully covered by a masking material, such as a dry film polymer coating (solder mask), prepregged glass cloth (prepreg), etc., in order to prevent

hole access by process solutions, solder, or contamination.

- **Through Via** A plated-through hole that connects the primary side and secondary side of a packaging and interconnecting structure.

2.0 REFERENCE DOCUMENTS

2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-SC-60 Post Soldering Solvent Cleaning Handbook

IPC-AC-62 Post Soldering Aqueous Cleaning Handbook

IPC-CM-78 Guidelines for Surface Mounting and Interconnecting Chip Carriers

IPC-RF-245 Rigid-Flex Printed Boards

IPC-D-249 Design Standard for Flexible Single- and Double-Sided Printed Boards

IPC-FC-250 Single- and Double-Sided Flexible Printed Wiring With Interconnections

IPC-D-319 Design Standard for Rigid Single- and Double-Sided Printed Boards

IPC-SD-320 Rigid Single- and Double-Sided Printed Boards

IPC-D-322 Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes

IPC-MC-324 Qualification and Performance Specification for Metal Core Boards

IPC-D-325 Documentation Requirements for Printed Boards

IPC-C-406 Design and Application Guidelines for Surface Mount Connectors

IPC-A-600 Acceptability of Printed Boards

IPC-A-610 Acceptability of Printed Board Assemblies

IPC-R-700 Modification and Repair for Printed Boards and Assemblies

IPC-CM-770 Printed Board Component Mounting

IPC-SM-782 Surface Mount Land Patterns (Configurations and Design Rules)

IPC-SM-784 Guidelines for Chip-On-Board Technology Implementation

IPC-S-804 Solderability Test Methods for Printed Boards

IPC-S-805 Solderability Tests for Component Leads and Terminations

IPC-S-815 General Requirements for Soldering Electronic Interconnections

IPC-SF-818 General Requirements for Electronic Soldering

IPC-AJ-820 Assembly and Joining Handbook

IPC-CC-830 Qualification and Performance of Electrical Insulating Compounds for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-H-855 Hybrid Microcircuit Design Guide

IPC-D-949 Design Standard for Rigid Multilayer Printed Boards

IPC-ML-950 Performance Specification for Rigid Multilayer Boards

IPC-SP-819 General Requirements and Test Methods for Electronic Grade Solder Paste Materials

2.2 Electronic Industries Association (EIA)²

Publication 95 JEDEC Registered and Standard Outlines for Solid State Products

EIA-RS-178 *No longer available*—replaced by

IPC-RS-186-9E Standard Test Methods for Passive Electronic Component Parts—Method 9: solderability Rev. E.

2.3 Military³

2.3.1 Standards

MIL-STD-129 Marking for Shipment and Storage

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-STD-275 Printed Wiring for Electronic Equipment

1. IPC, 2215 Sanders Road, Northbrook, IL 60062

2. Electronic Industries Association, 2001 Eye St., N.W., Washington, D.C. 20006

3. Publications are available from Naval Publications and Forms Control, 5801 Tabor Road, Philadelphia, PA 19120

MIL-STD-454 Standard General Requirements for Electronic Equipment

MIL-STD-883 Test Methods and Procedures for Microelectronics

2.3.2 Specifications

MIL-P-13949 Plastic Sheet, Laminated, Metal Clad, for Printed Wiring Boards

MIL-P-28809 Printed Wiring Assemblies

MIL-M-38510 Microcircuits, General Specification for

MIL-C-45662 Calibration System Requirements

MIL-P-55110 Printed-Wiring Boards, General Specification for

2.4 Federal³

QQ-S-571 Solder, Tin Alloy, Lead-Tin Alloy and Lead Alloy

2.5 American National Standards Institute (ANSI)⁴

ANSI Y-14.5 Dimensioning and Tolerancing

3.0 COMPONENT PACKAGING AND INTERCONNECTION (CPI) IMPLEMENTATION CONCEPT

An electronic system or subsystem design should contain the following:

- Needs Analysis
- Constraints
- Objective
- Feasibility Study
- Design Evaluation

This section will help the designer understand how to evaluate a design with respect to the parameters listed above, and how to judge the cost/benefits of minor variations in the selected design.

Relative cost comparisons of P&I structures and custom VLSI should not be done on a function-to-function basis, but on the complete electronic system. In order to compare costs realistically, you should compare a P&I structure which uses machine-inserted components and wave soldering to a P&I structure with components on both sides having less complex printed board assemblies. These latter assemblies will usually have less system interconnections, and fewer card connectors making the more complex system more cost effective.

Also, volume or quantity considerations should be applied to any cost tradeoff. Custom LSI may prove to be the most effective for very large quantities, but due to the higher nonrecurring costs of LSI circuits, they may not be cost effective for low volume systems.

The following are some of the specific items which can affect recurring and nonrecurring costs:

- A. Circuit Partitioning**—Partition the circuit for both testability and complexity; i.e., select a partitioning scheme which incorporates external test points for fault isolation at the component level and which also allows a reasonable first functional yield after test.
- B. Circuit Pinout Identification**—The P&I structure designer (not the circuit designer) should specify the pinout locations. This will simplify the layout task and allow the layout designer to design for cost effective production methods.
- C. Component Specification**—Select components with multiple sourcing so that costs remain competitive and delivery times short. Match component specifications to system requirements; i.e. use commercial parts on a common system, not military parts.
- D. Environmental Requirements**—Specify environments for the P&I assembly that are consistent with the systems true environment. This can significantly affect package selection (hermetic vs. nonhermetic), parts selection, electrical and environmental testing costs, and final circuit yields.
- E. Circuit Element Tolerances**—Specify tolerance values on resistors, capacitors, etc. The wider the tolerances, the higher the yields and the lower the cost. Also, where possible, specify matching tolerances rather than absolute tolerances since it is usually easier to match resistors and capacitors than to obtain precise absolute values.

In addition to costs, reliability considerations should be as important a part of the design cycle as financial, electrical, mechanical, and thermal considerations. Therefore the following should be considered:

- What is the expected life of the circuit?
- What is the specified failure rate of the final circuit?
- What failure modes are likely?
- To what types of environment will the assembly be exposed?
- What benefits will mechanical screening and electrical burn-in give?
- Will accelerated testing lead to reliable estimates of component reliability?

4. American National Standards Institute, 1430 Broadway, New York, NY 10018

3.1 System Design Sequence A successful design usually follows an optimized sequence of steps or states. The design sequence presented in Table 3–1 indicates the performance or design parameters to be considered at each step. At any step in this sequence, one or more of the criteria may constrain the design and require a reevaluation of previous steps.

3.1.1 System Requirements The environment in which the system must operate, system size, weight, reliability, power, and signal sources and levels should all be included in the system specification. In addition, manufactured-item cost, life-cycle cost, and cost-versus-performance criteria should be specified. System definition may include a schematic diagram or may be limited to block diagrams indicating simple functions and signal flow information. In either case, the system must be partitioned into realizable circuit functions.

3.1.2 Circuit Requirements Form, fit and function are primary considerations at this stage of design. Partitioning repetitive functions into multiple configurations can cut costs, while conversely, increasing complexity within a packaged function may increase costs. Also, consider output and input pinout requirements in the partitioning step in order to achieve final package commonality.

3.1.2.1 Breadboard Demonstration of the circuit function in breadboard form identifies performance restrictions that affect eventual substrate layout. Testability and verification of functional performance are determined at this stage.

3.1.2.2 Final Circuit Schematic Final definition of the circuit schematic diagram will follow a successful breadboard evaluation. At this stage, components must be selected that meet performance specifications and package compatibility with respect to alternate assembly processes.

The availability of semiconductor devices may well determine the process methods and/or the assembly sequence to be used.

3.1.2.3 Component Count and Availability Component definition and count will affect size because of topographical considerations. Layout restrictions associated with alternate process design rules and performance-related criteria developed in the breadboard stage must also be considered. If required, the custom development of a semiconductor package may affect the project schedule.

3.1.2.4 Process Definition Process definition follows final component selection. The assembly techniques to be used (e.g. surface mount, through-the-board mounting, mixed technologies), the reflowed solder assembly temperature hierarchy (for solder reflow, epoxy cure) and the system interconnect are influenced by component selection, packaging selection and system requirements.

3.1.2.5 Design Review The final design and selected processes should be evaluated at this stage. Compromises previously made should be reconsidered if they affect the product manufacturability.

3.1.2.6 Substrate Layout When component process and productibility issues have been resolved, substrate (circuit) layout can commence. This involves coupling module size, pinout, performance, and testability requirements with established design rules.

Figure 3–1 shows the relationship for P&I conductor routing lengths required to interconnect various package types. Routing density requirements are compared for standard dual-in-line packages, pin-grid arrays on 2.54 mm and 1.27 mm [0.100- and 0.050-inch] centers as well as chip carriers on 1.27 mm and 0.63 mm [0.050- and 0.025-inch] centers.

Table 3-1 System Design Sequence

State of Design	Parameters Considered
1. System Requirements	Environment • Size • Weight • Cost • Reliability • Power Supply • Signal
2. Circuit Requirements	Partitioning • Complexity • Form • Fit • Count • Input/Output (I/O) • Function
3. Breadboard	Testability • Functional Verification • Performance Restrictions
4. Final Circuit Schematic	Pinout/Layout Restrictions • Component Definition
5. Component Count and Availability	Layout Restrictions • Module Size • Component Compatibility/Availability
6. Process Definition	Technology Definition • Package Temperature Hierarchy • Assembly Techniques
7. Design Review	Producibility • Cost
8. Substrate Layout	Size • Pinout • Package
9. Prototype Fabrication	Process Verification • Producibility • Performance
10. Critical Design Review	Manufacturing Resources • Producibility • Cost • Performance • System Integration
11. Manufacturing	Capability Design Rule Update

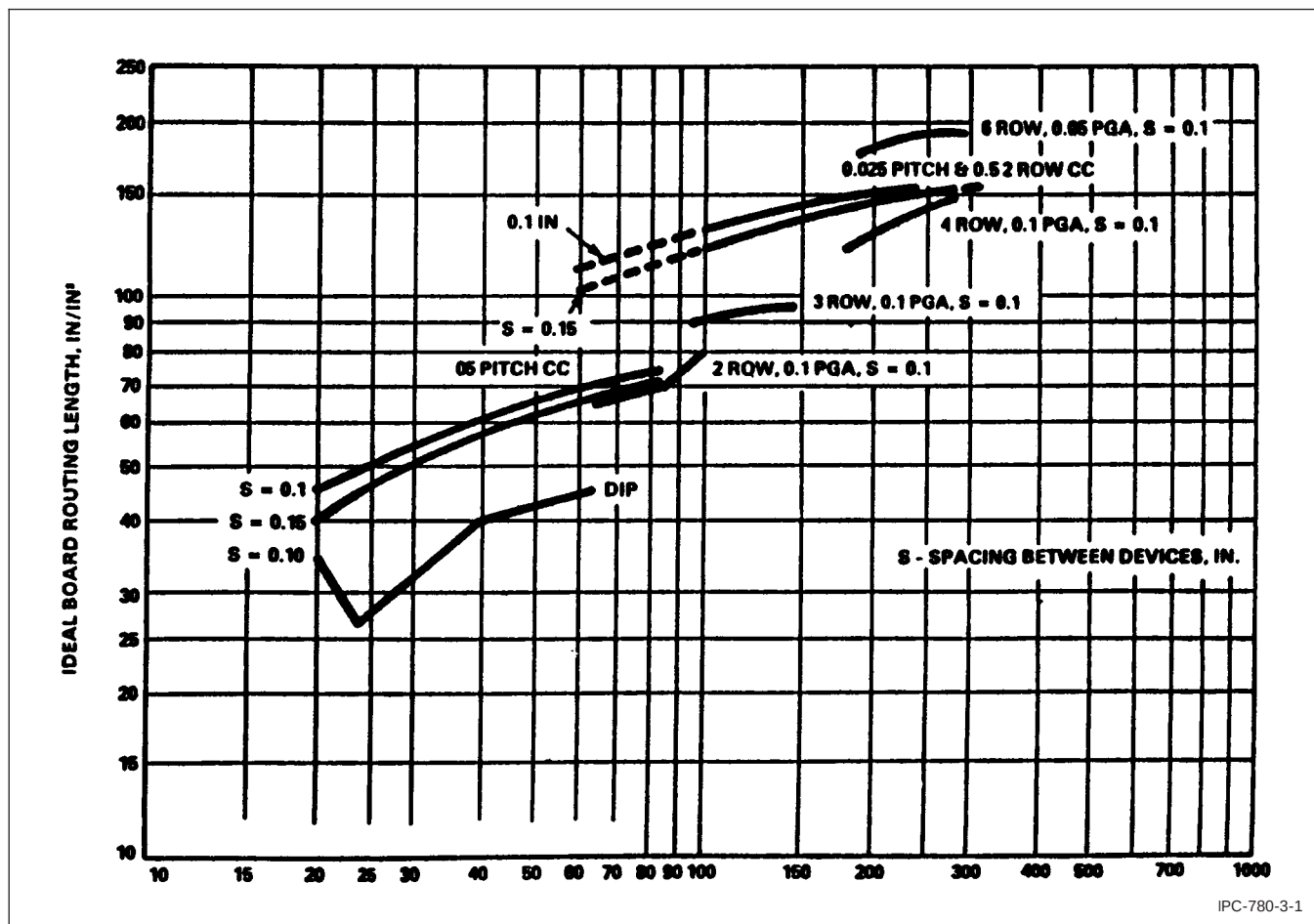


Figure 3-1 Ideal connective length needed versus number of pins and package type (all dimensions in inches)

3.1.2.7 Prototype Fabrication The inherent electronic performance improvement resulting from reducing the magnitude and complexity of interconnections must be balanced against possible interference due to this increased packaging density. With experience, design rules will evolve to increase the predictability of this tradeoff, but verification is best accomplished by prototype evaluation. Any addition to performance criteria should be evaluated for its effect on cost projections, producibility and the status of manufacturing resources.

3.1.2.8 Critical Design Review System design, Quality Control and Assurance, Manufacturing, Cost Accounting, and Management personnel should participate in a final Critical Design Review. Related personnel should agree on the design, or at least be aware of design parameters, if they are to effectively meet project objectives.

3.1.2.9 Manufacture Experience accumulated in manufacturing should be communicated to other various personnel to insure that product designs reflect changes in process capability.

3.1.3 Performance Considerations Some P&I structures offer distinct advantages over other circuit packaging

techniques with respect to performance parameters such as switching speed, high frequency applications, filter and tuning circuits, thermal characteristics, etc.

High-speed digital circuits require short interconnections between active elements. Surface mounted components offer short interconnections and transmission lines with well-controlled impedance. Such circuits can increase the operating rates of circuits using ECL, TTL and other digital techniques. Microwave circuitry is very susceptible to external and internal circuit noise and may necessitate custom laminates such as Teflon, or other special materials which can lower noise.

3.1.4 Reliability Considerations The P&I structure is the mechanical base and electrical insulating material used in fabrication. The material properties of the substrate affect both the fabrication processes and the inherent reliability of the final circuit. Important substrate properties for high reliability are dielectric strength, thermal conductivity, thermal coefficient of expansion, camber, surface finish and materials compatibility. A great deal of the circuit reliability depends on the reliability of the components. Thus, specifying components with known reliability is important.

Most commonly used silicon devices, monolithic capacitors, resistors, inductors, etc. have varying levels of reliability and thus should be chosen carefully.

When using chip-and-wire components, the components cannot be tested prior to assembly. Therefore, it may be advisable to burn-in the assembly to weed out infant mortality failures.

3.1.5 System Integration A P&I assembly is not an independent unit, but part of a system (or subsystem). Matching assembly characteristics to the system requirements can influence, or even determine the selection of the materials, devices and technologies for the assembly. Problems created by integration into the system are best handled at the first stage of design.

3.1.5.1 Position of P&IA Inside the System Some P&I assemblies withstand abnormal conditions better than others, due to their position and function in the system. Design for the worst conditions or for each assembly's individual condition. This can determine the materials, the sizes and the technologies that have to be selected.

3.1.5.2 Environmental Consideration P&I assemblies should be designed for their worst case stress conditions, which could be very different from the normal/functional conditions. Worst case stress conditions involve both functional and environmental conditions. Environmental conditions are related to, but not necessarily the same as, the ambient conditions. A good system designer will add protection elements. If protection elements are not used or are inadequate, the density of the P&IA may have to be reduced. Select materials, devices and interconnections to meet stress conditions.

3.1.5.3 System Cooling Heat dissipation is a major limitation in electronic equipment miniaturization. In many cases, the capacity for heat dissipation limits volume reduction. Air will remain the cooling media for sometime to come, even though liquids or other high pressure gases have been used. The cooling media, however, is only one factor in the cooling process selection. The selection of the cooling path(s), heat transfer mode and the ultimate heat sink is equally important.

Figure 3-2 represents a matrix of the cooling option combinations. However, not all of these combinations are feasible. The geometry of the P&IA, the materials, and the manufacturing technologies have to be consistent with the selected cooling process. The cooling process has to be selected during the initial design, in accord with the imposed system requirements stage.

3.1.5.4 Thermal Management While the power consumed per IC-function is decreasing, the number of functions per chip is increasing, thereby increasing power con-

sumption per device. Opinion is divided on what power the VLSI of the 1990s will dissipate, but a few watts per device is probable.

The greatest impact on thermal management will be the high density of devices. For one 68 pin chip carrier per square inch, the power density will be a few watts per square inch. Thermal management will not only determine junction temperature, but will also affect attachment reliability. If junction temperatures of the IC devices are to be held to a reasonable level (about 100°C) by using convection cooling or forced-air cooling in the worst case, a good thermal path from the chip to the P&I structure or to its own heatsink will be necessary. The heatsink (cooling fin) could be integrated into the individual chip carrier and/or else chip carriers will have integral cooling fins mounted together on a mothercarrier. However, the weight of these cooling fins might cause solder creep failures, depending upon the fin weight and mounting orientation.

With their multitude of high-speed, high-power chip carriers, highly sophisticated electronic computers dissipate vast amounts of power. Such a system may need to dissipate kilowatts of power to several thousand 5-watt devices, or to several one-kilowatt individual subassemblies. In these instances, complex compressors, manifolds, and tubing may be the only solution.

The technology for cooling these is based on water cooling pairs of board assemblies with leaded chip carriers that are separated by an aluminum cold plate. The outer layer of the cold plate is a plastic membrane of Tedlar compliant film enclosing a thermally conductive paste. The boards are pressed against the membrane forcing the chip carriers against the film, and the thermal paste conducts the heat of the chip carriers to circulating water running through the cold plate. The water flows from the cold plate to a cooling unit that serves as a heat exchanger between the coolant and a chilled water system.

Many other sophisticated thermal management tools exist. Some cool the P&I structure instead of the chip carriers directly; others use forced air cooling, and yet others utilize a high degree of conduction cooling.

All system designs involve extensive thermal management which must take into account the thermal properties of both the chip carrier and the P&I structure. Therefore, give careful consideration to this when a high degree of heat dissipation is required.

3.1.5.5 Corrosion Protection Corrosion involves moisture and high humidity. A common practice to protect against corrosion is coating. A good coating (applied on the board level) should reduce moisture penetration and thus reduce corrosion. This same improvement is expected from a hermetic enclosure for a device. However, neither the coating nor the enclosure can guarantee protection.

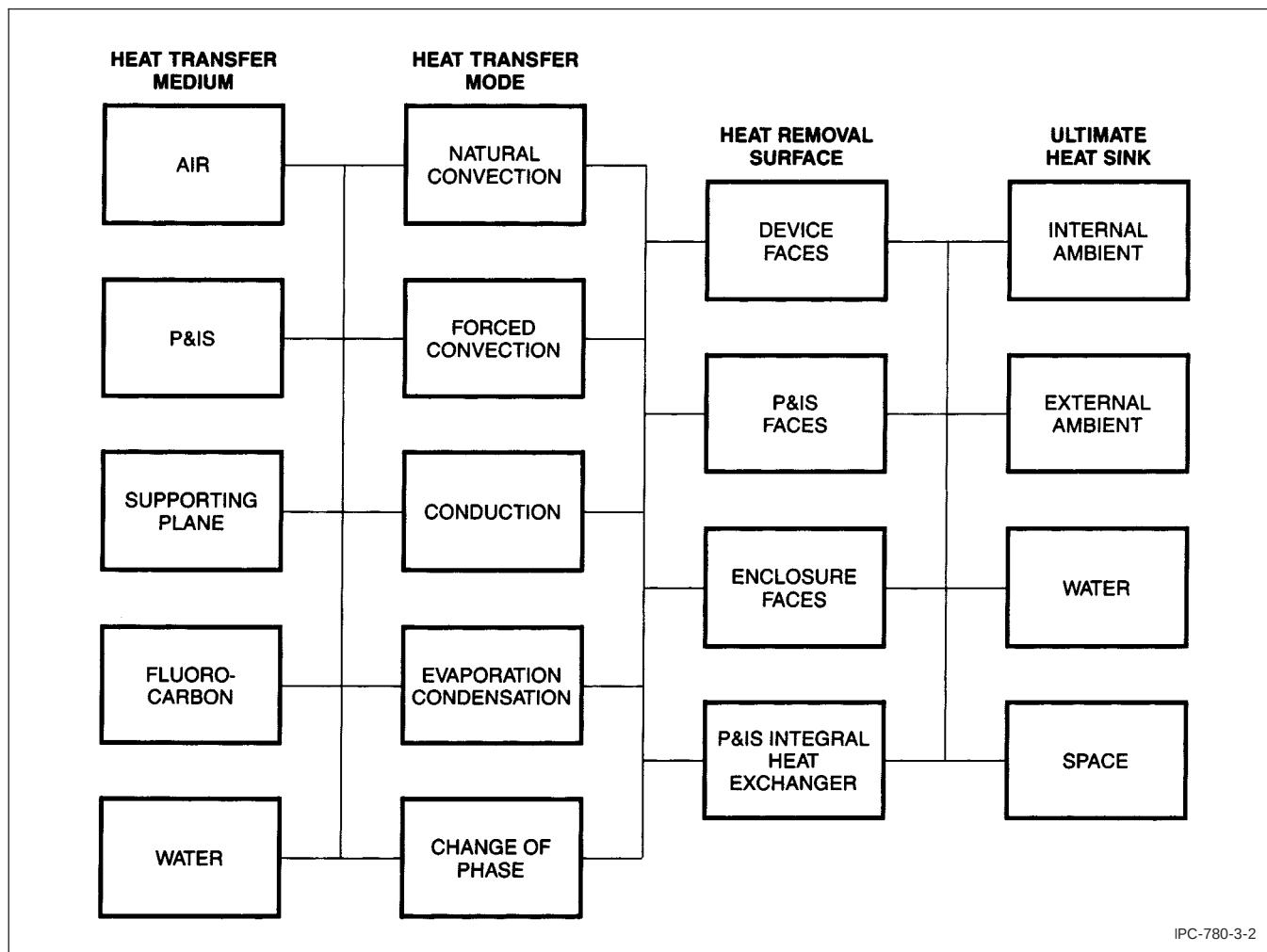


Figure 3-2 Cooling option combinations

never occur. Water can be captured inside the enclosure during the manufacturing process. More important, coating and enclosure can create some logistic problems connected with the heat dissipation.

In some conditions, the corrosion generated by humidity can be eliminated by maintaining a temperature difference between the air inside the cabinet and the ambient. The temperature differential can be achieved through a heater circuit or by the judicious distribution of the normal heat generated by the components and circuitry. As an example a temperature difference of 5°C (25°C at ambient heated to 30°C) could reduce 100% RH at ambient to 75% RH heated condition.

The cabinet design and cooling option selected could create different environmental conditions than the natural ambient conditions and minimize some corrosion problems. Conversely, an inadequate system design can accelerate degradation of the P&I assembly.

3.1.5.6 Electrical Overstress Protection Induced currents and voltages in transmission lines as well as faults in the network could create (usually for very short times)

abnormal conditions of electrical stress that in some cases could be orders of magnitude higher than under normal operational conditions. If the transient pulses pass inside the enclosure without causing breakdown of the interconnect system, the devices and the circuitry could be stressed by the voltages and currents that they are not designed to carry. If stress clamping or reduction elements are not available in the system, all exposed elements and the interconnection lines have to be selected to survive overstress conditions, at the expense of the density criteria.

A. Overvoltage Protection—Transient pulses of substantial amplitude could be caused by lightning, ESD, triboelectricity and steady state induction into conductors and cable pairs. The preferential entry port for these currents are the cables and the connections to the communication network. Lightning may induce voltages higher than 600 V into the P&I assembly. Overvoltage protectors are necessary, or to avoid catastrophic voltage breakdowns the distance between conductors must be selected according to the requirements of the abnormal conditions, and in this case the density of the P&IA may have to be reduced.

B. Overcurrent Protection—If current surges brought in by the connecting lines are not stopped before they reach the P&IA, they can easily melt the P&IS conductors. To avoid the catastrophic failure of the equipment, if overcurrent protectors are not available in the system, the conductor must be designed for current carrying capacity at surge levels. This may reduce the density of the P&IA and exclude materials (such as polymer films) that have low power transfer capacity.

C. Electrostatic Discharge Protection—ESD, as a dynamic process, is one of the most powerful transient voltage inducers. If the path of the currents created by ESD activities cannot be kept under control, the devices and their packages have to be selected to survive the maximum possible stress created by these currents.

D. Electromagnetic Interference Protection—EMI protection can be divided in two major concerns:

- Reduction of the effects that reception of external radiation has on electrical performance.
- Reducing the emissivity of the system to a level required by the legislation or customer requirements.

The first concern is treated (in most of the cases) at the electronic design stage. Filters and specific types of connectors are selected and introduced in the electrical layout. The second concern is mainly a function of the mechanical design and has to be solved at a later stage. From this point of view, for the designer, EMI protection involves reducing the emissivity more than reducing the susceptibility of the circuits to external EMI.

Emissivity can be reduced by the following:

- Controlling the design of the layout in order to achieve the minimum possible radiation from the system,
- Cutting down the radiation by using sealing and shielding against EMI. Both ways have a great impact on the P&IA layout design. Controlling the emission levels will change the layout design requirements and introduce new constraints on the design, affecting manufacturing technology selection. Shielding may cause other problems. Shielding could reduce heat dissipation and it usually interferes with most of the commercially available cooling options.

3.1.5.7 Design for Test Surface mount technology has raised new issues in designing systems which accommodate testing. The relatively higher cost of surface mount devices and the larger number of pinouts requires that testing be designed into the system to prevent use of detective parts and to insure that committed parts are easily testable, preferably without removal.

A. Component—Specifically, this means that the packaging design should incorporate easily testable components along with test sockets and burn-in sockets. The component should be compatible to rapid tests, both static and dynamic.

B. In Circuit Testing—The P&I structure should be designed to allow in-circuit testing of component parts. Because devices are costly and difficult to remove without damaging the P&I structure, it is imperative to build in design features which allow testing of components. One method for doing this is cuttable links. Other features should be built into the P&I structure to allow for in-circuit testing.

C. Functional—Functional testing means the ability to test the system by function. For this reason, the P&I structure must be designed to include some method of isolating functional elements of the circuitry in order to test by function, as opposed to board or chassis level tests.

D. Prototype—Prototype testing means testing of prototype assemblies instead of production type assemblies; the latter allows more permanent packaging techniques and closer conformity to the customer requirements and applicable specifications. The prototype design allows more liberty in land spacing, component spacing, and line widths and spaces in the interest of expediency. Necessarily, a prototype design must be capable of change, but close enough to the end item part (or assembly) that mechanical and electrical characteristics of the final equipment are duplicated in the prototype design.

3.2 Technology Trends Considerable progress has been achieved in extending the capabilities, conductor density, and yields of printed wiring technology. At present, however, further improvements in the state-of-the-art bring diminishing returns at greater cost. Also, it may be arguable that more stringent future demands can be met by the direct linear extension of current methods. An important factor is the emergence of new package types for complex LSI and VLSI devices, (see Figure 3–3). As LSI circuits grow in complexity, they require more input/output (I/O) capabilities for communication with the outside world. Advances in interconnection systems have occurred in response to the evolution of electronic technology, particularly the growth in component sophistication, complexity and number of terminals to be connected. It should also come as no surprise to find that printed wiring remains the most popular and universal method of interconnection. However, a basic concern has developed with the progress of printed-wiring technology.

A variety of factors contribute to this growing concern, including the following:

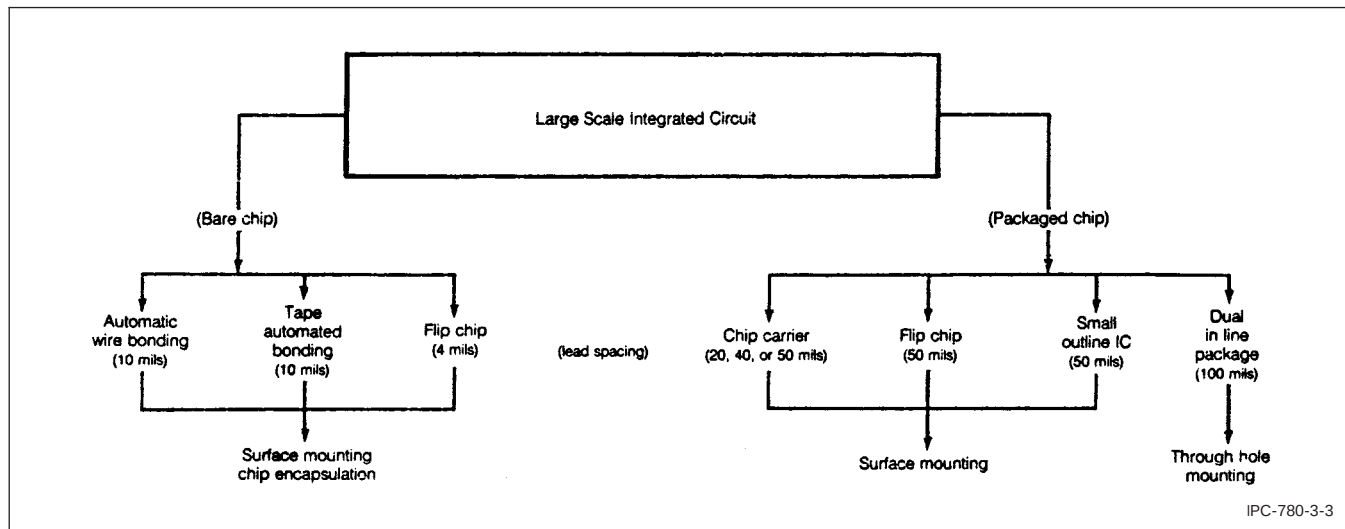


Figure 3-3 Packaging and assembling integrated circuits (all dimensions in inches)

- A. Interconnection Costs**—These have not followed the decline in device costs. Today a complete computer-on-a-chip costs less than the surrounding components and interconnection system.
- B. Operating Speeds**—The use of the faster-operating integrated circuits is increasing. The interconnection system serving them should have configurations that make it possible to locate all such devices within a very limited area in order to avoid or minimize excessive propagation delays in the wiring.
- C. Integration of Functions**—Further integration of circuit functions within dual-in-line-packages is becoming more limited, in part by the practical considerations of the economical size of the ICs and DIPs suitable for easy design change and field repair.
- D. Lead Spacing**—Any increase in the number of leads per IC package calls for increased interconnections between them (Table 3-2). LSIs having more than 48 leads cannot be efficiently packaged in the familiar DIP configuration with two rows of leads on 2.54 mm (0.400 inch) centers. These devices will require the new packages that are coming onto the market.

3.2.1 Package Technology The emerging higher-speed, higher-density ICs can increase the performance of complex electronic systems. This is especially true in applications where size, weight and power requirements are critical.

However, these new devices require compatible packaging technology, a new interconnection system. The significance of these new interconnection system requirements can be seen appreciated by reviewing the development of semiconductor technology (see Figure 3-4).

As VLSI use increases, a greater percentage of the total system cost, of the total design and manufacturing time,

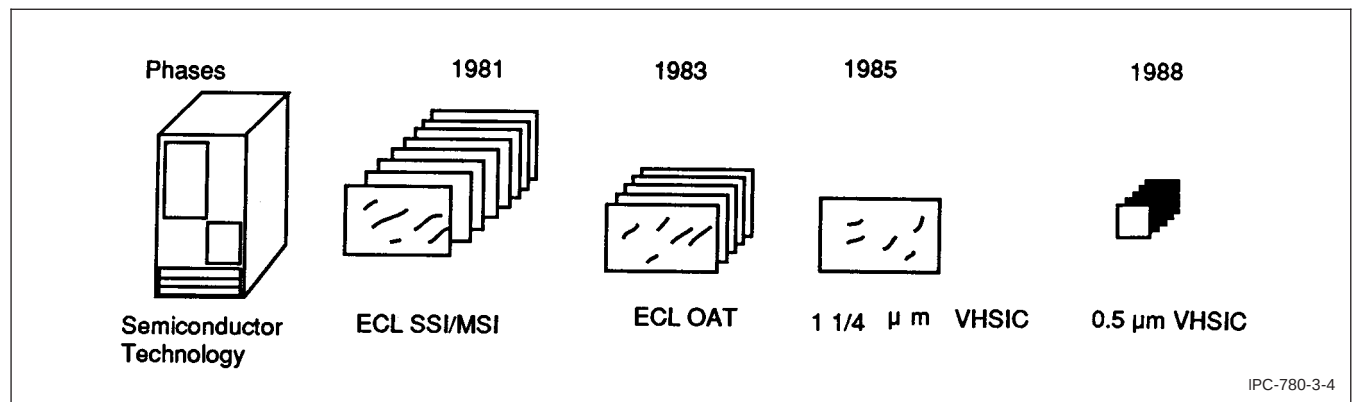
and of the testing costs will be affected by the packaging/interconnection system technology. Also, chip packaging levels will increase to over 10,000 gates/chip and board pinouts will approach 300, with proportional increases in power to be dissipated per unit volume (see Figure 3-5). Peripheral devices such as DIPs and chip carriers, or matrix devices such as pin-grid-arrays, will significantly affect packaging density (Figure 3-6) and therefore the interconnection system.

3.2.2 Interconnect Technology Until recently, component interconnection technology was almost exclusively based on plated-through holes and therefore, all devices or their packages had leads that were eventually soldered into these holes. These component leads added to material costs, assembly labor, and manufacturing problems. The newly-emerging packages resolve this problem, since they are designed for the surface mounting of planar packaged and unpackaged components on a planar surface and do not require discrete component leads and plated-through holes. This development will have a profound effect on future interconnection methods, because the surface attachment approach achieves the following:

- Eliminates the cost and labor for component leads and their forming.
- Simplifies the problems of component shipping and handling by the elimination of their delicate leads.
- Simplifies assembly, since there are no leads to preform. Also, the self-centering capability of many of these new devices during the soldering operation makes them tolerant to some component placement misalignment.
- Increases the component placement rate from today's 300 units/hour for manual assembly or 3,000 units/hour for automated methods, by one more order of magnitude; e.g., 10,000 units/hour on a 200 by 250 mm [8 by 10 inch] board is achievable.

Table 3-2 Connectivity Capacity Requirements for DIPs and Small Chip Carriers (Dimensions only in inches)

Case	Typical Packaging Situation	Approximate Number of Pins per in ²	Required Connective Capacity, in/in ²	Wiring Levels		
				50 mil Grid	25 mil Grid	20 mil Grid
1	1–16 pin DIP per square inch	16	34	~2 (1.7)	~1 (0.8)	1 (0.7)
2	22-pin DIP on 1 inch centers	20	45	2–3 (2.3)	1+ (1.13)	1 (0.9)
3	2–16 pin DIPs per square inch	30	67	3–4 (3.4)	2 (1.68)	2 (1.34)
4	40-pin DIP on 1 inch centers	20	45	2–3 (2.3)	1+ (1.13)	1 (0.9)
5	24-pin chip carriers on 0.7 inch centers	50	112	~6 (5.6)	~3 (2.8)	~3 (2.2)
6	24-pin chip carriers on 0.5 inch centers	96	216	~11 (10.8)	~6 (5.4)	~5 (4.3)
Connective capacity per level, in/in ²				20	40	50

**Figure 3-4 Semiconductor technology development**

- Simplifies the soldering process by assembling with solder-reflow systems that use the vapor-condensation methods without the need to worry about leads protruding on the underside of the substrate.
- Improves connectivity/unit area on the underlying substrate by reducing the hole diameters, or by eliminating the need for holes.

3.2.3 Size Considerations A variety of packaging techniques are available for the production of a system. These range from point-to-point-wiring to custom very large scale integration (VLSI). Selection of the technology can be based on many factors, but size of the P&IS is a major consideration. The relative sizes of the most commonly used technologies are outlined in Table 3–3.

As can be seen in Table 3–3, there is a significant size reduction potential with the VLSI. However, the extra size reduction can only be achieved with a significant increase in development cost and time. Comparisons should consider the size, cost and delivery cycle of a complete system.

3.3 Packaging/Interconnection Assembly Implementation Techniques The designer should constantly review

the end product for form, fit and function with respect to cutting costs, being competitive, and making the product more marketable. The concepts of form, fit and function are defined as follows:

- Form:** The form of a product includes size, weight and shape.
- Fit:** The fit of a product is its relationship to other functions within the product.
- Function:** Each product performs different functions. The system can be analyzed for cost per function, power dissipation per function, etc.

Having broken a system down in this manner, the designer then needs to consider how the product function is to be achieved, i.e. as an electronic assembly or as a mechanical assembly. For example, the clock function in an automobile can be realized as an electronic assembly or as a mechanical assembly.

Low profile (the height above the board mounting surface) and minimum printed board mounting area are initial considerations for all components. These two requirements govern the density of components on the board.

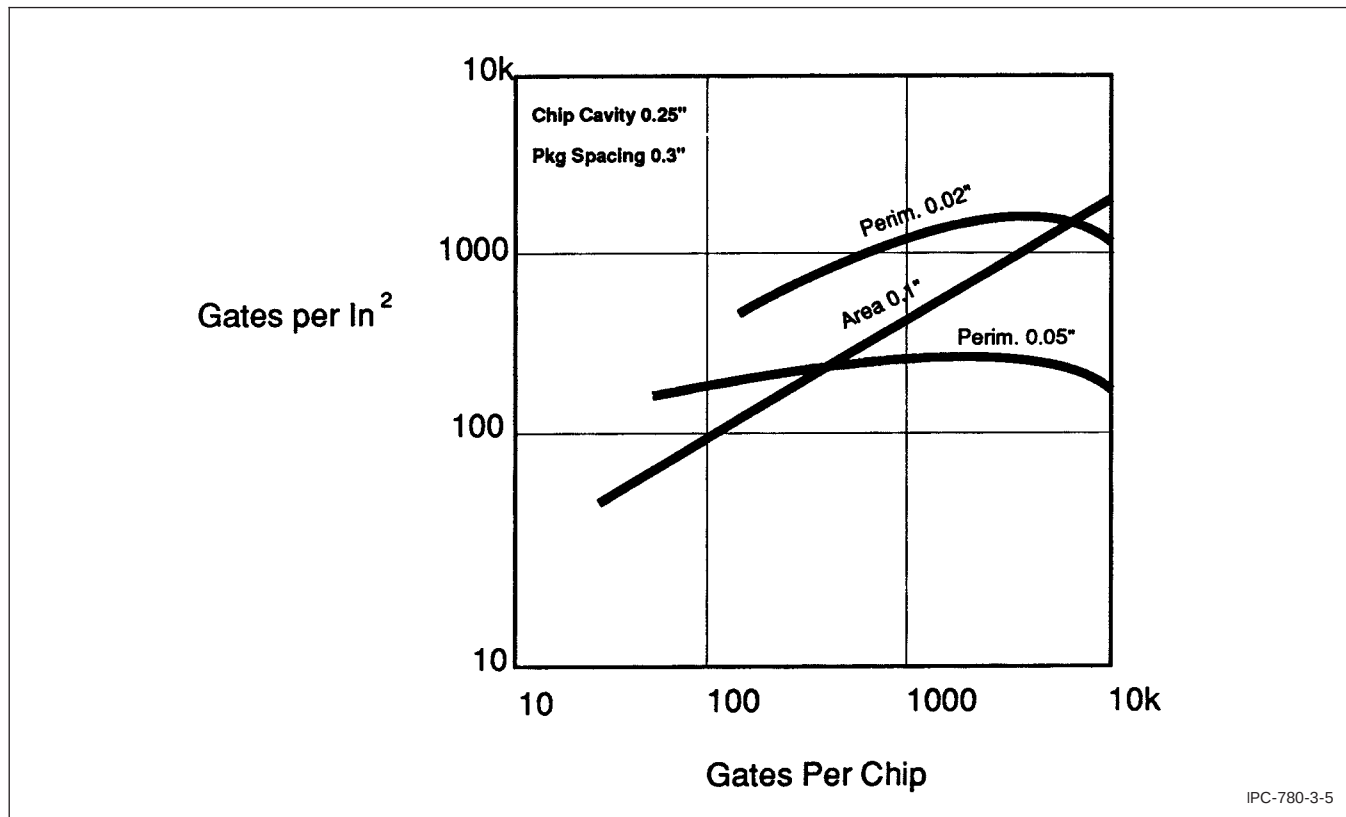


Figure 3-5 Gate density comparison (all dimensions in inches)

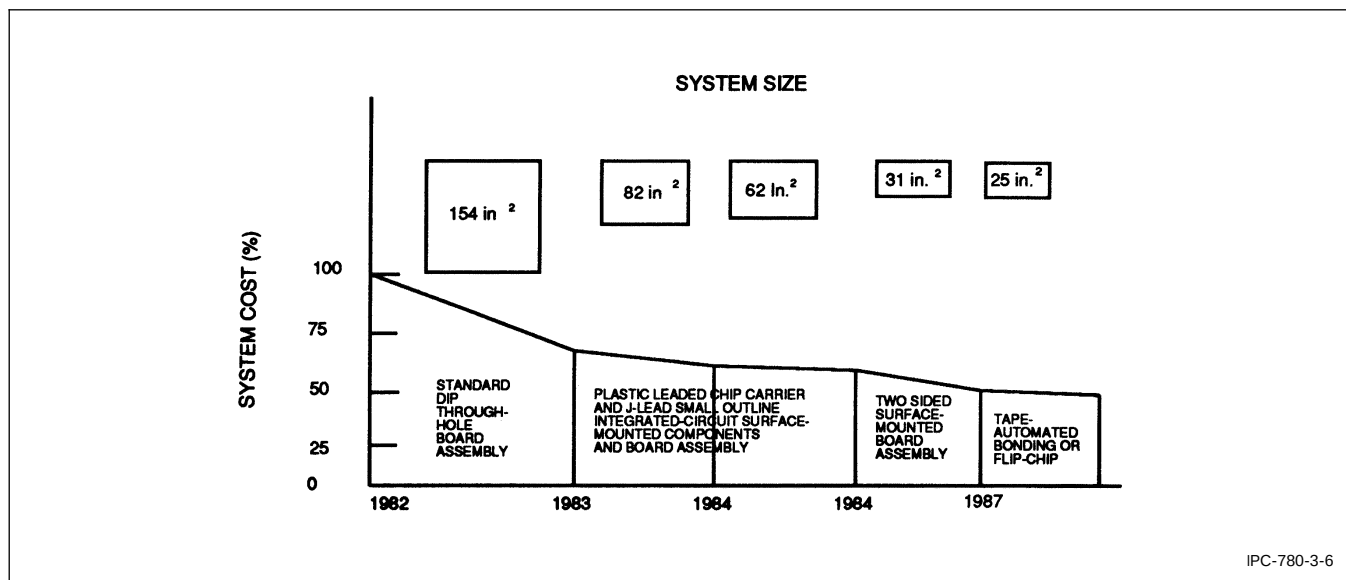


Figure 3-6 Packaging technology comparisons (all dimensions in inches)

the closest center-to-center dimensions for side-by-side mounting of printed boards within the card holder or equipment rack.

Determining factors will include development time, development cost, circuit element factors, manufacturing costs, thermal considerations and reliability. The following paragraphs will review some of the advantages and disadvantages of realizing an electronic function as a P&I assembly.

3.3.1 Comparisons Table 3-4 shows some of the comparisons between through hole mounting and surface mounted components.

3.3.2 Size Because the dimensions of the connectors and surfaces necessary for handling and mounting are practically independent of the design and manufacturing, the ratio of populated area to the total area is a function of the size. The larger size P&I assemblies are typically the most

Table 3-3 Relative Size of Packaging Techniques

Technique	Size (Relative Units)
Point-to-Point Wiring	10,000
P&IS—Through Hole (Type A1)	2,000
P&IS—Intermixed Components (Type C ₁ , C ₂)	1,000
P&IS—Surface Mount (Type B ₁ , B ₂)	500
P&IS—Chip & Conductive Ink Components	200
Custom Large Scale Integration (LSI)	50
Custom Very Large Scale Integration (VLSI)	10
Custom Ultra Large Scale Integration (ULSI)	1

effective from a labor cost per unit area processed, but may pose difficulties to the fabricator. Theoretically, considering printed boards as an independent entity, an optimal size can be found for any selected technology (for reference see IPC-D-322, Guidelines for Selecting Printed Wiring Board Sizes Using Standard Panel Sizes).

In order to minimize cost and maximize production efficiency, use the largest board size that is practical; however, size is often determined by other considerations such as the following:

- Limitation in external envelope of the equipment. Even though the external envelope is the ultimate constraint (as

in some military and space applications), restrictions on the shape/ configuration of the P&IA are imposed in any practical application.

- Testing and maintainability procedures. If a failure of the equipment has to be identified and repaired in the field (as in the communications industry), then divide the boards according to their electrical functionality. In this case, both density and optimum size criteria may have to be sacrificed.
- Thermal and mechanical strength limitations. Large P&I assemblies are more sensitive to mechanical stresses than small ones; environmental conditions and the protective measures used against harmful environments can limit actual size.

3.3.3 Through-Hole Mounting Technology Through hole mounting technology uses a leaded device configuration such as dual-in-line packages (DIP), single-in-line packages (SIP), or some other leaded device configuration. The DIP is approximately 15 mm [0.6 inch] wide by 2.5 mm to 75 mm [1.0 to 3.0 inch] in length with wire leads on 2.54 mm [0.1 inch] centers. The DIP is mounted with leads through the board usually in plated-through holes, and when the board is sent through an automatic soldering machine all connections are mass soldered in place during

Table 3-4 A Comparison of Integrated Circuit Packaging Technologies

Characteristics	Through Hole	Leaded Surface Mount	Leadless Surface Mount	Direct Deposit	Bare Chip
Packaging Density	low	moderate	good	good	high
Standardization	very good	good	good	good	limited
Thermal Performance	moderate	good	very good	good	fair
Substrate Choices	very good	very good	good	fair	limited
Fab Investment	low	low	moderate	moderate	high
Assembly Investment	moderate	low	moderate	moderate	high
Support Investment	low	moderate	moderate	high	high
External Assembly Services	very high	high	moderate	moderate	limited
Maintenance Skills	low	moderate	moderate	high	high
Change Risk	very low	low	moderate	moderate	high
Assembly Test	very easy	easy	moderate	moderate	complex
Documentation	easy	easy	moderate	complex	complex
Logistics Support	field change	field change	field change	field change	factory only
Inspect (Circuit)	100% test	100% test	100% test	100% test	lot accept
Component Burn-in	easy	easy	easy	easy	impractical
Pretest	very easy	very easy	easy	easy	impractical
Change & Repair	easy	easy	easy	easy	difficult
Chip availability	excellent	very good	good	good	limited
Multiple Sourcing	excellent	very good	good	good	limited
Footprint Commonality	excellent	very good	good	good	poor
Profile	high	high	moderate	low	low

the single pass over the solder wave. DIPs will be used for discussion purposes. The advantages of through hole mounting technologies compared to high density technologies are as follows:

- The technology is very mature.
- There is excellent component availability.
- Components are relatively cheap.
- Existing design systems can support the technology.
- Electrical test needs are well understood.
- Assembly tests already exist.
- Rework capability exists by using the component leads.
- Systems can be designed with known reliability.
- The disadvantages are as follows:
 - Density is limited by the large component size.
 - Through hole mounting requires the largest volume requirements.
 - Most systems will be heavier.
 - Limited interconnection, 4 to 64 I/O pins.
 - Additional processing required for component lead forming.
 - Requires increased component handling and shipping costs.
 - Low connectivity per unit area.
 - Relatively low routing density can require more layers.

3.3.4 Surface Mount Technology Surface mount technology uses flatpacks, quadpacks, leaded or leadless chip carrier devices and unpackaged devices such as Tape Automated Bonding, (TAB) and Chip on Board (COB) that are usually square (can be rectangular) with terminations on all sides. The surface mount devices are mounted directly to the board or ceramic substrate.

Surface mounting can decrease system volume, weight and increase system speed, but only with certain risks. There is much to be learned about system design, fabrication, and assembly, and this lack of knowledge increases system risk.

3.3.4.1 Leaded Packages Leaded packaged devices are those multiple I/O components that have leads, including the flatpacks, quadpacks, and leaded chip carriers. Typically gull-wing, J, and I leads are commonly used on surface mount devices. SOICs typically use gull-wing leads, while plastic chip carriers have J or I leads (see Figure 3-7).

Benefits and problems exist for each lead form, as shown in Table 3-5.

The advantages are as follows:

- Relatively high densities are available with surface mount technology, with slightly reduced densities with the flatpacks and quadpacks (approximately 3/1 increase over through-hole).

- Most systems will not require a constraining core for thermal management.
- Most systems are lighter than with DIPs.
- High interconnection operating speeds.
- Increased component placement rate.
- High connectivity per unit area.
- Faster electrical characteristics. Surface mount components will increase high-frequency and high-switching performance due to lower inductance, capacitance and resistance coupled with shorter lead lengths.
- High routing density allows for fewer layers.
- Self-centering capability for chip carriers makes components tolerant of some misalignment at assembly.
- The disadvantages are as follows:
 - Relatively new immature technology.
 - Requires the cost and labor for component lead forming.
 - Requires the careful shipping and handling of components due to their leads.
 - Limited component availability.
 - Higher component cost.
 - More complex CAD systems are required.
 - Limited design system function.
 - New assembly technology is required.
 - New board test technology is required.

3.3.4.2 Leadless Packages Leadless packaged devices include leadless ceramic chip carriers. These components are mounted directly to the board without any leads. The advantages are as follows:

- Relatively high densities are available.
- Most systems are lighter than with DIPs.
- A significant reduction in P&I structure size (approximately 3/1) over through hole.
- High interconnect operating speeds.
- Eliminates cost and labor for component leads and their forming.
- Simplifies the problems of component shipping and handling for leadless packages.
- A self-centering capability makes components more tolerant of some misalignment at assembly.
- Increased component placement rate.
- Higher connectivity/unit area.
- Faster electrical characteristics, because the size of the surface mount components will increase high-frequency and high-speed switching performance due to lower inductance, capacitance, and resistance coupled with shorter signal paths.
- Higher routing density uses less layers.

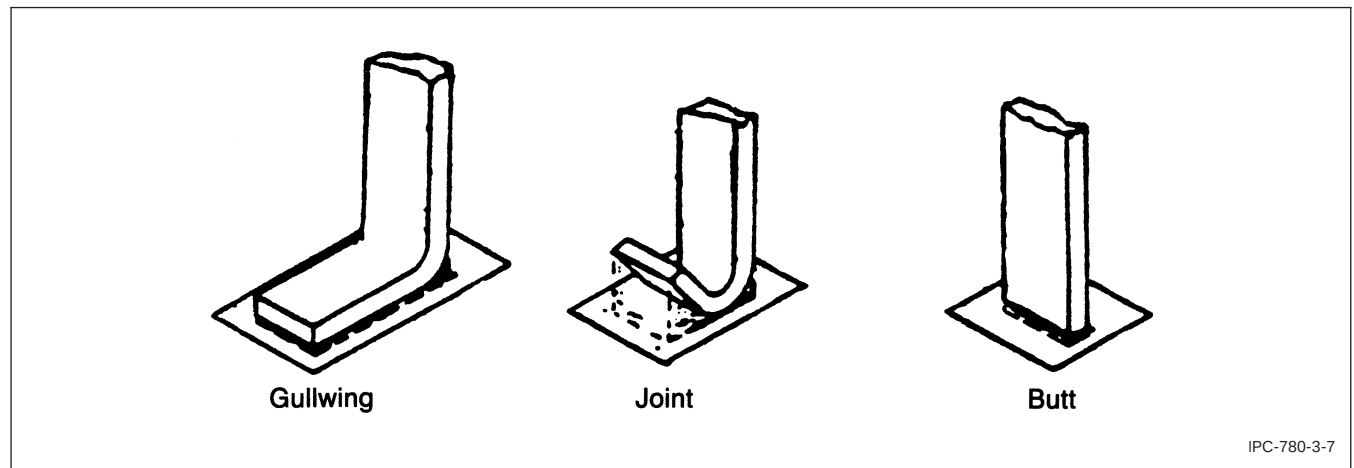


Figure 3-7 Joint geometries

Table 3-5 Joint Geometry Benefits and Problems

Joint Geometry	Benefits	Problems
L Lead (Gull wing)	• Visible solder joint • Top-side electrical probe • Low profile • Easy repair	• Extends package size • Leads easily bent • Difficult to clean under package • Lead planarity
J Lead	• Leads are protected • Minimum board area • Space under body for cleaning	• Lead planarity • Solder joint marginally visible • Difficult to electrically probe • High profile • Correct lead form in IC manufacturing process
I Lead (Butt)	• Minimum board area • Space under body for cleaning • Easy lead formation • Highest shipping density • Best solder geometry	• Difficult to probe • Solder joint marginally visible

- The disadvantages are as follows:
- Relatively new, immature technology.
- Leadless components will likely require a constraining core, with its increased design, fabrication and assembly cost.
- Limited component availability.
- Higher component cost.
- Thermal expansion mismatch problem could cause long-term reliability deficiencies.
- More complex CAD systems are required.
- New assembly technologies are required.
- New board assembly test technologies are required.

3.3.4.3 Bare Chip (Chip-On-Board) Except for hybrid circuits, IC chips have been used almost exclusively in packages supplied by the IC manufacturer. However, during the past several years, bare IC chips have begun to be used, both singly and in multiples, on printed wiring boards in what is referred to as bare chip (Chip-On-Board), or TAB (Tape Automated Bonding), and passive components.

Chip on board components constitute those that do not have a package. The component is mounted directly to the board.

The advantages are as follows:

- Input/Output counts can be as high as 300 or more leads.
- Very low 0.75 mm [0.030 inch] profile COB assemblies can be made.
- Bonding lands can be as small as 0.05 mm [0.002 inches] square on 0.1 mm [0.004 inch] spacing.
- A wire-bonded chip takes about 1/4 of the area of a DIP.
- Long term cost reduction due to the elimination of the package.
- Processing appears to be easily automated.

The disadvantages are as follows:

- There is limited availability of unpackaged chips, both with respect to type and quantity.
- An additional processing step is required to protect the chip from its environment.
- The heat dissipation of bare chips is not as high as that for packaged devices, due to their small package.

- Processing yields must be taken into account when deciding on the number of wire bonds per chip and the number of chips per board.
- Relatively high-production volume is usually required to justify the capital expenditures involved.
- The technology is extremely sensitive to process controls and substrate quality.
- As a relatively new technology, there are undefined risks in reliability, in component availability and in processing capability.

3.3.4.4 Tape Automated Bond (TAB) The most distinctive feature of the TAB system is the carrier tape, which is stored on reels in widths from 8 to 70 millimeters. Like other unpackaged devices, TAB components greatly increases packaging density since there is no chip carrier or package. The chip mounts directly onto the board, eliminating a chip carrier or other mounting device. The advantages are as follows:

- Component density is greatly increased.
- The bonding area on the chip can be hermetically sealed.
- Less gold is required for TAB than for wire bonding.
- TAB provides a means for pretesting and burn-in of the chips prior to their mounting to the board.
- Bonding lands can be as small as 0.002 square inches on 0.004 in center spacing.
- Input/Output counts exceed 300 leads.
- Very low [0.030 inch] profile assemblies.
- The TAB process chips require only a fraction of the board surface required for mounting packaged chips.
- The rectangular TAB lead provides a lower inductance than does a round wire.
- They can be used in other applications such as smart credit cards that are unavailable to packaged devices.
- Relatively lower long term component costs.

The disadvantages are as follows:

- Limited availability of TAB components.
- An additional processing step is required to protect the chip from the environment.
- The heat dissipation of small chips is not as high as that for packaged devices, due to their small size.
- Processing yields must be taken into account when deciding on the number of wire bonds per chip and the number of wire bonds per board.
- Relatively high production volume is usually required to justify the capital expenditures involved.
- The technology is extremely sensitive to process controls and substrate quality.
- It requires specially-designed equipment to match each application, both at the chip and board interfaces.

- In general, TAB chips cannot be purchased economically in small quantities.
- TAB bonding and bonding equipment is rather sophisticated.
- There are several risks involved including the limited component availability, the undefined reliability risks, and the processing capability problems.

3.3.4.5 Direct Deposition Direct deposition provides a rigid interconnecting structure. Films of conductive, resistive, or dielectrically insulative materials can be deposited on the substrate to make conductors, resistors, or capacitors. Circuits are formed by sequentially screen printing or sputtering, pastes on a substrate, then drying, and last firing these pastes conductive, resistive, or dielectric.

The advantages are as follows:

- There is no thermal coefficient of expansion mismatch between the substrate and the component.
- A factory for relatively low volumes can be established without extensive major capital costs.
- The reliability of the direct deposition systems is known.
- Direct deposition may be the best alternative for low quantity systems.
- Monolithic integrated circuit technology can provide semiconductor densities.

The disadvantages are as follows:

- There are limitations in the maximum attainable working frequencies.
- Single-layer circuit density is limited.
- The upper dimension is limited.
- Direct deposition may be expensive for high volume systems.
- The direct deposition technologies are best suited for low volume customer circuits, complex arrays, and applications requiring medium to high power, high voltage and stable, tight toleranced passive components.

3.3.5 Intermixed Technology Intermixed technology combines through hole mounting technology with surface mount technology. It increases the system density by replacing through the board components with surface mount components as available.

The advantages are as follows:

- Increases density by using surface mount components to replace existing DIP components.
- Overcomes limited component availability in existing or new designs.
- Discrete components can be easily accommodated.

The disadvantages are as follows:

- Requires a double assembly process

- Difficult board electrical test.
- Extremely difficult with leadless chip carriers and DIPs as the constraining core for the leadless chip carriers will require special processing for the leaded components.
- Only moderate density increase over through the board components.
- Difficult assembly test.
- Requires increased tolerance control.
- Requires special design considerations in order to assure adequate assembly location tolerance.
- Intermixed technologies increase performance over and through the board technology, including the weight, size, signal speed and signal frequency that are available on surface mounting. It still uses some of the advantages of through the board technology, such as component availability.

3.3.6 Other Considerations

3.3.6.1 Mechanical Tolerances Close tolerance on leads and terminals (for electrical and mechanical connections) is important to assure that components can be mated to the printed boards with minimum difficulty. An assembly with flexible interconnecting leads shouldn't present much trouble, although time for assembly may increase. The problem becomes more critical when components with rigid leads are used on semi-automated or automated machinery in high speed long production runs.

3.3.6.2 Mounting and Interlead Spacing Whether a component is self supported or employs separate fastening devices, shock and vibration characteristics are a primary cause of failure, first for the component itself, then for the component mounting. Interlead spacing and compatibility with preforming operations, such as pig-tailing, pre-solder mounting, and cutting and crimping of leads are important. If automatic equipment is to be used for insertion, prepackaged components can be specified with the following mechanical and electrical operations already performed:

- Components arranged in predetermined sequences.
- Leads straightened, tinned, trimmed.
- Tests (including electrical value, working voltages, shorts, opens, polarity).

3.3.6.3 Prepackaged Components There are now complete systems for processing components which perform these operations and others, including coating and drying (infrared, radiant heat, forced hot air), banding with color codes, printing (electrical values, tolerances, company identifying symbols), deflashing, and packaging. Common types of packaging are reel, bulk, and corrugated cardboard packaging.

To obtain maximum economies from long production runs, prepackaged components can be assembled onto taped

strips in preparation for automatic insertion. One component sequencing system available on the market is controlled by a conventional punched tape. Under programmed control it selects axial-lead components from up to 39 individual input stations and reel-packages them in predetermined sequences. Input stations feeding the machines can contain lead taped components, or magazine and corrugated cardboard packaged parts.

3.3.6.4 Special Mounting Polarized components must be mounted correctly. Symmetrical leads or mounting feet or lugs must be checked (usually special visual checks) to assure that components are correctly assembled on printed wiring boards. This usually is no problem for resistors, but for transformers, some types of capacitors, diodes, and semiconductor devices, incorrect mounting can lead to immediate damage when the first electrical test is made. Transistors and diodes can be ruined in a fraction of a second. It is somewhat commonplace as well as costly to find a blown diode which was carefully inserted and soldered into place backwards.

3.3.6.5 Identifying Components Easily identifiable component value, polarity markings and terminal identity are required to assure minimum maintenance time. A crowded printed wiring board complicates repair and replacement procedures. Just as electronic packaging printed boards have become complex and valuable, so have the rules for assuring their acceptability and repairability.

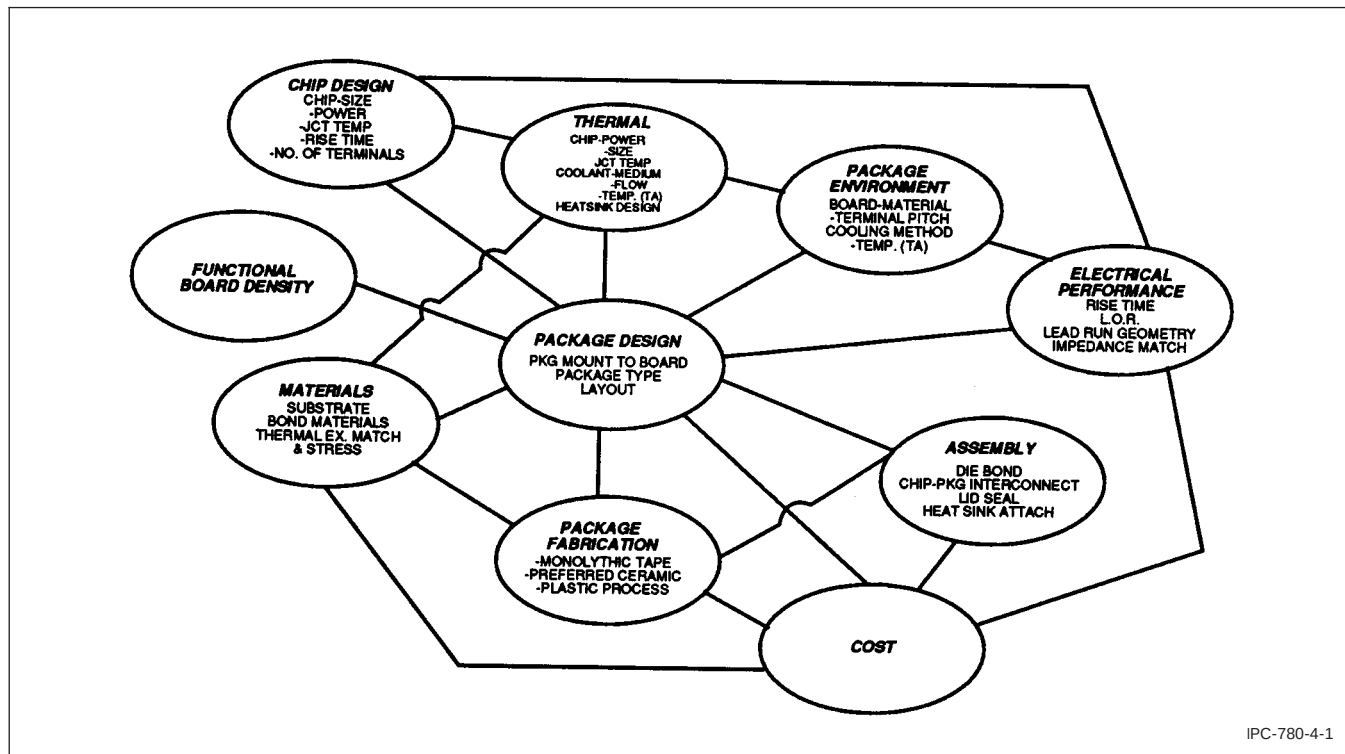
3.3.6.6 Automated Assembly Component adaptability to automatic insertion should also be considered with respect to the number of components to be mounted per board and the total number of boards to be assembled. For very short production runs (prototype, and low number of units), hand or semi-automated assembly may be most economical.

4.0 ELECTRONIC COMPONENT TYPES AND INTERCONNECTION DEVICES

Component packages protect components from the environment, provide communication links, remove heat, and provide a means for handling and testing. With larger, higher-density ICs, these functions will be more difficult to meet. At the same time there will be an emphasis on decreasing the costs of these more-complex packages. This will require increases in functional density and higher-performance designs, as device density increases.

4.1 General Considerations Many factors such as board real estate, environmental conditions, and electrical parameters are important when choosing a component for your specific application (Figure 4-1).

4.1.1 Lead/Termination Finishes Finishes on the leads of leaded component packages and on the metallized terminations of leadless packages, whether the component is



IPC-780-4-1

Figure 4-1 Interrelated package design factors

surface mounting, preserve and assure the solderability of the interconnection surfaces without decreasing the assembly yield or the attachment reliability. The large number of solder joints, which frequently cannot be visually inspected not only because of their sheer numbers but also because they are physically inaccessible, makes it imperative that the solderability of the component I/Os be positively assured prior to assembly. The only lead finish that accomplishes this is fused or reflowed tin or solder. The solder coating can be obtained either by solder dipping or tin/lead plating with a subsequent reflow process. It might be necessary to remove excess solder, which could interfere with the assembly or socketing process, with a hot air knife or similar method.

The above conditions expressly exclude gold plating, since gold forms brittle intermetallics with the tin in the solder causing solder joint reliability problems, and silver plating since silver not only forms very brittle silver/tin intermetallics, replacing most of the lead in the solder, but can form slag-like non-metallic silver/tin compounds which create voids in the solder joints. Caution should be used when leads are coated with tin or tin/lead plating without reflowing prior to assembly because the plating does not always assure solderability.

In addition, some user specifications require fusing of tin plate to eliminate the possibility of tin whisker growth.

The foregoing considerations are more critical for surface mounting than for through-hole mounting. Through-hole

mounting provides considerable margin because of the mechanical anchoring of the leads and the larger solder volumes.

For devices which are exclusively destined for non-soldered interconnections (sockets, connectors, elastomeric), the surface finish coatings depend on the design of the mating contact (normal force, geometry, etc.), the number of insertion/ withdrawal cycles and the service environment. The following is a general guide:

Critical—gold

Intermediate—palladium

Non-Critical—tin/lead

It should be noted that the reliability of a tin/lead application can be increased by lubricating the contact surfaces with proper contact lubricants. Lubricants prevent fret and corrosion that may occur on tin/lead due to changing environmental conditions. For Burn-In applications, hardened gold or a nickel boron contact finish is recommended.

4.1.2 Component Handling Automated assembly for surface mount technology involves packaging considerations as well as reference points on components. The packaging scheme should maintain packaging flexibility while protecting the compliant leads dedicated for surface or through-hole mount. Two basic elements of automated assembly are package choice and conductor registration points.

Several basic packaging schemes are in use today, so give careful consideration to the packaging used for automated

assembly. One common method of packaging is an “egg crate” matrix tray, shown in Figure 4-2. This type of package is usually a molded plastic tray. Keying features molded into the tray insure proper orientation of the product. Features can also be molded to orient the tray to a robotic assembly station.

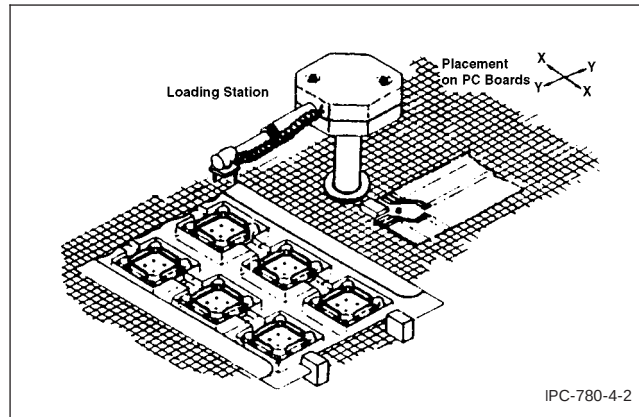


Figure 4-2 Matrix tray

Another form of packaging is taped product. Taped product positively orients the product and simplifies the feeder system at the assembly station. As tape sizes grow and the technology advances, larger taped products will be available.

Tubes or magazines are also used for a variety of component parts. Tubes can be extruded in a wide variety of shapes and sizes. Features insure proper orientation of product, as shown in Figure 4-3. Product is usually gravity fed to the assembly equipment from the tube.

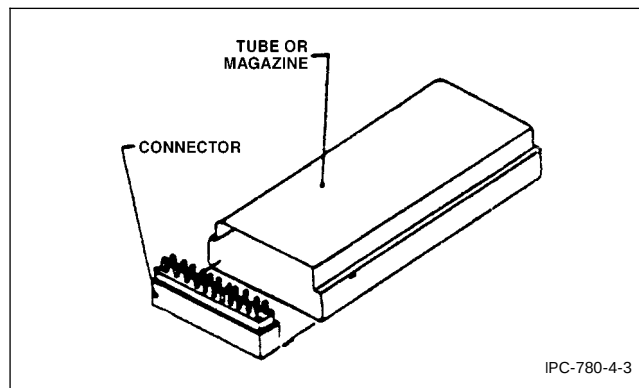


Figure 4-3 Tube or magazine packaging

A very common type of packaging used today is bulk packaging. All bulk packaged product must be properly registered and layered. Figure 4-4 shows a typical bulk packaging layout.

The registration points for an automatic placement head are important for automated assembly. Three basic gripping methods are used for automatic placement. With a vacuum head, the device must be very accurately located in its

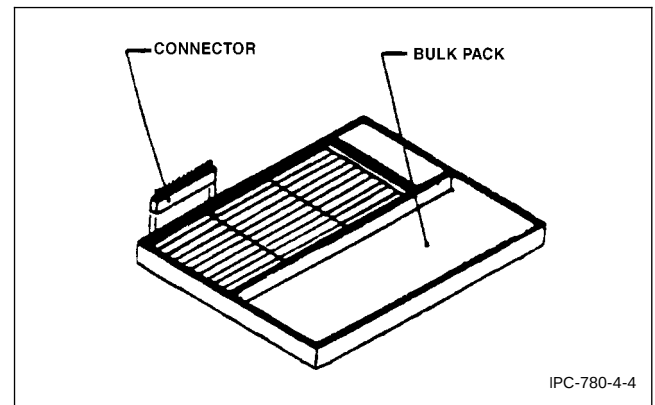


Figure 4-4 Bulk packaging

package or else a secondary alignment method on the assembly machine will be necessary.

A body type grip can be easily incorporated into a connector design. A molded-in locating feature will help register the product to the assembly head.

Another method is a pin-and-hole design. Molded in holes in the connector (as shown in Figure 4-5) mate with pins on the assembly head. A variation of this has the head designed to simulate a mating device in the connector. This method is the most accurate to locate the interconnect device to the assembly head.

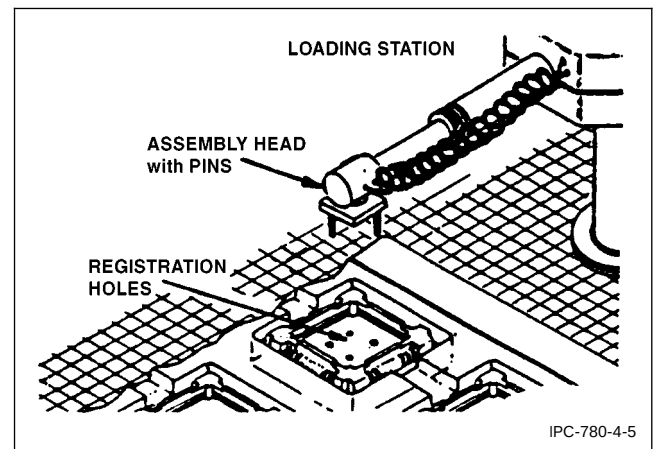


Figure 4-5 Pin and hole locating feature

4.1.2.1 Incoming Inspection Inspection of surface mount product involves these vital areas:

A. Lead Position

- Absolute Position
- Coplanarity
- Relative to Reference Plane

B. Plating

- Composition
- Position
- Quality

C. Housing/Body Material

D. Contact/Lead Material

E. Sampling Plan

- Random
- Lot Size

4.1.2.2 Component Preparation Surface mounting uses RMA fluxes to clean the reflow zone of the contact leg. Be careful to prevent undue exposure of the separable contact interface to the flux agents. A properly designed interconnect device will have stand-offs for adequate draining of cleaning agents used to remove flux.

4.1.3 Precleaning Techniques Printed boards and component leads may need cleaning prior to assembly and/or soldering. If required, surfaces to be soldered should be cleaned as follows:

- Remove grease, oil, and other foreign matter from conductors and terminals with a suitable cleaning solution. Cleaners shall not remove markings or damage the part in any way.
- Remove oxides and varnishes by methods which do not damage leads or parts, nor cause contamination or hinder solder wetting.
- Do not sand blast.
- Remove dust or other loose matter.

4.2 Discrete Component Types Electrical circuit components vary both in type and shape. Often the selection of such components is limited by specification, availability and/or cost. However, many common components, such as resistors and capacitors, are available in several configurations.

Microminiature leadless devices are available in resistor, capacitor, transistor, zener diode, chip form. The chips are placed in a nonconductive carrier and encapsulated in epoxy or hermetically sealed. Metallized surfaces are often plated to permit thermocompression or ultrasonic bonding.

4.2.1 Axial Leaded Perhaps the most common type of printed wiring component is the axial leaded component (see Figure 4-6). These are usually cylindrical and have leads, usually round, exiting from both ends of the component along its axis. Axial leaded components are most suited for automatic insertion. Many resistors, capacitors, and diodes are supplied in this configuration.

4.2.2 Radial Leaded Components Radial lead components are used in many printed wiring assemblies. This type of component has all of its leads exiting from a common side of the component. The actual body shape is variable; two common types of radial lead components are dipped capacitors (Figure 4-7) and transistor cans (Figure 4-8).

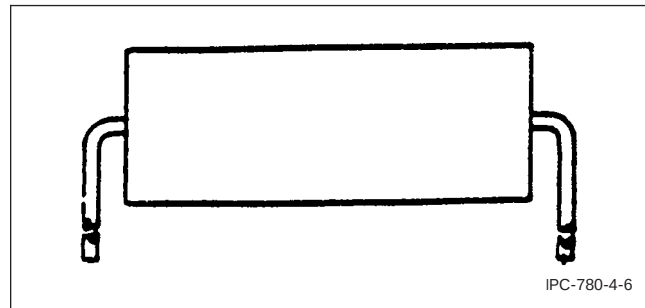


Figure 4-6 Axial leaded component

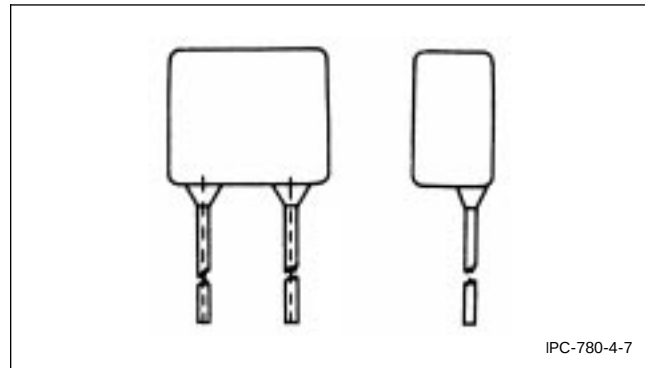


Figure 4-7 Radial lead (dipped) capacitor

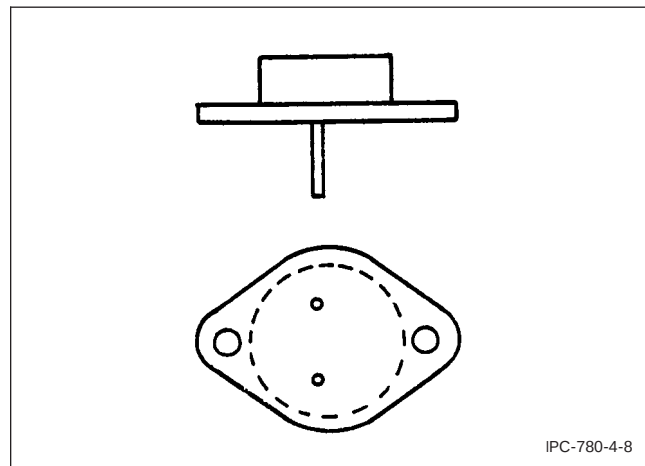


Figure 4-8 Radial lead transistor can

4.2.3 Chip Components (Leaded and Leadless) A discrete-chip component is nothing more than a miniature axial-leaded component minus the leads with metallized areas at the ends. They are available in both cylindrical and flat rectangular shapes (Figure 4-9). Although it is possible to fabricate resistors and capacitors directly on a substrate, this process has severe limitations. Also, it is difficult to obtain close tolerances, the capacitance range is restricted, and close process control is required. Therefore, in most applications, discrete chip capacitors are preferable.

4.2.3.1 Chip Resistors Chip resistors are available either in a wrap-around termination configuration, or a wire bonding configuration. Figure 4-10 shows the two configurations.

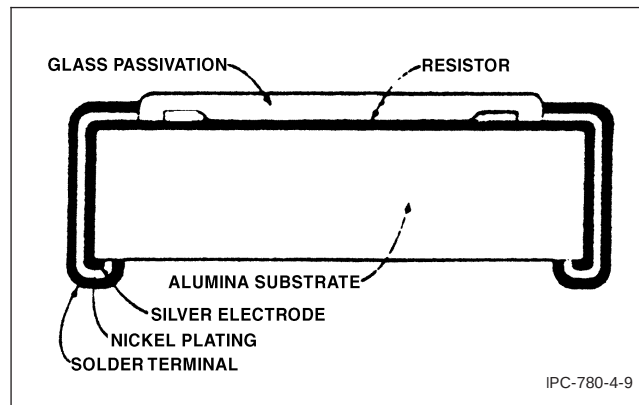


Figure 4-9 Flat rectangular chip resistor

A. Wrap-Around Terminations

This style resistor is face up after attachment so that post-attachment inspection and/or trimming is practical. More importantly, the resistor itself is away from the solder joint and from the attachment pad area.

The metallization of this style is platinum-silver or nickel-tin.

B. Wire Bond Construction

All metallization is on the top of the resistors in this style. Wire bonds make the connections. Attachment to the substrate is with epoxy (although it is possible to have backs of these style chips metallized so they can be soldered to the substrate).

The standard metallization of this style is gold, although other materials can be used if there is a need. The back can be metallized with gold, platinum-gold, or platinum-silver.

4.2.3.2 Chip Capacitors The most popular chip capacitors are ceramic capacitors. Silicon, porcelain, tantalum, and glass capacitors are also available.

Small silicon chip capacitors are available with excellent temperature stability and low leakage current. However,

they are limited in value and have relatively loose tolerances. Ceramic chip capacitors are used more extensively than any other capacitor type because of their ruggedness, ease of handling, wide range of capacitance, high volumetric efficiency and low cost.

The cost of a capacitor in a hybrid is usually greater than the cost of a discrete capacitor mounted on a printed board. So before using capacitors in hybrids, consider the total system cost and size. Also, since large-value chip capacitors are physically large, space must be traded-off.

Chips are built in various sizes and configurations to suit user demand. Configurations include circular feed-thru and multi-feed-thru as well as standard chips. Sizes vary from 1.27 x 1.0 mm [0.050 inch x 0.040 inch] (L x W) to approximately 1.5 x 10 mm [0.60 inch x 0.40 inch] for the larger units. The industry is now standardizing recommended dimensions. Multiple layer ceramic chip capacitors are considered ideal components for surface mounting on printed wiring boards or substrate materials such as alumina for hybrid circuits, and porcelainized metal.

These chips have a monolithic construction: A solid block of ceramic with an enclosed electrode system and metallized ends for lead attachment (Figure 4-11). This solid block is rugged enough to withstand the harsh environment and treatment associated with hybrid circuit manufacturing processes.

Electrodes are given a common terminal by coating the chip ends with a precious metal-glass formulation suspended in an organic vehicle. Consequent drying and firing eliminates the organic components and bonds the ceramic dielectric and glass constituent in the termination. Most common termination materials include palladium-silver alloy, silver, gold, and nickel-tin.

Common package styles are shown in Figure 4-12 while outline drawings of the leadless cylindrical MELF (metalized electrode face) styles are shown in Figure 4-13.

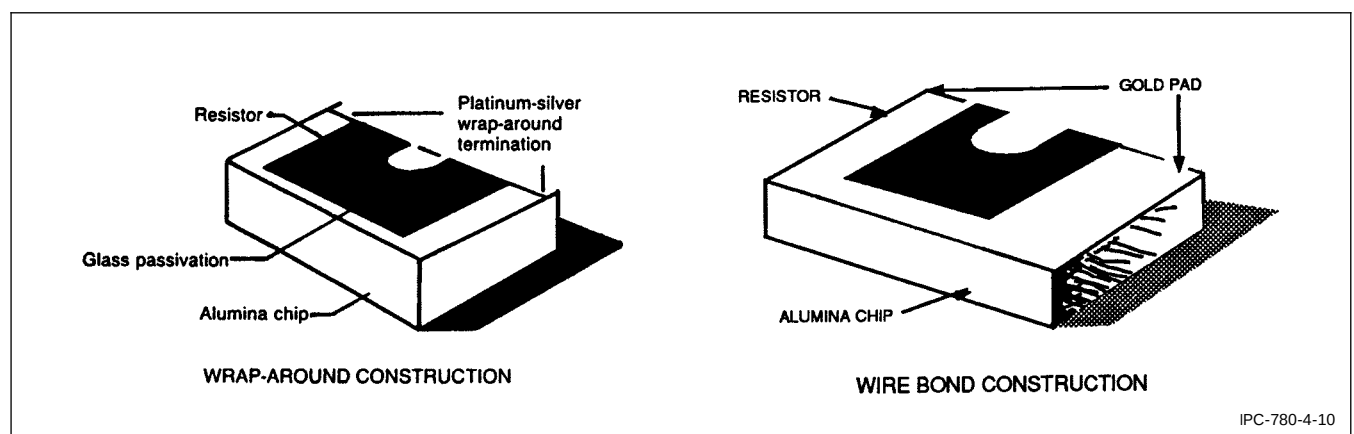


Figure 4-10 Chip resistor constructions

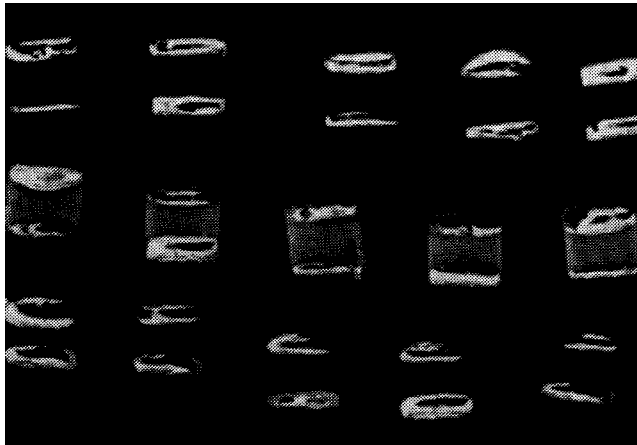


Figure 4-11 Multiple layer ceramic chip capacitor

4.2.3.3 Chip Inductors Chip inductors are available in either ceramic or ferrite variations. Typical wire used is polyurethane/nylon insulated copper magnet wire, ranging in size from 38 AWG to 48 AWG. The terminations are usually molybdenum or nickel, coated with 95% tin, 5% silver solder. Typical outlines are shown in Figure 4-14 and 4-15.

4.2.4 Direct Deposition Integrally-deposited capacitors, in both thick- and thin-film circuits, are used for special applications. However, present state-of-the-art process techniques and compatible dielectrics seriously limit tolerance, capacitance value and dissipation factor control. Therefore, in most cases, add-on chip capacitors are employed in circuits when optimum characteristics are achievable only by unique material systems, fabrication techniques, and geometries.

4.2.4.1 Deposited Resistors Resistor choice depends upon electrical, thermal, and processing capability considerations. For example, integrally-deposited thick- and thin-

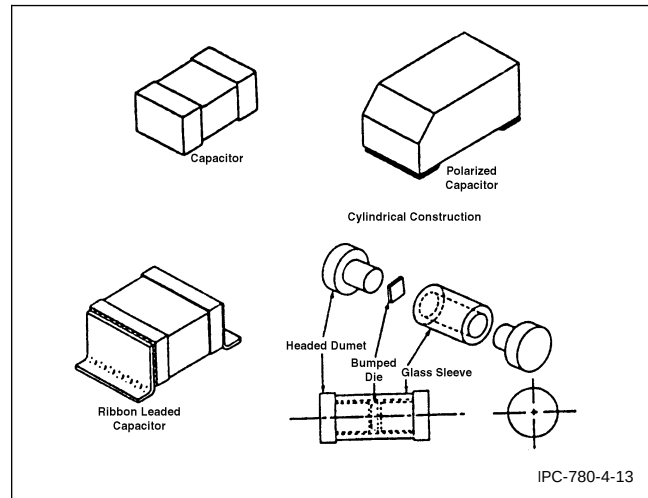


Figure 4-13 MELF body outlines

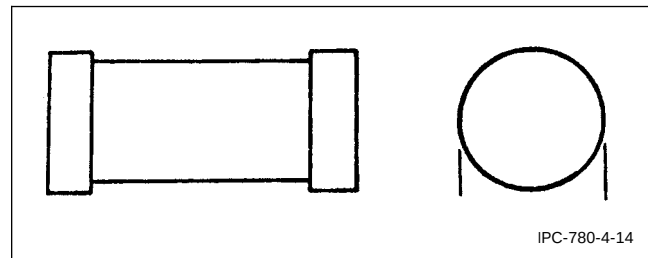


Figure 4-14 A chip inductor

film resistors are frequently used if they meet circuit requirements for precision, temperature stability, etc. The capability to trim- to-value is usually required.

If requirements cannot be met with trimmed integrally-deposited resistors, add-on chip resistors of both thick- and thin-film varieties are available in both discrete and network configurations.

The circuit designer must carefully specify the desired resistor characteristics, such as ohmic value, tolerance,

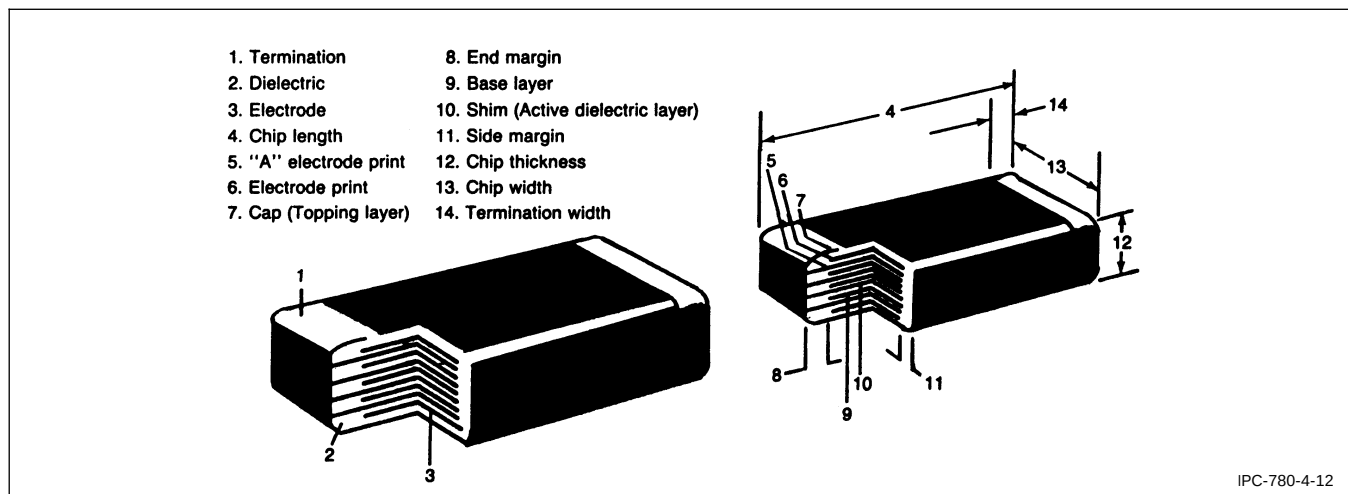


Figure 4-12 Chip capacitor package

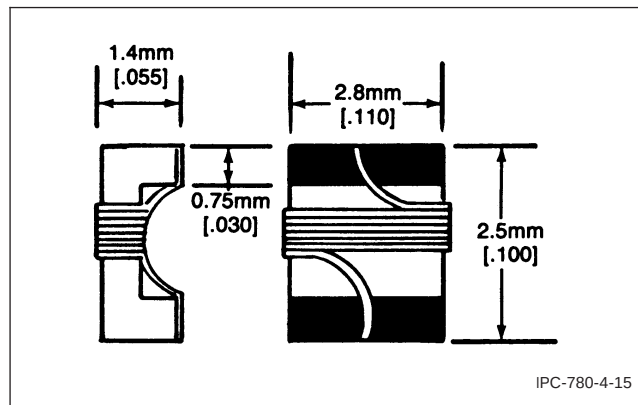


Figure 4-15 Typical surface mount inductor

temperature range/coefficient, and power dissipation. However, the hybrid- circuit designer has the additional problem of determining what temperatures the resistor may actually experience in use.

The importance of load-life characteristics of the resistors depends upon the end use of the circuit.

Thick-film chip resistors are available in standard values and tolerances from a size of 1.27 x 1.27 x 0.5 mm [0.050 inch x 0.050 inch x 0.020 inch] at 0.1 W dissipation capability to increased dimensions in proportion to higher power dissipation capabilities. Thin-film (tantalum nitride and nickel-chromium) chip resistors are available in a wide variety of networks or discrete values. Thin-film resistors can be obtained in several configurations with sizes from 0.4 x 0.3 mm [0.017 inch x 0.011 inch] for a single-value resistor. Some configurations include several different values on a larger chip.

Resistive materials provide a variety of characteristics in a circuit, and these materials are considered separately as passive elements in the circuitry. Table 4-1 compares the properties of thick-polymeric and thin-film resistors.

Table 4-1 Film Resistor Characteristics

Parameter	Units	Thick Film		Thin Film	
		Ceramic	Polymer	Ni-Cr	Tantalum Nitride
Resistivity Range	Ohms/Sq	1–1000 M	10–100K	10–300	5–500
Temperature Coefficient of Resistance	PPM/°C	± 50–300	± 250–1000	± 0–50	± 40
TCR Tracking	PPM	10	50	1	1
Power Handling Capacity	Watts/in ²	≤100	25	≤100	40
Thermal Stability (150°C/1000 hrs.)	%ΔR	≤± 0.25	≤± 2	≤± 0.1	≤± 0.2
Voltage Coefficient of Resistance	PPM/V	0.5–5	25–100	0	1
High Voltage Stability	%ΔR	<± 0.5	≤± 2	≤± 1	≤± 1
Noise	dB	–35 to +20	0 to +35	<–30	<–10
Trim Stability	%ΔR	≤± 0.25	≤± 2	≤± 0.01	≤± 0.01
Load Life 25°C–1000 hrs (rated power)	%ΔR	≤± 0.25	≤± 3	0.1	≤± 0.1
Aging Stability 25°C/50% RH/1000 hrs.	%ΔR	≤± 0.25	≤± 2	≤± 0.1	≤± 0.1
Conductor Compatibility	—	Au, Ag, Cu, PdAg, PtAg	Au, Ag	Au, Cu, Al	Au, Cu, Al

4.2.5 Switches Switches in surface mount configurations are now becoming available. DIP, slide, pushbutton, rotary DIP and toggle switches withstand the temperatures of batch or mass soldering as well as immersion cleaning. SMD switches usually have “I” lead, “J” lead or “L” lead. To ensure solder connection reliability, the lead configuration must comply with thermal expansions while providing a mechanically sound solder joint during switch actuation.

4.2.6 Other Devices Other passive devices are being adapted to surface mounting applications. One noteworthy example is a surface mount sealed single-turn cermet trimmer in a vertical and horizontal style. This particular product is available in a 1K to 200K ohms resistance range. Figure 4-16 shows an outline of this trimmer.

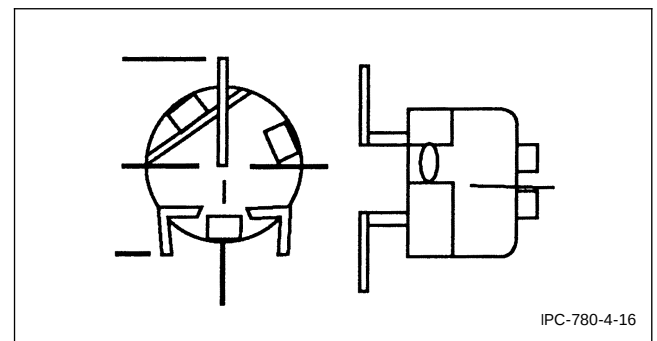


Figure 4-16 Surface mount cermet trimmer

4.3 Semiconductor Package Types There are many packages for semiconductor chips (Table 4-2).

Standard mechanical outlines have been established for these devices by JEDEC (Joint Electron Device Engineering Council). Complete outlines can be found in JEDEC Publication 95.

Table 4-2 Typical Integrated Circuit Packages

LSI Package Type	Maximum Number of Leads	Method of Attachment	Removal from Board	Board Area, Including Leads (in.)	Hermetic Seal
Co-fired ceramic DIP	64	wave solder or socket	difficult	2 x 0.600 (40 lead)	yes
Cerdip	40	wave solder or socket	difficult	2 x 0.600 (40 lead)	yes
Plastic DIP	40	wave solder or socket	difficult	2 x 0.600 (40 lead)	no
Co-fired ceramic chip-carrier	150 @ 0.050"	socket	simple	0.460 x 0.430 (40 lead)	no
Leaded chip carrier	156 @ 0.050"	reflow-solder	simple	0.770 x 0.770 (36 lead)	yes
Minipak	26	reflow-solder	simple	0.500 x 0.500 (28 lead)	no
Flatpack with leads out all four sides	64	reflow-solder	simple	approx. the same as leaded chip carrier	yes
Ceramic substrate with clips on 4 sides	up to 156	reflow solder or socket	simple	0.650 x 0.650 (44 lead)	yes
Plastic pre-molded chip carrier	up to 156	reflow solder or socket	simple	0.650 x 0.650 (44 lead)	no
Leadless inverted device (LID)	40	reflow-solder	simple	0.450 x 0.450 (40 lead)	no
Film carrier	40 to 64	reflow-solder or wire-bond	simple	about 0.312 x 0.132 (40 lead)	no

4.3.1 Multileaded Radial Type Components The general term for a transistor outline component is a "TO" can (see Figure 4-17). This type of component consists of a hermetically sealed can with up to twelve round leads exiting from the bottom of the device (usually in a circular pattern).

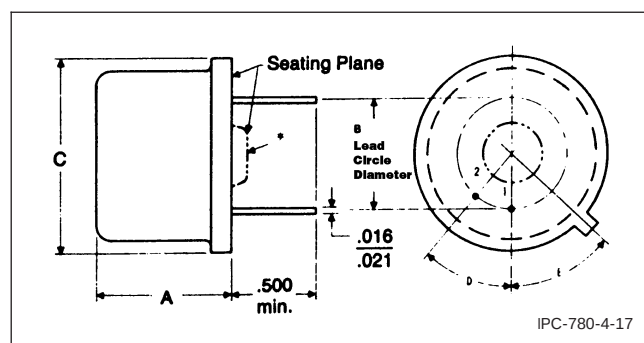


Figure 4-17 "TO" can outline drawing

Available tooling, hermetic sealing, and a rugged construction made the can with 10 or 12 leads a natural first IC package. It requires special punching dies or drilling templates for the 5.84 mm [0.230 inch] diameter pin circle, making it difficult for users to conform to carrier requirements for double-sided printed wiring and internal or core planes for voltage and ground distribution. Printed land and line technology does not solve this problem, because of lead geometry.

4.3.2 Small Outline Packages Despite all of the recognition given to chip carriers, another relatively-new entry

in the microminiature packaging arena, the small outline (SO) package, is finding its applications. Resembling miniature versions of molded-plastic DIPs, SO transistors (SOTs) and SO integrated circuits (SOICs) are quickly gaining acceptance at several major semiconductor companies.

4.3.2.1 Small Outline Transistor package (SOT) One of the first active devices in packaged form for surface mounting was the SOT device. Plastic encapsulated, three terminal devices with leads formed out from the body were surface mounted to overcome some of the problems and difficulties in handling chip transistors. Common SOT packages are the SOT-23, SOT-89 and SOT-143. In general SOT packages are used with diodes, transistors and small I/O devices.

The SOT-23 package is the most common three leaded surface mount device configuration. Figure 4-18 shows this device.

SOT-89 packages are used for high power devices where heat transfer to the supporting printed wiring board is important. Figure 4-19 shows this device.

The SOT-23 package had several redesigns by some semiconductor manufacturers. The dimensional characteristics are designed to meet differing needs of both the hybrid and surface mount industries. Figure 4-20 shows low, medium, and high profile SOT-23s. Each of these SOT-23s is intended to provide different clearances away from the printed board or hybrid substrate.

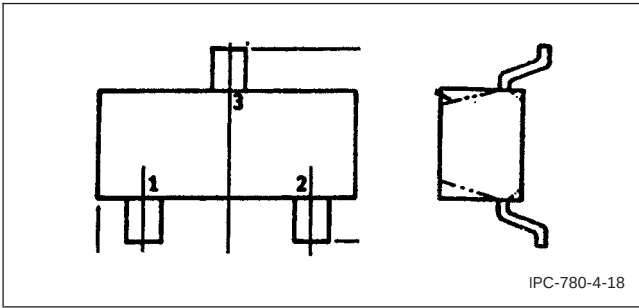


Figure 4-18 SOT-23 package

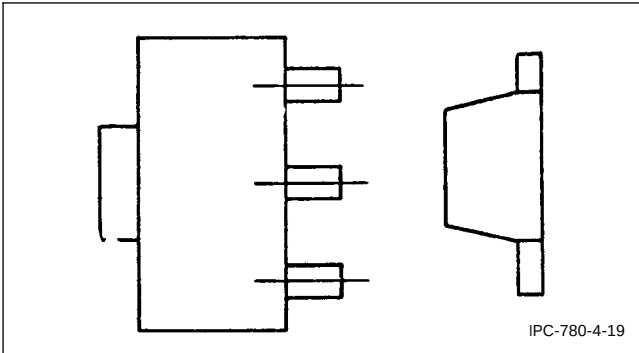
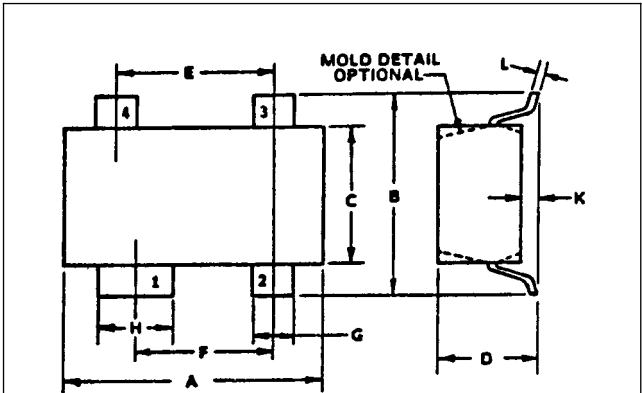


Figure 4-19 SOT-89 package

SOT-143 parts are for dual diodes and Darlington transistors. Figure 4-21 provides the outline and dimensions for the SOT-143.

4.3.2.2 Small Outline IC Packages (SOIC) The SO or small outline package was conceived for the watch industry. There are standards for the SO package established by the Joint Electron Device Engineering Council and by EIA Japan. The standards have some minor differences so unfortunately at this time no international standard for the SO package exists. The package style has become more widely used in hybrid applications in the past few years for active devices with up to 40 terminals.



Note: All dimensions apply after solder coating

Dimension	Min.-Max. Dimensions
A	2.80–3.10 mm [0.110–0.122 inches]
B	2.10–2.60 mm [0.083–0.102 inches]
C	1.20–1.70 mm [0.047–0.067 inches]
D	0.85–1.20 mm [0.033–0.047 inches]
E	1.80–2.00 mm [0.071–0.079 inches]
F	1.60–1.80 mm [0.063–0.071 inches]
G	0.37–0.48 mm [0.015–0.019 inches]
H	0.78–0.88 mm [0.031–0.035 inches]
K	0.05–0.25 mm [0.002–0.010 inches]
L	0.09–0.15 mm [0.004–0.006 inches]

Figure 4-21 SOT-143 dimensions

The SOIC is manufactured in 150-mil wide and 300-mil wide versions. A 300-mil version is called small outline—large (SOL) and offers a larger die cavity. Figure 4-22 shows the overall outline of a 16 pin SO and SOL package, basically a dual-in-line package (DIP) with leads on 1.27 mm [0.050 inch] centers that are extended and formed similar to a flat pack for surface mounting.

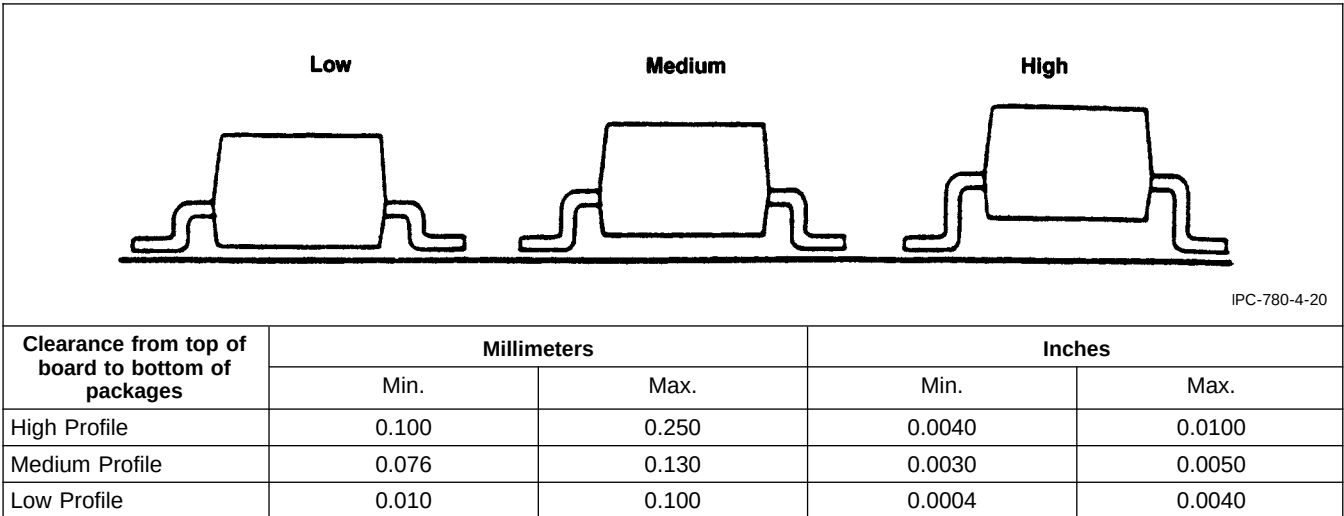


Figure 4-20 SOT-23 comparisons

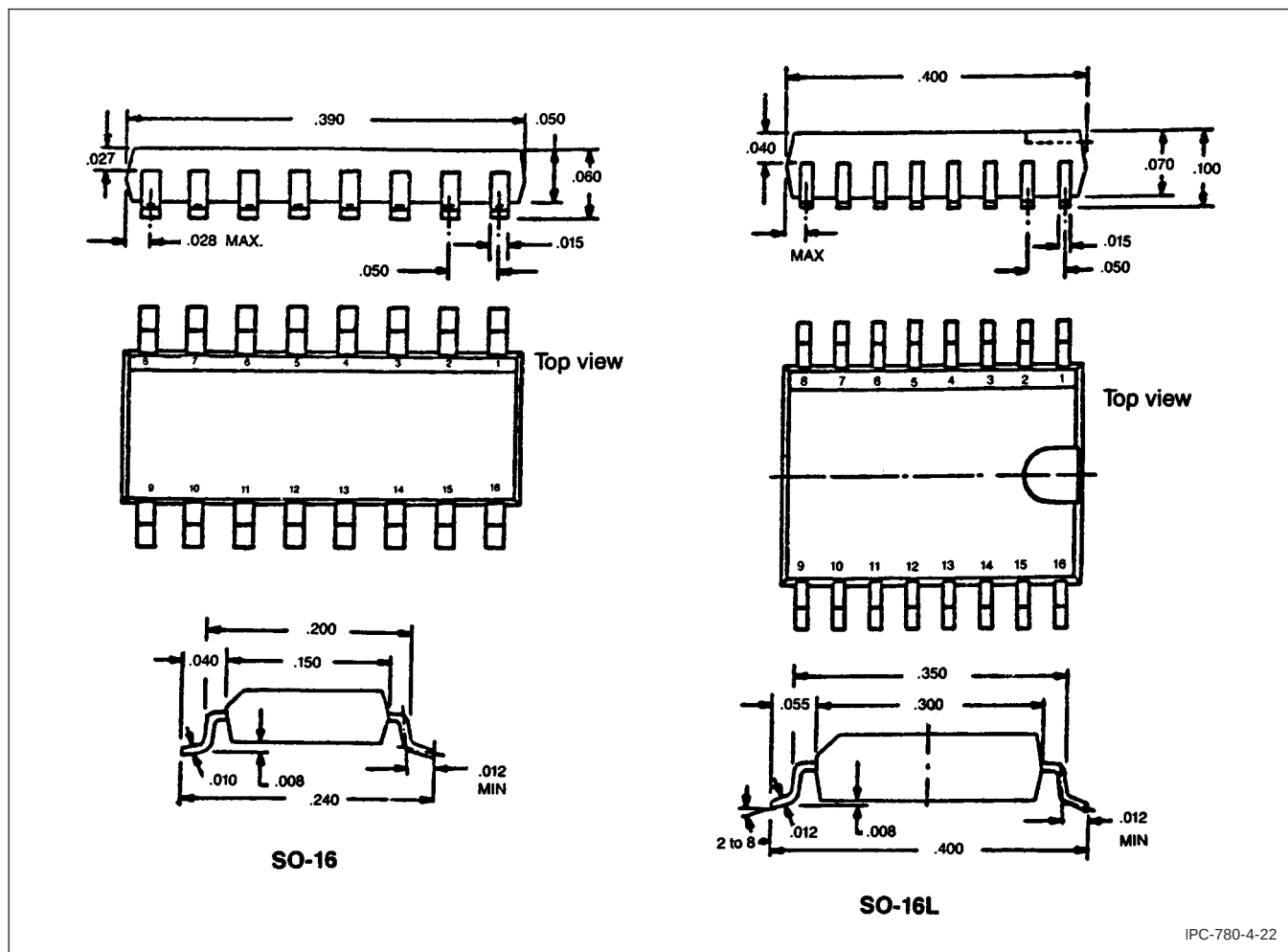


Figure 4-22 16-pin SO and SOL outline

A major advantage of this package style is that it can be pretested prior to substrate assembly while still offering relatively high density. It is smaller, lower, and weighs less (1/6 to 1/10 as much) than a DIP. The package has orientation features on the edge of the package to aid in handling and identification.

4.3.2.3 Small Outline Package J Lead (SOJ) A small outline package with J leads has been proposed as a JEDEC standard for the next generation of memory packages. The small outline J (SOJ) package has leads on two sides, similar to a DIP. In some applications, the leads on each side are split into two groups separated by a large center gap. The gap provides a space for power traces to pass under the package. An outline drawing for this package is shown in Figure 4-23.

The SOJ package takes advantage of chips having parallel address or data line layouts. For example, memory ICs are often used in multiples and bus lines connect to the same pin on each chip. Memory chips in SOJ packages can be placed close to one another because of the parallel pin layout and the use of "J" leads. With high capacity memory

systems, the space savings can be significant. The present proposed outline includes terminal counts of 14, 16, 18, 20, 22, 24, 26 and 28.

4.3.3 In-Line Packages Configurations

4.3.3.1 Dual In-Line Packages (DIPs) The dual in-line multiple lead component (DIP) has leads pointing downward, ready for insertion into holes in a printed board.

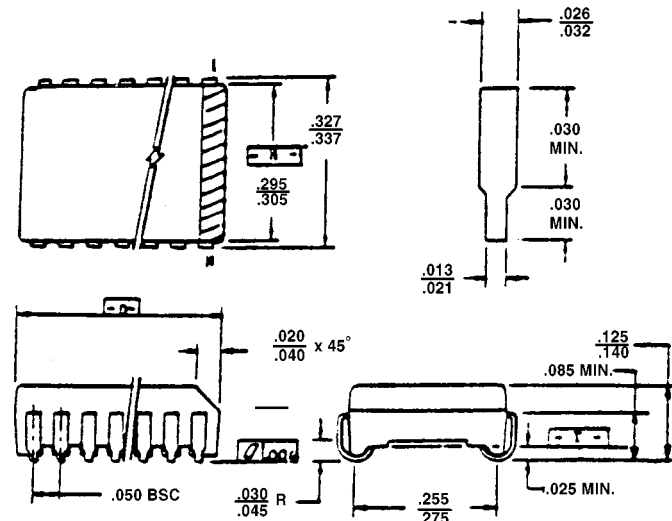
A DIP is made of metal, ceramic, glass, plastic, or a combination. Leads, body, and glass sealing are designed to make this a rugged package. Lead configuration (shoulder) provides a stand-off feature. Leads formed into a $10^\circ \pm 5^\circ$ provide retention of the components.

The standard DIP has 2.54 mm [0.100 inch] pin spacing in each row of pins with the rows spaced 7.6, 10.2, 15.2 and 22.9 mm [0.300, 0.400, 0.600 and 0.900 inches] apart, depending on the lead count. Each additional two pins add an additional 2.54 mm [0.100 inch] length to the DIP. A typical DIP is shown in Figure 4-24.

A very large DIP can supply the more-than-40 pins that most complex IC chips demand. However, since 75 mm [3 inch] long components take up a lot of space, designers

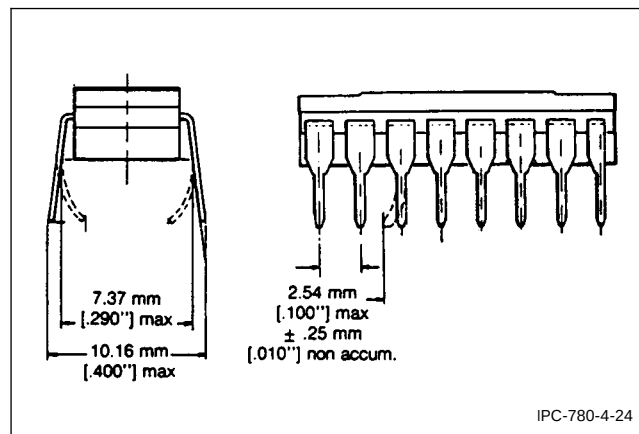
No. of Terminals	D	
	Min.	Max.
14	.371	.379
16	.421	.429
18	.471	.479
20	.521	.529
22	.571	.579
24	.621	.729
26	.671	.679
28	.721	.729

Note: All dimensions in inches



IPC-780-4-23

Figure 4-23 Proposed JEDEC outline for SOJ packages

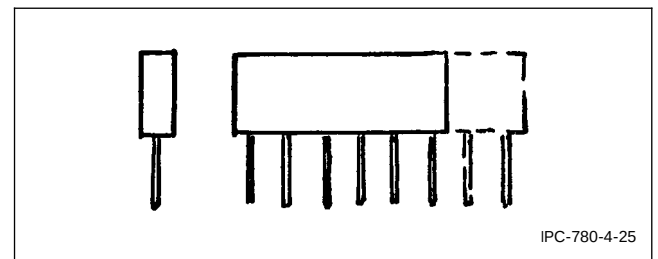


IPC-780-4-24

Figure 4-24 Typical DIP outline

turning to the more exotic and more appropriate packages. To utilize all of the high performance of large-scale integration (LSI), the package must hold 8.9 mm [0.350 inch] square chips with lead counts up to and over 80, while dissipating as much as 5 watts of power. Until recently, DIPs have housed about 95% of all LSI. However, molded-plastic DIPs usually have no more than 40 leads and only at the lower, metal-oxide-semiconductor (MOS) levels of power dissipation.

4.3.3.2 Single In-Line Packages (SIPs) The single in-line (SIP) components are similar to the dual in-line (DIP) components with leads that exit the component body in-line 2.54 mm [0.100 inch] apart center to center, but in a single row pattern rather than the dual row (square) pattern of the DIP (see Figure 4-25). As with DIP components, SIP component lead spacing is also artwork restrictive.



IPC-780-4-25

Figure 4-25 Typical SIP outline

4.3.3.3 Quad In-Line Package (QUIP) The QUIP is similar to the dual in-line package, however, leads are in a staggered configuration. Several I/O counts and lead spacing variations exist. Complete outline drawings exist in JEDEC Publication 95. Figure 4-26 shows a typical 14 pin QUIP.

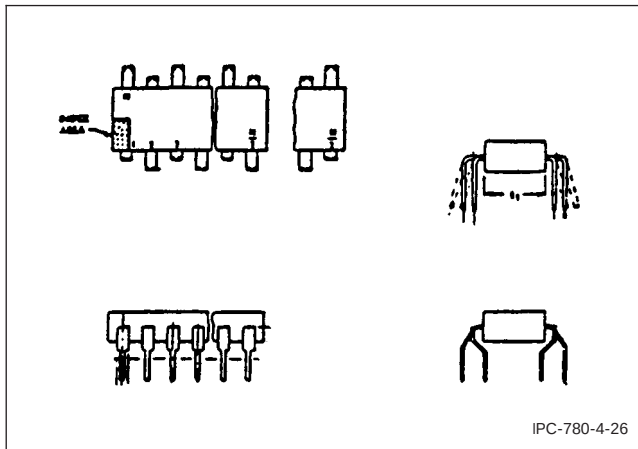


Figure 4-26 Typical QUIP outline

4.3.3.4 QUIP Package The QUIP is similar to the Dual In-Line Package, however, leads exit from all four sides of the package. Standard outlines exist for 52 I/O and 64 I/O variations. Figure 4-27 shows a typical 64 I/O configuration.

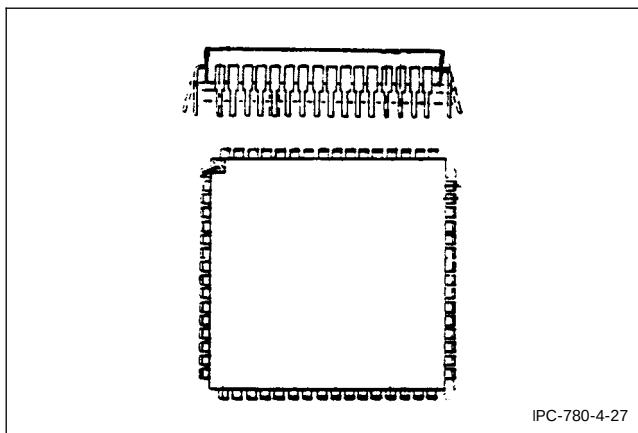


Figure 4-27 Typical QUIP outline

4.3.4 Ribbon Multileaded Component Types (Flat Packs and Quad Packs) Flat packs are widely used for high reliability application (primarily military). They are available with 14 to 84 and more terminals. The typical flat pack has leads on both sides; the leads exit the body of the package on 1.27 mm [0.050 inch] centers. They are formed in a gull-wing fashion and surface attached to a printed wiring board. Figure 4-28 shows typical flat pack designated by JEDEC. Flat packs are usually metal, ceramic, glass, or combinations of these materials and are hermetically sealed. Flat packs and quad packs are similar to SO devices, but with a number of important differences. Flat packs are normally supplied by the vendors with the leads extending straight out from the body on two opposite sides, or from all four sides. Although this requires the user to form the leads, this permits either surface mounting or through-the-board mounting techniques. (SO device leads are preformed by the vendor for surface mounting only.)

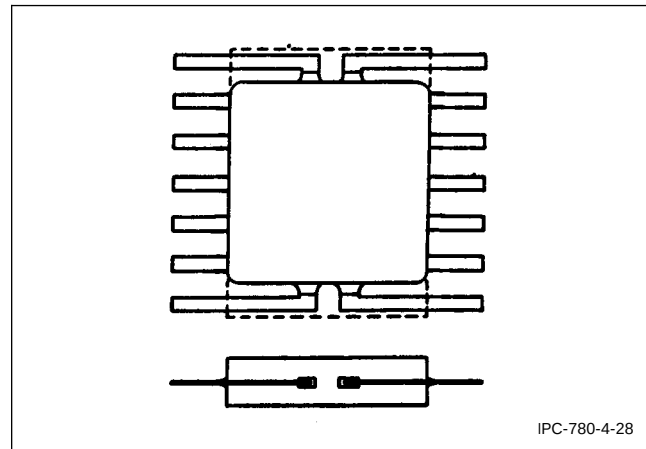


Figure 4-28 Flatpack outline

Flat packs are available in both hermetically sealed and molded plastic styles. Hermetically sealed devices are packaged in metal, ceramic, glass, or combinations of these materials. SO devices are normally available only in molded plastic cases.

Flat pack multiple lead components are highly suitable for high density printed board applications due to their close lead spacing 1.2 mm (0.050 inch) and small body sizes. The wide variety of flat pack configurations permits a wide variety of mounting methods.

The basic flat pack mounting techniques can be categorized as either the through-the-board or surface. These can be further divided into the following:

- Through-the-board, unclined lead
- Through-the-board, clinched with circumscribing full land
- Through-the-board, clinched with offset land
- Surface post
- Surface land
- A number of discrete devices (transistors and diodes) are also available as ribbon leaded devices. Most of these have been designed specifically for high frequency, strip-line mounting.

4.3.4.1 Part Type Description

A. Flat Pack Device Type

One of the smallest multiple lead components is the flat pack. The body of these components can be as small as 3.18 mm [0.125 inch] wide, 6.35 mm [0.250 inch] long, and 0.79 mm [0.031 inch] thick. The component leads are normally flat ribbons 0.5 x 0.25 mm [0.020 x 0.010 inch] or smaller, and are located on 1.27 mm [0.050 inch] centers.

Flat packs are secured several ways:

- Form leads to fit a staggered hole-land pattern, using pot or wave soldering.

- Weld or solder leads to lands or tabs.
- Form leads with stress relief bends to protect the glass seals, then weld or solder to lands or tabs that are 0.79 mm [0.031 inch] wide x 1.9 mm [0.075 inch] long. In an alternate method, all leads are simultaneously solder coated and then reflow-soldered with semiautomatic insertion equipment. As with all metal cased components, flat packs must be insulated when placed over conductive traces. Unless the user has control over the particular package material, it may be appropriate to provide insulation between the bottom of the flat pack and any conductive traces, regardless of the case material being used.
- Nonstandard shipping containers for flat packs have caused problems. Another flat pack problem is the very high automated assembly cost, compared to other packages, due to the fragile leads and the special care required in assembly.
- Flat pack devices are usually similar to the outline depicted in Figure 4-28. Dimensions of standard flat pack devices are listed in MIL-M-38510 and in JEDEC publication 95.

B. Quad Pack Device Type

Four-sided flat packs, i.e., quad packs (Figure 4-29), are used to increase the I/O capacity of the device without significantly increasing the component size. In this respect, they closely resemble leaded chip carriers.

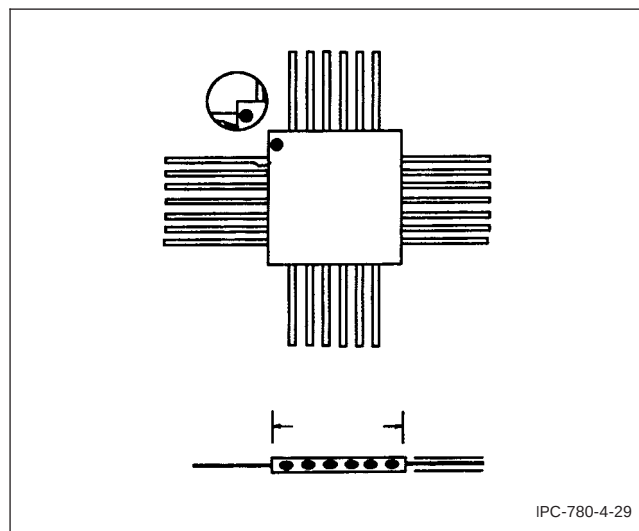


Figure 4-29 Quad pack configuration

C. Discrete Device Type

Ribbon leaded discrete devices are also very small leaded discrete devices. The case is normally no larger than necessary to provide mechanical support for the leads. These devices were originally developed for use on stripline-boards, where the part body is recessed into the board such that the part leads are aligned with the stripline circuit traces.

The special characteristics of these devices—small lead inductances, low capacitance between leads, and small physical size—have made these devices useful in non-stripline applications also. Figure 4-30 is typical of the ribbon leaded transistors available. JEDEC publication 95 lists the dimensions of ribbon leaded discrete devices.

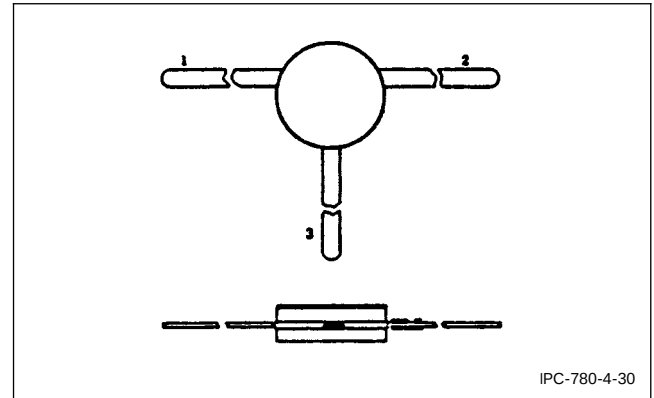


Figure 4-30 Typical ribbon leaded transistor

4.3.5 Chip Carriers (Leaded and Leadless) Chip carriers are available in many constructions and materials comparable to dual-in-line-packages (DIPs). Plastic premolded chip carriers, recommended primarily for commercial application, share the advantages and drawbacks of a plastic DIP: Low cost, nonhermetic, 0°C to 70°C operating temperature range (sometimes -25° to 85°C), and nominal environmental protection.

Glass frit sealed chip carriers are similar in construction to ceramic DIPs (Cerdips). They are hermetic, environmentally testable, and cost more than the plastic construction but less than the solder sealed carrier. They are useful for some high reliability packaging applications, but may require special handling to avoid damage.

Solder-sealed 3-layer chip carriers are the equivalent of solder-sealed DIPs. These hermetic devices are the most expensive chip carriers because of high gold content. However, seal temperature is lower than that of the lower cost Cerdip type, and the package accepts all high-reliability processing required for MIL-M-38510.

There are two types of plastic chip carriers: premolded and postmolded. Both types are composite metal/dielectric assemblies that include a conductor lead frame and a molded insulating body. The premolded chip carrier has one or more apertures for mounting microelectronic elements, while the postmolded chip carrier is a complete assembly without apertures. All necessary plating operations are performed by the package manufacturer to eliminate plating or tinning by the user. The ceramic chip carrier is usually constructed from a 90% to 96% alumina or beryllia base, using a single layer or multilayer co-fired metallization process originally developed for the DIP. The metallization is generally a trimetallic system.

refractory metal (such as tungsten or molybdenum, nickel and gold).

4.3.5.1 Centerline Families

A. 50-Mil-Center Family

Chip carriers have been used since the early seventies and became popularized, particularly for LSI applications, with the standardization activities of the Joint Electron Devices Engineering Council. Through an activity begun in 1976, certain chip carrier packages were approved as JEDEC standards in April 1980. The standard defines various styles and sizes of both leadless and leaded packages. All have their input/output terminals on the perimeter of the package on 1.27 mm [0.050 inch] centers.

The 50-mil-center family demonstrates the concepts developed for the standard. Figure 4-31 shows the variations of the 50-mil center family. There are four leadless types. Type A, B, C, D, E and F, which mount in different orientations depending on the type, the mounting structure, and the preferred thermal orientation. The leadless packages are typically ceramic packages with hermetically sealed metal or ceramic lids.

When chip leads are added to the leadless types the chip carriers become the Leaded Type B package. The other leaded package is the Leaded Type A, which was initially a plastic premolded package, but can now use other constructions.

The 50-mil-center family, which includes both leadless and leaded devices, can mount on a common mounting pattern (Figure 4-32). They may be directly attached to the mounting structure or plugged into sockets. Figure 4-33 shows some of the common features of the 50-mil family. One basis restriction is that there shall be no terminals in the

corners of the package. There are a number of common sizes in the 50-mil-center family; they include 28-, 44-, 52-, 68-, 84-, 100-, 124- and 156-input/output terminal sizes. The Leadless Type C also includes 16-, 20-, and 24-terminal packages.

Two new additions to this family include rectangular variations designated type E and type F. Type E consists of either a 28 or 32 I/O device. The type F family has two 18 I/O variations (one has a longer ceramic) and a 20 I/O variation. Figure 4-34 details these types.

B. 40-Mil-Center Family

The 40-mil family is of ceramic leadless construction and originally intended for direct attachment to ceramic P&I structures. The standard includes square chip carriers with 16-, 20-, 24-, 32-, 40-, 48-, 64-, 84-, and 96- input/output terminals.

In addition, JEDEC recently proposed a rectangular variation of this package with 32 I/O and staggered terminals.

C. 25-Mil-Center and 20-Mil-Center Families

The JEDEC 50-mil and 40-mil centerline standard chip carriers are inefficient for 100 to 124 terminal counts. To solve some limitations of JEDEC chip carriers for packaging LSI and VLSI circuits with high terminal counts, an ad hoc task group was established through the IEEE Computer Society's Technical Committee on Packaging in late 1980. The group agreed on a number of basic requirements:

- Both 0.5 and 0.635 mm [0.020 and 0.025 inch] centerline spacing chip carrier packages will be used and should be standardized.
- Ceramic and plastic packages should be standardized following the compatible mounting concept of the JEDEC 1.27 mm [0.050 inch] standard packages.

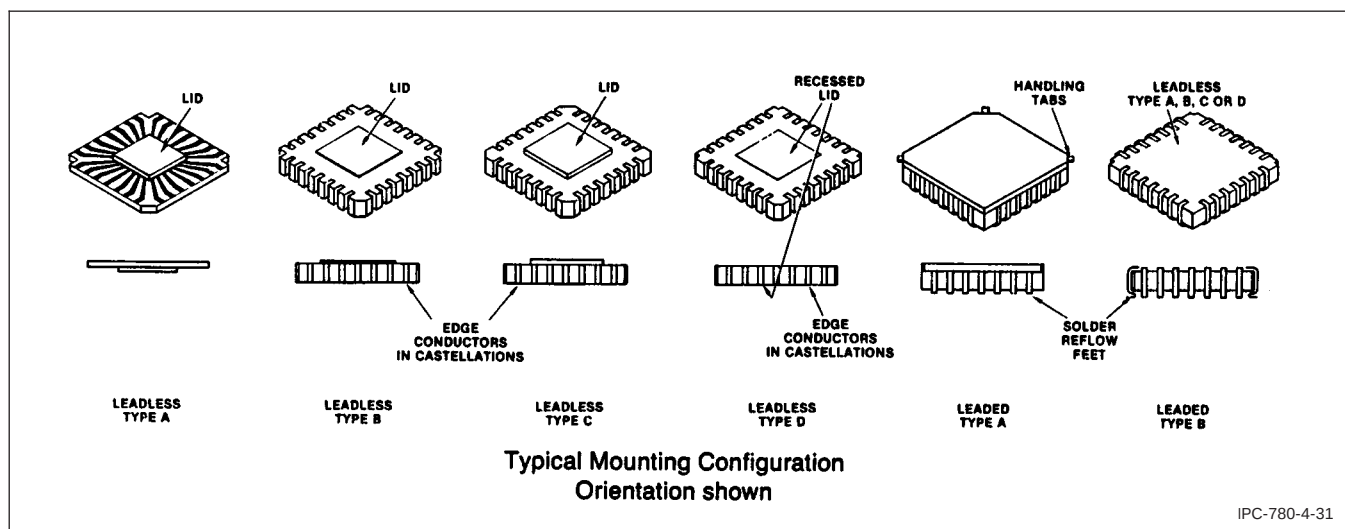


Figure 4-31 The 50-mil center JEDEC packages

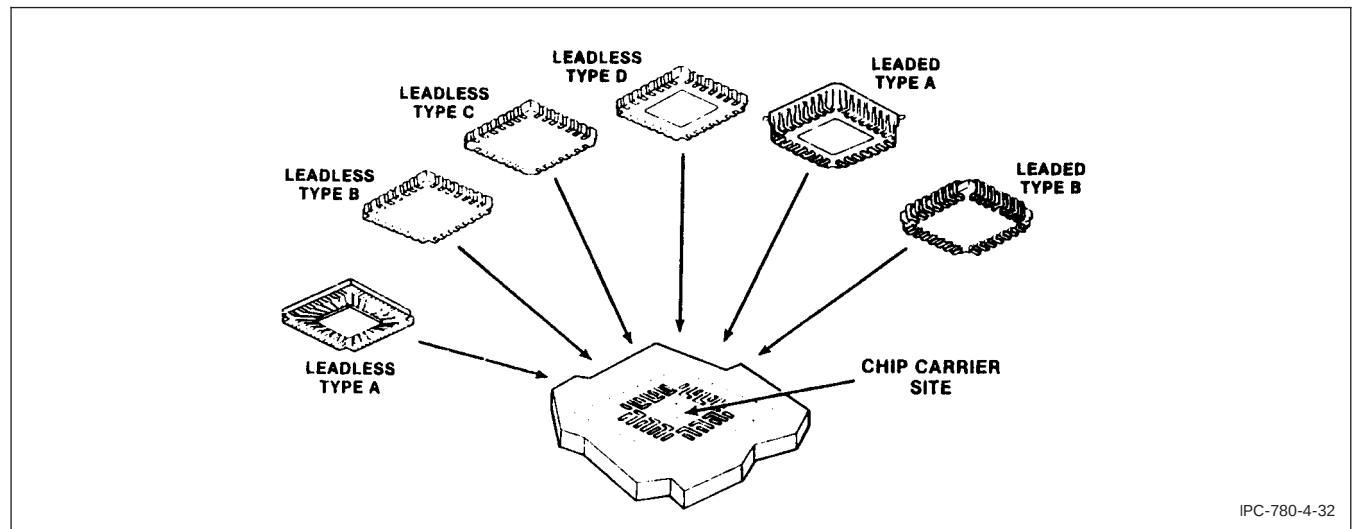


Figure 4-32 Mounting compatibility of JEDEC packages

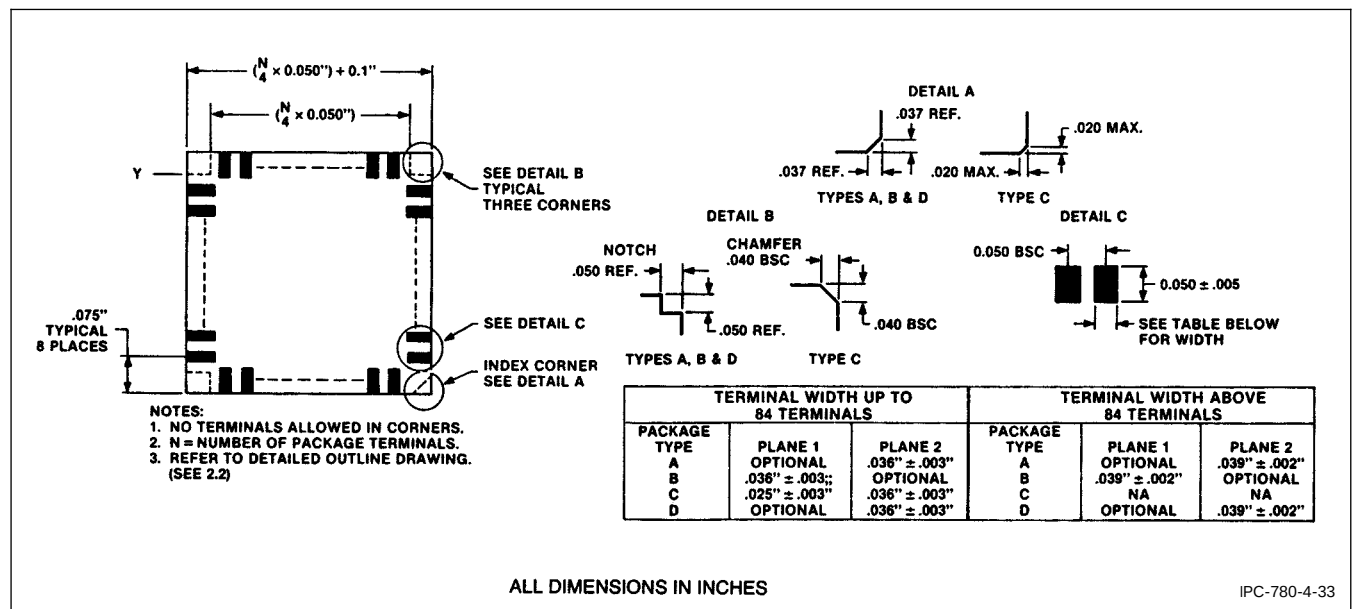


Figure 4-33 Features common to the 50-mil center packages

- Certain mechanical tolerances must be maintained and specific mechanical features for socketing are required.
- All sizes would specify corner notches; no chamfers are recommended except in the index corner.
- Reference notch to terminal centerline tolerance should be 0.05 mm [0.002 inch].
- Land width for the 0.635 mm [0.025 inch] spacing should be 0.3 mm [0.12 inch] 0.002 inch and, for the 0.5 mm [0.020 inch] spacing should be 0.25 mm [0.010 inch] 0.025 mm [0.001 inch].

If possible, use ceramic sizes common to JEDEC standard packages.

A set of outline drawings has been accepted by JEDEC for this fine pitch family. Lead counts and ceramic sizes are shown in Table 4-3.

4.3.5.2 Leadless Chip Carriers A leadless chip carrier is a ceramic or plastic package with integral surface-metallized terminations. Leadless Types A, B and D chip carriers have a chamfered index corner larger than that of Type C. Another difference between the A, B and D types and Type C is the feature in the other three corners (see Figure 4-32). The Types A, B and D were designed for socket applications and printed wiring interconnections. The Type C is primarily intended for direct attachment though reflow soldering. This application difference is the main reason for their mechanical differences. All have compatible terminal locations. These packages mount in different orientations, depending on type, mounting structure and preferred thermal orientation.

Leadless Type A is intended for lid-down mounting in a socket, which places the primary heat of operation in the

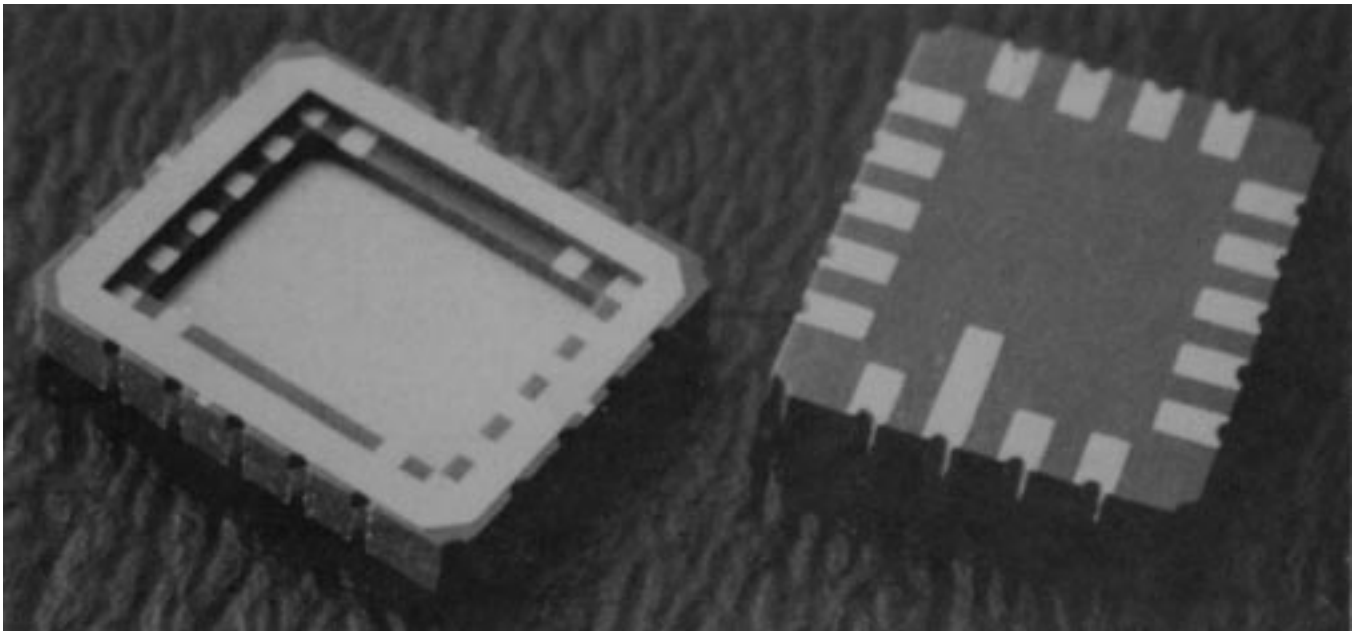


Figure 4-34 Type E package variations

Table 4-3 JEDEC Ceramic Sizes and Fine Pitch Terminal Counts

Ceramic Size	Terminal Count	
	0.025 in.	0.020 in.
0.450	52	64
0.560	68	
0.650	84	104
0.750	100	124
0.950	132	164
1.150	164	204
1.350	196	244
1.450		264
1.550		284
1.650	244	304

away from the mounting surface for more effective cooling in air cooled systems. Leadless Type B is for lid-up socket mounting on a printed board or for direct soldering to other types of packaging and interconnecting structures. Type C is a ceramic package similar to Leadless Type B except for corner configuration (see Figure 4-33), and Type D is for lid-down mounting on a P&I structure. Type E packages are for rectangular memory chips (see Figure 4-34).

Chip carriers have short leads that allow higher operating frequencies due to less inductance and capacitance. Other advantages include reduced signal lead resistance and improved power distribution.

A disadvantage of the leadless ceramic chip carrier is the thermal expansion mismatch between the ceramic material and the printed board. This mismatch can cause solder joint failures, especially in surface mounting.

Castellated leadless chip carriers (see Figures 4-31 and 4-32, leadless types B, C, and D), can use two basic types of solder joints. The first type uses a footprint pad extension to provide a 45° solder fillet. This type typically gives a solder joint height of 2–4 mils. The second type uses a minimal pad extension past the component outline (0.010") to achieve a solder joint height in excess of 8 mils. Components without castellations may also be used with this second method as shown in Figure 4-35A. Figure 4-35B shows a leadless ceramic chip carrier attached to a CTE-tailored P&I structure with solder columns. Note the deformation of corner solder joints due to extensive functional cycle testing.

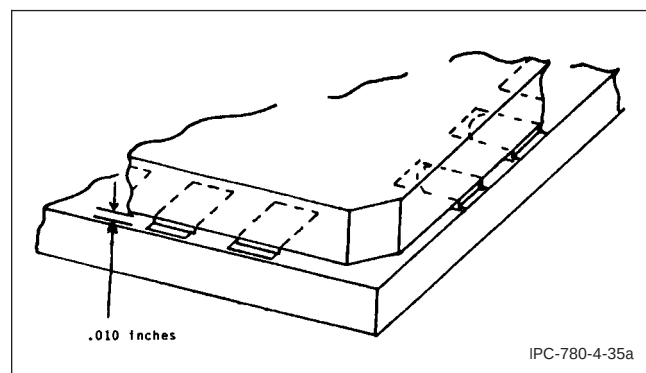


Figure 4-35A Chip carrier land pattern design

The solder joint is designed to extend from the top of the metallization to an elongated mounting land. This should produce a fillet at about a 45° angle to the substrate (see Figure 9-12).

4.3.5.3 Leaded Chip Carriers The Joint Electron Device Engineering Council presently defines three types of leaded chip carriers. Type A is a plastic package with leads.

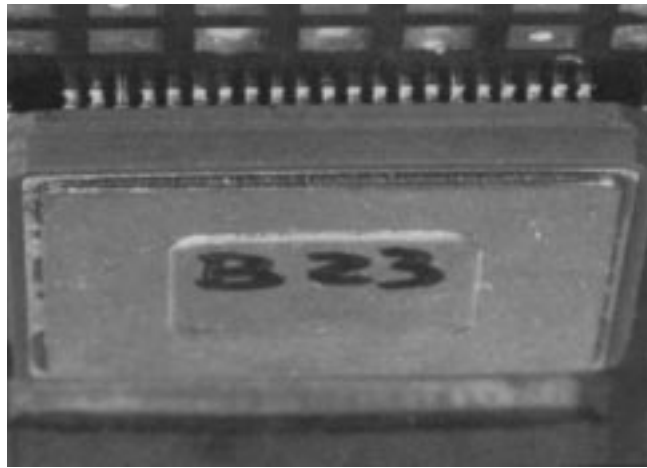


Figure 4-35B Leadless ceramic chip carrier attached to a CTE-tailored P&I structure with solder columns. Note the deformation of corner solder joints due to extensive functional cycle testing. (Courtesy AT&T Bell Laboratories)

wrapped down and around the body of all four sides. These packages can either be directly mounted to a printed board or used with a socket. This package was originally intended as a premolded package; however, the package could be a post-molded construction.

Leaded Type B packages are the type A, B, C, or D standard leadless chip carriers with the addition of substrate clips.

A third type is the plastic chip carrier, which has been optimized for post-molded fabrication. This construction uses the same fabrication techniques used for plastic DIP packages. Plastic chip carriers will probably replace ceramic versions as a low-cost alternative for those who do not need high temperature capabilities, high power dissipation or hermeticity.

The leads of these packages offer compliance for surface mount applications. They are also being specified for socketing.

4.3.5.4 Plastic Chip Carrier Square A JEDEC registered outline exists for square plastic chip carriers having lead counts of 20, 28, 44, 52, 68, 84, 100 and 124. Figure 4-36 shows an abbreviated drawing of the JEDEC outlines. Note that the leads are folded under the package during manufacture. This configuration is required for surface mounting, but it also reduces lead bending during shipping and handling.

4.3.5.5 Plastic Chip Carrier Rectangular A JEDEC registered outline exists for rectangular plastic chip carriers having lead counts of 18, 22, 28 and 32. Figure 4-37 shows an abbreviated drawing of the JEDEC outline.

4.3.5.6 Double-Row Plastic Chip Carrier This surface mounting plastic chip carrier nearly doubles the number of

available pins in standard sized units. For example, in the 0.950 sq. in. occupied by a 68-pin standard plastic leadless chip carrier, this design provides 128 pins in two rows of surface mount leads around the carriers perimeter (see Figure 4-38).

Moreover, the leads in the individual rows are still separated (after indentation) by standard 50 mil spacing. A castellated structure holds the two rows of pins an inner and an outer row 50 mils apart; within each row the leads are on 50 mil centers.

In the new two-row design, the wiring traces to the outer row proceed along the outside of the carrier. However, the traces to the inner row pass through the board and proceed on the board's underside to other points in the board circuit. In this way, the spacing and width of the traces to a double-row chip carrier remain standard.

4.3.5.7 Glass Epoxy Leadless Chip Carriers A glass epoxy chip carrier consists of three parts: a metallized base, a cavity wall and a lid to enclose the package. The base is a double-sided plated through hole glass epoxy printed board (normally FR-4, although other materials may be used) containing a number of outlines in array formats. The cavity walls are formed by routing out holes in another piece of glass epoxy board which is then press laminated to the base. The array is then sliced into individual chip carriers with a standard diamond impregnated dicing saw. The lids are made in similar arrays and also sliced up with the dicing saw.

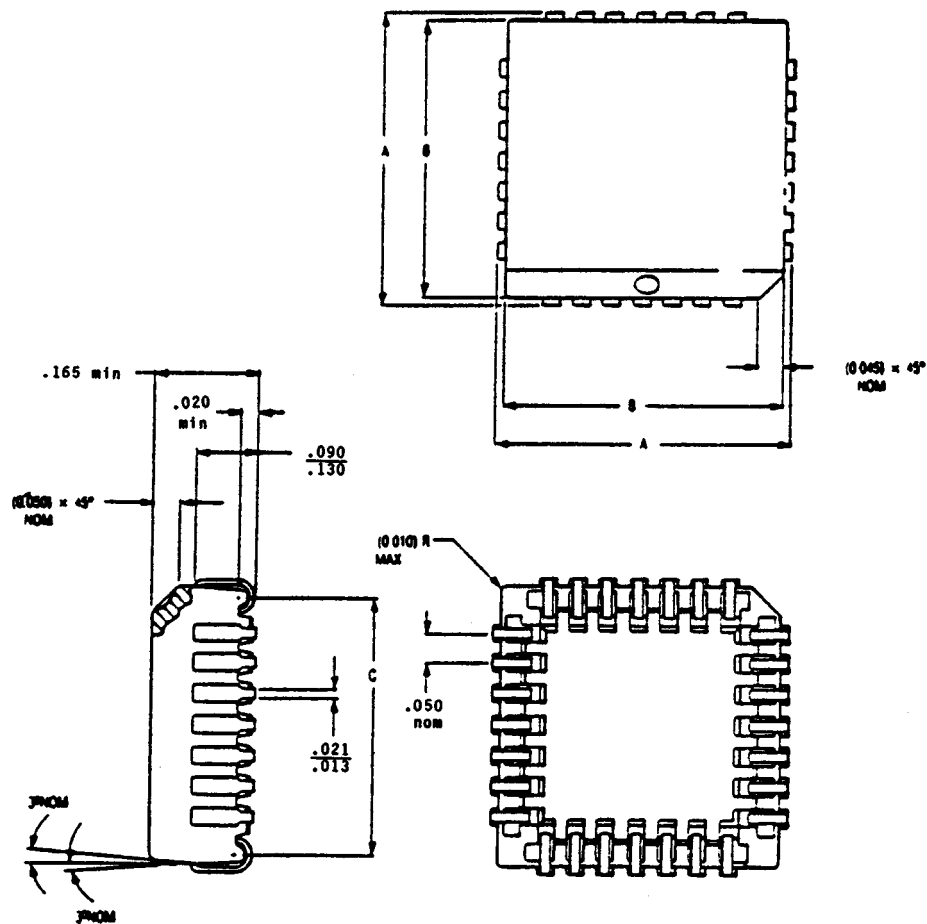
The photographic precision of the metallization together with the accuracy of the dicing saw operation yield an extremely clean package with very close dimensional tolerances and smooth edges with no fiber dust in the bonding area. The smooth edges and surfaces together with the close tolerances make these packages particularly adaptable to automatic assembly, testing and handling equipment.

The conductors consist of clad copper which is electroplated with copper to 0.005 mm [2 x 10⁻⁵ inches], then electroplated with nickel to 0.000125–0.00025 mm [0.000005–0.000010 inch] and finally electroplated with gold to 0.00005–0.0001 mm [2–4 x 10⁻⁷ inch]. This combination of metallization provides an excellent base for automatic wire bonding in the cavity area, and yet does not put enough gold on the footprint to embrittle the solder joint.

4.3.5.8 The Open Via Chip Carrier Another high density chip carrier is the open via chip carrier (OVCC). The salient features of the OVCC are two-fold:

- Overall package sizes are the same as those approved for JEDEC 1.27 mm [0.050 inch] terminal center chip carriers, but almost twice the number of terminals are available for a given package size.

Number of Terminals	A (Inches)		B (Inches)		C (Inches)	
	Min	Max	Min	Max	Min	Max
20	0.385	0.395	0.350	0.356	0.290	0.330
28	0.485	0.495	0.450	0.456	0.390	0.430
44	0.685	0.695	0.650	0.656	0.590	0.630
52	0.785	0.795	0.750	0.756	0.690	0.730
68	0.985	0.995	0.950	0.958	0.890	0.930
84	1.185	1.195	1.150	1.158	1.090	1.130
100	1.385	1.395	1.350	1.358	1.290	1.330
124	1.685	1.695	1.650	1.658	1.540	1.630

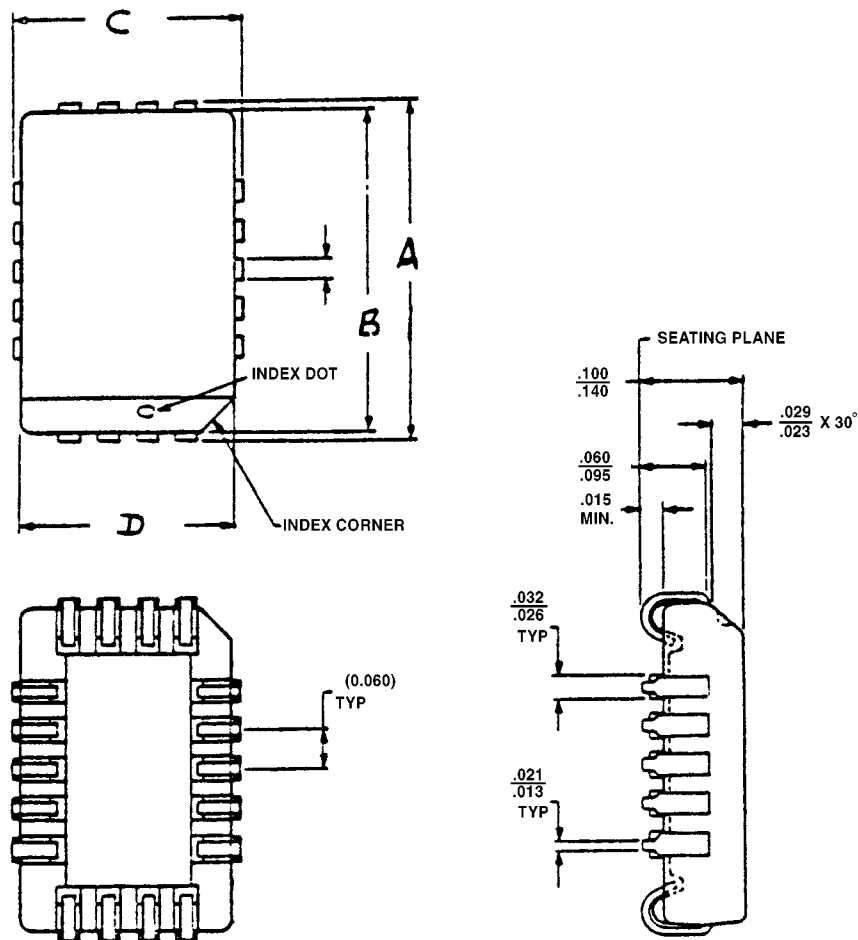


ALL DIMENSIONS IN INCHES

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Figure 4-36 Square plastic chip carrier

Number of Terminals	A (Inches)		B (Inches)		C (Inches)		D (Inches)	
	Min	Max	Min	Max	Min	Max	Min	Max
18	0.457	0.467	0.422	0.428	0.317	0.327	0.282	0.288
18	0.525	0.535	0.487	0.493	0.325	0.335	0.287	0.293
22	0.525	0.535	0.487	0.493	0.325	0.335	0.287	0.293
28	0.585	0.595	0.547	0.553	0.385	0.395	0.347	0.353
32	0.585	0.595	0.547	0.553	0.485	0.495	0.447	0.453



ALL DIMENSIONS IN INCHES

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Figure 4-37 Rectangular plastic chip carrier

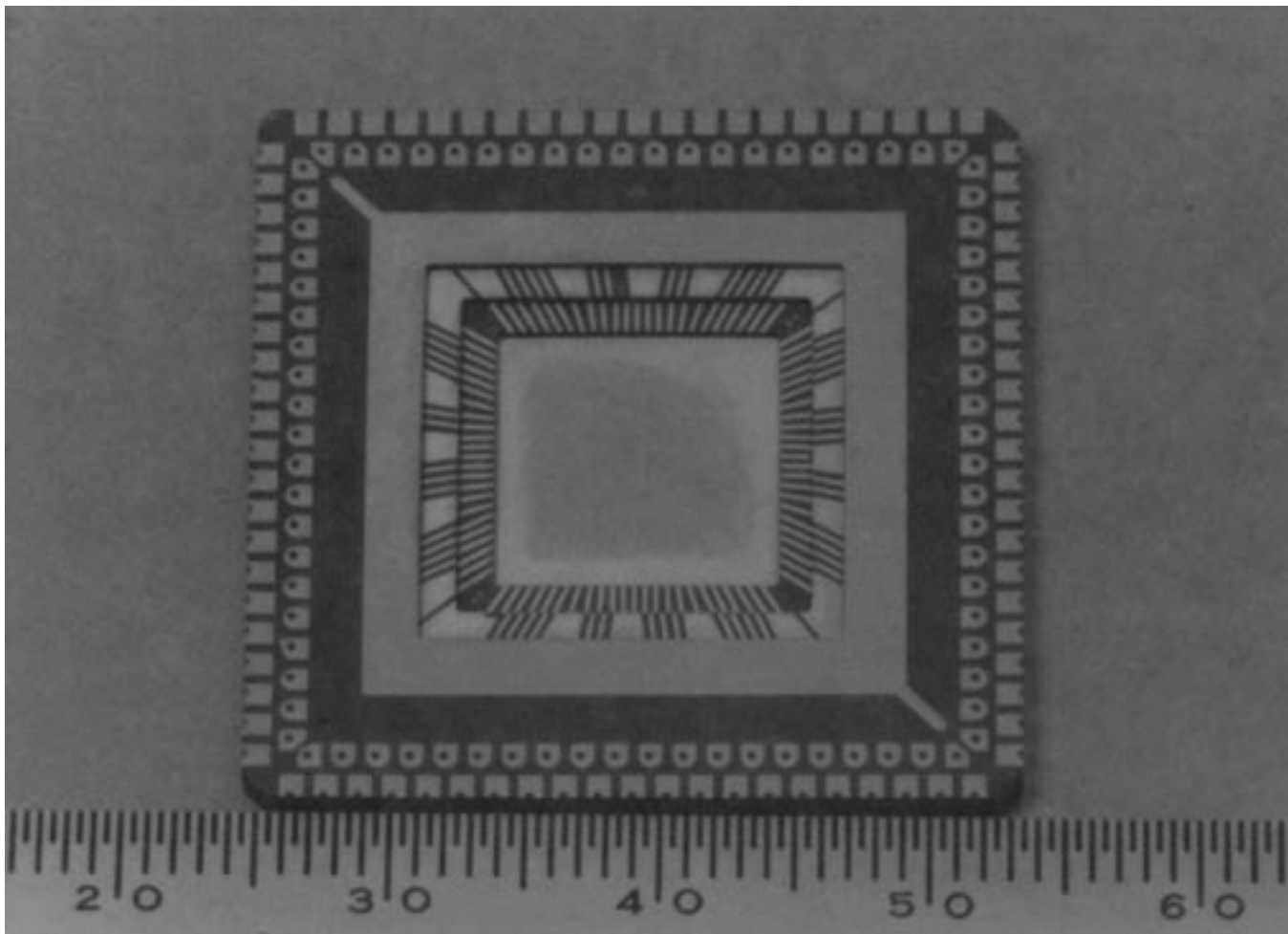


Figure 4-38 Double row plastic chip carrier

- The additional terminals are obtained through metallized hole terminals with pads on the top and bottom of the package, which are arranged in rows behind (inboard from) the peripheral contacts. These inner rows of terminals are on 1.27 mm [0.050 inch] centers, and are offset from the peripheral terminals by 0.635 mm [0.025 inch] (see Figure 4-39).

4.3.6 Grid Arrays Grid arrays are pinned or leadless carriers with I/O contacts that populate one surface of the package on a 0.100 inch (eventually 0.050 inch) grid. The use of a solid grid necessitates placing the die cavity on the side opposite the I/O contacts. A double or multiple concentric row grid permits having die cavity and I/O contacts on the same side with an optional heat sink on the opposite side.

4.3.6.1 Pin Grid Arrays (PGAs) A typical pin grid array is a square, multilayer (usually ceramic package having terminals on 2.54 x 2.54 mm [0.100 x 0.100 inch] centers. These packages are available in either cavity up or cavity down versions.

A cavity up configuration mounts the die opposite the pins, thereby allowing a full grid of pins and the highest I/O density.

A cavity down configuration has the die on the same side as the pins, and is generally used with high power circuits in air cooled applications to allow a heat sink opposite the die. However, this version is not as space efficient.

Pin grid arrays have good electrical characteristics due to the short signal paths from I/O pin to die. Pin grid arrays overcome thermal expansion problems typically encountered at ceramic/ printed board interfaces because the pins are compliant. Conventional soldering techniques such as wave soldering can attach these packages to printed boards. The higher the I/O lead count becomes, the lower the percentage of the total package area any given-size die cavity will occupy. (For example, the 96-lead, 40-mil center chip carrier is over one-inch square.)

For optimum packaging density, this percentage should be as high as possible. Therefore, 0.635 and 0.5 mm [0.025 and 0.020 inch] chip carriers and grid arrays are used (Figure 4-40).

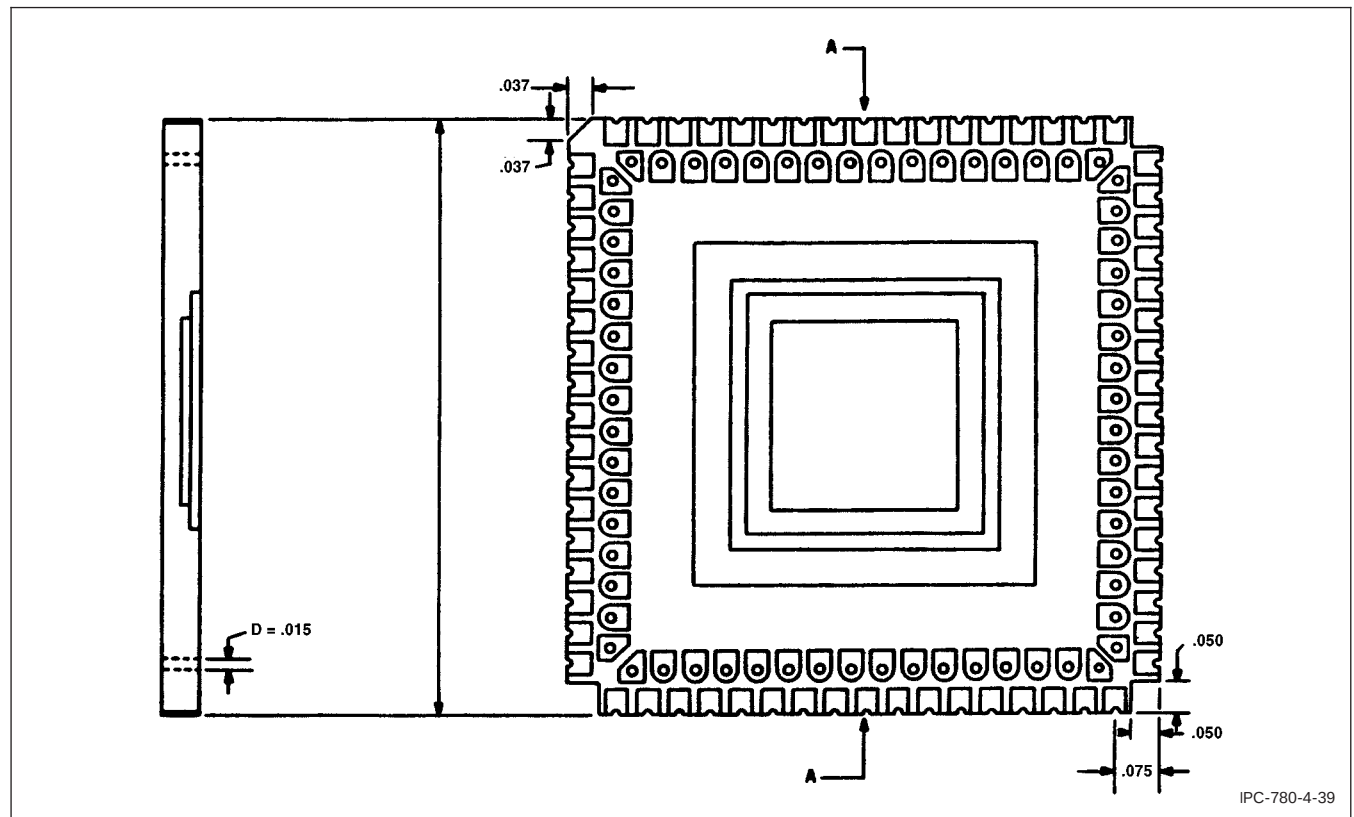


Figure 4-39 Open-via chip carrier (OVCC)

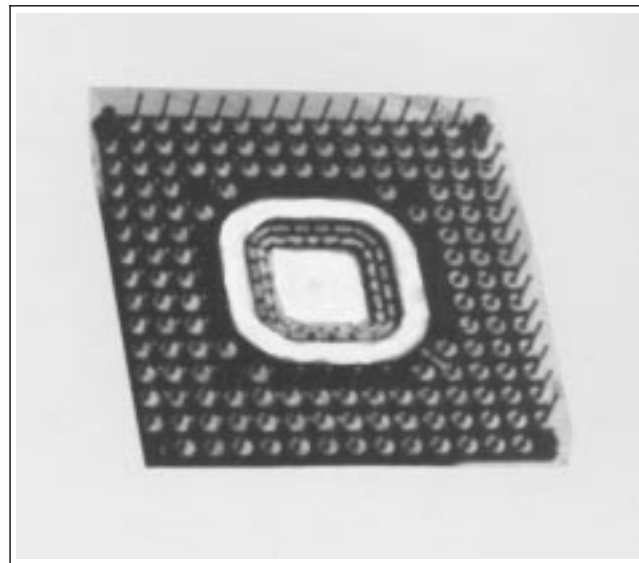


Figure 4-40 149-pin array package

Figure 4-41 shows the I/O density achievable with the various packages. As can be seen, for lead count requirements in excess of 100, a 0.10-mil centerline solid grid provides greater I/O density than either 50- or 40-mil centerline chip carriers.

The 25-mil centerline chip carrier is clearly more I/O efficient than is a 0.100-mil grid array. However, a double-row 50-mil solid grid provides the greatest I/O density. With pins brazed on 100-mil centers, pin grid arrays are a logi-

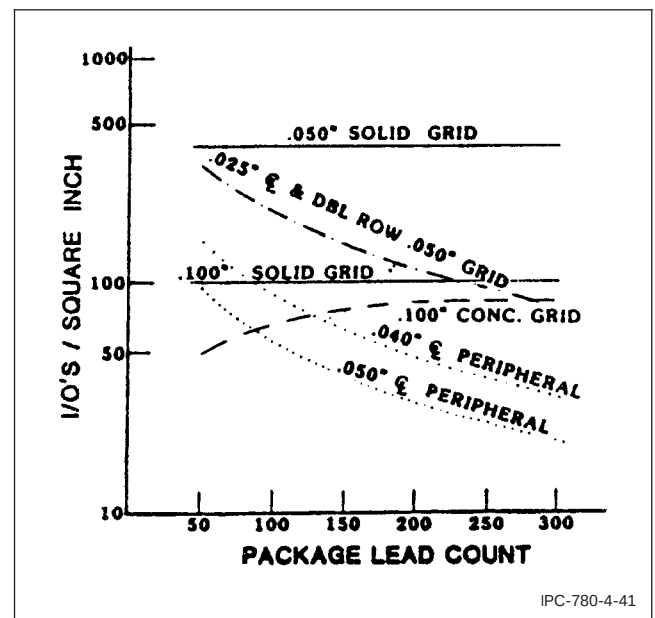


Figure 4-41 I/O density versus lead count (all dimensions in inches)

cal carrier for high lead counts intended for through-hole (not surface mount) board assembly compatible with DIPs. This should extend the useful life of present day technology for some high lead count applications.

4.3.6.2 Land (Leadless) Array The grid array package may also be leadless. This package normally has a central

array package omits the pins but retains the lands which are reflow solder attached to a matching land matrix on the P&IS.

Making 100-mil or even 50-mil grid arrays by the co-fired process is a known and practiced technology. Because of the larger dimensional tolerances, a leadless grid array is cheaper to fabricate than a tight toleranced fine pitch chip carrier. In addition, the lack of brazed pins lowered the package cost.

However, solder joint inspection, is now a problem. In addition, registration features are a concern.

JEDEC is developing a standard for this package; however, only preliminary proposals exist.

Each manufacturer's die and topography is different from other manufacturers. Therefore, die bonding patterns and chip sizes from different manufacturers should be examined to optimize part selection. **(Caution: It is easy to design with the smallest possible component, but if delivery is unreliable or the source disappears, layout may be in jeopardy.)**

Often, integrated circuit substrates affect the performance of the device. Depending upon the type of device, the substrate may be required to float or to be tied to the most negative potential. Unlike packaged devices, extensive testing cannot be performed on components in the die form. Thus, circuit designs that require low-current/voltage off-sets, AC responses, or temperature responses, might not function because faulty die cannot be probe tested before incorporation. Testing die components is generally limited to DC parameters at 25°C or, in some instances, at elevated temperatures.

Although only limited testing can be accomplished in the unpackaged state, 100% visual inspection to MIL-STD-883 can and should be performed.

A sample quantity of selected devices may be packaged and evaluated through test and burn-in. While this does not guarantee how the remaining die will perform, it will indicate the electrical performance and the possible yield level in a P&IA. It will also help to identify defective lots.

4.4 Sockets and Connectors Sockets and connectors are interconnection devices manufactured for various applications. These devices are used to facilitate the rapid connect/disconnect of P&I assemblies or devices on those assemblies.

Connectors and sockets are usually broken down into two major categories: production and test burn-in.

A production device is usually produced in mass quantities for lower cost and has limited functions. Characteristics of this type of device are limited temperature extremes, durability cycles, and applications

A test or burn-in device is built more ruggedly, because of its operating environments. This type of device could be designed for many thousands of operating cycles and large temperature extremes. These devices are usually larger and more expensive than their production or OEM counterparts.

4.4.1 Materials The composition and texture of the housing material is crucial, especially in reflow processing. Proper plating on the contact areas is also fundamental. In surface mount processes, the behavior of the metal in the reflow zone is critical for a high reliability joint.

4.4.1.1 Housing Materials Plastics for connector or sockets can be broken into two categories: thermosets or thermoplastic. Thermoset plastics are cured with the application of heat or by a chemical reaction. They survive higher temperatures but are also more costly to mold because of processing considerations. Thermoplastics can reflow when heated. At present, few thermoplastics can survive the rigors of burn-in applications and/or convective/convection reflow processing. Thermoplastics are readily processed at reasonable cost.

The ideal housing material for surface mount applications will exhibit the following qualities.

- High Glass Transition Temperatures
- Dimensional Stability
- Low Cost
- Chemically Process Inert
- Non-Hygroscopic
- Relatively Low Coefficient of Thermal Expansion

4.4.1.2 Contact Materials. Most contact materials, typically copper alloys, can be used with surface mount technology. Some alloys such as beryllium copper and phosphor bronze have operating temperatures below those encountered in some of the solder reflow processes. This is usually not a problem because they are at high temperature for only a short time and are not usually flexed or stressed during processing.

Typical production devices use materials such as phosphor bronze and beryllium copper. Burn-in devices use beryllium copper for lower temperature (150°C) applications and beryllium nickel for applications of 175°C to 200°C.

4.4.2 Lead Configuration and Spacing A variety of lead configurations are available on surface mount products. Selection criteria includes strength, solderability, area occupied, inspectability, and processability. Spacing is established along a single plane in orthogonal coordinates. The state of the art is described as multiple rows of lands located on 100 mil centerlines, 50 mil