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ELECTRONICS INDUSTRIES

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Includes: Amendment 1 and 2

Surface Mount Design and Land Pattern Standard

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October 1996

Amendment 2

April 1999

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IPC-SM-782A

Surface Mount Design and Land Pattern Standard

Developed by the Surface Mount Land Patterns Subcommittee (1-13)
of the Printed Board Design Committee (1-10) of IPC

Users of this standard are encouraged to participate in the
development of future revisions.

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Table of Contents

1.0 SCOPE	1	7.3 Component Placement	53
1.1 Purpose	1	7.4 Soldering	56
1.2 Performance Classification	1	7.5 Cleaning	57
1.3 Assembly Types	2	7.6 Repair/Rework	57
1.4 Presentation	2		
1.5 Profile Tolerances.....	2	8.0 DISCRETE COMPONENTS	
1.6 Land Pattern Determination	2	8.1 Chip Resistors	
2.0 APPLICABLE DOCUMENTS	4	8.2 Chip Capacitors	
2.1 IPC	4	8.3 Inductors	
2.2 Electronic Industries Association	4	8.4 Tantalum Capacitors	
2.3 Joint Industry Standards (IPC).....	5	8.5 Metal Electrode Face (MELF) Components	
2.4 American Society of Mechanical Engineers.....	5	8.6 Small Outline Transistor (SOT) 23	
3.0 DESIGN REQUIREMENTS	5	8.7 Small Outline Transistor (SOT) 89	
3.1 Terms and Definitions.....	5	8.8 Small Outline Diode (SOD) 123	
3.2 Component Acronyms	7	8.9 Small Outline Transistor (SOT) 143	
3.3 Dimensioning Systems	7	8.10 Small Outline Transistor (SOT) 223	
3.4 Design for Producibility	17	8.11 Modified Through-Hole Component (TO) 252	
3.5 Environmental Constraints	18	9.0 COMPONENTS WITH GULLWING LEADS ON TWO SIDES	
3.6 Design Rules	20	9.1 Small Outline Integrated Circuits (SOIC)	
3.7 Outer Layer Finishes	34	9.2 Small Outline Integrated Circuits (SSOIC)	
4.0 QUALITY AND RELIABILITY VALIDATION	37	9.3 Small Outline Package Integrated Circuit (SOPIC)	
4.1 Validation Techniques.....	37	9.4 Thin Small Outline Package	
4.2 Test Patterns—In-Process Validator	38	9.5 Ceramic Flat Pack (CFP)	
4.3 Stress Testing	38		
5.0 TESTABILITY	45	10.0 COMPONENTS WITH J LEADS ON TWO SIDES	
5.1 Testing Considerations	45	10.1 Small Outline Integrated Circuits with J Leads (SOJ)—7.63 mm [0.300] Body Size	
5.2 Nodal Access.....	45	10.2 Small Outline Integrated Circuits with J Leads (SOJ)—8.88 mm [0.350] Body Size	
5.3 Full Nodal Access.....	46	10.3 Small Outline Integrated Circuits with J Leads (SOJ)—10.12 mm [0.400] Body Size	
5.4 Limited Nodal Access.....	47	10.4 Small Outline Integrated Circuits with J Leads (SOJ)—11.38 mm [0.450] Body Size	
5.5 No Nodal Access	47		
5.6 Clam Shell Fixtures Impact.....	48	11.0 COMPONENTS WITH GULLWING LEADS ON FOUR SIDES	
5.7 Printed Board Test Characteristics	48	11.1 Plastic Quad Flat Pack (PQFP)	
6.0 PACKAGING AND INTERCONNECTING STRUCTURE TYPES	48	11.2 Shrink Quad Flat Pack (SQFP), Square	
6.1 General Considerations.....	49	11.3 Shrink Quad Flat Pack (SQFP), Rectangular	
6.2 Organic-Base Material P&IS.....	50	11.4 Ceramic Quad Flat Pack (CQFP)	
6.3 Non-Organic Base Materials	50	12.0 COMPONENTS WITH J LEADS ON FOUR SIDES	
6.4 Supporting-Plane P&I Structures	50	12.1 Plastic Leaded Chip Carrier (PLCC), Square	
6.5 Constraining Core P&I Structures	52	12.2 Plastic Leaded Chip Carrier (PLCC), Rectangular	
7.0 ASSEMBLY CONSIDERATIONS FOR SURFACE MOUNT TECHNOLOGY (SMT)	53	12.3 Leadless Ceramic Chip Carrier (LCC)	
7.1 SMT Assembly Process Sequence	53	13.0 MODIFIED DUAL-IN-LINE PIN (DIP) COMPONENTS	
7.2 Substrate Preparation Adhesive, Solder Paste	53		



13.1 DIP

14.0 COMPONENTS WITH BALL GRID ARRAY CONTACTS

14.1 Plastic Ball Grid Array

14.2 1.27 mm Pitch Rectangular PBGA JEDEC MS-028

Figures

Figure 1–1	Electrical assembly types.....	3
Figure 3–1	Examples of typical package styles and package descriptive designators.....	9
Figure 3–2	Lead-form (or terminal-shape) examples.....	10
Figure 3–3	Profile tolerancing examples	11
Figure 3–4	Example of C1206 capacitor dimensioning for optimum solder fillet conditions	12
Figure 3–5	Profile dimensioning of a gullwing leaded SOIC.....	13
Figure 3–6	Pitch for multiple-leaded components.....	15
Figure 3–7	Simplified electronic development organization	20
Figure 3–8	Recommended minimum land-to-land clearances	21
Figure 3–9	Component orientation for wave solder applications.....	21
Figure 3–10	Alignment of similar components	22
Figure 3–11	Local/global fiducials	23
Figure 3–12	Panel/global fiducials.....	23
Figure 3–13	Fiducial types for vision systems	24
Figure 3–14	Fiducial clearance requirements	24
Figure 3–15	Fiducial locations on a printed circuit board ...	25
Figure 3–16	Packaging and geometries.....	25
Figure 3–17	Surface mount conductor widths/clearances vs. routing grids	26
Figure 3–18	Section view of multilayer board with vias on 1.0 mm [0.040 in] centers	26
Figure 3–19	Narrowed conductor	27
Figure 3–20	Conductor routing.....	27
Figure 3–21	Surface routing geometries	28
Figure 3–22	Conductor routing capability test pattern	28
Figure 3–23	Routing channels under SOIC land pattern with 28 pins.....	29
Figure 3–24	Land pattern to via relationships.....	29
Figure 3–25	Examples of via positioning concepts.....	30
Figure 3–26	Vias under components	30
Figure 3–27	Conductor characteristics.....	31
Figure 3–28	Examples of modified landscapes	32
Figure 3–29	Typical copper glass laminate panel.....	33
Figure 3–30	Conductor clearance for V-groove scoring	34
Figure 3–31	Breakaway (routed pattern).....	35
Figure 3–32	Routed slots	35
Figure 3–33	Gang solder mask window.....	36
Figure 3–34	Pocket solder mask windows.....	36

Figure 4–1	Component temperature limits	37
Figure 4–2	General description of process validation contact pattern and interconnect.....	39
Figure 4–3	Photo image of IPC-A-49 test board for primary side.....	39
Figure 4–4	Flat ribbon, “L,” and gullwing lead joint description	40
Figure 4–5	Round or flattened (coined) lead joint description	40
Figure 4–6	“J” lead joint description	41
Figure 4–7	Rectangular or square end components.....	41
Figure 4–8	Cylindrical end cap terminations—joint illustration	42
Figure 4–9	Bottom only terminations.....	42
Figure 4–10	Leadless chip carriers with castellated terminations—joint description	43
Figure 4–11	Butt joint description.....	43
Figure 4–12	Thermal cycle excursion rate	44
Figure 5–1	Test via grid concepts	47
Figure 5–2	General relationship between test contact size and test probe misses	49
Figure 5–3	Test probe feature distance from component.....	50
Figure 7–1	Typical process flow for underside attachment type 2c (simple) surface mount technology	54
Figure 7–2	Typical process flow for full surface mount type 1b and 2b surface mount technology	54
Figure 7–3	Typical process flow for mixed technology type 2c (complex) surface mount technology	55
Figure 7–4	In-line placement equipment.....	55
Figure 7–5	Simultaneous placement equipment.....	55
Figure 7–6	Sequential placement equipment.....	56
Figure 7–7	Sequential/Simultaneous placement equipment.....	56

Tables

Table 3–1	Terminal Position Prefixes.....	8
Table 3–2	Package-Outline-Style Codes	8
Table 3–3	Lead-Form (or Terminal-Shape) Suffixes	11
Table 3–4	Tolerance Analysis Elements for Chip Devices	17
Table 3–5	RLP Numbers.....	17
Table 3–6	Worst-Case Environments and Appropriate Equivalent Accelerated Testing	19
Table 3–7	Component Stand Off	23
Table 3–8	Typical Values to Be Added or Subtracted to Nominal Production to Achieve Desired Nominal Conductor Width	31
Table 3–9	Conductor Width Tolerances	32
Table 6–1	Packaging and Interconnecting Structure Comparison	51
Table 6–2	P & I Structure Selection Considerations	52
Table 6–3	P & I Structure Material Properties.....	52

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Surface Mount Design and Land Pattern Standard

1.0 SCOPE

This document provides information on land pattern geometries used for the surface attachment of electronic components. The intent of the information presented herein is to provide the appropriate size, shape and tolerance of surface mount land patterns to insure sufficient area for the appropriate solder fillet, and also to allow for inspection and testing of those solder joints.

1.1 Purpose Although, in many instances, the land pattern geometries can be slightly different based on the type of soldering used to attach the electronic part, wherever possible, land patterns are defined in such a manner that they are transparent to the attachment process being used. Designers should be able to use the information contained herein to establish standard configurations not only for manual designs but also for computer aided design systems. Whether parts are mounted on one or both sides of the board, subjected to wave, reflow, or other type of soldering, the land pattern and part dimensions should be optimized to insure proper solder joint and inspection criteria.

Although patterns are standardized, since they are a part of the printed board circuitry geometry, they are subject to the producibility levels and tolerances associated with plating, etching, or other conditions. The producibility aspects also pertain to the use of solder mask and the registration required between the solder mask and the conductor patterns. (See paragraph 1.2.2).

1.2 Performance Classification Three general end-product classes have been established in associated IPC standards and specifications to reflect progressive increases in sophistication, functional performance requirements and testing/inspection frequency. It should be recognized that there may be an overlap of equipment between classes.

Design requirements determine class. Class definitions are useful for identifying degrees of precision needed to meet design/performance requirements of packaging and interconnecting structures, and establish communication media between design and manufacture and disciplines.

The printed board user has the responsibility to determine the class to which his product belongs. The contract shall specify the performance class required and indicate any exceptions to specific parameters, where appropriate. In the event of conflict between the design requirements and the classes defined herein, the former shall take precedence and be reflected in the master drawing.

These classes are:

CLASS 1 General Electronic Products

Includes consumer products, some computer and computer peripherals, as well as general military hardware suitable for applications where cosmetic imperfections are not important and the major requirement is function of the completed printed board or printed board assembly.

CLASS 2 Dedicated Service Electronic Products

Includes communications equipment, sophisticated business machines, instruments and military equipment where high performance and extended life is required, and for which uninterrupted service is desired but is not critical. Certain cosmetic imperfections are allowed.

CLASS 3 High Reliability Electronic Products

Includes the equipment for commercial and military products where continued performance or performance on demand is critical. Equipment downtime cannot be tolerated, and functionality is required for such applications as life support items, or missile systems. Printed boards and printed board assemblies in this class are suitable for applications where high levels of assurance are required and service is essential.

The land patterns in this standard have the capability of accommodating all three performance classifications.

1.2.1 End-Use Applications In addition to the three performance classifications, the Surface Mount Council has established end use applications for electronic products. These are:

1. *Consumer products* including games, toys, audio and video electronics. In general, convenient size and maximum functionality are important but product cost is extremely important.
2. *General purpose computers*, as used in businesses and personal applications. Compared to consumer products, customers expect longer life and more consistent service.
3. *Telecom products* including telephone, switching systems, PBXs, and exchanges. These products are used in applications expecting long service life and enduring relatively harsh environments.
4. *Commercial aircraft* requiring small size, light weight and high reliability.
5. *Industrial products and passenger compartment automotive applications*. Size and function is a byword of these products. Cost is very important, provided that reducing product cost doesn't forfeit the highest achievable product quality, performance and reliability.

6. *High performance products* consisting of ground-based and shipbound military products, high speed and high capacity computers, critical process controllers, and life supporting medical systems. Quality, reliability and performance are paramount, closely followed by size and function. Cost is optimized based on these requirements but is less important.
7. *Space products* include all of the products above which are built to meet harsh outer space conditions. This implies high quality and performance over a wide range of environmental and physical extremes.
8. *Military avionics products* built to meet demanding mechanical and thermal changes. Size, weight, performance and reliability are paramount.
9. *Under the hood automotive electronics products* endure the harshest of all use environments. These products face extreme temperatures and mechanical variations. Adding to this is the pressure of achieving the lowest cost and optimum manufacturability in high volumes.

1.2.2 Producibility Levels When appropriate this standard will provide three design complexity levels of features, tolerances, measurements, assembly, testing of completion or verification of the manufacturing process that reflect progressive increases in sophistication of tooling, materials or processing and, therefore progressive increases in fabrication cost. These levels are:

- Level A General Design Complexity—Preferred
- Level B Moderate Design Complexity—Standard
- Level C High Design Complexity—Reduced Producibility

Producibility levels also pertain to the assembly. The three component mounting complexity levels which reflect progressive increases in sophistication of tooling, assembly and joining techniques and therefore progressive increases in cost are:

- Level A simple assembly techniques used to describe through the board component mounting;
- Level B moderate assembly techniques used to describe surface component mounting and
- Level C complex assembly techniques used to describe intermixing of through-the-board and surface mounting on the same assembly.

Classification of complexity should not be confused with the performance classification of end-item use described in paragraph 1.2.

1.3 Assembly Types A type designation signifies further sophistication describing whether components are mounted

on one or both sides of the packaging and interconnecting structure. Type 1 defines an assembly that has components mounted on only one side; type 2 is an assembly with components on both sides. Type 2 is limited to only class B or C assemblies.

Figure 1–1 shows the relationship of two types of assemblies.

The need to apply certain design concepts should depend on the complexity and precision required to produce a particular land pattern or P&I structure. Any design class may be applied to any of the end-product equipment categories; therefore, a moderate complexity (Type 1B) would define components mounted on one side (all surface mounted) and when used in a Class 2 product (dedicated service electronics) is referred to as Type 1B, Class 2. The product described as a Type 1B, Class 2 might be used in any of the end-use applications; the selection of class being dependent on the requirements of the customers using the application.

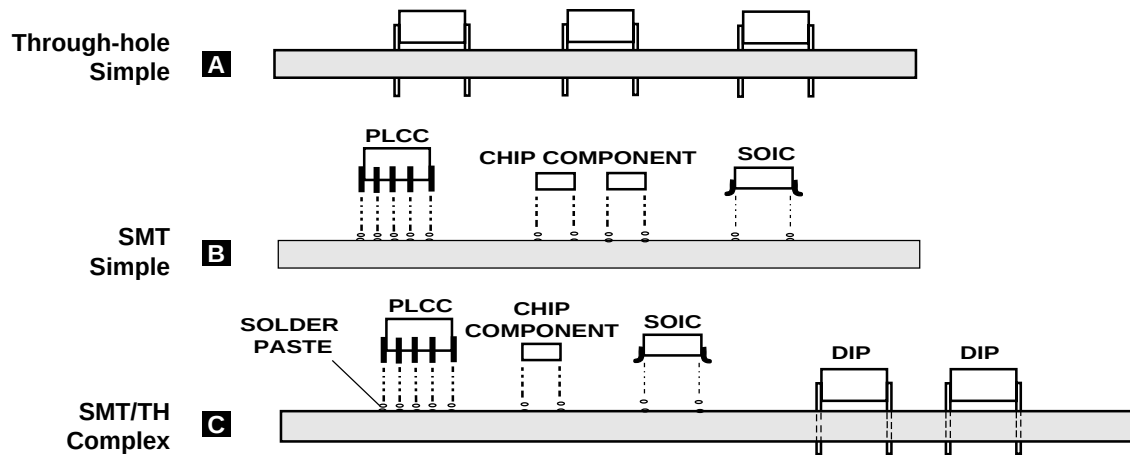
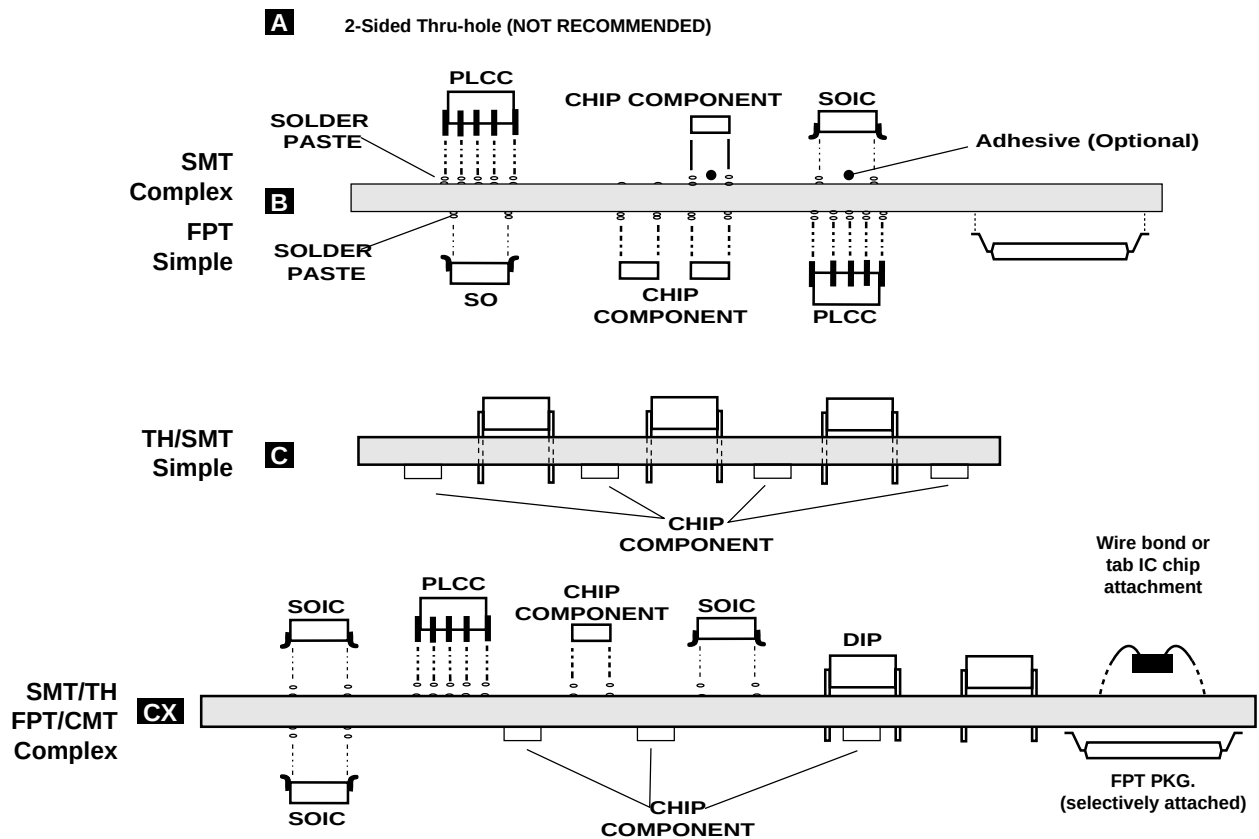
1.4 Presentation Dimensions and tolerances are expressed in millimeters (mm) or microns (mn) as appropriate. When no unit of measurement is shown, the unit shall be assumed to be “mm.” Reference information for inch conversion is shown in the appendix.

1.5 Profile Tolerances Profile tolerances are used in the dimensioning system for determining the relationship between component outlines and land pattern geometries. The details are described in Section 3.3, and follow the principles set forth in ANSI Y14.5. All dimensions are considered maximum or minimum material condition (depending on the features being analyzed), thus the profile tolerances are unilateral (one-direction—maximum to minimum, or minimum to maximum) as opposed to bilateral (plus or minus) from a nominal characteristic.

1.6 Land Pattern Determination This document discusses two methods of providing information on land patterns:

- (1) exact details based on industry component specifications, board manufacturing and component placement accuracy capabilities. These land patterns are registered to a specific component, and have a registered land pattern number, see Table 3.5 and paragraph 3.3.3.4.
- (2) equations that can be used to alter the given information to achieve a more robust solder connection, when used in particular situations where the equipment for placement or attachment are more or less precise than the assumptions made when determining the exact land pattern details.

1.6.1 General Usage of SMT In general, a product is a good candidate for SMT if it needs to be:

Type 1**Type 2**

IPC-782-1-1

Figure 1-1 Electrical assembly types

- Small in size, real estate constrained
- Able to accommodate large amounts of memory
- Light in weight
- Able to accommodate several large, high lead count complex ICs, such as ASICs and silicon arrays
- Able to function at high frequencies and speeds
- Able to transmit little or no noise, EMI and RFI resistant
- Able to be built in large volumes using automation

Currently, most SMT boards that have 50 or more components use a combination of SMT and through-hole technologies. The mix is a function of component availability, multiplicity of vendors, and cost. A mix of 80 percent SMT and 20 percent through-hole parts is very common. However, the number of 100% SMT assemblies is increasing.

Fine Pitch Technology (FPT) involves a process change as well as a packaging family, because the package to board assembly steps are different than SMT. For example, several commercially available FPT parts require lead excise and forming prior to placement. They are encapsulated or molded with plastic and delivered to users as a separate packaged device, and these parts may be shipped with a molded guard-ring or a slide carrier securing the leads in place. The full encapsulated device will be used for direct board mounting.

FPT packages are available under package names such as PQFP (Plastic Quad Flat Pack), CQFP (Ceramic Quad Flat Pack), QFP (Quad Flat Pack) and VSOIC (Very Small Outline Integrated Circuits).

2.0 APPLICABLE DOCUMENTS

The following documents, of the issue currently in effect form a part of this document to the extent specified herein. Other documents listed are for reference purposes to assist the user.

2.1 IPC¹

IPC-A-48 Surface Mount Land Pattern Artwork (Mantech)

IPC-A-49 Surface Mount Land Pattern Artwork (IPC-SM-782A)

IPC-T-50 Terms and Definitions

IPC-SC-60 Post Solder Solvent Cleaning Handbook

IPC-AC-62 Post Solder Aqueous Cleaning Handbook

IPC-2221 Generic Standard on Printed Board Design

IPC-6012 Qualification and Performance Standard for Rigid Printed Boards

IPC-D-330 Printed Wiring Design Guide

IPC-A-610 Acceptability of Printed Board Assemblies

IPC-7711 Rework of Electronic Assemblies

IPC-SM-780 Guidelines for Component Packaging and Interconnection with Emphasis on Surface Mounting

IPC-SM-784 Guidelines for Chip-on-Board Technology Implementation

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments

IPC-SM-786 Recommended Procedures for Handling of Moisture Sensitive Plastic IC Packages

IPC-AJ-820 Assembly and Joining Handbook

IPC-CC-830 Electrical Insulating Compounds for Printed Board Assemblies

IPC-SM-840 Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

IPC-1902/IEC 60097 Grid System for Printed Circuits

2.2 Electronic Industries Association²

IS-30 Surface Mount Resistors

JEDEC-95 JEDEC Registered and Standard Outlines for Solid State Products

EIA-PDP-100 Registered and Standard Mechanical Outlines for Electronic Parts

RS-198 Ceramic Dielectric Capacitors

RS-228 Fixed Electrolytic Tantalum Capacitors

RS-367 Dimensional and Electrical Characteristics Defining Receiver Type Sockets

RS-376 Fixed Film Dielectric Capacitors in Metallic and Non-Metallic Cases for D.C. Application

RS-415 Dimensional and Electrical Characteristic Defining Dual-In-Line-Type Sockets

RS-428 Type Designation System for Microelectronic Devices

1. IPC, 2215 Sanders Road, Northbrook, IL 60062-6135

2. Electronic Industries Association, 2001 Eye Street N.W., Washington, DC 20006

RS-471 Symbol and Label for Electrostatic Sensitive Devices

RS-481 Tape and Reel Specification

2.3 Joint Industry Standards (IPC)¹

J-STD-001 Requirements for Soldered Electrical and Electronic Assemblies

J-STD-002 Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

J-STD-003 Solderability Tests for Printed Boards

2.4 American Society of Mechanical Engineers³

ANSI Y14.5M—1982 Dimensioning and Tolerancing

3.0 DESIGN REQUIREMENTS

3.1 Terms and Definitions Terms and definitions used herein are in accordance with IPC-T-50 except as otherwise specified. **Note:** Any definition denoted with an asterisk (*) is a reprint of the definition defined in IPC-T-50.

***Assembly** – A number of parts or subassemblies or any combination thereof joined together.

Note: When this term is used in conjunction with other terms listed herein, the following definitions shall prevail.

Assembly, double-sided – A packaging and interconnecting structure with components mounted on both the primary and secondary sides.

Assembly, multilayer printed circuit – a multilayer printed circuit board on which separately manufactured components and parts have been added.

Assembly, multilayer printed wiring – a multilayer printed wiring board on which separately manufactured components and parts have been added.

Assembly, packaging and interconnecting (P&IA) – The generic term for an assembly that has electronic components mounted on either one or both sides of a packaging and interconnecting structure.

Assembly, printed board – an assembly of several printed circuit assemblies or printed wiring assemblies, or both.

Assembly, printed circuit – a printed circuit board on which separately manufactured components and parts have been added.

Assembly, printed wiring – a printed wiring board on which separately manufactured components and parts have been added.

Assembly, single-sided – A packaging and interconnecting structure with components mounted only on the primary side.

***Base material** – The insulating material upon which the conductor pattern may be formed. The base material may be rigid or flexible. It may be a dielectric sheet or insulated metal sheet.

Basic dimension – Theoretically exact location of a component feature, indicated by a symbol or a number in a box. (The tolerance on a basic dimension provides the limits of the variation from the basic dimension location.)

Castellation – Metallized features that are recessed on the edges of a chip carrier which are used to interconnect conducting surfaces or planes within or on the chip carrier.

Chip carrier – A low-profile rectangular component package, usually square, whose semiconductor chip cavity or mounting area is a large fraction of the package size and whose external connections are usually on all four sides of the package.

Chip-on-board (COB) – Integrated circuit device mounted directly to the printed board and interconnected with wire bonds.

Coefficient of thermal expansion (CTE) – The linear thermal expansion per unit change in temperature.

Component – A separable part of a printed board assembly which performs a circuit function (e.g., a resistor, capacitor, transistor, etc.)

Component mounting site – A location on a P&I structure that consists of a land pattern and conductor fan-out to additional lands for testing or vias that are associated with the mounting of a single component.

***Conductive pattern** – The configuration or design of the conductive material on the base material. (Includes conductors, lands, and through connections when these connections are in integral part of the manufacturing process.)

***Conductor** – A single conductive path in a conductive pattern.

Constraining core – A supporting plane that is internal to a packaging and interconnecting structure.

***Dual in-line package (DIP)** – A component which terminates in two straight and parallel rows of pins or lead wires.

Fine-pitch technology (FPT) – Surface mounted components with a lead or termination pitch of 0.63 mm or less.

Fiducial – A feature of the PB used to provide common measurable points for all steps in the assembly process.

Flat pack – A component with two straight rows of leads (normally on 1.27 mm centers) which are parallel to the component body.

3. Publications are available from the American Society of Mechanical Engineers, 345 East 47th St., New York, NY 10017.

Footprint – (see preferred term “Land Pattern”)

***Grid** – An orthogonal network of two sets of parallel equidistant lines used for locating points on a printed board. (Note: Connections should be located on the cross-points of the gridlines. The position of conductors may be independent of the grid, i.e., not necessarily following the gridlines.)

Integrated circuit (IC) – An assembly of miniature electronic components simultaneously produced in batch processing, on or within a single substrate to perform an electronic circuit function.

***Jumper wire** – An electrical connection that is a part of the original design, added between two points on a printed wiring board after the intended conductive pattern is formed.

***Land** – A portion of a conductive pattern usually, but not exclusively, used for the connection, or attachment, or both of components.

Land pattern – A combination of lands intended for the mounting, interconnection and testing of a particular component.

Leadless chip carrier – An electronic component whose external connections consist of metallized terminations containing a single integrated circuit chip.

Leaded chip carrier – An electronic component whose external connections consist of leads emanating from the sides of the package, which contains a single circuit chip.

***Master drawing** – A document that shows the dimensional limits or grid locations applicable to any or all parts of a printed board (rigid or flexible), including the arrangement of conductive and nonconductive patterns or elements; size, type, and location of holes; and any other information necessary to describe the product to be fabricated.

Mixed mounting technology – A component mounting technology that uses both through-hole and surface mounting technologies on the same packaging and interconnecting structure.

***Module** – A separable unit in a packaging scheme

Nominal – Design dimension for the size of a feature. (The tolerance on a nominal dimension gives the limits of variation of a feature size.)

Packaging and interconnecting structure (P&IS) – The generic term for a completely processed combination of substrates, metal planes or constraining cores, and interconnection wiring used for the purpose of mounting components.

***Plated-through hole (PTH)** – A hole in which electrical connection is made between internal or external conductive patterns, or both, by the plating of metal on the wall of the hole.

Primary side – That side of the packaging and interconnecting structure that contains the most or more complex components. The primary side establishes layer one of the P/I structure. (The same as the “component side” in through-hole component mounting technology.)

***Printed board** – The general term for completely process printed circuit or printed wiring configurations. It includes rigid or flexible, single, double and multilayer boards.

***Printed wiring** – The conductive pattern intended to be formed on a common base, to provide point-to-point connection of discrete components, but not to contain printed components.

***Registration** – The degree of conformity of the position of a pattern, or a portion thereof, with its intended position or with that of any other conductor layer of a board.

Secondary side – That side of the packaging and interconnecting structure that is opposite of the primary side. (The same as the “solder side” in through-hole component mounting technology.)

Single in-Line package (SIP) – A component which terminates in one straight row of pins and lead wires.

Static electricity – An electrical charge that has accumulated or built up on the surface of a material.

Static electricity control – A technique where materials and systems are employed to eliminate/discharge static electricity buildup by providing continuous discharge paths.

***Supported hole** – A hole in a printed board that has its inside surface plated or otherwise reinforced.

Supporting plane – A planar structure that is a part of a packaging and interconnecting structure to provide mechanical support, thermo-mechanical constraint, thermal conduction and/or electrical characteristics. (It may be either internal or external to the packaging and interconnecting structure.)

Surface mount technology (SMT) – The technology where electrical connection of components is made to the surface of a conductive pattern of a printed board and does not utilize component lead holes.

Thermal expansion mismatch – The absolute difference in thermal expansion of two components.

***Through connection** – An electrical connection between conductive patterns on opposite sides of an insulating base, e.g., plated-through hole or clinched jumper wire.

Through-hole technology (THT) – An assembly process for mounting component packages where leads are passed through supported (plated through) or unsupported (bare) holes in an interconnection substrate.

***Tooling feature** – A specified physical feature on a printed board or a panel such as a marking, hole, or registration mark.

slot or edge, used exclusively to position the board or panel or to mount components accurately. (See Fiducial)

***Via** – A plated-through hole used as a through connection, but in which there is no intention to insert a component lead or other reinforcing material.

Blind via – A via that is connected to either the primary side or secondary side and one or more internal layers of a multilayer packaging and interconnecting structure, but not to both sides.

Buried via – A via that is connected to neither the primary side nor the secondary side of a multilayer packaging and interconnecting structure, i.e., it connects only between inner layers.

Tented via – A blind or through-hole via that has the exposed surface of the primary or secondary or both sides of a packaging and interconnecting structure fully covered by a masking material, such as a dry film polymer coating (solder mask), prepregged glass cloth (prepreg), etc., in order to prevent hole access by process solutions, solder, or contamination.

3.2 Component Acronyms In an attempt to standardize on component characteristics the Joint Electronic Device Engineering Council (JEDEC) of the Electronic Industries Association (EIA) has developed a set of recommended acronyms that can be used to describe the shape, material, lead position, package style, lead form and lead count. These details are defined in JEDEC Publication JESD1C and have been circulated and approved as an international document published by the International Electrotechnical Commission (IEC) as IEC Publication 30. These concepts are supported and adopted in this land pattern document to facilitate communication between design, component manufacturer, board manufacturer, quality assurance etc.

Some of the information from the JEDEC publication is presented to assist the reader. The acronym systems is divided into six parts. They are:

- **SHAPE** – A single-letter prefix that identifies the mechanical package profile (round, rectangular, square, etc.)
- **MATERIAL** – A single-letter prefix that identifies the predominant package body material (glass, metal, plastic, etc.)
- **POSITION** – A single-letter prefix that identifies terminal or lead position related to the package profile (see 3.2.1)
- **PACKAGE** – A double-letter designation that identifies the package-outline style (see 3.2.2)
- **FORM** – A single letter suffix that identifies the terminal or lead form (see 3.2.3)
- **COUNT** – A one, two, or three-digit suffix that identifies the number of leads or terminations (12, 84, 160, etc.)

The minimum acronym consists of the position, package, form and count identifiers. Shape and material prefixes are optional acronym designations. As an example the designation R-PDIP-T14 describes a rectangular part (R), made of plastic (P), with dual terminals or leads (D), coming from an in-line package style (IP) with through-hole leads (T) and a lead count of 14.

3.2.1 Position Designation The single-letter prefix for terminal position shall be identified in accordance with Table 3–1. The position definition “terminal” applies to either lead or leadless. The descriptions assume that the seating plane is the bottom of the package. Reference to package shape does not take into account flanges, notches or irregularities.

3.2.2 Package-Outline Style Designators The package double-letter designator shall be in accordance with Table 3–2. Figure 3–1 provides some examples of the compulsory package outline style acronyms.

3.2.3 Form Designation The single-letter suffix that defines the terminal form (termination or lead) configuration shall be in accordance with Table 3–3. Figure 3–2 shows a few diagrams of various package lead configurations.

3.3 Dimensioning Systems There are many methods of dimensioning and tolerancing mechanical parts, all of which are defined in ANSI Y14.5. All the methods work, but it must be recognized that some methods work better than others and some methods cost less to inspect or evaluate product than others. This section describes a set of dimensional criteria for components, land patterns, positional accuracy of the component placement capability and the opportunity to create a certain size solder joint commensurate with reliability or product performance analysis.

Sections 8.0 through section 13.0 define the specific details of various electronic and electromechanical component families. Each section describes the mounting dimensions for the component and the specific land pattern that may be used to surface mount that particular component or component family. In addition, an analysis is made to establish the land pattern sizes that take into account the accuracy of the placement operation and requirements for the solder joint.

Profile tolerances are used in the dimensioning system to control the size range between maximum and minimum component/lead dimensions without ambiguity. The profile tolerance is intended to control both size and position of the land. Figure 3–3 shows the profile tolerancing method.

The use of the profile dimensioning system requires an understanding of the concepts detailed in ANSI Y14.5. The use of a set of requirements are adopted and invoke the following rules, unless otherwise modified.

Table 3-1 Terminal Position Prefixes

Code	Name	Position (see notes 1 and 2)
A	Axial	Terminal extend from both ends in the direction of the major axis of a cylindrical or elliptical package.
B	Bottom	Terminals beneath the seating plan of the package.
D	Dual	Terminals on opposite sides of a square or rectangular package or located in two parallel rows.
E	End	Terminals are package endcaps having circular or elliptical cross section.
L	Lateral	Terminals are on the four sides of a square or rectangular package. The preferred name is "Quad," code Q.
P	Perpendicular	Pins are perpendicular to seating plan on a square or rectangular package. Restrict to PGA family.
Q	Quad	Terminals are on the four sides of a square or rectangular package or located in four parallel rows.
R	Radial	Terminals extend radially from the periphery of a cylindrical or spherical package
S	Single	Terminals are on one surface of a square or rectangular package in a single row.
T	Triple	Terminals are on three sides of a square or rectangular package.
U	Upper	Terminals are perpendicular to and opposite the seating plane, and are on one surface of a package.
X	Other	Terminal positions other than those described.
Z	Zig-zag	Terminals are on one surface of a square or rectangular package arranged in a staggered configuration. Restrict to ZIP family.

NOTE 1: These descriptions assume the seating plane is the bottom of the package.

NOTE 2: Reference to package shape does not take into account flanges, notches, or irregularities.

Table 3-2 Package-Outline-Style Codes

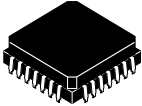
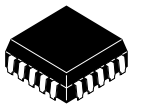
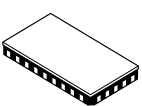
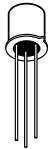
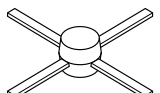
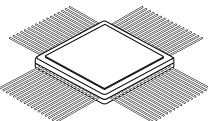
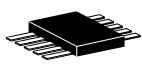
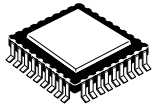
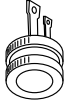
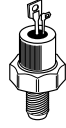
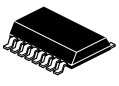
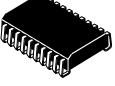
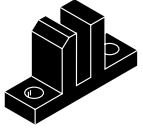
Code	Outline Style
CC	Chip-carrier package
CY	Cylinder or can package
DB	Disc-button package
FM	Flange-mount package
FO	Fiber-optic-device package
FP	Flatpack package
GA	Grid-array package
IL	In-line package. The preferred designator is IP
IP	In-line package or inserted package. Restrict to DIP/SIP/ZIP.
LF	Long-form horizontal package.
MA	Microelectronic assembly.
MW	Microwave package
PF	Press-fit package
PM	Post-/stud-mount package
SO	Small-outline package
SS	Special-shape package
UC	Uncased chip
XA-XZ	Nondefiend family; vendor or user option.

- All dimensions are basic (nominal)
- Limits of size control form as well as size.
- Perfect form is required at maximum dimensions.
- Datum references and position tolerances apply at maximum dimensions, and are dependent on feature size.

- Position dimensions originate from maximum dimensions.
- Tolerances and their datum references other than size and position apply regardless of feature size (RFS).
- Interpretations are per ANSI Y14.5.

The dimensioning concepts used for this system of analysis consider the assembly/attachment requirements as their major goal. Specification (data) sheets for components or dimensions for land patterns on boards may use different dimensioning concepts, however, the goal is to combine all concepts into a single system. Users are encouraged to establish the appropriate relationship between their dimensioning system(s) and the profile dimensioning system and analysis concepts described herein to allow for ease of tailoring these concepts for robust process performance. As an example, if the tolerance used for positioning is larger than the machine tolerance used in production, a single dimensional change in a "spread sheet" program could modify the land pattern dimensions shown in sections 8.0 through 13.0 in order to optimize the process for a given facility.

3.3.1 Component Tolerancing The component manufacturers and the Electronic Industries Association (EIA) are responsible for the dimensioning and tolerancing of electronic components. Their concepts have been converted to a functional equivalent using the profile tolerancing method with all components shown with their basic dimensions as limit dimensions (maximum or minimum).

Package Outline Style and Code	Examples
CC Chip Carrier	    PQCC PQCC (PLCC) PQCC (CLCC) PQCC (CLCC)
CY Cylinder	   MBCY MBCY PBCY
DB Disk Button	    PADB LRDB GRDB PRDB
FP Flatpack	   CQFP CDFP PQFP
PF Press Fit	 MUPF
PM Post/Stud Mount	   MUPM MUPM CRPM
SO Small Outline	   PDSO PDSO PSSO
SS Special Shape	 PDSS

IPC-782-3-1

Figure 3-1 Examples of typical package styles and package descriptive designators

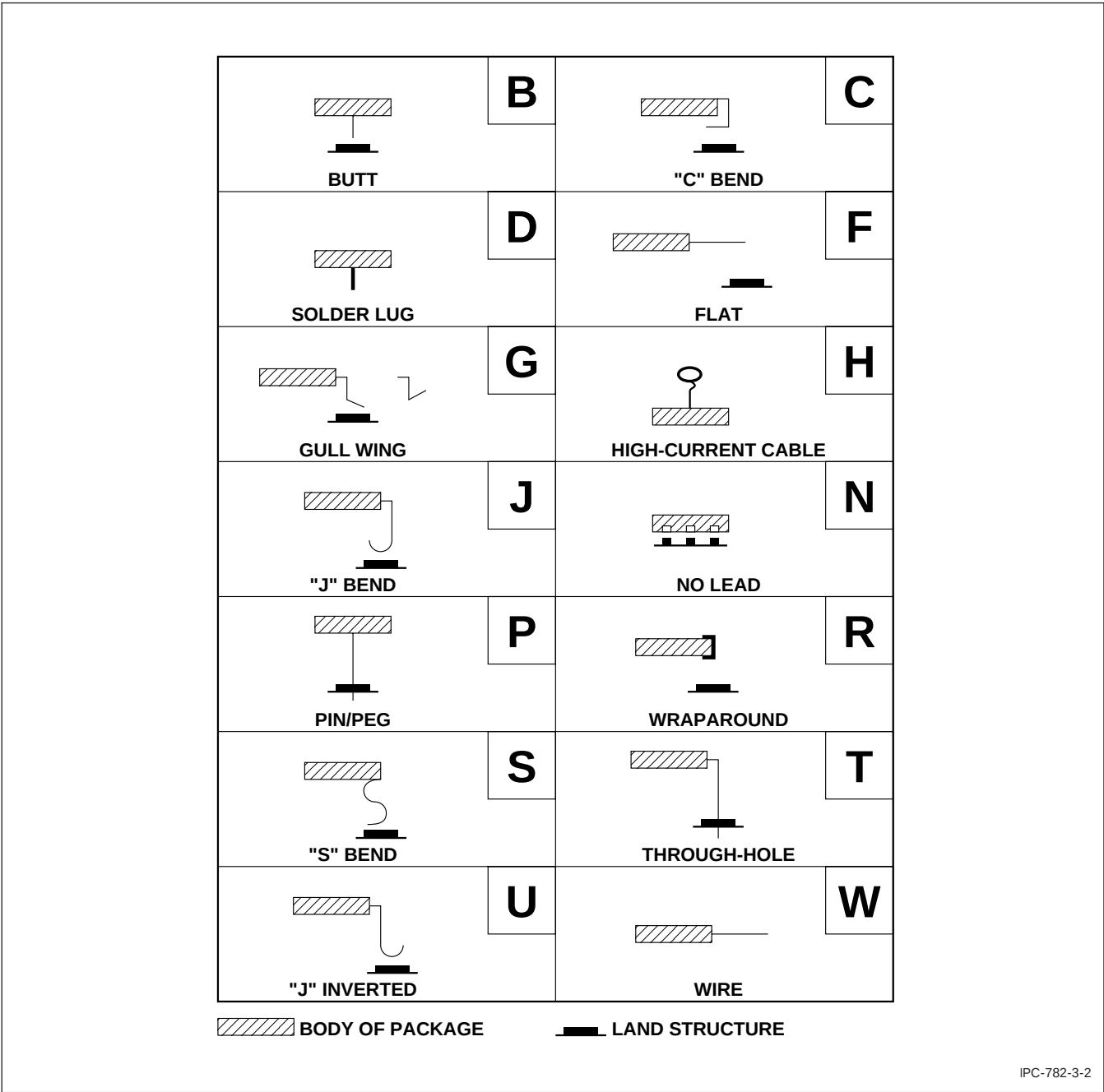


Figure 3-2 Lead-form (or terminal-shape) examples

Profile tolerances are unilateral, and are described to reflect the best condition for solder joint formation usually at minimum component size. As the profile tolerance moves in this unilateral direction toward maximum component size, the opportunity for a robust solder joint decreases.

The concept for component dimension evaluations is based on evaluating the surfaces of the component termination and component lead that are involved in the formation of the acceptable solder joint. Component manufacturers usually provide dimensions for their parts with a nominal size and then put a tolerance on that nominal dimension. Inor-

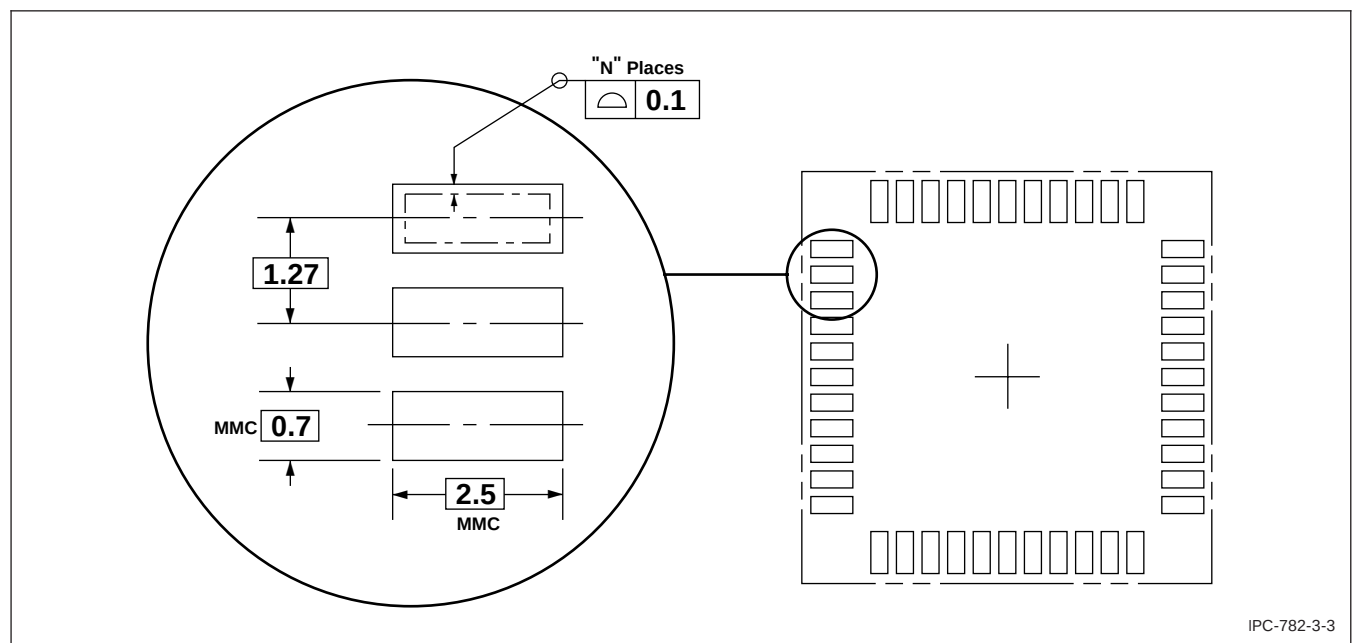
der to facilitate the dimensioning system, these dimensions and their associated tolerances are converted to minimum and maximum size.

As an example, capacitor C1206 has a manufactured nominal dimension for its length (L) of 3.2 mm. The tolerance described by the manufacturer is ~ 0.2 mm. Thus, the minimum dimension of “L” is 3.0 mm with a unilateral tolerance of 0.4 mm, resulting in its maximum dimension being 3.4 mm.

Figure 3-4 shows the characteristics for the C1206. Figure 3-4a shows the component manufacturers dimensions.

Table 3-3 Lead-Form (or Terminal-Shape) Suffixes

Code	Form/Shape	Description (see Figure A2)
B	Butt	A noncompliant lead intended for attachment perpendicular to the land structure.
C	"C" bend	A "C" shaped noncompliant lead bent down and under the body of the package.
D	Solder lug	A lug terminal on the package
F	Flat	A noncompliant, nonformed flat lead that extends away from the body of the package.
G	Gull wing	A compliant lead bent down from the body of the package with a foot at the end pointing away from the package.
H	High-current cable	A lug terminal at the end of a flexible lead.
J	"J" bend	A "J" shaped compliant or noncompliant lead bent down and back under the body of the package.
N	No lead	Metallized terminal pads located on the body of the package.
P	Pin/Peg	A tempered lead extending from the body of the package and intended for attachment to a plated through-hole in the land structure.
R	Wraparound	A metallized noncompliant terminal wrapped around the package body.
S	"S" bend	An "S" shaped compliant lead bent under the body of the package.
T	Through-hole	A terminal with flat or V-shaped cross section intended for attachment to a plated through-hole in the land structure.
U	"J" inverted	A "J" shaped compliant or noncompliant lead bent down from the body of the package with the curved end pointing away from the package.
W	Wire	An untempered wire lead extending from the body of the package.
X	Other	A lead form or terminal shape other than those defined.



IPC-782-3-3

Figure 3-3 Profile tolerancing examples

the length of the capacitor. Figure 3-4b shows the component length at its minimum size in the converted dimensions of the new system using profile tolerancing. Figure 3-4c shows the land pattern at its maximum size. These conditions provide for an optimum toe fillet. For optimum heel fillet the component basic dimensions are at the maximum and the land pattern is at its minimum.

Similar concepts are applied to leaded surface mount parts. The critical dimensional characteristics identified are those that relate to the formation of the toe and heel solder fillet.

For components with gull wing leads the basic dimensions apply across the outer extremities of the part for toe solder fillet formation; and within the inside of the formed radius of opposing leads for heel solder fillet formation.

The outer dimensions of leaded or even leadless chip carriers are usually easy to determine since these are readily available from the component manufacturer. The inner (heel-to-heel) dimensions are not provided in industry standards or manufacturer's specifications, and are more difficult to determine, not only because of the difficulty of

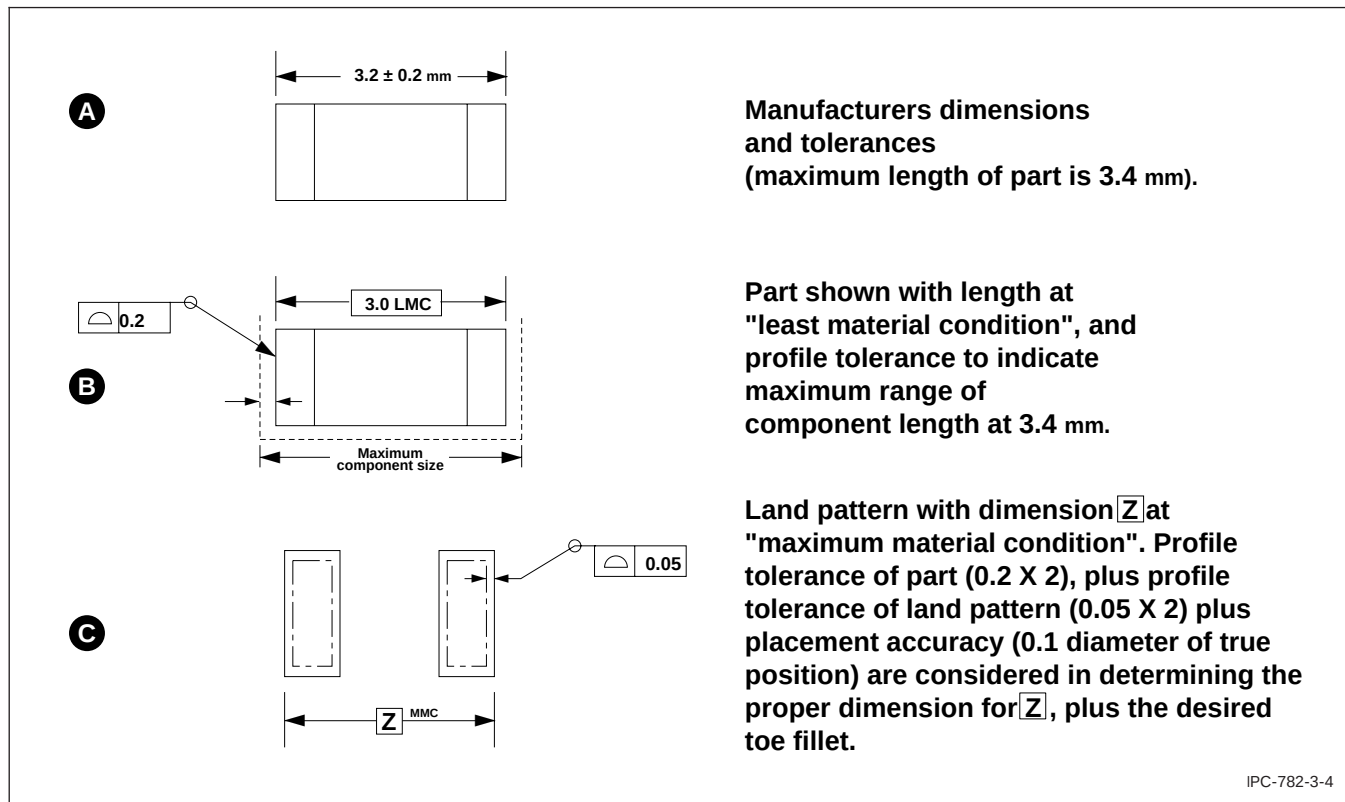


Figure 3-4 Example of C1206 capacitor dimensioning for optimum solder fillet conditions

termination, or castellation; but also because the inner dimensions must be derived by subtracting the sum of the dimensions of the leads (with all their inherent tolerances) from the overall dimensions of the part.

Figure 3-5a shows the concept for the manufacturers dimensions and tolerances for a gull-wing SOIC. Figure 3-5b shows the converted dimensions to be considered in the overall mounting system requirements. Figure 3-5c shows the land pattern dimensions. The basic dimensions define the minimum length as measured across the two outer extremities. Tolerances increase this dimension to the maximum width, reducing toe fillet opportunity. The inner dimensions between heel fillets on opposing sides are the most important. Inner dimensions are derived by:

- Establishing the maximum width of the component as measured from lead termination to lead termination. (This dimension is shown as "L," and is provided by the manufacturer).
- Establishing the minimum amount of the lead length as measured across the "footprint" (from heel to toe for gull-wing leads). (This dimension is "T," and is provided by the manufacturer).
- Subtracting twice the minimum lead length of (b) from the maximum overall component length of (a) to arrive at the maximum length inside the leads across the length of the component (the inner dimension between oppos-

ing heel fillets). Including the tolerances on dimensions (a) and (b) will yield the minimum dimension between opposing heels. This signifies worst case tolerance analysis.

- Three sets of tolerances are involved in the analysis described in (c.); tolerances on the overall component, plus the tolerances for the lead on each end. Since not all three tolerances are considered at their worse case, a recommended method for determining the statistical impact is to summarize the squares of the tolerances and take the square-root of their sum as the rms (root-mean-square) tolerance difference.

For example:

$$\text{RMS tolerance accumulation} = \sqrt{(L_{\text{tol}})^2 + 2(T_{\text{tol}})^2}$$

Where:

$$L_{\text{tol}} = L_{\text{max}} - L_{\text{min}}$$

$$T_{\text{tol}} = T_{\text{max}} - T_{\text{min}}$$

As an example, the SOIC with 16 leads has the following limits for the "L" (component length) and "T" (terminal length) dimensions:

$$L_{\text{min}} = 5.8 \text{ mm}, L_{\text{max}} = 6.2 \text{ mm}$$

$$L_{\text{tol}} = L_{\text{max}} - L_{\text{min}} = 6.2 - 5.8 = 0.4 \text{ mm}$$

$$T_{\text{min}} = 0.4 \text{ mm}, T_{\text{max}} = 1.27 \text{ mm}$$

$$T_{\text{tol}} = T_{\text{max}} - T_{\text{min}} = 1.27 - 0.4 = 0.87 \text{ mm}$$

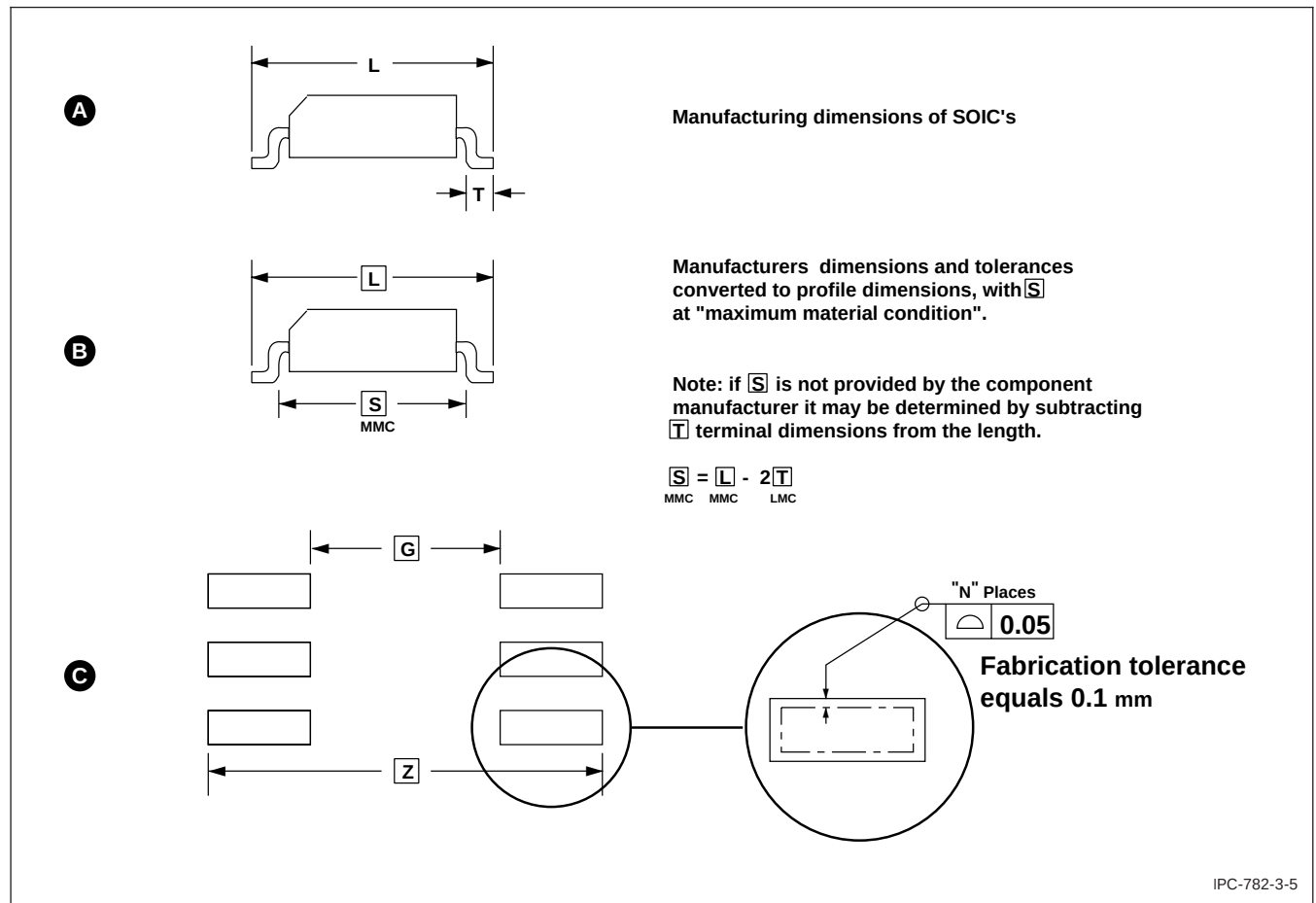


Figure 3-5 Profile dimensioning of a gullwing leaded SOIC

Therefore, the calculations for "S" minimum and maximum dimensions are as follows:

$$S_{\min} = L_{\min} - 2T_{\max} = 5.8 - 2(1.27) = 3.26$$

$$S_{\max} = L_{\max} - 2T_{\min} = 6.2 - 2(0.4) = 5.4 \text{ mm}$$

$$S_{\text{tol}} = S_{\max} - S_{\min} = 5.4 - 3.26 = 2.14 \text{ mm}$$

The difference between $S_{\min}$ and $S_{\max}$ is 2.14 mm, which is probably a larger tolerance range than the actual range within which these components are manufactured. This worst-case scenario for the tolerance range for "S" can also be calculated by adding the tolerances for the component length and the two terminals:

$$S_{\text{tol}} = L_{\text{tol}} + 2T_{\text{tol}} = 0.4 + 2(0.87) = 2.14 \text{ mm}$$

In order to arrive at a more realistic tolerance range, the RMS (root-mean-square) value is calculated using the tolerances on the dimensions involved ("L" and "T"):

$$S_{\text{tol}} (\text{rms}) = (L_{\text{tol}})^2 + 2(T_{\text{tol}})^2 = \sqrt{0.4^2 + 2(0.87)^2} = 1.29 \text{ mm}$$

$S_{\text{tol}} (\text{rms})$ is added to $S_{\min}$ to arrive at a maximum "S" dimension. This technique is used so that a more realistic $S_{\max}$ dimension is used in the land pattern equations for calculating $G_{\min}$ (minimum land pattern gap between

heel fillets). In this example, the following calculation is used for $S_{\max}$:

$$S_{\max} (\text{rms}) = S_{\min} + S_{\text{tol}} (\text{rms}) = 3.26 + 1.29 = 4.55 \text{ mm}$$

To determine the $G_{\min}$ dimension for the land pattern, $S_{\text{tol}} (\text{rms})$ is used for the component tolerance (i.e., $S_{\text{tol}} (\text{rms}) = "C"$). The calculations for $G_{\min}$ are as follows:

$$G_{\min} = S_{\max} - 2J - \sqrt{C^2 + F^2 + P^2}$$

Where:

$J = 0.5 \text{ mm}$ (target heel fillet)

$C = S_{\text{tol}} (\text{rms}) = 1.29 \text{ mm}$ (see above calculations from component dimensions)

$F = 0.1 \text{ mm}$ (assumed fabrication tolerance)

$P = 0.1 \text{ mm}$ (assumed assembly equipment placement tolerance)

Therefore:

$$G_{\min} = 4.55 - 2(0.5) - \sqrt{(1.29)^2 + (0.1)^2 + (0.1)^2} = 2.25 \text{ mm}$$

Another major condition for multiple-leaded components that must be considered in land pattern design is lead, termination, or castellation pitch. The pitch dimension is

basic dimension of the spacing of one component lead termination or castellation to its adjacent counterpart(s). No tolerance is assigned to pitch in the profile dimensioning concept. Differences in pitch shall be included in the width dimensions of the lead, termination, or castellation which are dimensioned as basic at the minimum size.

3.3.2 Land Tolerancing Profile tolerancing is used for lands in a manner similar to that of the components. All tolerances for lands are intended to provide a projected land pattern with individual lands at maximum size. Unilateral tolerances intend to reduce the land size and thus result in a smaller area for solder joint formation. In order to facilitate companion dimension systems the land pattern is dimensioned across outer and inner extremities.

The dimensioning concept in this standard uses limiting dimensions and geometric tolerancing to describe the allowable maximum and minimum dimensions of the land pattern. When lands are at their maximum size, the result is a minimum acceptable space between conductors; conversely when lands are at their minimum size, the result is the minimum acceptable land pattern necessary to achieve reliable solder joints. These thresholds allow for gauging of the land pattern for go/no-go conditions. The whole concept of the dimensioning system described in this document is based on these principles and extends to component mounting dimensions, land pattern dimensions, positioning dimensions etc., so that the requirements may be examined using optical gauges at any time in the process in order to insure compliance with the tolerance analysis.

Figure 3-5 shows the land pattern for an SOIC with gull-wing leads intended to be a companion to the chip component dimensioning concepts shown in Figure 3-4. The basic dimension is across the outer extremities.

Dimension "Z" is at maximum size, while the inner extremities (dimension "G") are dimensioned at minimum size. Unilateral tolerances decreased the basic dimension for "Z" while increasing the basic "G" dimension. This action results in a reduced land pattern, thus processing target values should be as close to the basic "Z" and "G" dimensions as possible. This concept also holds true for the width (X) of the land dimension which is specified at maximum size.

3.3.3 Dimension and Tolerance Analysis In analyzing the design of a component/land pattern system, several things come into play. The size and position tolerances of the component lead or termination, the tolerances of the land pattern, the placement accuracy of the man/machine to center the part to the land pattern, and finally the amount of solder area available for a solder joint for formation of a toe, heel or side fillet.

System equations have been developed for chip components and multiple leaded parts. These concepts assume

that the target values of parts and land patterns are maximized to reflect solder joint formation (i.e., outer dimensions of components at minimum size with outer dimensions of land patterns at maximum size). The equations use the following symbols:

C = the unilateral profile tolerance(s) for the component

F = The unilateral profile tolerance(s) for the board land pattern

P = the diameter of true position placement accuracy to the center of the land pattern

With the assumption that a particular solder joint or solder volume is desired for every component, some methods use the worst case criteria for determining a dimension. This would require that "C," "F," & "P" be added to the minimum dimension of the component length plus the solder joint requirements, in order to determine the maximum dimension of the outer land pattern.

Experience shows that the worst case analysis is not always necessary, therefore statistical methods are used by taking the square root of the sum of the squares of the tolerances. This method assumes that all features will not reach their worst case. The equations for determining chip component land pattern requirements are as follows:

$$Z_{\max} = L_{\min} + 2J_T + \sqrt{C_L^2 + F^2 + P^2}$$

$$G_{\min} = S_{\max} - 2J_H - \sqrt{C_S^2 + F^2 + P^2}$$

$$X_{\max} = W_{\min} + 2J_S + \sqrt{C_W^2 + F^2 + P^2}$$

Where:

Z = Overall length of land pattern

G = Distance between lands of the pattern

X = Width of land pattern

L = Overall length of component

S = Distance between component terminations

W = Width of component

J = Horizontal dimension of solder fillet

J_t = Solder fillet at toe

J_h = Solder fillet at heel

J_s = Solder fillet at side

C = Component tolerances

C_L = Tolerance on component length

C_S = Tolerance on distance between component terminations

C_W = Tolerance on component width

F = Printed board fabrication (land pattern geometric) tolerances

P = Part placement tolerance (placement equipment accuracy)

The formula (the square root of the sum of the squares) is identical for both toe and heel solder joint formation (different tolerances are used, however). However, the same

solder joint dimension and the square root of the sum of the squares are added for outer land pattern dimensions and subtracted for inner land pattern dimensions. The result provides the final land pattern dimensions (Z, G, and X) for chips.

The same concept is true for multiple leaded or leadless components. Additionally, pitch with land-to-lead overlap (M) can be evaluated as well as the space (N) to reflect the clearance between a lead, termination, or castellation and the adjacent land(s). These latter values are not used in the equations to determine the land pattern sizes, but may be used to limit lead-to-adjacent land proximity and to adjust lead-to-land overlap. See Figure 3-6.

The equation for determining if the clearance “N” or the attachment overlap “M” are sufficient is as follows:

$$M = \left[\frac{W + X}{2} \right] - \sqrt{C^2 + F^2 + P^2}$$

$$N = E - \left[\frac{W + X}{2} \right] + \sqrt{C^2 + F^2 + P^2}$$

3.3.3.1 Tolerance Analysis The following tolerance concepts are used to determine the land patterns for all electronic components. These concepts are detailed in Table 3-4, and reflect the tolerances on the component, the tolerances on the land pattern (on the interconnecting substrate), and the accuracy of the equipment used for placing components.

Solder joint minimums are shown for toe, heel and side fillets. These conditions are minimum, since the equations in 3.3 address the tolerance of component, board, and placement accuracy tolerances (sum of the squares). The minimum solder joint is increased by the amount that the tolerances are not used up.

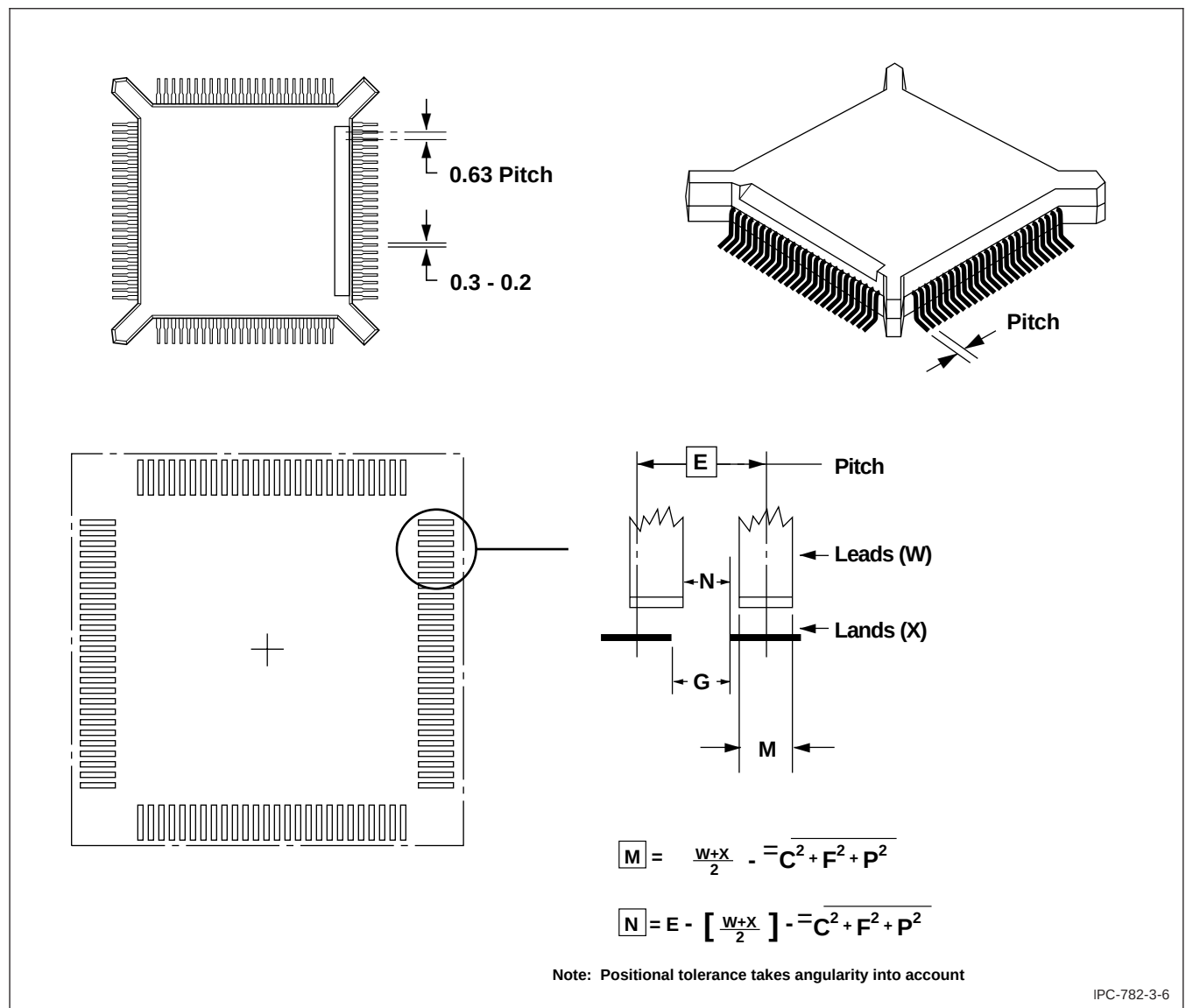


Figure 3-6 Pitch for multiple-leaded components

If the user of these land patterns desires a more robust process condition for placement and soldering equipment, individual elements of the analysis may be changed to new and desired dimensional conditions. This includes component, board or placement accuracy spread as well as minimum solder joint expectations.

Table 3-4 Tolerance Analysis Elements for Chip Devices

Tolerance Element	Detailed Description
Component Tolerance	The difference between the MMC and the LMC of each component dimension, length, width and distance between electrodes or leads. This number is the "C" tolerance in the equations.
Board Tolerance	The difference between the MMC and the LMC of each land pattern dimension. This number is "F" tolerance in the equations.
Positional Accuracy	0.1 – 0.2 mm DTP
Toe Fillet	0.4 – 0.6 mm
Heel Fillet	0.0 – 0.2 mm
Side Fillet Width	-0.02 – 0.02 mm

3.3.3.2 Component Dimensions Illustrations of component dimensions beginning in each component section are accompanied by table of figures for each of the different part numbers, as taken from EIA-PDP-100, JEDEC-95 and other world wide component standards.

EIA-PDP-100 is a catalogue listing of outline drawings illustrating the dimensions of supplier registered passive components; JEDEC-95 as the outlining document for solid state products. At times, the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturers data sheet. Usually, this occurs when industry component specification ranges are so broad that they defy good surface mount design principles. When this action is taken, the tolerance is indicated with an asterisk (*).

Component dimensions are provided according to the concepts of maximum and least materials condition (MMC and LMC). Both conditions are presented in the tables. The component manufacturer may not always dimension his component in accordance with the limits shown in the tables, however, these limits may be used as a gauge for go/no-go acceptance of the component. The LMC dimensions of the figure are those that have been used in the equations described in 3.3 for determining the recommended land pattern.

Dimensions that have had their tolerance spread reduced are so indicated in the tables. Parts that are available with shape characteristics or tolerance limits that fall outside the recommended norms require land patterns that must be altered slightly from those presented.

Users of these specialized parts are encouraged to develop their own land patterns which then become unique to a specific component vendor part. A dimensioning system with specific equations has been provided to facilitate unique land pattern development or enhance process usage.

3.3.3.3 Land Pattern Dimensions Land pattern dimensions are provided according to the concepts of maximum material conditions (MMC). Sometimes a dimension is presented as a minimum distance. This occurs when defining a space(s) that exists between lands at MMC. The printed board manufacturer may not always inspect his board in accordance with the limit concepts shown in the table. However, these limits may be used as a gauge for go/no-go acceptance of the printed board land pattern. The dimensions shown in each table are those that have been used in the equations described in 3.3 for determining the recommended land patterns.

All land patterns are designed to be transparent to the soldering process to be used in manufacturing. This reduces the number of land sizes in the component library, and is less confusing for the designer, but may not be the most robust for the placement or the soldering process.

3.3.3.4 Land Pattern Registration Each land pattern has received a registration number. The RLP (Registered Land Pattern) number is a three digit number with a set of numbers assigned to land patterns for a particular family of components. The original number assigned to a particular component, uses that analysis shown for the specific section (sections 8 through 16). The analyses assume certain tolerances for board fabrication, placement machine accuracy and minimum desired solder joint. Changes in the assumptions will result in a revision letter to the number. Thus the first change to RLP 106 would be identified as RLP 106A, the second change would be RLP 106B etc.

The letters x, y & z are reserved for user modifications to the standard land pattern. If a company wishes to change the approved standard land pattern the user would identify his customized version as RLP 106X, RLP 106Y or RLP 106Z. It should be recognized that X, Y & Z type RLP's reflect unique land patterns and will differ company to company. The number reservations are shown in Table 3-5.

Not every RLP is assigned in Sections 8 through 16, however all three digit number from 100 to 999 are reserved as IPC standard RLP numbers. Users of the system may enhance their computer libraries by tailoring the IPC RLP's (adding X, Y or Z), using numbers 001 to 099 or using four digit numbers to describe their custom standard land patterns. The letter "W" may be used to signify a special user pattern signifying that it is for wave soldered attachment application (i.e. RLP 102 defines as RLP 102W).

Table 3-5 RLP Numbers

IPC-SM-782 Section	Component Type	Reserved Registered Land Pattern Numbers
8.1	Chip Resistors	100 to 129
8.2	Chip Capacitors	130 to 159
8.3	Inductors	160 to 179
8.4	Tantalum Capacitors	180 to 199
8.5	Metal Electrode Face Components (MELFS)	200 to 209
8.6	Small Outline Transistor (SOT) 23	210 to 214
8.7	Small Outline Transistor (SOT) 89	215 to 219
8.8	Small Outline Diode (SOD) 123	220 to 224
8.9	Small Outline Transistor (SOT) 143	225 to 229
8.10	Small Outline Transistor (SOT) 223	230 to 234
8.11	Modified Through-Hole Component (TO) 252	235 to 239
9.1	Small Outline Integrated Circuits (SOIC)	300 to 329
9.2	Small Outline Integrated Circuits (SSOIC)	330 to 359
9.3	Small Outline Package Integrated Circuit (SOPIC)	360 to 389
9.4	Thin Small Outline Package (TSOP)	390 to 419
9.5	Ceramic Flat Pack (CFP)	420 to 459
10.1	Small Outline with "J" Leads (SOJ)	480 to 529
11.1	Plastic Quad Flat Pack (PQFP)	530 to 549
11.2	Shrink Quad Flat Pack, Square (SQFP)	550 to 579
11.3	Shrink Quad Flat Pack, Rectangular (SQFP)	580 to 629
11.4	Ceramic Quad Flat Pack (CQFP)	630 to 649
12.1	Square Plastic Leaded Chip Carrier (PLCC)	700 to 719
12.2	Rectangular Plastic Leaded Chip Carrier (PLCC)	720 to 739
12.3	Leadless Ceramic Chip Carrier (LCC)	740 to 759
13.1	Modified Dual-In-Line Pin Components (DIP)	760 to 779
14.1	Ball Grid Arrays (BGA)	900 to 1069
14.2	Plastic Rectangular Ball Grid Arrays	1080 to 1082

3.3.4 Dimension Tailoring The concepts indicated in this section are reflected in the individual component/land pattern section of this document, sections 8.0 onward. In each instance, the tolerances used for C, F, or P are identified as well as the desired solder joints—"J." At times the component tolerances or component gauge requirements do not necessarily reflect the exact tolerance on a manufacturer's data sheet. Usually this occurs when industry component specification ranges are so broad that they defy good surface mount design principles. When the action to modify the tolerance range is taken, the tolerance "C" is indicated with an asterisk (*).

In addition, solder joint formation has been considered as being transparent to the soldering process or equipment used for mass reflow solder processes. This technique facilitates a single land pattern for the computer aided design (CAD) system and allows the assembly to be processed by more than one type of assembly operation. As designs become more complex with denser component/

land pattern geometries, the land patterns may have to be customized for specific components, and assembly processes, in order to make the entire process more robust and increase first pass defect-free assembly yields.

Users are encouraged to follow the equation principles defined in this section and in sections 8.0 onward. Maintaining the data in computer "spread sheet" formats will facilitate ease of modification to specific land pattern requirements for process yield improvements.*

Note: Electronic media (3.5 in disk) containing Lotus spreadsheets are available with instructions for use. They are identified as IPC-EM-782, "Land Pattern Data Analysis Spreadsheets for IPC-SM-782 Land Patterns."

3.4 Design for Producibility As part of the planning cycle of a product's development, a concurrent engineering task group should be assembled to determine the criteria for each new design. During this planning phase, the product function and configuration is clearly defined and the

assembly process options outlined. Product size, component types, projected volume and the level of manufacturing equipment available may affect process options.

Following the substrate development, the assembly will be evaluated for many of the fundamentals necessary to insure a successful SMT process. Specific areas addressed during the evaluation will include:

- Land pattern concepts
- Component selection
- Mounting substrate design
- Need for testability
- Phototool generation

3.4.1 SMT Land Pattern The use of process proven land patterns for the solder attachment of surface mount devices will provide a benchmark to evaluate solder joint quality. Land pattern geometry and spacing utilized for each component type must accommodate all physical variables including size, material, lead contact design and plating.

3.4.2 Standard Component Selection Whenever possible, SMT devices should be selected from standard configurations. The standard components will be available from multiple sources and will usually be compatible with all assembly processes. For those devices developed to meet specific applications, standard packaging is often available. Select a package type that will be similar in materials and plating of standard device types when possible.

3.4.3 Circuit Substrate Development Design the circuit substrate to minimize excessive costs. Surface Mount Technology often pushes the leading edge of substrate technology. When estimating circuit density, allow for the greatest latitude in fabrication processes and tolerance variables. Before adopting extreme fine line and utilizing small plated holes, understand the cost impact, yield, and long-term reliability of the product.

3.4.4 Assembly Considerations Other factors that will impact manufacturing efficiency include component placement. Maintaining a consistent spacing between components, common orientation or direction of polarized devices will impact all steps of the assembly process. In addition, when common orientation is maintained, machine programming is simplified and component verification, solder inspection and repair are simplified.

3.4.5 Provide for Automated Test Testability of the assembled circuit substrate must be planned well in advance. If component level testing is necessary, one test probe contact area is required for each common node or net. Ideally, all probe contact pads are on one side. Provide

grid-based test nodes to accommodate standard probes. Functional testing may also employ the same test nodes used for in-circuit test but will include all connectors that interface to cables and other assemblies.

3.4.6 Documentation for SMT Documentation used to fabricate the circuit substrate and assemble the product must be accurate and easy to understand. Details, specifications and notes will guide both the assembly processing and control the quality level of a product. Unique materials or special assembly instructions should be included on the face of the detail drawings or included in the documentation package.

3.5 Environmental Constraints

3.5.1 Handling Moisture Sensitive Components Several large plastic packages may be susceptible to absorbing moisture. The component manufacturer usually packages these parts with a desiccant, and provides instruction for use or maintaining those parts in a controlled storage environment. See J-STD-020 and J-STD-033 for instructions and proper handling and testing procedures.

3.5.2 Usage Environments In Table 3–6, worst-case, but realistic, use environments for SM electronic assemblies are shown in nine major use categories. These use environment categories are listed in order of increasing severity, without consideration of the number of expected service years. It should be noted that the cyclic temperature range, delta T, is not the difference between the possible minimum, T_{min}, and maximum, T_{max}, operational temperature extremes; delta T is significantly less. It has to be recognized that these temperature extremes are possible only during different times of the year, and then only at significantly different geographic locations. The delta T values represent the temperature swings that typically can be expected during a given operating cycle.

Also given are the expected dwell durations at operating temperatures; they are significant because they determine the degree of completeness of the stress relaxation in the solder joints and thus determine the amount of cyclic fatigue damage relative to the maximum fatigue damage at complete stress relaxation. Table 3–6 also gives estimates of the number of operating cycles occurring during a service year. For some of the use categories, the use environments are described in terms of the sum of multiple use environments resulting from either significant seasonal dependence or broadly foreseeable use conditions; the military avionics category is subdivided into three subcategories reflecting differing use conditions due to type of aircraft, mission profile, geographic effects, etc. The space category contains two different environments for satellites in low-earth orbit (LEO) or geo-synchronous (stationary relative to earth) orbit (GEO).

3.5.3 Service Life The design service life, N , can vary significantly for the use categories in Table 3–6. The design service lives can range from less than one year, barely exceeding the warranty period for consumer products, to 20 years or more for telecommunications equipment and commercial aircraft. For some military applications the service life is measured in thousands of hours.

3.5.4 Acceptable Cumulative Failure Probability The acceptable cumulative failure probability, $F(N)$, at the end

of the design service life, N , can vary significantly depending on the specific purpose of the product, the complexity (number and mix of components) of the product, and perhaps the design service life. $F(N)$ values could range from 1 ppm for products whose failure has critical consequences, e.g., cardiac pacemakers, to perhaps 10,000 ppm (1%) for consumer products or products which provide redundancy or “limp-home capability” in case of electrical system failure. (See IPC-SM-785).

Table 3–6 Worst-Case Environments and Appropriate Equivalent Accelerated Testing

USE CATEGORY	WORST-CASE USE ENVIRONMENT						ACCELERATED TESTING				
	Tmin °C	Tmax °C	$\Delta T^{(1)}$ °C	t_D hrs	Cycles/ year	Typical Years of Service	Approx. Accept. Failure Risk, %	Tmin °C	Tmax °C	$\Delta T^{(2)}$ °C	t_D min
1) CONSUMER	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) COMPUTERS	+15	+60	20	2	1460	5	0.1	+25	+100	75	15
3) TELECOM	-40	+85	35	12	365	7-20	0.01	0	+100	100	15
4) COMMERCIAL AIRCRAFT	-55	+95	20	12	365	20	0.001	0	+100	100	15
5) INDUSTRIAL & AUTOMOTIVE PASSENGER COMPARTMENT	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0.1	0	+100	100 & COLD ⁽³⁾	15
6) MILITARY GROUND & SHIP	-55	+95	40 &60	12 12	100 265	10	0.1	0	+100	100 & COLD ⁽³⁾	15
7) SPACE leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0.001	0	+100	100 & COLD ⁽³⁾	15
8) MILITARY AVIONICS a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0.01	0	+100	100 & COLD ⁽³⁾	15
9) AUTOMOTIVE UNDER HOOD	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0.1	0	+100	100 & COLD ⁽³⁾ & LARGE $\Delta T^{(4)}$	15

& = in addition

- 1) ΔT represents the maximum temperature swing, but does not include power dissipation effects; for power dissipation calculate ΔT ; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, ΔT , is not the difference between the possible minimum, T_{MIN} , and maximum, T_{MAX} , operational temperature extremes; ΔT is typically significantly less.
- 2) All accelerated test cycles shall have temperature ramps <20°C/minute and dwell times at temperature extremes shall be 15 minutes measured on the test boards. This will give ~24 test cycles/day.
- 3) The failure/damage mechanism for solder changes at lower temperatures; for assemblies seeing significant cold environment operations, additional “COLD” cycling, from perhaps –40 to 0°C, with dwell times long enough for temperature equilibration and for a number of cycles equal to the “COLD” °C operational cycles in actual use is recommended.
- 4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain –20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate “LARGE ΔT ” testing with cycles similar in nature and number to actual use is recommended.

3.6 Design Rules During the component selection phase of a design, manufacturing engineering should be consulted regarding any components outside the scope of this document.

The printed board design principles are a statement of current test and manufacturing capabilities. Exceeding or changing these capabilities requires concurrence of all participants in the process including manufacturing, engineering and test technology.

Involving test and manufacturing early in the design helps to move a quality product quickly into production. Figure 3-7 shows a list of concurrent engineering team participants that should be involved.

3.6.1 Component Spacing

3.6.1.1 Component Considerations The land pattern design information discussed so far is important for reliability of surface mount assemblies. However, the designer should not lose sight of manufacturability, testability and repairability of SMT assemblies. A minimum interpackage spacing is required to satisfy all these manufacturing requirements. There is no limit on maximum interpackage spacing; the more the better. Some designs require that surface mount components are positioned as tightly as possible. Based on experience, the examples shown in Figure 3-8 meet manufacturability requirements.

The land to land spacing between adjacent components should be 1.25 mm [0.050 in] clear space all around the edges of printed boards if boards are tested off the connector or 2.5 mm [0.100 in] minimum if vacuum seal for testing is used. The requirements specified herein are recommended minimums excluding conductor geometry tolerances.

3.6.1.2 Wave Solder Component Orientation All polarized surface mount components should be placed in the same orientation, when possible. On any printed board assembly where the secondary side is to be wave soldered, the preferred orientation of devices on that side is described and shown in Figure 3-9. The preferred orientation is used in order to optimize the resulting solder joint quality as the assembly exits the solder wave.

- All passive components shall be parallel to each other.
- All SOICs shall be perpendicular to the long axis of passive components.
- The longer axis of SOICs and of passive components shall be perpendicular to each other.
- The long axis of passive components shall be perpendicular to the direction of travel of the board along the conveyor of the wave solder machine.

3.6.1.3 Component Placement Similar types of components should be aligned on the board in the same orientation for ease of component placement, inspection, and soldering. Also, similar component types should be grouped together whenever possible, with the net list or connectivity and circuit performance requirements ultimately driving the placements. See Figure 3-10. In memory boards, for example, all of the memory chips are placed in a clearly defined matrix with pin one orientation the same direction for all components. This is a good design practice to carry out on logic designs where there are many similar component types with different logic functions in each package. On the other hand, analog designs often require a large variety of component types making it understandably difficult to group similar components together. Regardless if

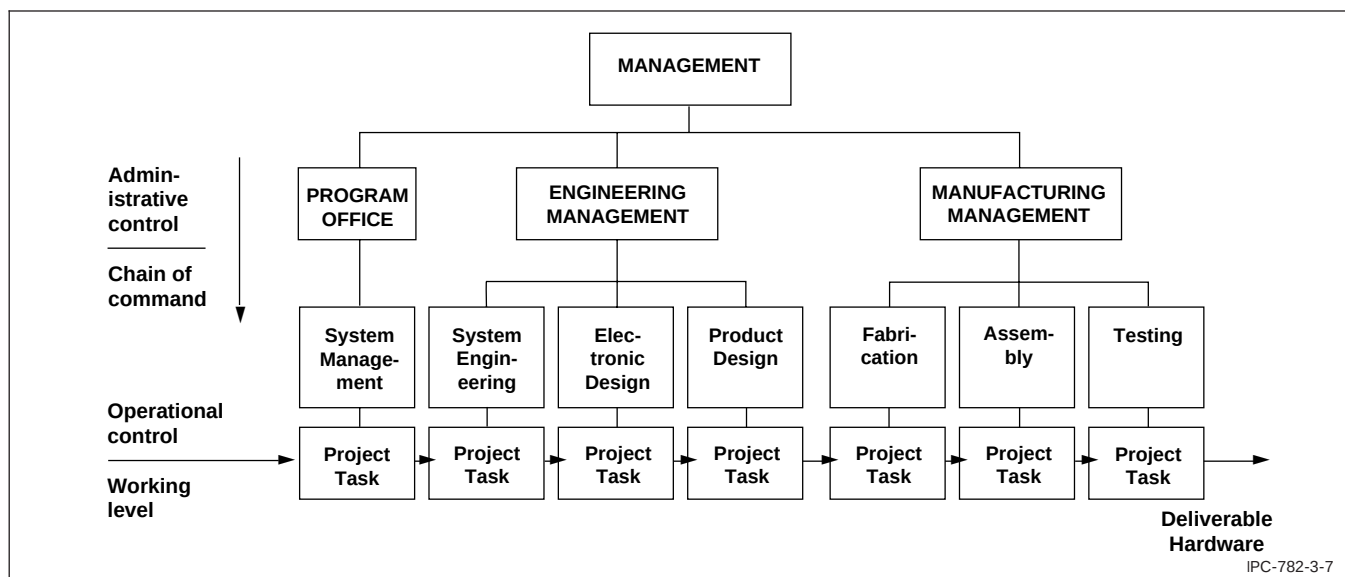


Figure 3-7 Simplified electronic development organization

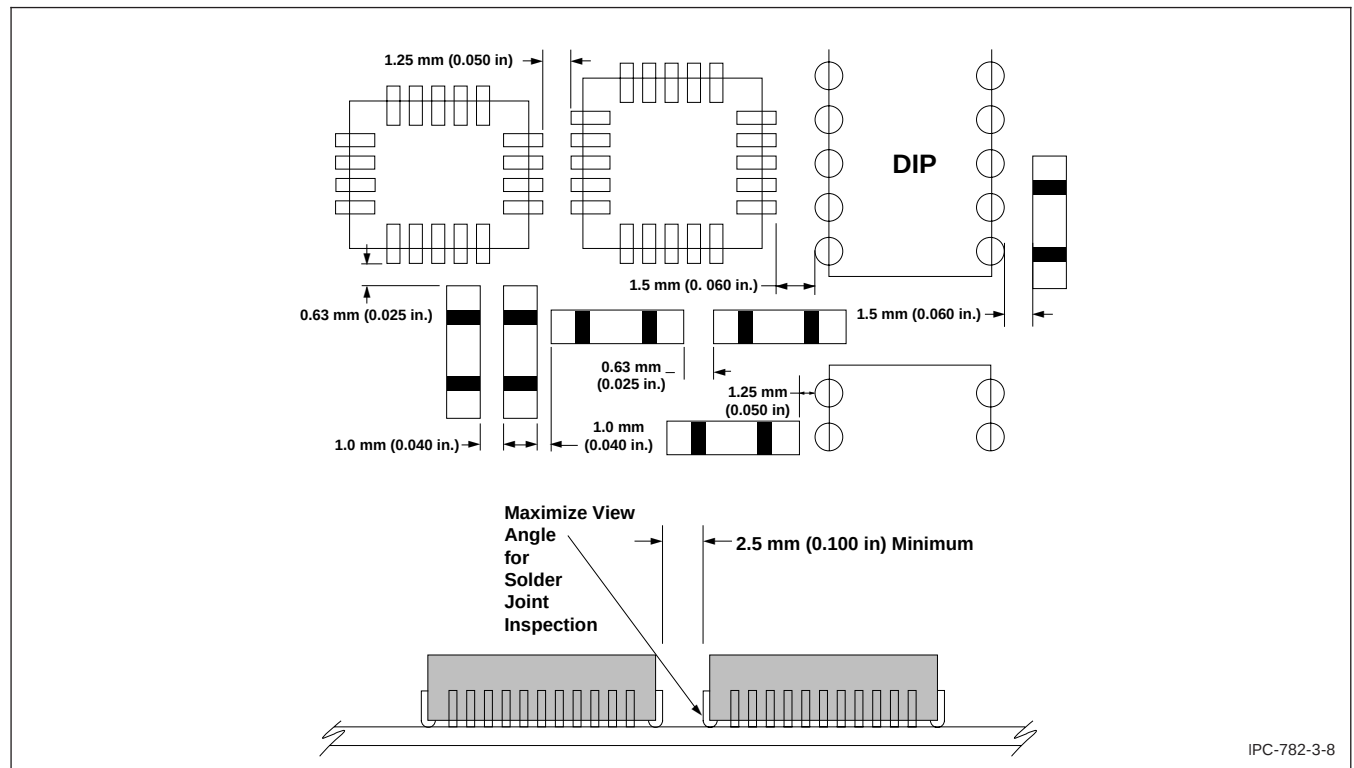


Figure 3-8 Recommended minimum land-to-land clearances

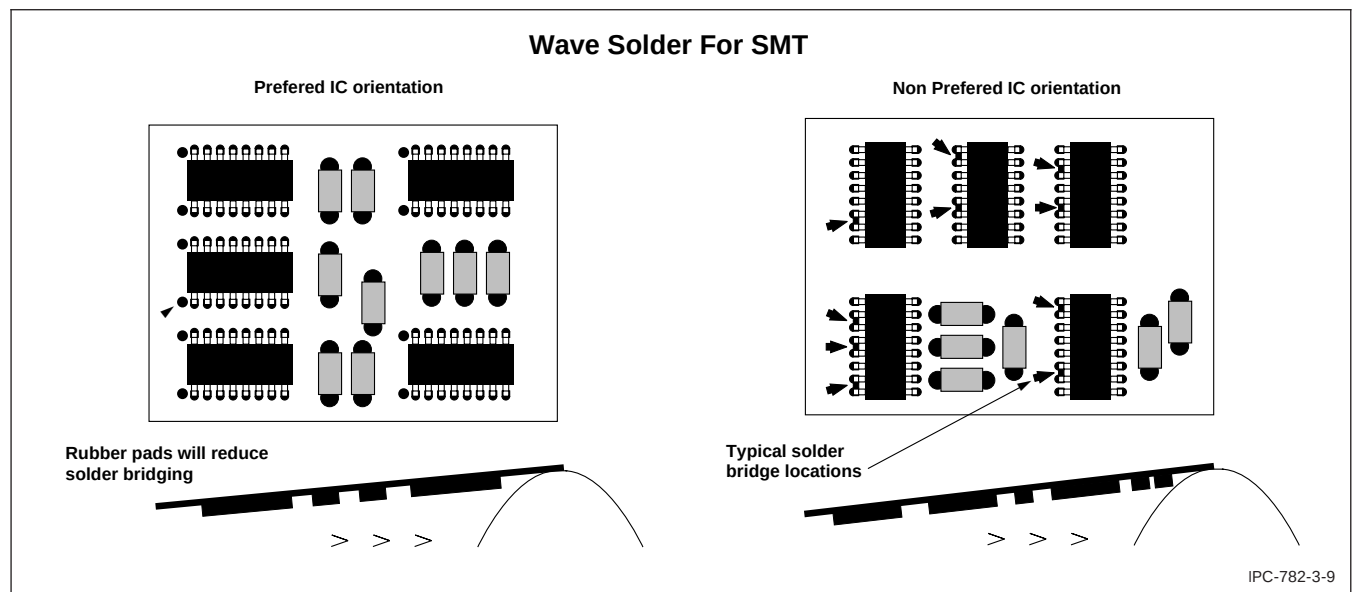


Figure 3-9 Component orientation for wave solder applications

the design is memory, general logic, or analog, it is recommended that all component orientations are such that pin one orientation is the same.

3.6.1.4 Grid-Based Component Placement SMT component placement and orientation is generally more difficult than THT printed boards for two reasons: higher component densities, and the ability to put components on both sides of the board. For THT designs, the component leads

are on 2.54 mm [0.100 in] centers and, assuming 1.3 mm [0.065 in] lands, the spacing between lands would be 1.2 mm. In high density SMT designs, however, the spacing between lands is often less, down to 0.63 mm [0.025 in] and smaller. Grid based component placement (0.100 inch grid is standard with THT) is complicated by the large variety of land sizes associated with the SMT component packages now becoming available. Most SMT designs being done today have abandoned the 2.54 mm [0.100 in]

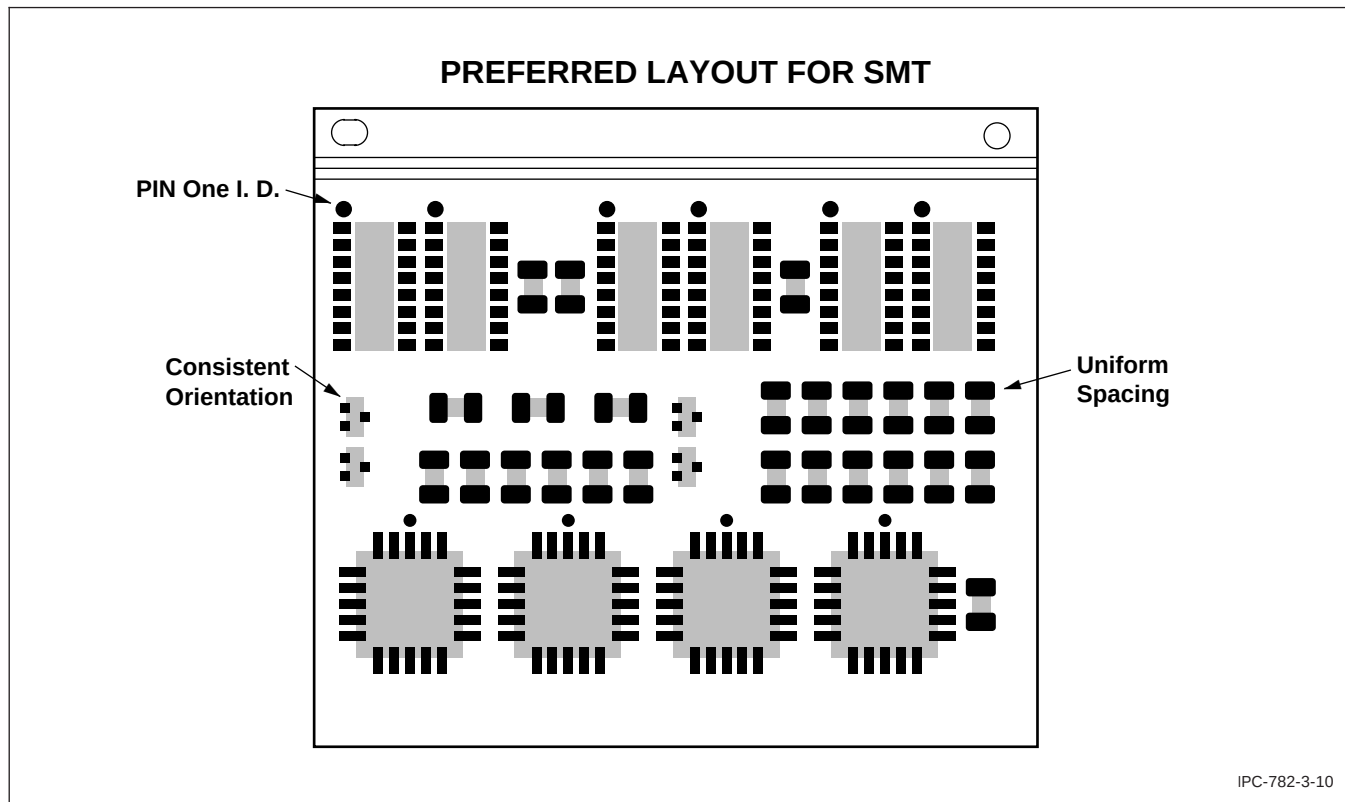


Figure 3-10 Alignment of similar components

grid based placement rules of the THT boards. This ultimately results in components being randomly placed, and vias being even more randomly placed across the board.

Two problems created by random component placement are a loss of uniform grid based test node accessibility and a loss of logical, predictable routing channels on all layers (possibly driving layer counts). In addition the accepted international grid identified in IPC-1902 states that for new designs the grid should be 0.5 mm, with a further subdivision being 0.05 mm. One solution to the problem is to build CAD libraries with all component lands connected to vias on 0.05 mm centers (or greater, based on design) to be used for testing, routing, and rework ports. Then when doing the component placement on the CAD system, simply place the components so that there is a minimum space of 0.5 mm between lands, then snap the vias of the component being placed out to the next 1.0 mm grid point. With this procedure, all of the components should have between 0.4 mm and 0.6 mm (or an average of 0.5 mm) spacing between the lands. From the assembly point of view, it is easier to process a PCB which has the component centroids on a 1.0 mm grid, with approximately equal spacing between all of the lands across the board in both directions.

3.6.1.5 Single vs Double Sided Boards The term single or double sided referred to one or two conductor layers on a printed board prior to the advent of Surface Mount. Now, however, the term single side refers to components

mounted on one side (Type 1 assembly), and the term double refers to components mounted on both sides (Type 2 assembly) of the board. It has been observed that many SMT designers, especially novices, are too quick to place components on the secondary side of the PB, forcing the assembly process to be executed twice instead of once. Designers should concentrate on getting all components on the primary side of the board whenever possible without creating component spacing violations. This will result in a lower assembly cost. If double sided placement is definitely required, then grid-based placement, although more difficult, is even more crucial for accurate final component placement, circuit routability, and testability. Double sided boards using conventional SMT design rules often require double sided, or clamshell test fixtures that are 3 to 5 times the cost of single sided test fixtures. Grid based component placements have been known to improve nodal accessibility as well as eliminate the need for dual sided testing.

3.6.1.6 Solder Stencil Design The solder stencil is the primary vehicle by which solder paste is applied to the SMT printed board. With it, the exact location and volume of solder paste deposition is precisely controlled. The artwork for the stencil generally consists of the component mounting lands from the outer layers of the board with all other circuitry deleted. The openings in the stencil should be the same size as the lands on the board for all components. The printed board assembler may alter the stencil

opening size prior to manufacturing the stencil to change the volume of solder paste which is deposited on the lands.

3.6.1.7 Component Stand Off Height for Cleaning The minimum component stand off height for cleaning is based on the distance across the diagonal of the component. This dimension implies a component surface area that may trap contamination if care is not exercised. Table 3–7 shows the relationship for recommended component standoff distances.

If the minimum stand off cannot be achieved, proper cleaning under the component may not be possible. In this case it is recommended that a no clean flux be used.

3.6.1.8 Fiducial Marks A Fiducial Mark is a printed artwork feature which is created in the same process as the circuit artwork. The fiducial and a circuit pattern artwork must be etched in the same step.

Table 3–7 Component Stand Off

Component Diagonal	Component Surface Area	Component Stand Off
$\leq 50 \text{ mm}$	$\leq 2500 \text{ mm}^2$	$\geq 0.5 \text{ mm}$
$\leq 25 \text{ mm}$	$\leq 625 \text{ mm}^2$	$\geq 0.3 \text{ mm}$
$\leq 12 \text{ mm}$	$\leq 144 \text{ mm}^2$	$\geq 0.2 \text{ mm}$
$\leq 6 \text{ mm}$	$\leq 36 \text{ mm}^2$	$\geq 0.1 \text{ mm}$
$\leq 3 \text{ mm}$	$\leq 9 \text{ mm}^2$	$\geq 0.05 \text{ mm}$

The Fiducial Marks provide common measurable points for all steps in the assembly process. This allows each piece of equipment used for assembly to accurately locate the circuit pattern. There are two types of Fiducial Marks. These are:

A. Global Fiducials

Fiducial marks used to locate the position of all circuit features on an individual board. When a multi image circuit is processed in panel form, the Global Fiducials are referred to as Panel Fiducials when present for the panel. (See Figures 3–11/3–12.)

B. Local Fiducials

Fiducial marks used to locate the position of an individual component requiring more precise placement. (See Figure 3–11.)

A minimum of two global fiducial marks is required for correction of translational offsets (x and y position) and rotational offsets (theta position). These should be located diagonally opposed and as far apart as possible on the circuit or panel.

A minimum of three fiducial marks is required for correction of non linear distortions (scaling, stretch and twist).

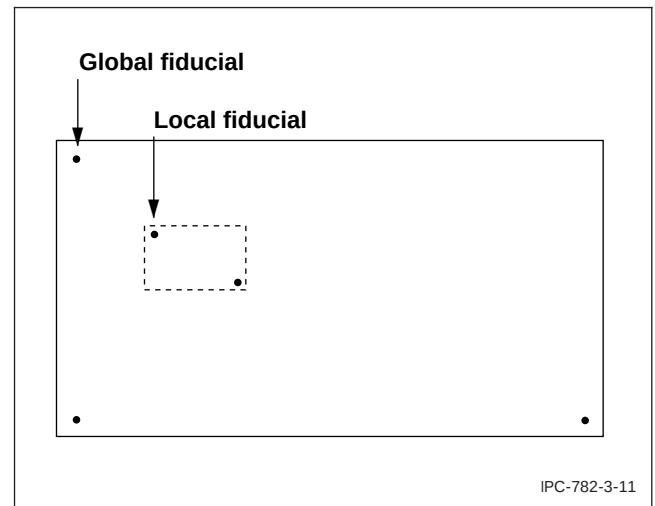


Figure 3–11 Local/global fiducials

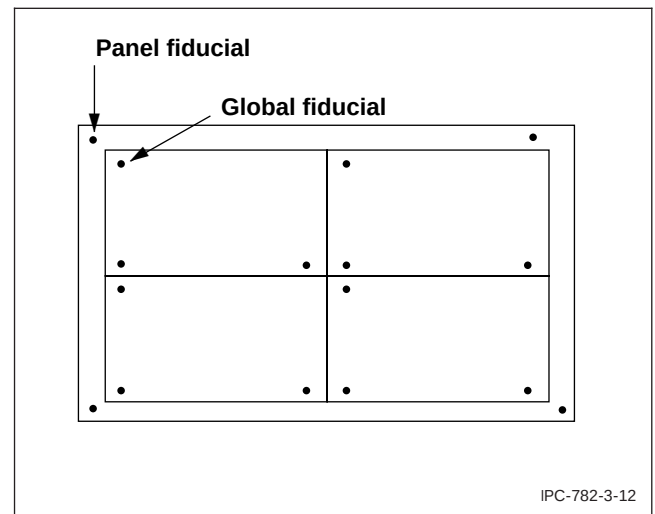


Figure 3–12 Panel/global fiducials

These should be located in a triangular position as far apart as possible on the circuit or panel.

A minimum of two local fiducial marks are required for correction of translational offsets (x and y position) and rotational offsets (theta position). This can be two marks located diagonally opposed within the perimeter of the land pattern.

If space is limited, a minimum of one local fiducial mark may be used to correct translational offsets (x and y position). The single fiducial should be located inside the perimeter of the land pattern with a preference for the center.

The minimum size for local, global or panel fiducials is 1.0 mm. Some companies have chosen a larger fiducial (up to 1.5 mm) for panel fiducials. It is a good practice to keep all fiducials the same size.

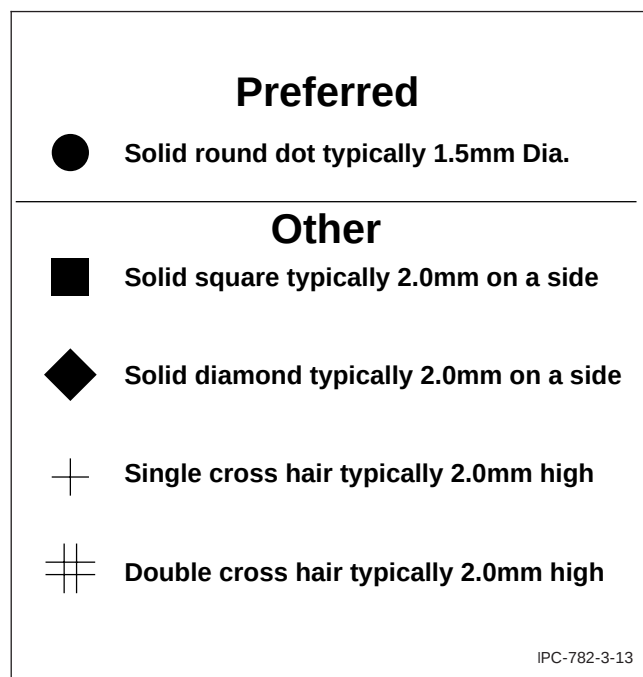


Figure 3-13 Fiducial types for vision systems

3.6.1.9 Fiducial Mark Design Specifications The Surface Mount Equipment Manufacturers Association (SMEMA) has standardized on the design rules for fiducials. These rules are supported by the IPC and consist of:

A. Shape

The optimum fiducial mark is a solid filled circle. See Figure 3-13.

B. Size

The minimum diameter of the fiducial mark is 1 mm [0.040 in]. The maximum diameter of the mark is 3 mm [0.120 in]. Fiducial marks should not vary in size on the same PB more than 25 microns [0.001 in].

C. Clearance

A clear area devoid of any other circuit features or markings shall exist around the fiducial mark. The size of the clear area shall be equal to the radius of the mark. A preferred clearance around the mark is equal to the mark diameter. (See Figure 3-14)

D. Material

The fiducial may be bare copper, bare copper protected by a clear anti oxidation coating, nickel or tin plated, or solder coated (hot air leveled).

The preferred thickness of plating or solder coating is 0.005 mm to 0.010 mm [0.0002 to 0.0004 in]. Solder coating should never exceed 0.025 mm [0.001 in].

If solder mask is used, it should not cover the fiducial or the clearance area. It should be noted that oxidation of a fiducial mark's surface may degrade its readability.

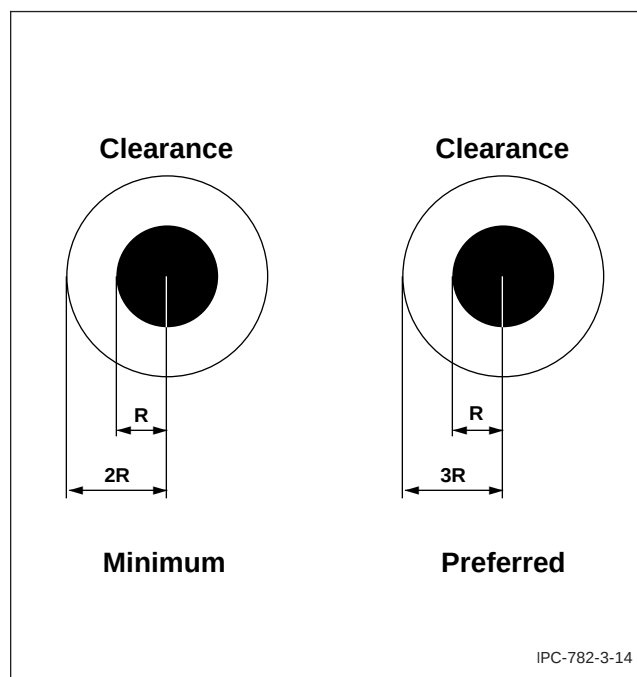


Figure 3-14 Fiducial clearance requirements

E. Flatness

The flatness of the surface of the fiducial mark should be within 0.015 mm [0.0006 in].

F. Edge Clearance

The fiducial shall be located no closer to the PB edge than the sum of 4.75 mm [0.187 in] (SMEMA Standard Transport Clearance) and the minimum fiducial clearance required.

G. Contrast

Best performance is achieved when a consistent high contrast is present between the fiducial mark and the PB base material.

It is good design practice to locate global or panel fiducials in a three point grid based datum system as shown in Figure 3-15. The first fiducial is located at the 0,0 location. The second and third fiducials are located in the X and Y directions from 0,0 in the positive quadrant. The global fiducials should be located on the top and bottom layers of all printed boards that contain Surface Mount as well as Through Hole components since even Through Hole assembly systems are beginning to utilize vision alignment systems.

All Fine Pitch components should have two local fiducials system designed into the component land pattern to insure that enough fiducials are available every time the component is placed, removed and/or replaced on the board. All fiducials should have a soldermask opening large enough to keep the optical target absolutely free of solder mask.

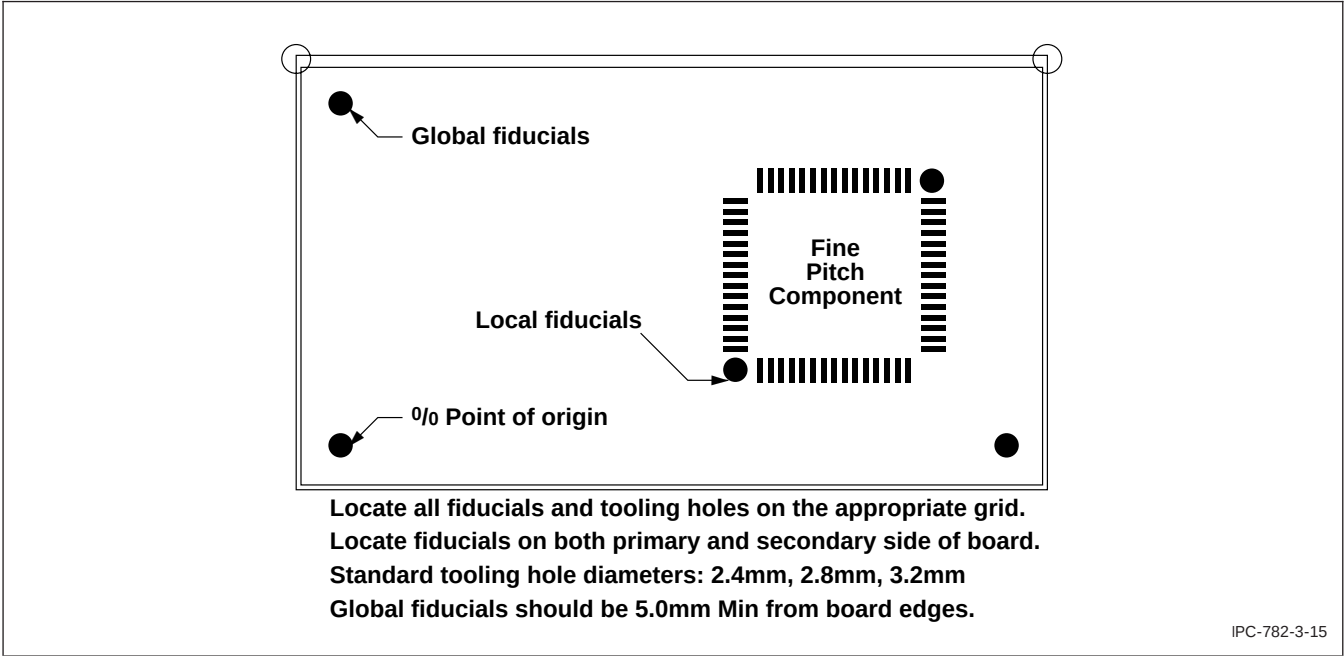


Figure 3–15 Fiducial locations on a printed circuit board

soldermask should get onto the optical target, some vision alignment systems may be rendered useless due to insufficient contrast at the target site.

The internal layer background for all fiducials must be the same. That is, if solid copper planes are retained under fiducials in the layer below the surface layer, all fiducials must have copper retained. If copper is clear under one fiducial, all must be clear.

3.6.2 Conductors

3.6.2.1 Conductor Width & Clearances Increased component density on SMT designs has mandated the use of

thinner conductor density and clearance between conductors with increased PB layer counts requiring the use of more vias to make the necessary connections between the additional layers. Figure 3–16 shows the effects of SMT and Fine Pitch Technology (FPT) on printed board geometries.

Conductor width/clearances of 0.15 mm [0.006 in] have become commonplace today, and have basically replaced the 0.3 mm [0.012 in] line/ space as a commonly used geometry (see Figure 3–17). As more fine pitch (including Tape Automated Bonding) devices are used on printed boards, the 0.125 mm [0.005 in] geometry may be used in more SMT boards to reduce layer counts. Figure 3–18

GEOMETRY	2.54mm Pitch	1.25mm Pitch	0.63mm Pitch
PIN COUNTS	8 TO 64	8 TO 124	84 TO 244
PLACEMENT TOLERANCE	.25mm	0.125mm	0.05mm
CONDUCTORS/CLEARANCE	.3mm	0.15mm	0.125mm
LANDS	1.5mm	0.75mm	0.63mm
HOLES	1.0mm	0.4mm	0.40mm
ANNULAR RING	.25mm	0.2mm	0.125mm

Figure 3–16 Packaging and geometries

ROUTING GRIDS	MINIMUM CONDUCTORS/CLEARANCE	MANUFACTURING ALLOWANCE
.63mm	0.3/0.2mm	0.1mm
0.5mm	0.2/0.2mm	0.1mm
0.4mm	0.2/0.15mm	0.05mm
0.3mm	0.15/0.1mm	0.05mm
0.25mm	0.10/0.10mm	0.05mm

IPC-782-3-17

Figure 3-17 Surface mount conductor widths/clearances vs. routing grids

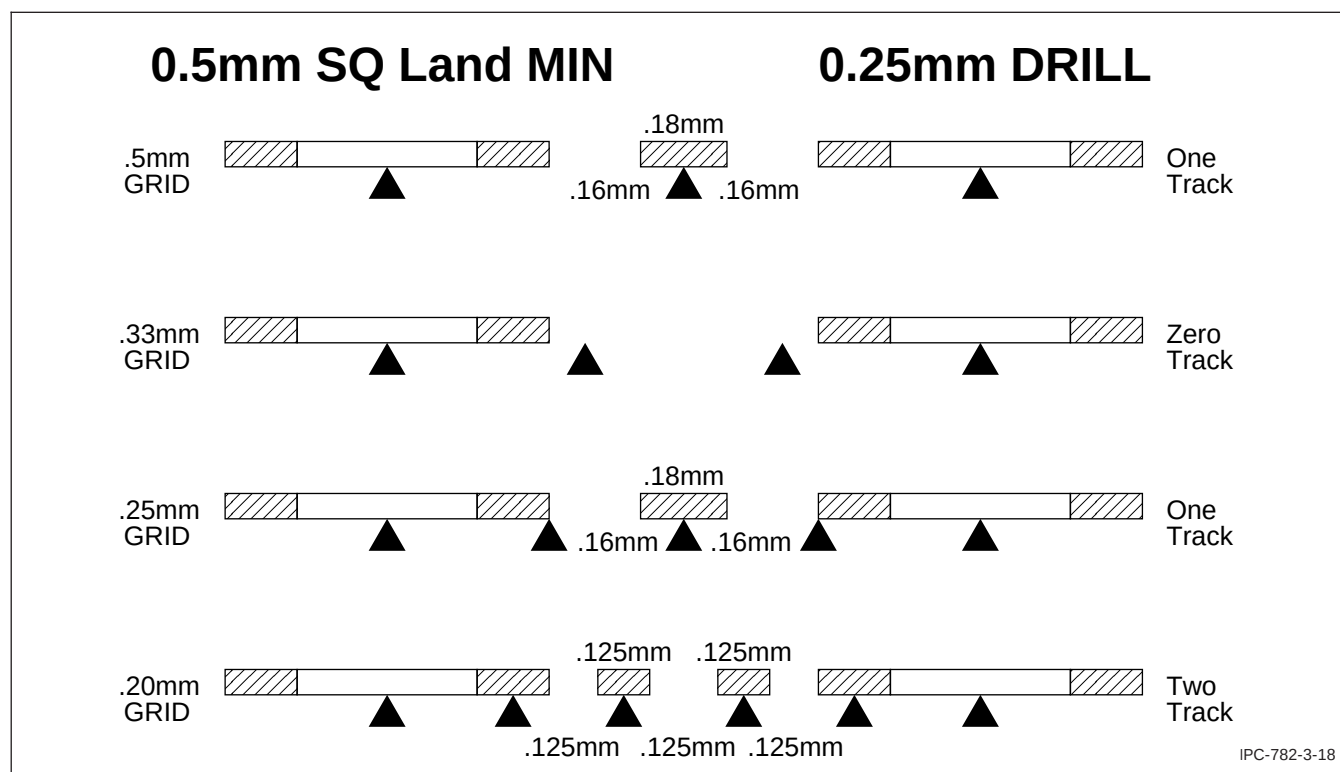


Figure 3-18 Section view of multilayer board with vias on 1.0 mm [0.040 in] centers

shows a grid routing analysis with vias on 1.0 mm [0.050 in] centers. On the left side are listed the routing grids with the actual routing channels denoted by solid triangular points. It can be seen that with SMT geometry of vias placed on 1.0 mm [0.040 in] centers, there is one routing channel between lands using a 0.3 mm [0.012 in] grid with 0.15 mm [0.006 in] conductor width/clearances. The bottom routing grid of 0.25 mm [0.010 in] with 0.125 mm [0.005 in] has two routing channels between vias.

3.6.2.2 Surface Conductors Wide conductors connecting to a land area can act as a solder thief by drawing sol-

der away from the land and down the conductor. Furthermore, if the conductor goes to a via which is connected to an inner layer power or ground plane, the wide conductor may act as a heat sink and draw heat away from the land/lead area during reflow solder resulting in a cold solder joint.

- Narrow the conductor as it enters the land area. Maximum conductor width should be 0.25 mm [0.010 in] (see Figure 3-19). The minimum conductor length should be 0.50 mm [0.020 in]. This neckdown provides an effective solder restriction, and may also be used to

need to use a soldermask to prevent the migration of solder away from the component land.

- B. Routing conductors into the lands as shown in Figures 3–20, 3–21 may restrict discrete component movement during reflow soldering. In the case of active IC's this routing geometry will allow the designer to use the same library shape for surface routing or pad cap (no surface routing) printed board configuration. Additionally, using this generic library shape allows ease of switching between the two configurations midstream in the design process without changing or editing component libraries. In either case, 100% test node access is retained. If wider conductors are required, the via land size may be decreased accordingly to allow sufficient spacing between the conductor and the land.
- C. Use solder mask over bare copper (SMOBC) or copper that has had the solder plating selectively removed. The solder mask and bare copper provide an effective barrier to solder migration. This may provide sufficient protection even if options A and B are not possible.

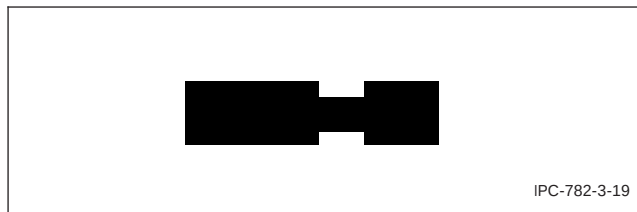


Figure 3–19 Narrowed conductor

3.6.2.3 Inner Layer Conductors The use of 0.2 mm [0.008 in] conductors and clearance often drives layer counts up because there is no routing channel available between vias on 1.27 mm [0.050 in] centers. It is for this reason that there is an increased usage of the conductors on internal layers at or less than 0.15 mm [0.006 in] for SMT designs, and 0.125 mm [0.005 in] conductors and clearances for designs with heavy usage of FPT. Figure 3–22 and 3–23 show the number of routing channels available between lands using the 0.15 and 0.125 mm [0.006 and 0.005 in] geometries. Since conductor width control is much more difficult to maintain on outer layers of the PB, it is better to keep the small geometries on the inner layers of a multilayer printed board. Doing so may reduce the need for soldermask and dramatically improve printed board fabrication yields. Generally, the option of using smaller geometries is driven by the need to reduce layer counts. Decreasing layer counts may reduce the overall board thickness and improve the aspect ratio for small hole drilling.

3.6.3 Via Location Guidelines

3.6.3.1 Via Holes Size of the via holes should be selected based upon the printed board thickness vs. hole diameter or aspect ratio limits as defined by printed board

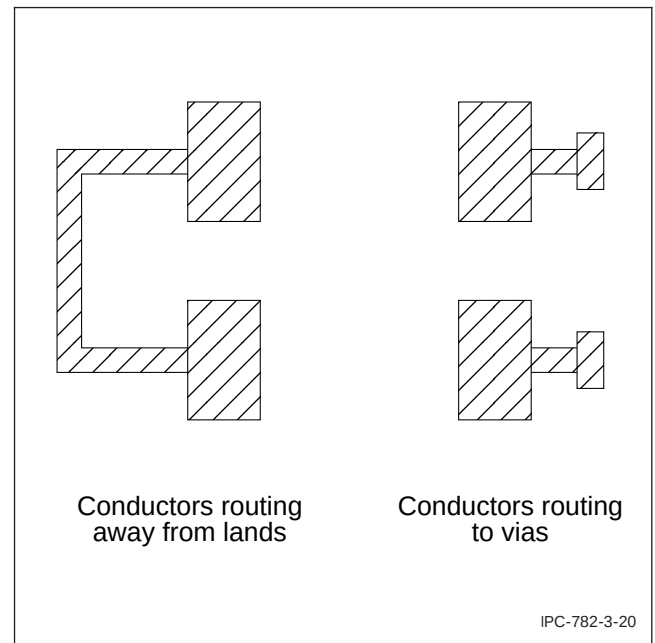


Figure 3–20 Conductor routing

fabricator. In addition, specific via lands and holes can be accessed for automatic in-circuit test (ICT). See 5.3.1. Figure 3–24 shows the land pattern-to-via relationships.

3.6.3.2 Vias and Land Pattern Separation Vias are plated-through holes for example 0.63 mm to 1.0 mm [0.025 to 0.040 in] diameter lands. They must be located away from the component lands to prevent solder migration off the component land during reflow soldering. This migration will cause insufficient solder fillets on components. (Solder drain) The solder migration can be restricted by providing a narrow bridge between the land area and the via or prevented by using the soldermask over bare copper circuitry. (See Figures 3–19 and 3–20.)

The relationship for mounting land and via locations should consider the conductor routing requirements. Figure 3–25 provides several examples of via positioning concepts.

Specifying tented or filled vias will also reduce solder migration on assemblies manufactured with a solder reflow process. Filled or tented vias also take care of potential flux entrapment problems under components and are highly desirable for attaining good vacuum seal during in-circuit bed-of-nails testing. Tenting is done with a dry film type of soldermask, or the via may be filled with a resin prior to liquid soldermask application.

3.6.3.3 Vias Under Components If the assembly is to be wave soldered, via holes underneath zero clearance components on the primary side should be avoided on boards unless tented with soldermask. During wave soldering of the assembly, flux may potentially block copper surfaces

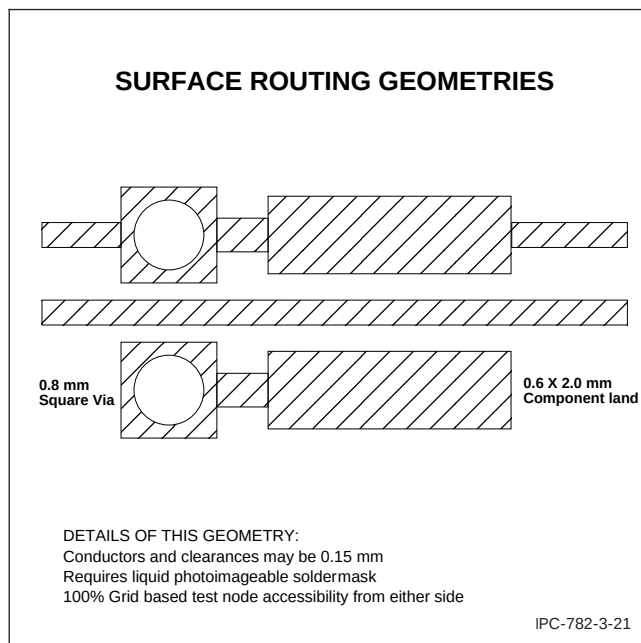


Figure 3-21 Surface routing geometries

zero clearance devices. Via holes may be located underneath zero clearance surface mount packages in full surface mount assemblies that will not be wave soldered. See Figure 3-26.

3.6.3.4 Vias as Test Points Via holes are used to connect surface mounted component lands to conductor layers. They may also be used as test targets for bed-of-nails type probes and/or rework ports. Via holes may be tented if they are not required for node testing or rework. When a via is used as a test point it is required that the location of a test land be defined. See Section 5.0.

3.6.4 Standard Fabrication Allowances Manufacturing tolerances or Standard Fabrication Allowances (SFA) exist in all PB fabrication shops. Virtually every registration or alignment operation that is performed has some potential for misregistration. There are approximately 42 basic steps in fabricating a multilayer PB, several of which involve operations that require precision in location. They are as follows: artwork generation, artwork tooling hole locations, core material tooling hole size, inner layer image printing operation, laminating fixture tooling pin locations, material shrinkage during lamination, drill tooling pin location, drill x/y table tolerances, drill spindle tolerances, drill wander, outer layer imaging, to name a few. The SFA considers all of the tolerances of all the steps mentioned above. If all of the equipment in a fabrication shop is old and worn the SFA could be as high as 0.3 mm, whereas, a manufacturer with new, precise equipment may have an SFA of 0.2 mm. An industry average SFA of 0.4 mm may be used. The tolerance varies according to the printed board maximum diagonal dimension and must be included in the land size calculations. The fabricator should be consulted prior to beginning a design to determine his SFA. With this number, the designer can proceed accordingly, preventing tolerances from stacking up and creating yield and/or production problems. (See IPC-2221.)

3.6.4.1 Manufacturing Characteristics Figure 3-27 shows the various characteristics of conductor geometry. End product drawings and specifications should specify only minimums for conductor width and spacing. Tolerance with plating of ± 0.03 mm [± 0.001 in] can be achieved under special conditions. Artwork allowances that should be incorporated into a design are shown in Table 3-8.

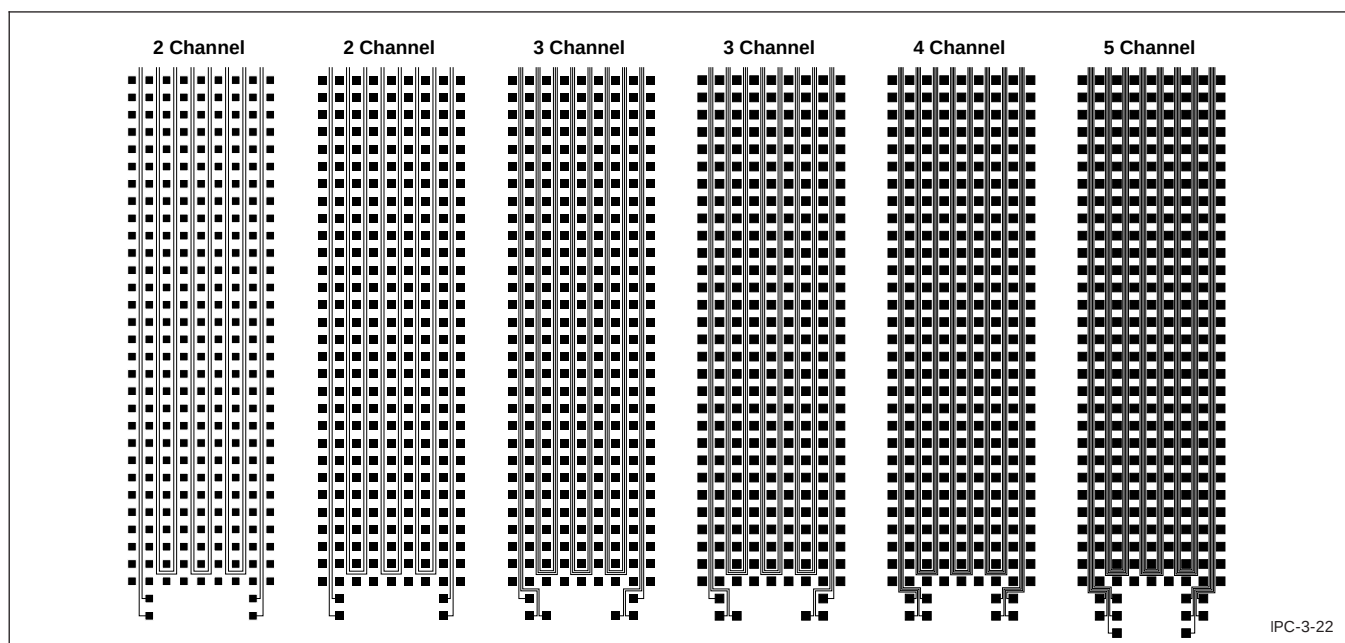


Figure 3-22 Conductor routing capability test pattern

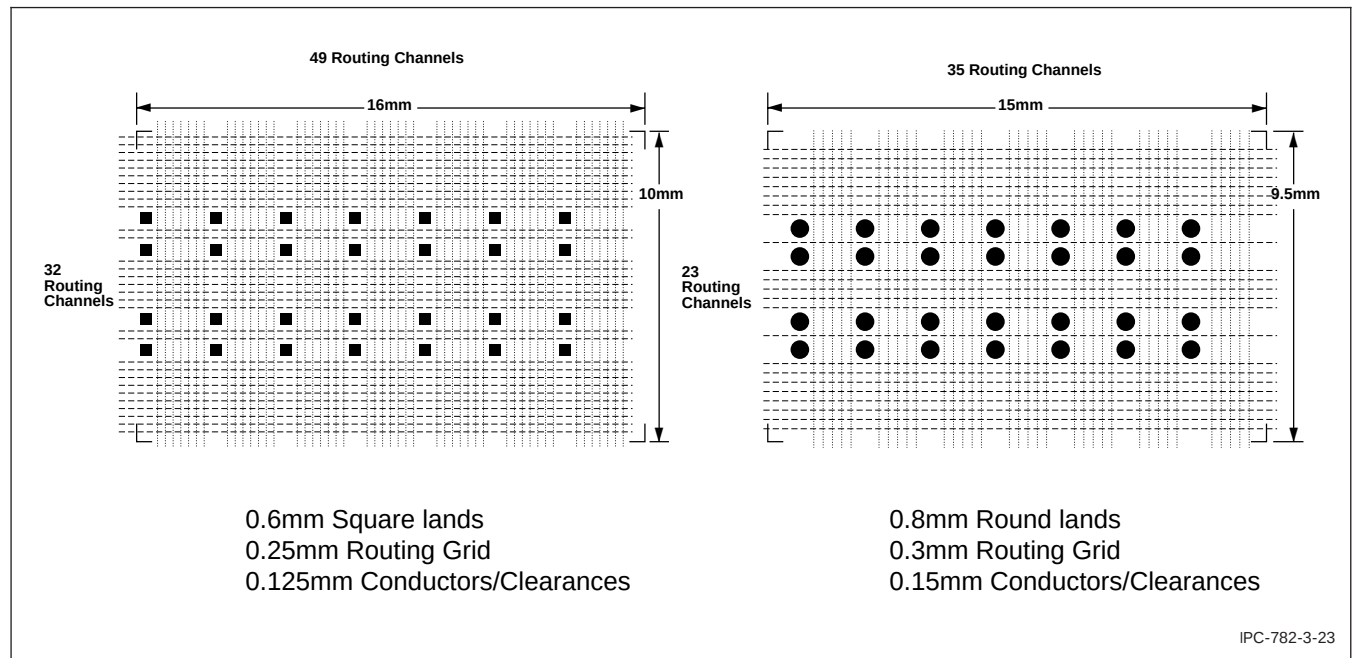


Figure 3-23 Routing channels under SOIC land pattern with 28 pins

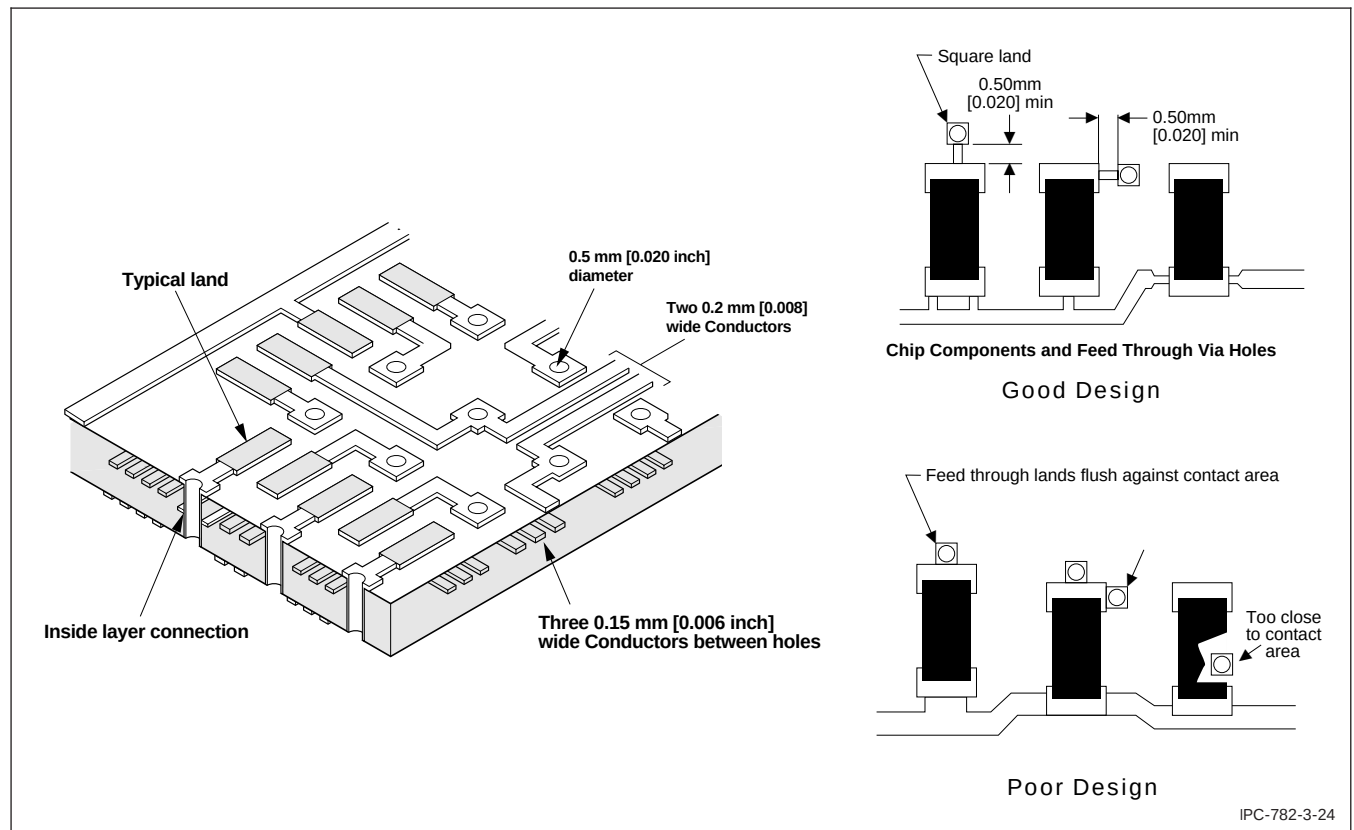


Figure 3-24 Land pattern to via relationships

Spacing requirements are usually the inverse of the tolerances shown for conductors in Table 3-9. For additional information see IPC-D-310, Artwork Generation and Measurement Techniques.

3.6.4.2 Conductor Width and Spacing Tolerances The presentation in Table 3-9 represents process tolerances that can be expected with normal processing. (Specific process

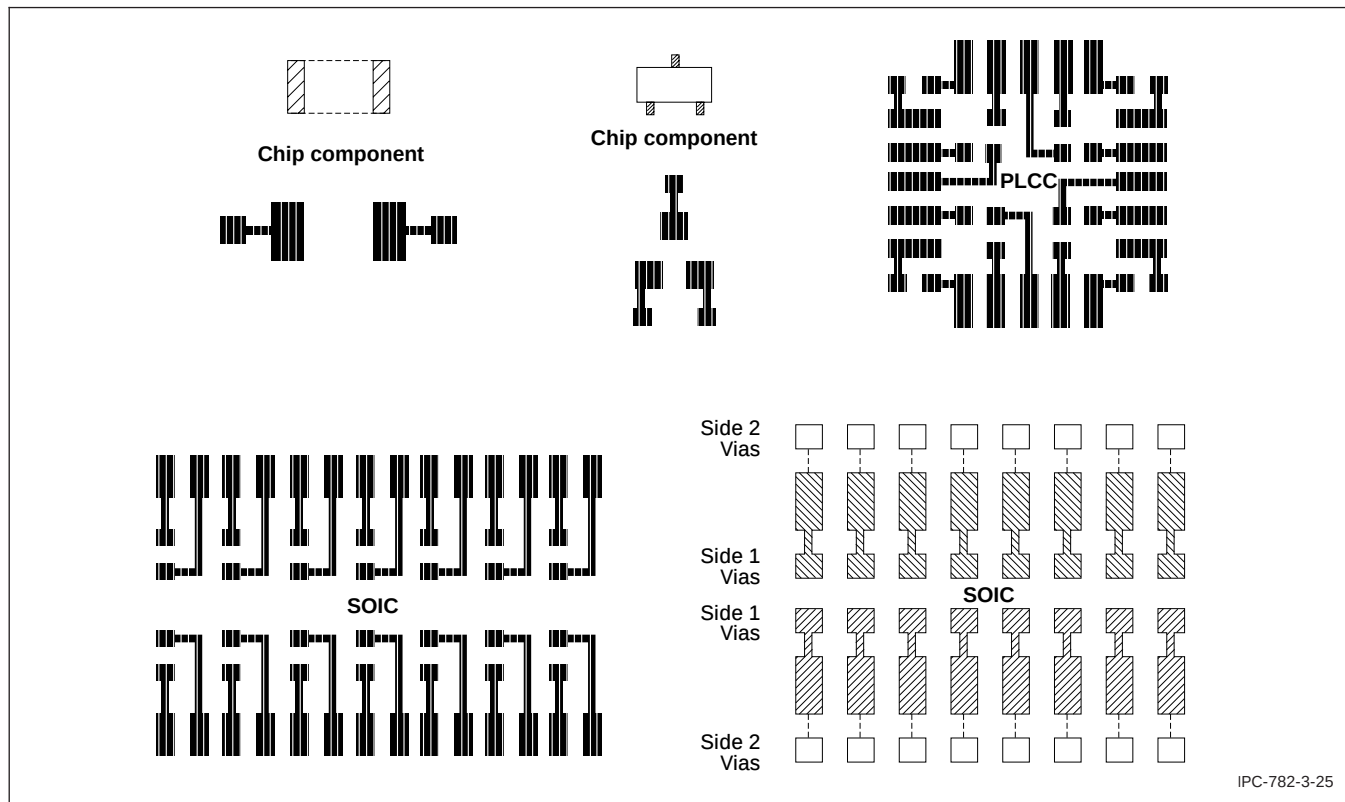


Figure 3-25 Examples of via positioning concepts

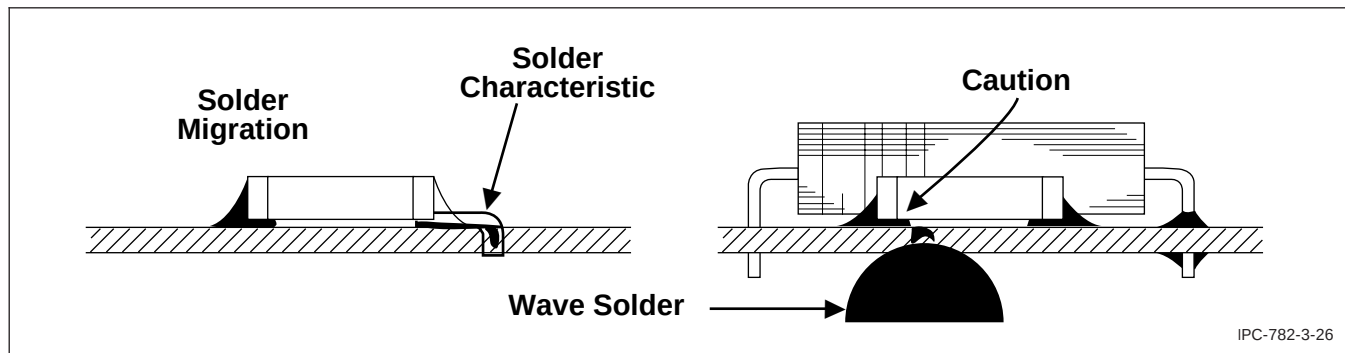


Figure 3-26 Vias under components

tolerances should be discussed with the board manufacturer.) The tolerances are based on copper thickness up to and including one ounce copper. For each ounce of additional copper, an additional 0.03 mm [0.001 in] variation per conductor edge can be expected.

3.6.4.3 Conductive Pattern Feature Location Tolerance

The presentation in Table 3-10 is for the tolerance to be applied to the nominal dimension chosen for the location of the lands, connector contacts and conductors in relation to the datums. This tolerance includes tolerances for master pattern accuracy, material movement, layer registration and fixturing.

3.6.4.4 Annular Ring Control The annular ring is defined as the amount of land that is remaining after a hole

is drilled through it. With high density SMT designs, maintaining minimum annular requirements has emerged as one of the most difficult parts of multilayer PB fabrication in terms of producibility. Perfect registration will maximize the annular ring all around the drilled hole. Using a 0.8 mm [0.030 in] land with a 0.5 mm [0.020 in] drill will result in a 0.15 mm [0.006 in] annular ring under perfect registration conditions. If misregistration of 0.15 mm [0.006 in] occurs in any direction, the result will be a 0.3 mm [0.010 in] annular ring on one side of the pad, and no annular ring on the other side. If misregistration is greater than 0.15 mm [0.006 in], i.e., 0.2 mm [0.008 in], then the drill will actually break out of the land. If the breakout is in the direction where the conductor connects to the land, the drill will effectively disconnect the conductor from the land.

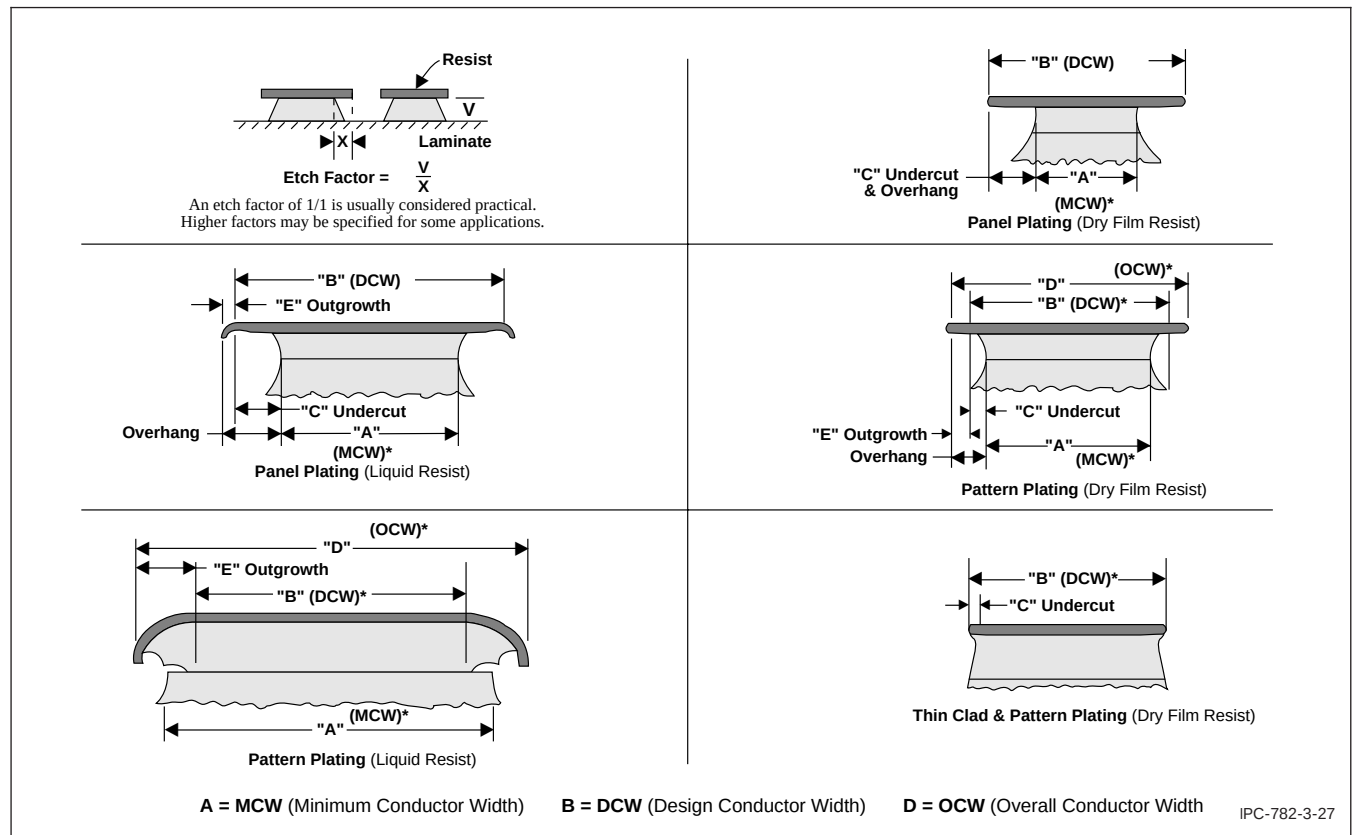


Figure 3-27 Conductor characteristics

Table 3-8 Typical Values to Be Added or Subtracted to Nominal Production to Achieve Desired Nominal Conductor Width

Description	1/2 Oz. Copper						1 Oz. Copper						2 Oz. Copper					
	Panel			Pattern			Panel			Pattern			Panel			Pattern		
	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo	Screen	Liquid Photo	Dry Film Photo
Subtractive Method Simple Etch	+25µm [+0.0010]	+25µm [+0.0010]	+25µm [+0.0010]	—	—	—	+38µ [+0.0015]	+38µm [+0.0015]	+38µm [+0.0015]	—	—	—	+63µm [+0.0025]	+63µm [+0.0025]	+63µm [+0.0025]	—	—	—
Bare Copper [PTH]	+38µ [+0.0015]	+38µm [+0.0015]	+50µm [+0.0020]	-25µ [-0.0010]	-25µm [-0.0010]	-25µm [-0.0010]	+50µm [+0.0020]	+50µm [+0.0020]	+63µm [+0.0025]	0	0	+50µm [+0.0020]	+76µm [+0.0030]	+76µm [+0.0030]	+89µm [+0.0035]	+38µm [+0.0015]	+38µm [+0.0015]	+89µm [+0.0035]
Tin-Lead [PTH]	+38µm [+0.0015]	+38µm [+0.0015]	+50µm [+0.0020]	-25µm [-0.0010]	-25µm [-0.0010]	+25µm [+0.0010]	+50µm [+0.0020]	+50µm [+0.0020]	+63µm [+0.0025]	0	0	+50µm [+0.0020]	+76µm [+0.0030]	+76µm [+0.0030]	+89µm [+0.0035]	+38µm [+0.0015]	+38µm [+0.0015]	+89µm [+0.0035]
Gold Nickel [PTH]	+38µm [+0.0015]	+38µm [+0.0015]	+50µm [+0.0020]	-25µm [-0.0010]	-25µm [-0.0010]	+25µm [+0.0010]	+50µm [+0.0020]	+50µm [+0.0020]	+63µm [+0.0025]	0	0	+50µm [+0.0020]	+76µm [+0.0030]	+76µm [+0.0030]	+89µm [+0.0035]	+38µm [+0.0015]	+38µm [+0.0015]	+89µm [+0.0015]
For Deposited Copper Thickness Equivalents																		
Additive Method Electroless Copper No-Etch	—	—	—	-50µ [-0.0020]	-25µm [-0.0010]	-0µm [0.0000]	—	—	—	-76µm [-0.0030]	-50µ [-0.0020]	-0µ [-0.0000]	—	—	—	-101µ [-0.0040]	-76µm [-0.0030]	-0µm [-0.0000]
Semi Additive Method Copper-No Overplate	—	—	—	-50µm [-0.0020]	-25µm [-0.0010]	-0µm [-0.0000]	—	—	—	-76µm [-0.0030]	-50µm [-0.0020]	-0µm [-0.0000]	—	—	—	-101µm [-0.0040]	-76µm [-0.0030]	-0µm [-0.0000]
Tin Lead Overplate	—	—	—	-76µm [-0.0030]	-50µm [-0.0020]	-25µm [-0.0010]	—	—	—	-101µ [-0.0040]	-76µm [-0.0030]	-25µm [-0.0010]	—	—	—	-127µm [-0.0050]	-101µm [-0.0040]	-25µm [-0.0010]

Table 3–9 Conductor Width Tolerances

Feature	Level A	Level B	Level C
Without plating	+0.05 –0.10 [+0.002] [–0.004]	+0.03 –0.05 [+0.001] [–0.002]	+0.02 –0.04 [+0.0008] [–0.0016]
With plating	+0.10 –0.10 [+0.004] [–0.004]	+0.08 –0.08 [+0.003] [–0.003]	+0.05 –0.05 [+0.002] [–0.002]

Table 3–10 Conductive Pattern Location Tolerances

Greatest Board/ X, Y Dimension	Level A	Level B	Level C
Up to 300 mm [12.0]	0.30 mm [0.012]	0.20 mm [0.008]	0.10 mm [0.004]
Up to 450 mm [18.0]	0.40 mm [0.016]	0.30 mm [0.012]	0.20 mm [0.008]
Up to 600 mm [24.0]	0.40 mm [0.016]	0.30 mm [0.012]	0.20 mm [0.008]

result is a scrapped PB. Since signal conductors intersect the lands from all directions, any breakout has the potential to randomly disconnect conductors all over the PB.

Maintaining consistent annular ring control is difficult at best, another method had to be developed to insure connectivity between lands and conductors. This method is called filleting, corner entry or keyholing. Explained simply, each method is intended to provide excess original copper material at the junction where the conductor enters the land. The land which is filleted resembles a teardrop; it is square for the corner entry, and looks like a figure eight for keyholing. All features point in the direction of the conductor to permit additional misregistration allowances (see Figure 3–28).

3.6.4.5 Fabrication Panel Format Components can be mounted on individual boards or on boards that are still organized in panel form. Boards or panels that will be moved by automatic handling equipment or pass through automated operations, (parts placement, soldering, cleaning, etc.) must have the sides kept free of parts or active circuitry. Special tooling and fixturing holes are generally located within the edge clearance areas. The clearance areas are needed to avoid interference with board handling fixtures, guidance rails and alignment tools.

Typically a clear area of 3.0 to 5.0 mm [0.118 to 0.200 in] must be allowed along the sides for the clearance. The required clearance width is dependent upon the design of the board handling and fixturing equipment. These dimensions should be obtained from the equipment manufacturer before board or panel design. (See Figure 3–29.)

For accurate fixturing, a minimum of two (and preferably four) nonplated holes are located in the corners of the board to provide accurate mechanical registration on board transfer equipment. Board handling holes (typically 3.2 mm [0.125] diameter) may also be located in the clearance areas. These holes are used by automated board handling equipment to move boards (or panels) from station to station in automated assembly lines. Specific sizes should be obtained from the equipment manufacturer. In addition, optical fiducial marks may be located near the fixturing holes if optical alignment is used, to improve registration (see Figure 3–14).

3.6.4.6 Board Size and Panel Construction In order to fully utilize the automation technology associated with surface mount components, a designer should consider how a printed board or P&I structure will be fabricated, assembled and tested. Each of these processes, because of the particular equipment used, requires fixturing which will

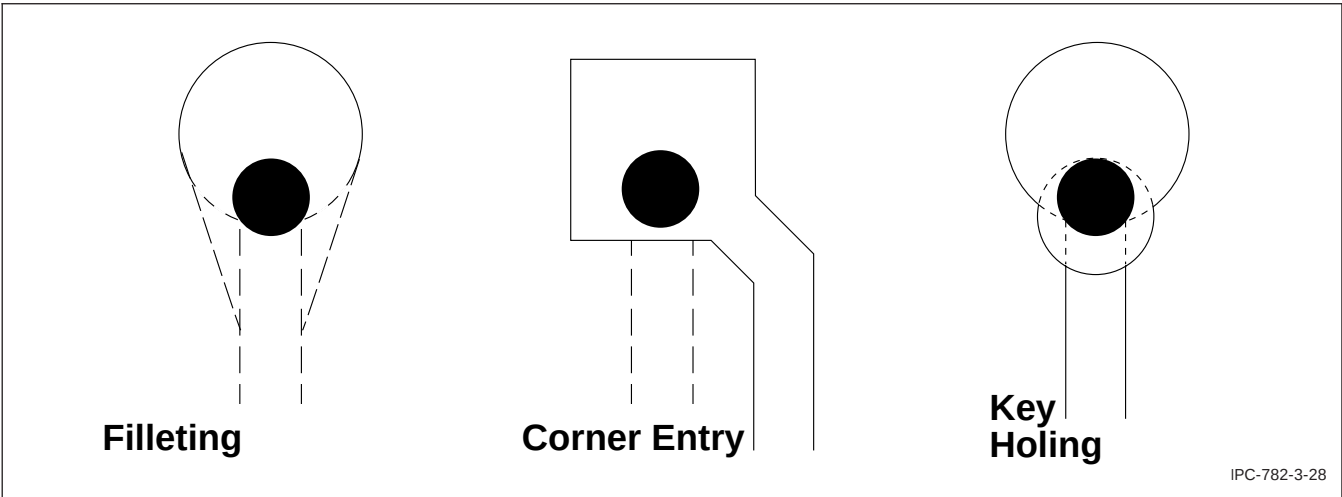


Figure 3–28 Examples of modified landscapes

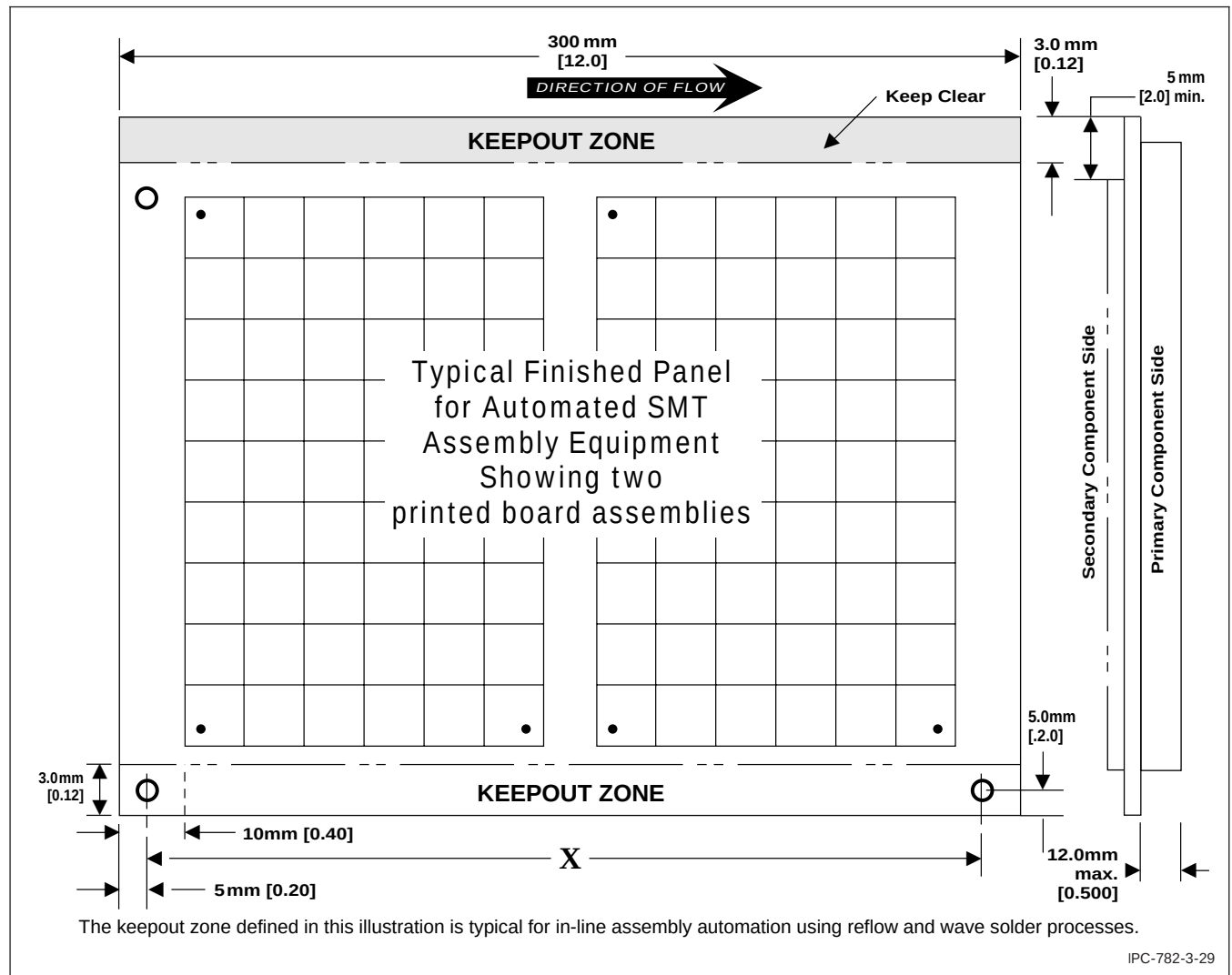


Figure 3-29 Typical copper glass laminate panel

affect or dictate certain facets of the board layout. Tooling holes, panel size, component orientation and clearance areas (both component and conductor) on the primary and secondary sides of the board are all equipment and process dependent.

To produce a cost effective layout through optimum base material utilization a designer should consult with the board fabricator to determine optimum panel size. The board should be designed to utilize the manufacturer's suggested usable area. Smaller boards can be ganged or nested on this same panel size to simplify fixturing and reduce excessive handling during assembly. Most manufacturers will suggest various methods of retaining assemblies in panels. A method should be chosen taking the assembly and test processes into consideration.

Figure 3-29 shows the typical use of a copper clad glass laminate panel. See IPC-D-322 for panel to board relationship.

Small boards can effectively be arranged on a single working panel, if the designer works closely with manufacturing. These are commonly called nested panels or pallets.

Panel construction may include several boards arranged in a matrix or simply one board requiring additional material retained for efficient assembly processing. The large board or several smaller boards are retained in the panels and separated after all assembly processes are completed. Excising or separating the individual boards from the panel must be planned as well. Several methods are used to retain circuits in a panel, including V-groove scoring and routed slot with break-away tabs.

V-groove scoring is generally provided on both surfaces of the board, and only in a straight line. A small cross section of board material is retained at the break line. An allowance for the scoring angle must be made as well. Conductors that are located too close to the score groove will be

exposed or damaged, and rough edges must be sanded lightly to remove burrs and rough fabric particles. See Figure 3–30.

The routed slot and tab pattern is widely used for panel construction and break-away tab extensions. Routing is more precise than scoring, and edge surfaces are smooth, but the break-away “tab” points will require consideration. Tabs can be cut and ground flush with the board edge or pre-drilled in a pattern. The drilled pattern furnishes a low stress break point on the “tab”. If the hole pattern is recessed within the board edge, secondary sanding or grinding can be bypassed. See Figures 3–31 and 3–32.

3.6.4.7 Artwork Compensation and Scaling Artwork compensation and scaling are two adjustments that are made by the printed board fabricator to the original printed board artwork film or CAD data prior to beginning the fabrication process.

Modifications are made to the artwork feature sizes to compensate for the etch factor that occurs when etching away unwanted copper from the inner and outer layers of a printed board. The outer layers require more compensation than inner layers due to the overplating of copper and other metals that form the copper protection during the etching process. This is one of the reasons conductor width control on outer layers of printed boards can be substantially more difficult than inner layer conductor width control.

Scaling is an adjustment made to the artwork by the fabricator offset printed board material shrinkage, which is in

the range of 8–13 μm [0.00035–0.0005 in] per 25 mm, that occurs during the lamination process. When the annular ring requirements fall below a nominal 0.25 mm [0.010 in], artwork scaling will typically be invoked by the printed board fabricator.

3.7 Outer Layer Finishes

3.7.1 Soldermask vs. Lands Only In referring to the outer layers of the multilayer PB, there is a dramatic difference between the concepts of soldermask and having no conductors on the outer layers. Conventional SMT design rules allow routing conductors on the outer layers, running the conductors between Surface Mount lands, then applying soldermask to cover the conductors and leave the lands exposed. For high density SMT applications, the conductors and clearances on the outer layers are generally in the 0.15–0.2 mm [0.006–0.008 in] range.

Aside from the soldermask registration, maintaining precision conductor width control on the outer layers is significantly more difficult than on the inner layers. Outer layer conductor integrity can be a cause of poor fabrication yields. The soldermask rule is very simple: the conductors between lands must be covered with soldermask, while the lands must not have any soldermask on them. When using smaller geometries, adding the Standard Fabrication Allowance of 0.2 mm [0.008 in] can make soldermask registration very difficult.

Given the two distinct yield difficulties of conductor width control and soldermask application, board manufacturers with experience in high density SMT printed conductor

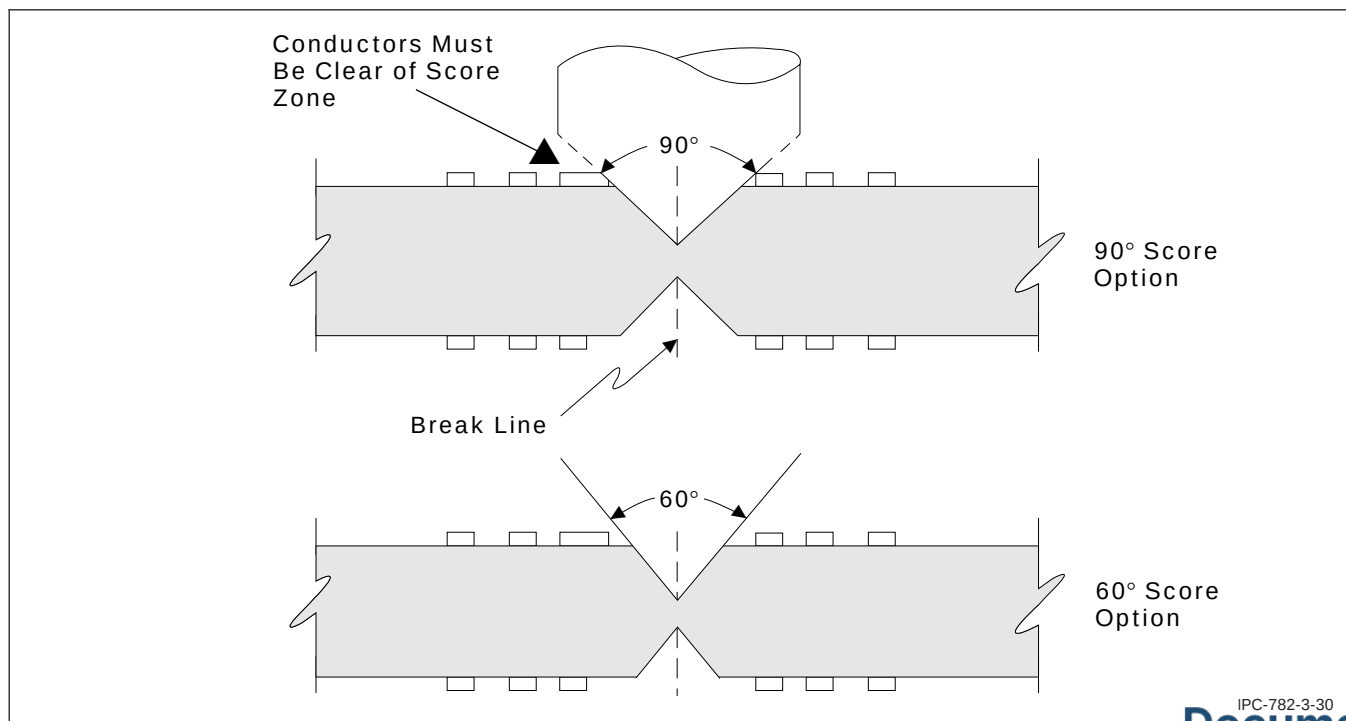


Figure 3–30 Conductor clearance for V-groove scoring

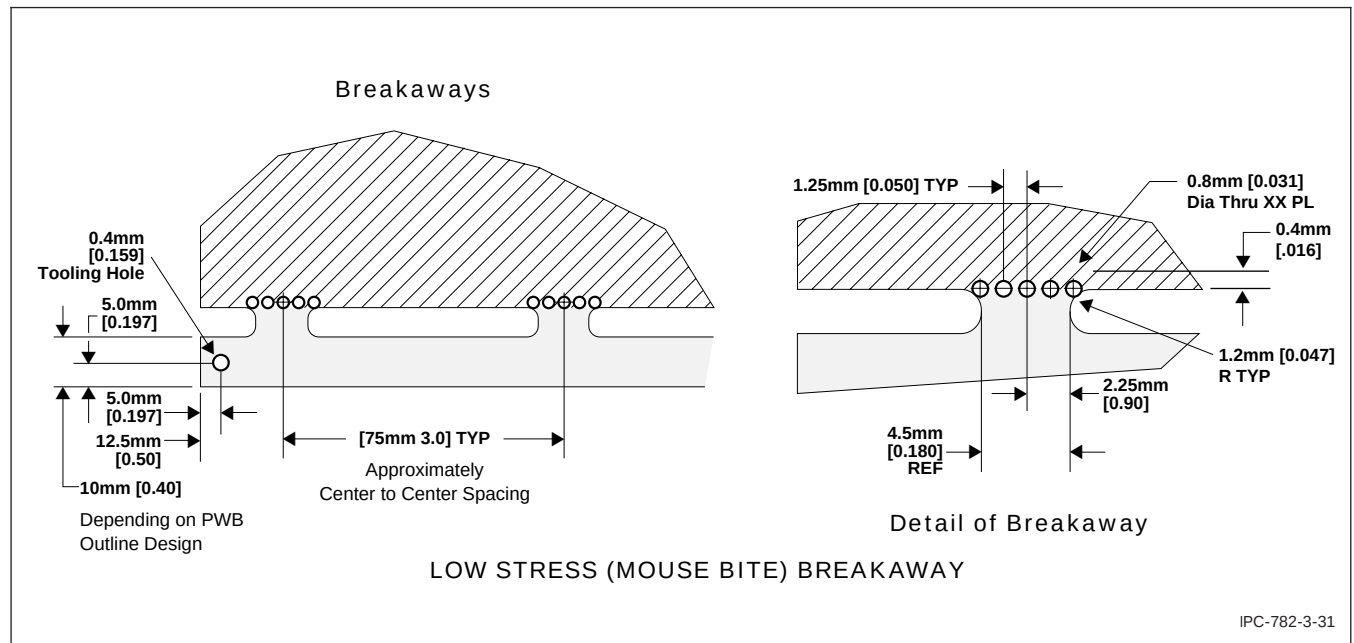


Figure 3-31 Breakaway (routed pattern)

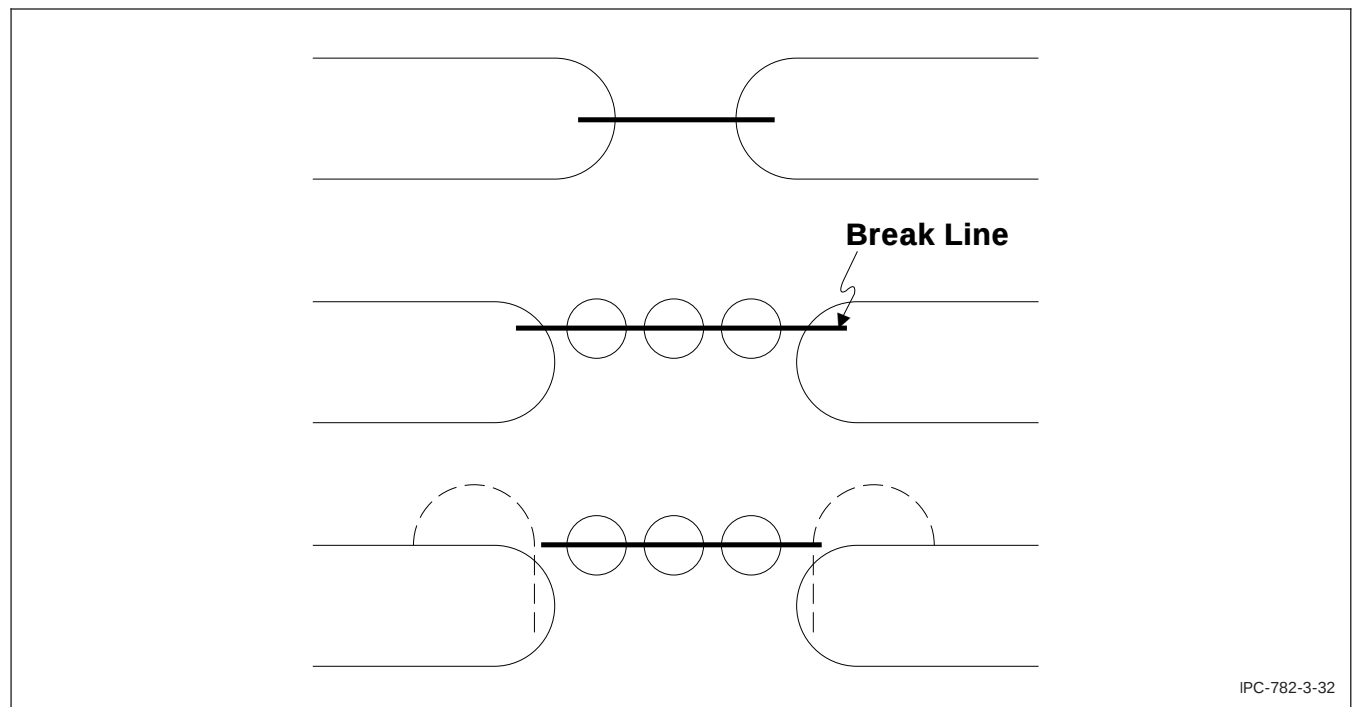


Figure 3-32 Routed slots

boards may favor the lands only (pad cap) concept. The pad cap concept has two yield improvement benefits: 1) no fine conductor geometries on the outer layers because they are buried in the inner layers where conductor width control is significantly easier, and 2) the need for soldermask is reduced or eliminated because there are no small spaces to protect from the soldering process.

In general, an 8-layer printed board, with lands only on the outer layer, is similar in cost to a 6-layer printed board with

solder mask, assuming both have SMT geometries. The primary reason for this is that some PB fabricators are realizing about a 12% yield improvement by not having the fine line conductors on the outer layers.

The benefits of pad caps continue into the assembly process by increasing yields through the reduction of solder shorts or bridging. The pad cap concept provides 100% testability, thus testing benefits are both economical and practical.

3.7.2 Soldermask Issues Rework of Surface Mount Assemblies due to soldermask related defects is cited as a major cause of problems by assembly people. Following are two classes of assembly problems caused by improperly applied soldermask: 1) soldermask on the component mounting lands; 2) insufficient soldermask coverage of unrelated circuit features in close proximity to the component mounting land.

Regarding soldermask on the lands and assuming that the solderability requirements of the component leads and board mounting lands have been met, the solder paste composition, viscosity, and aging are within limits, and the thermal profile of the reflow oven is correct, the only other variable which could be detrimental to good solder joint integrity is soldermask material on the lands. If there is any soldermask (even if invisible to the naked eye) on the lands during reflow, solder joint integrity can be lost through improper surface wetting.

The second class of assembly defects is created when there is insufficient soldermask coverage of circuitry in close proximity to the component mounting land leading to solder shorts or bridging. The majority of SMT designs incorporate very small geometries of 0.15–0.2 mm [0.006–0.008 in] conductors and spacing on the outer layers of the printed board. Designing a soldermask to cover a 0.15 mm [0.006 in] conductor and only half of the 0.15 mm [0.006 in] space between the conductor and the land is easy enough to accomplish during design. However, photo imaged soldermask will overcome most of the above issues (see Section 3.7.4).

Close examination of solder bridging on Printed Board Assemblies will reveal that most of the bridging actually occurs between the component leads above the surface of the PB, and not between the lands on the board. Even if a soldermask has sufficient resolution and registration to provide a solder dam between lands, it still may not prevent bridging between the leads. Soldermask should not, and can not, be expected to compensate for deficiencies in the soldering process if the assembly uses Fine Pitch components.

3.7.3 Solder Mask Clearances A soldermask may be used to isolate the land pattern from other conductive features on the board such as vias, lands or conductors. Where no conductors run between lands, a simple gang mask can be used as shown in Figure 3–33. Tolerance requirements for this design can generally be met by a screen printed soldermask. A 0.38 mm [0.015 in] spacing could be acceptable. Any class of solder mask per IPC-SM-840 could be applied. The most commonly chosen solder mask would be a Class 3 mask because of its higher temperature characteristics. Due to the close proximity of the solder mask to the land pattern, care must be taken in choosing a mask that

has low flow and low solvent-bleed characteristics to avoid land pattern contamination.

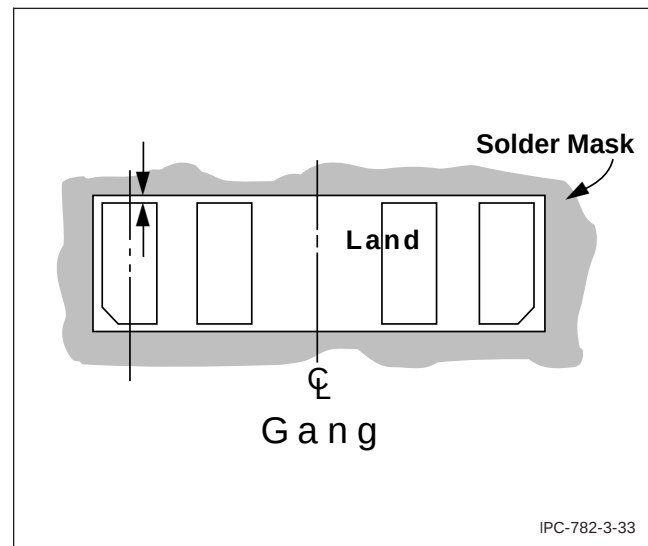


Figure 3–33 Gang solder mask window

For land pattern designs with routed conductors between lands (Figure 3–34) the tolerance requirement would require a photo-imageable soldermask. This is necessary because of the tight tolerance needed to cover the conductors without encroaching on the land area. A 0.08 to 0.125 mm [0.003 to 0.005 in] clearance is required with this type of design.

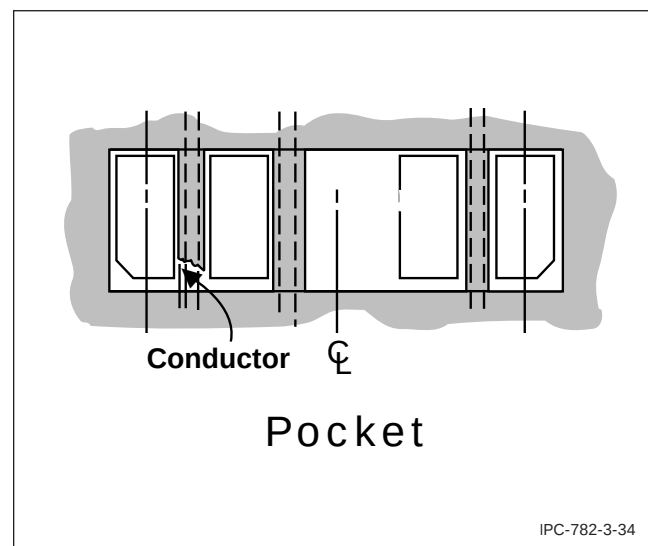


Figure 3–34 Pocket solder mask windows

3.7.4 Soldermask Types Solder mask coatings are available in two forms, liquid and dry film. The polymer mask material is applied using several process methods and are furnished in varying thicknesses. As an example, liquid materials will have a finished thickness of 0.02 to 0.025 mm while the dry film products are supplied in thicknesses of 0.025 to 0.076 mm.

mm thickness and a low profile 0.04 mm finished thickness. Although pattern screen printing is available, photo-imaged soldermask is recommended for surface mount applications.

The photo process provides a precise pattern image and when properly developed eliminates mask residue from land pattern surfaces. The mask thickness may not be a factor on most surface mount assemblies but when fine pitch (0.63 mm or less) devices are mounted on the printed boards, the lower profile soldermask will provide better solder printing characteristics.

4.0 QUALITY AND RELIABILITY VALIDATION

4.1 Validation Techniques The variety of component tolerances, and the possibility that tolerances may vary on interconnection products, users are encouraged to establish validation of the land pattern and component geometry. In addition, components should be checked for their maximum operating temperature limits. Figure 4-1 shows a general graph of the upper and lower limits of various components.

Validations of parts and circuits may be accomplished through the use of standard test patterns. These patterns may be used not only to evaluate a particular part to a land

pattern, but may also be used to evaluate a particular interconnection product that must go through the various processes being used in assembling surface mounted parts.

4.1.1 Test Patterns—Process Evaluations The following test patterns have been developed as standards that may be used for the evaluation of standard board materials, with a variety of standard parts. IPC-A-49 artwork is available for these tests. The land patterns represent land pattern designs from the original IPC-SM-782.

The test specimen contains conductors and plated through holes and parts connected in a single daisy chain. One end of the daisy chain is connected to a common ground while the other end of the chain is connected to land patterns, then to a plated through hole in which a wire may be soldered for test purposes.

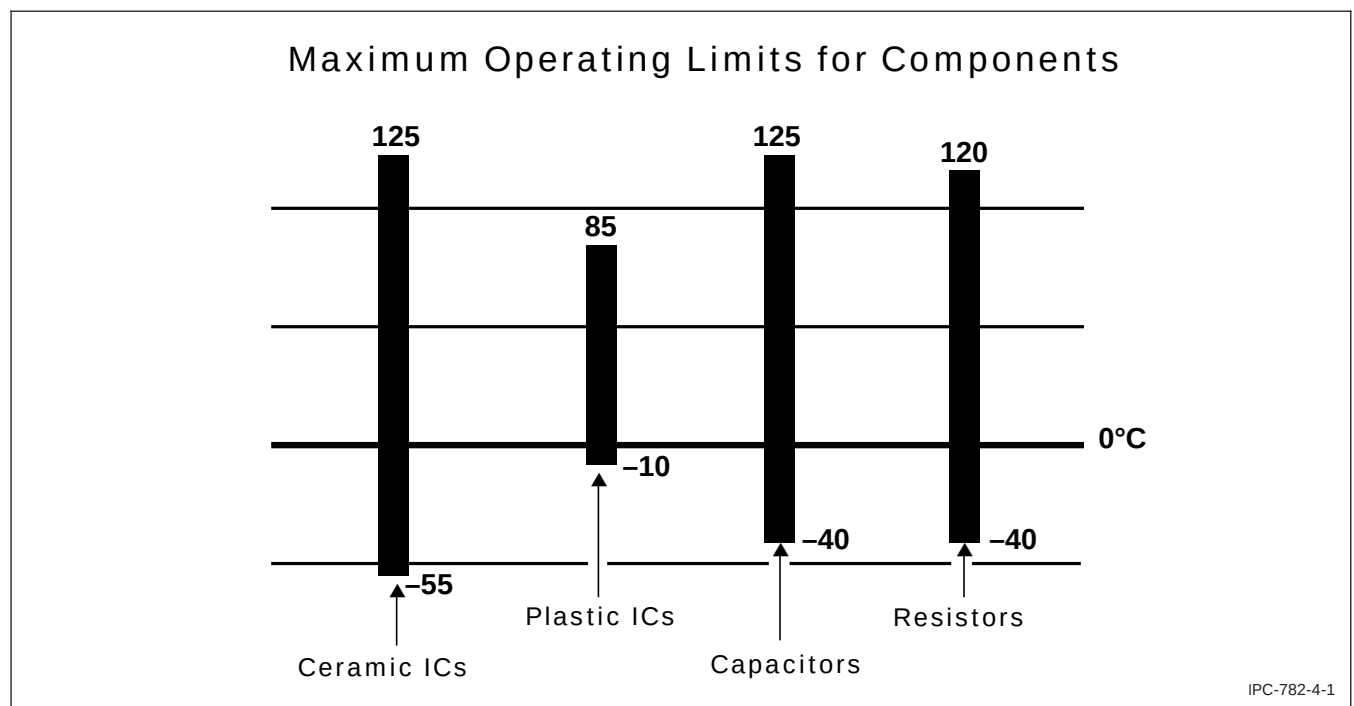


Figure 4-1 Component temperature limits

Circuits that are shown in Figures 4–2 and 4–3 contain the various components listed:

Test Vehicle

Primary (Top) Side	Secondary (Bottom) Side
— SITE #1 (2) 44 I/O PLCC-J	— SITE #1 Empty
— SITE #2 (2) 16 I/O DIP-I	— SITE #2 Empty
— SITE #3 (8) RC1206 (8) SOT-23	— SITE #3 (8) RC1206 (8) SOT-23
— SITE #4 (1) 68 I/O CLCC-J	— SITE #4 Empty
— SITE #5 (68) I/O PLCC-J	— SITE #5 Empty
— SITE #6 (8) MELF 1/4W (8) CC1825	— SITE #6 (8) MELF 1/4W (8) CC1825
— SITE #8 (2) 24 I/O SOIC-L	— SITE #8 Empty

Another test specimen is used for the testing of printed board structures that are intended to provide P&I structures used primarily for the mounting of leadless chip carriers. This test board is described in surface mount land pattern round robin artwork (IPC-A-48). The board is a 12-layer multilayer board which contains 38 positions for mounting leadless chip carriers used by an Air Force Mantech Program to evaluate printed board and substrate materials. The test boards produced from this artwork may contain metal cores, or other planes that control the coefficient of thermal expansion of the P&I structure.

The following are some examples of the type of materials that may be used as the constraining core.

- Nonorganic materials (alumina)
- Porcelainized clad Invar materials
- Printed boards bonded to low-expansion support (metal or nonmetal)
- Compliant layer constructions
- Metal core boards

4.2 Test Patterns—In-Process Validator Test patterns to validate in-process conditions are encourage to be incorporated into the panel of a printed board assembly. These designed-in land patterns provide special features for automatic optical inspection and visual inspection.

The land patterns shown in section 8–13 are designed to provide a clear view of the soldering characteristic such that land geometry is visible, and solder joint evaluation can be achieved. The same in-process validator are used to check the registration of solder paste prior to reflow soldering.

Figures 4–4 through 4–11 are illustrations from J-STD-001 that provide the key variables for meeting soldering requirements that are necessary for various surface mount parts. Land pattern samples provided around the periphery of a panel, should be designed to provide clear visibility of the solder joints shown in these figures.

4.3 Stress Testing Stress testing usually consists of temperature cycling of the printed board assembly that has been surface mounted through various extremes. The temperature cycling of the assembly or a coupon may be a standard MIL-STD-202 test method which cycles the board from –65°C to 125°C.

Alternate temperature cycles are also available. A temperature cycle test of 400 consecutive cycles to 1000 cycles has been identified for some assemblies. In these examples, the ramp time from high to low temperature is 30 minutes, and the time at the extreme is also 30 minutes. Figure 4–12 shows an example of the excursion rate of the various conditions of temperature cycling.

During the cycling processes, daisy chained plated-through holes and daisy chained solder joints, are measured during the initial phase as to their resistance, and then monitored for increased resistance during the thermal cycling. Increased resistance of 30 microohms in most instances constitutes a failure of the either the plated-through hole, or the solder joint.

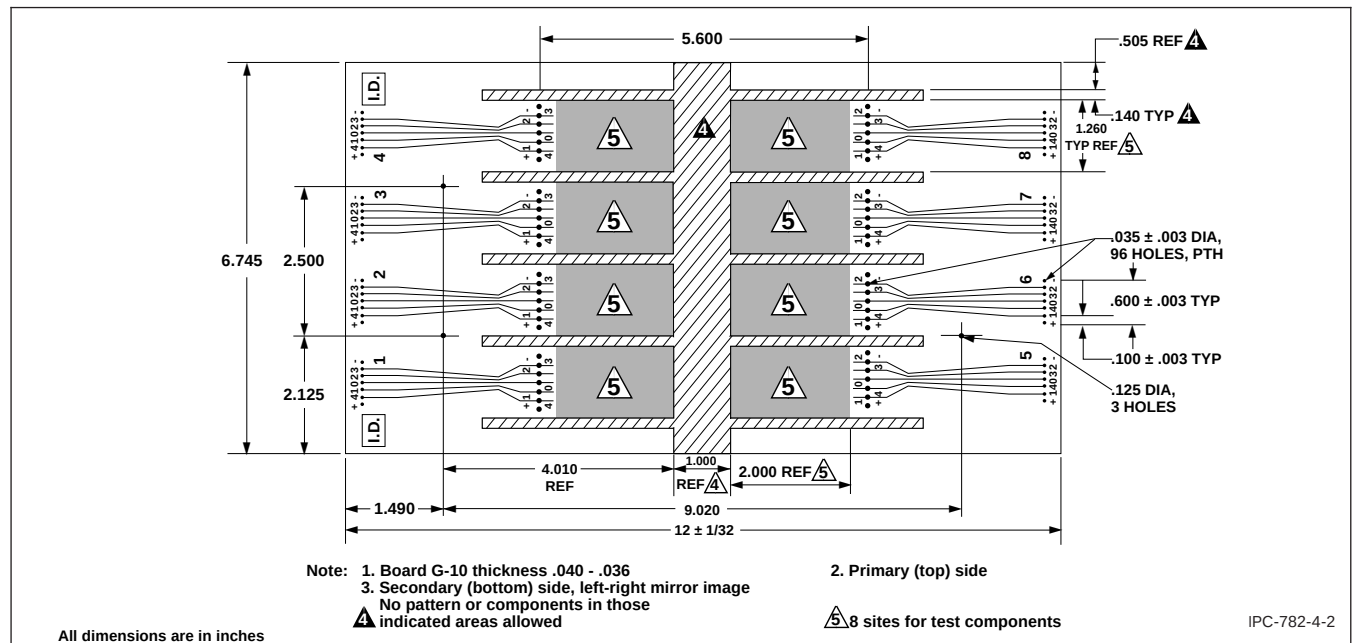


Figure 4-2 General description of process validation contact pattern and interconnect

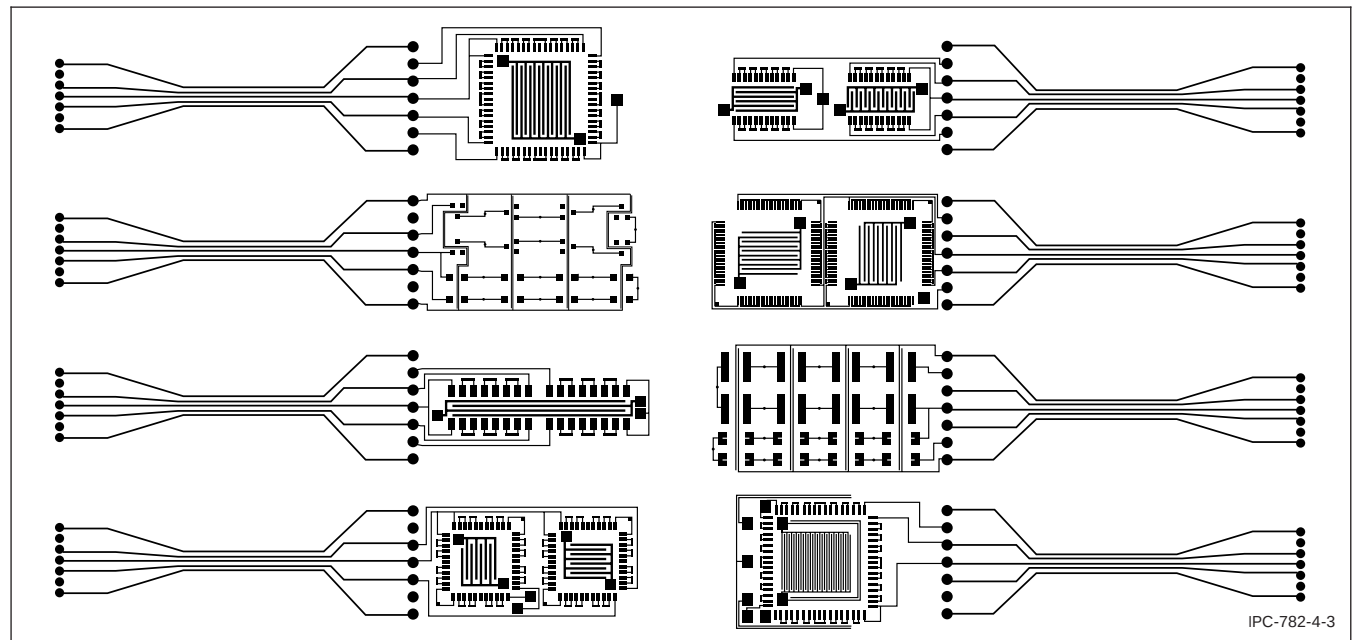


Figure 4-3 Photo image of IPC-A-49 test board for primary side

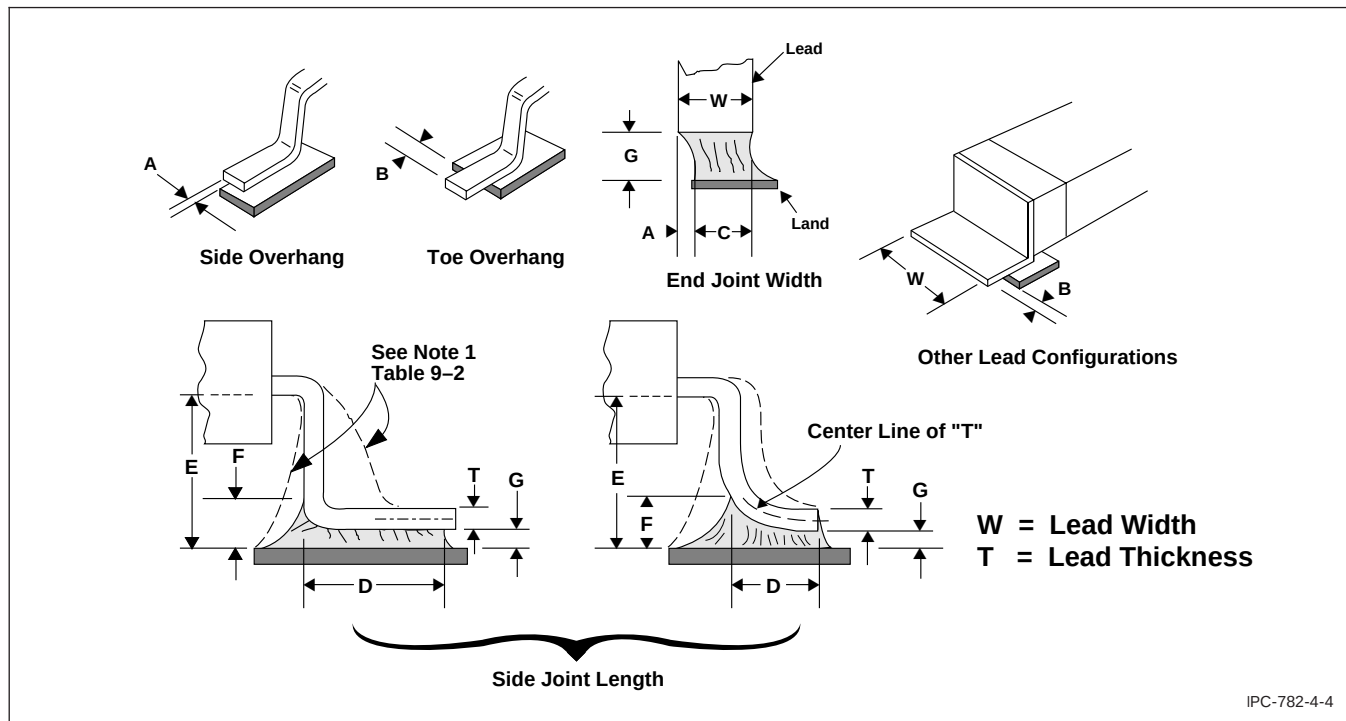


Figure 4-4 Flat ribbon, "L," and gullwing lead joint description

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

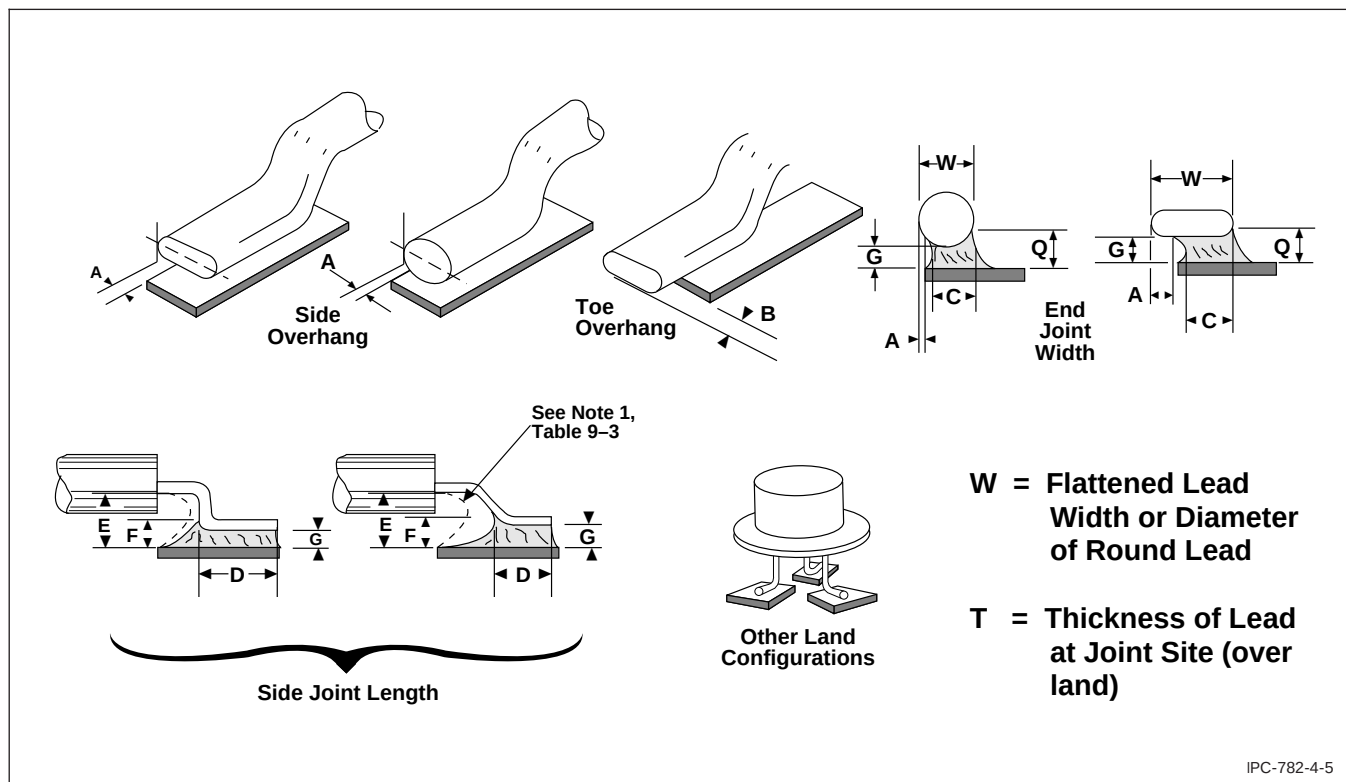


Figure 4-5 Round or flattened (coined) lead joint description

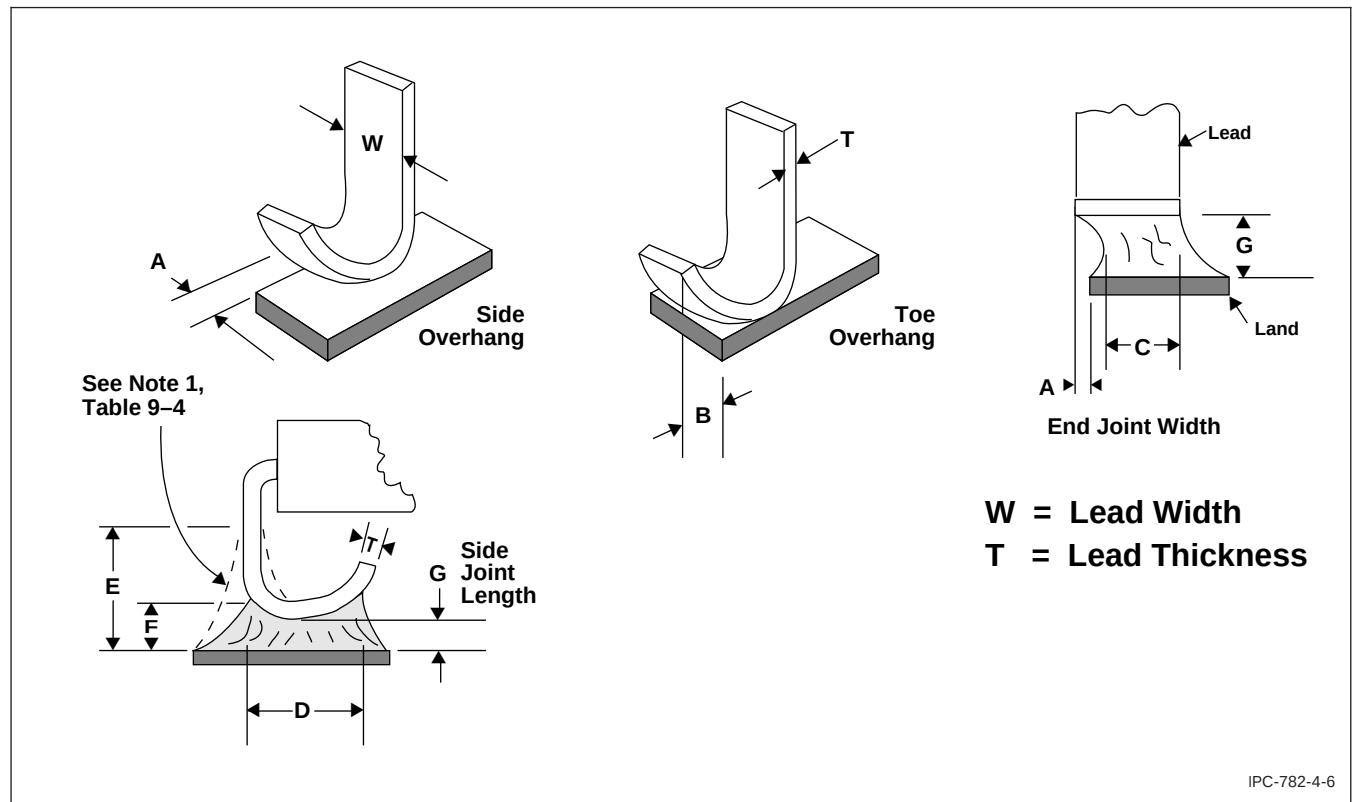


Figure 4-6 "J" lead joint description

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

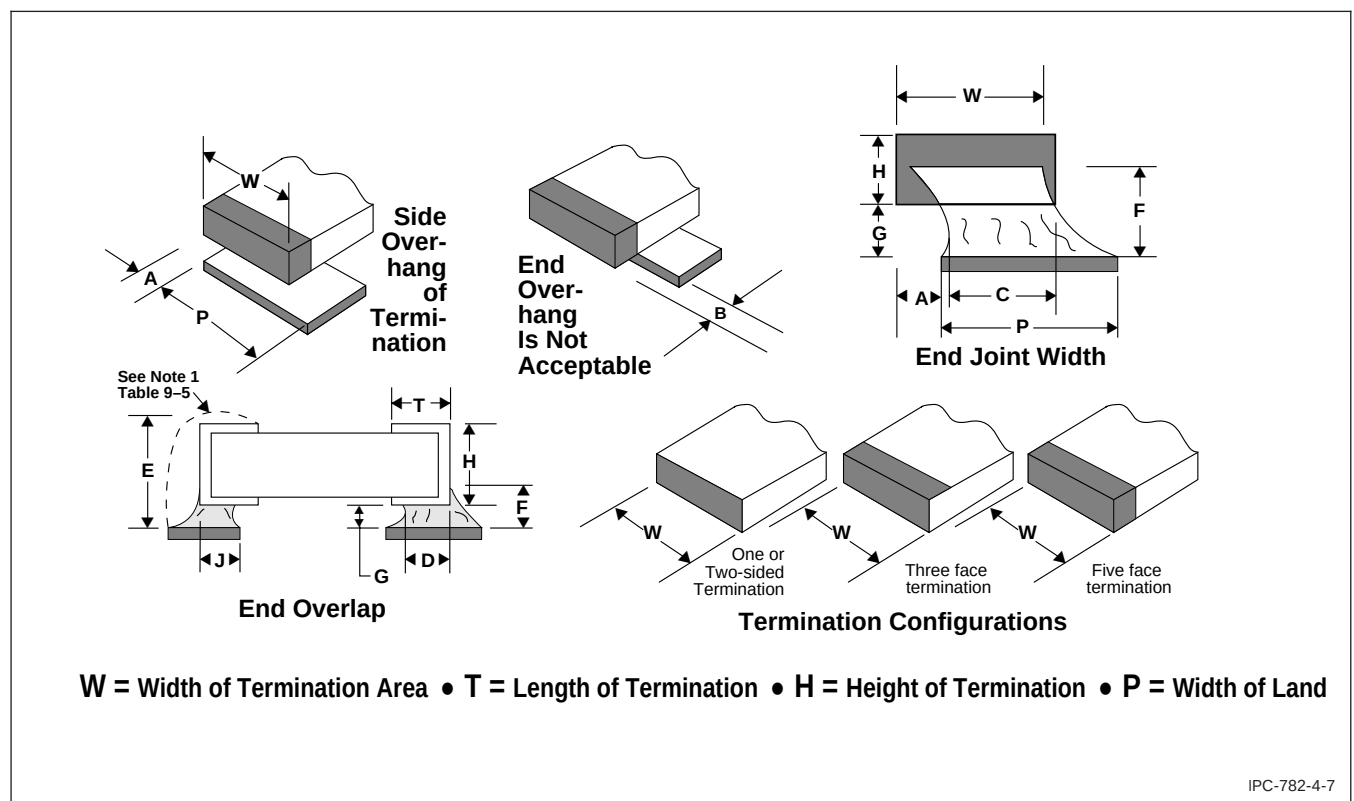


Figure 4-7 Rectangular or square end components

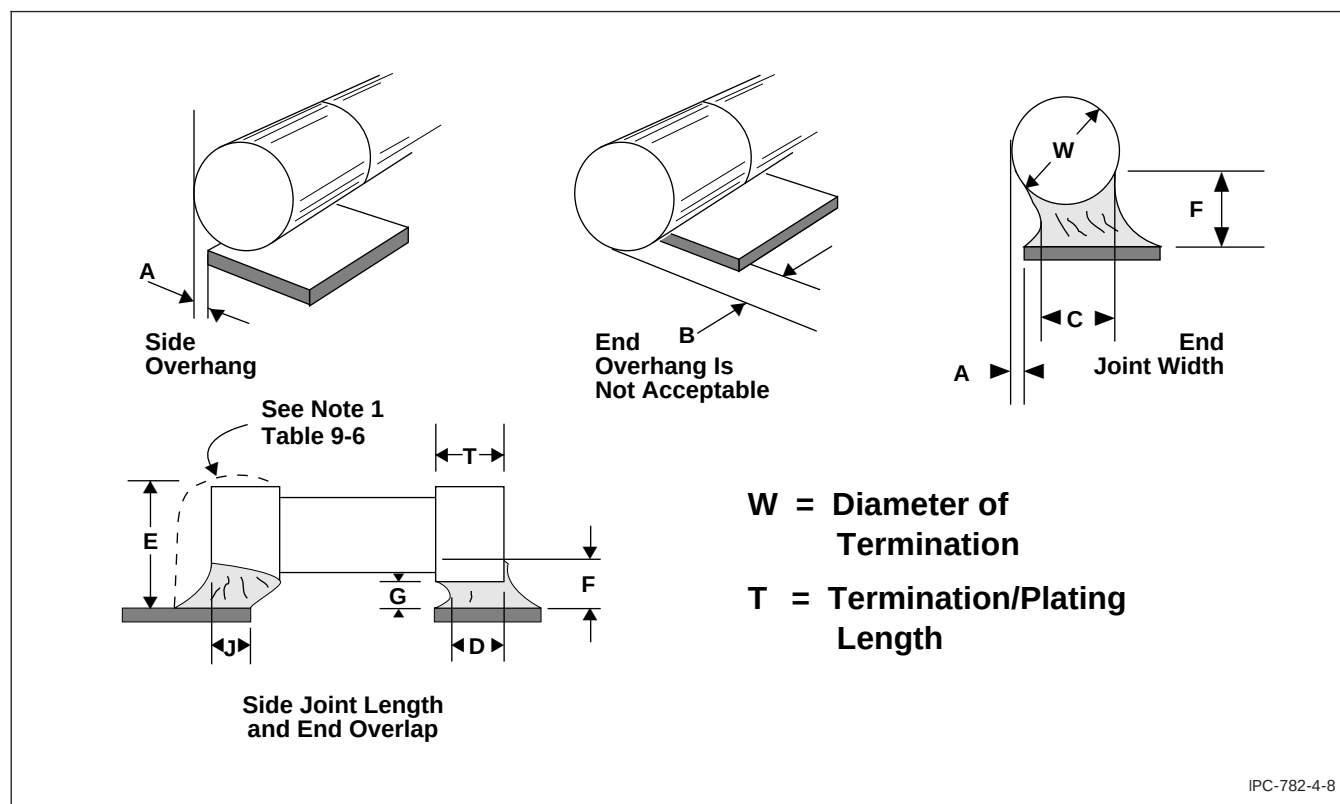


Figure 4-8 Cylindrical end cap terminations—joint illustration

Note: See ANSI/J-STD-001 for specific details on minimum acceptability requirements.

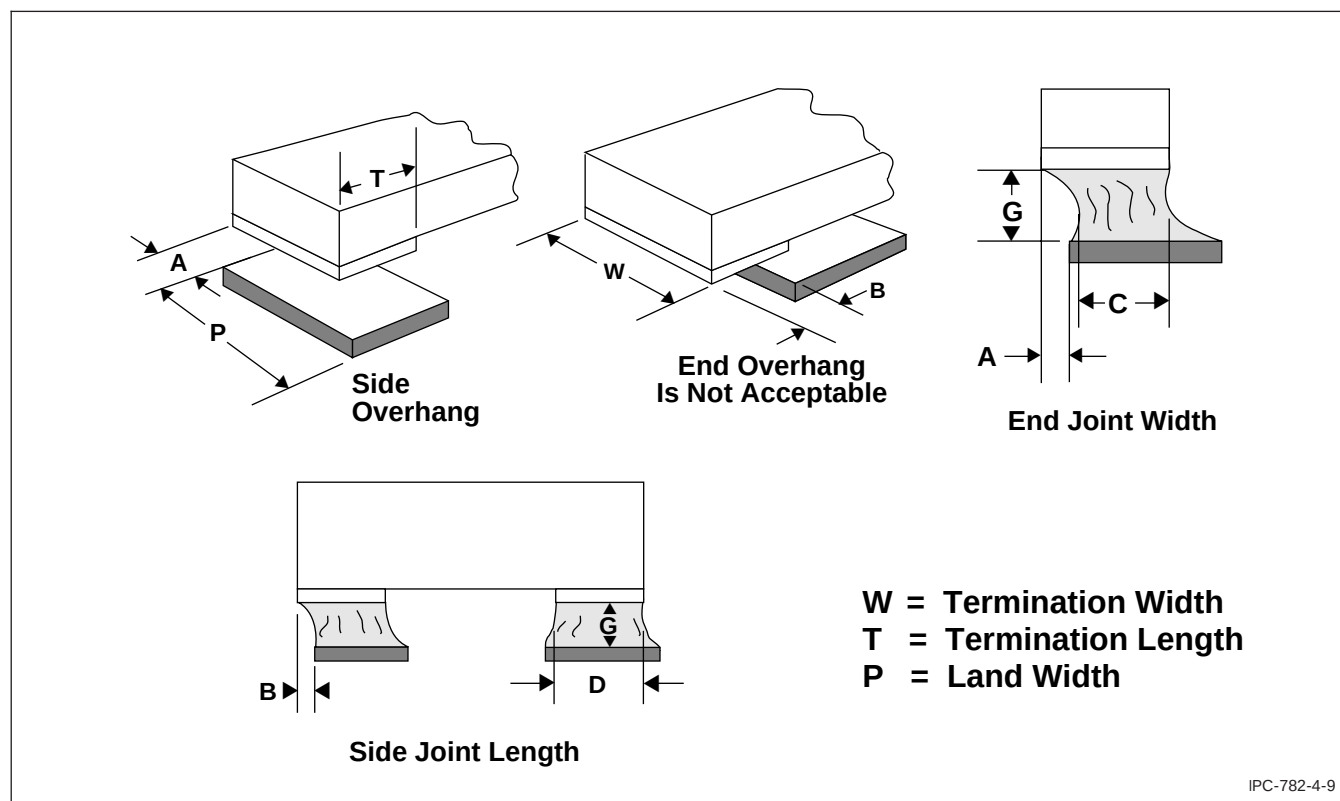


Figure 4-9 Bottom only terminations