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## Guidelines for Chip-on-Board Technology Implementation

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A standard developed by IPC

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# **Guidelines for Chip-on-Board Technology Implementation**

Developed by the Direct Chip Attachment Task Group of the  
Hybrid and Related Technologies Committee of IPC

APPROVED DECEMBER 20, 1990 BY



AMERICAN NATIONAL STANDARDS INSTITUTE

Users of this standard are encouraged to participate in the  
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# Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the Direct Chip Attachment Task Group of the IPC Hybrid and Related Technologies Committee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

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# Guidelines for Chip-on-Board Technology Implementation

## 1.0 INTRODUCTION

The ancient philosopher Heraclitus said, "There is nothing permanent except change." This aphorism is perhaps nowhere better exemplified than it is in the field of electronics fabrication. Since the middle of this century, the rate of technological change in the electronics industry has accelerated at a dizzying pace. No sooner does one garner a sense of the current technology base than it is outdated.

Technology has evolved from simple point-to-point discrete wiring to very complex multilayer rigid-flex printed wiring boards; from metal eyeleted through holes to through holes metallized in vacuum using sputtering technology; and from circuit lines big enough to be drawn by hand to microscopically small circuit conductors.

Change is with us, change that can make future electronic products cheaper, faster and more reliable. However, in order to profit from that change it must be harnessed. We must be masters of change, not slaves to it. How do we achieve this? We must control change through documentation. This document provides guidance for designers, assemblers, and users in the emergent Chip-On-Board (COB) technology so that they can harness the power and energy of this changing technology more effectively.

COB has found its greatest application in the consumer electronics market in such items as programmed game cards for electronic video games. COB has two major subsets:

- Chip-and-Wire technology where the integrated circuit die is first adhesively bonded to a printed wiring board and is then interconnected by wire bonding with either gold or aluminum wire; and
- Flip Chip technology where the integrated circuit die is plated with solder bumps at the interconnect points and soldered in an inverted fashion to the board, thus effecting both attachment and interconnection in one step. Flip chip bonding has also been done using a conductive organic-based adhesive (rather than solder) onto organic based printed boards.

An allied technology of note is Tape Automated Bonding (TAB). This technology uses reel-to-reel processing and gang bonding assembly equipment. It is typically processed in rolls of 8 mm to 70 mm metal clad polyimide or modified epoxy tapes, not unlike standard photography film.

TAB technology has been used extensively to produce the digital watches we wear and the credit card calculators we carry. Another new technology being developed will incorporate elements of both COB and TAB, though information

is insufficient at this writing to accurately portray the technique.

COB technologies will see increased usage in all sectors of electronic production, perhaps even in military and aerospace applications, once their long term reliability is proven. It is the technology of the future.

**1.1 Scope** This document provides guidelines for the use of Chip-on-Board Technology (hereafter this term may be referenced by the acronym COB). These guidelines include:

- Design guidelines,
- Manufacturing information,
- Assembly guidelines,
- Testing guidelines, and
- Bibliographic references.

**1.2 Purpose** COB is the logical extension of hybrid circuit technology, but with additional advantages to be discussed later. This document is intended to be an aid to the provider or user of COB technology by providing guidelines for its successful implementation as a continuation of the evolution of electronic assembly from through-hole mount to surface mount and on to the finer pitch of COB.

**1.3 Applications** Applications for COB circuits include:

- Consumer,
- Industrial/Telecommunications/Computers,
- Military,
- Avionics, and
- Medical/Life Support.

The type of application will dictate the materials and assembly processes to use. Once a suitable materials system has been chosen, size and cost will determine the physical appearance of the completed circuit. Different physical appearances (types) include:

- Only bare devices on one side,
- Only bare devices on both sides,
- Bare devices and surface mount components on one side,
- Bare devices and surface mount components on both sides, and
- Mixed circuits consisting of combinations of bare devices, surface mount components and through hole components.

COB technologies are certain to see increased usage in all sectors of electronic production, possibly even in military and

way into military and aerospace applications, once the data is presented that assures long term reliability. It is much like standard Surface Mount Technology, the technology of the future that is here today, awaiting only a cohesive guiding light to show the way; one that will come to bear on all the important issues that block the way of our industry to more fully embrace this important new technology and make it a wide spread reality.

## 2.0 REFERENCE DOCUMENTS

Although many of the following are not specifically referenced in this document, they are cited as being pertinent to chip-on-board technology implementation.

### 2.1 Institute for Interconnecting and Packaging Electronic Circuits (IPC)

**IPC-T-50** Terms and Definitions for Interconnecting and Packaging Electronic Circuits

**IPC-D-249** Design Standard for Flexible Single- and Double- Sided Printed Boards

**IPC-FC-250** Specification for Flexible 1 & 2 Sided Printed Boards

**IPC-D-319** Design Standard for Rigid Single- and Double-Sided Printed Boards

**IPC-D-325** End Product Documentation for Printed Boards

**IPC-A-600** Acceptability of Printed Boards

**IPC-A-610** Acceptability of Printed Board Assemblies

**IPC-CM-770** Printed Board Component Mounting

**IPC-SM-780** Guidelines for Component Packaging and Interconnecting with Emphasis on Surface Mounting

**IPC-SM-782** Surface Mount Land Patterns (Configurations and Design Rules)

**IPC-CC-830** Qualification and Performance of Electrical Insulating Compounds for Printed Board Assemblies

**IPC-SM-840** Qualification and Performance of Permanent Polymer Coating (Solder Mask) for Printed Boards

**IPC-H-855** Hybrid Microcircuit Design Guide

**IPC-D-949** Design Standard for Rigid Multilayer Printed Boards

**IPC-ML-950** Performance Specification for Flexible Multilayer Boards

### 2.2 Electronic Industries Association (EIA)

**IS-30** Resistors, Surface Mount

**JEDEC Publication 95** Registered and Standard Outlines for Solid State Products

### 2.3 Department of Defense (DoD)

#### 2.3.1 Standards

**MIL-STD-202** Test Methods for Electronic and Electrical Components

**MIL-STD-275** Printed Wiring for Electronic Equipment

**MIL-STD-454** Standard General Requirements for Electronic Equipment

**MIL-STD-810** Environmental Test Methods

**MIL-STD-883** Test Methods and Procedures for Microelectronics

#### 2.3.2 Specifications

**MIL-P-13949** Revision G, Plastic Sheet, Laminated, Metal Clad for Printed Boards

**MIL-C-14550** Copper Plating, Electrodeposited

**MIL-P-28809** Printed Wiring Assemblies

**MIL-M-38510** Microcircuits, General Specification for

**MIL-G-45204** Gold Plating, Electrodeposited

**MIL-P-55110** Printed Boards, General Specification for

**MIL-P-81728** Plating, Tin Lead, Electrodeposited

### 2.4 Federal

**QQ-S-571** Solder, Tin Alloy, Lead-Tin Alloy and Lead Alloy

### 2.5 American National Standards Institute (ANSI)

**ANSI Y-14.5** Dimensioning and Tolerancing

### 2.6 American Society For Testing Materials (ASTM)

**ASTM-F-72** Specification for Gold Wire for Semiconductor Lead-Bonding

**ASTM-F-219** Testing Fine Round and Flat Wire for Electronic Devices and Lamps

**ASTM-F-487** Specification for Fine Aluminum 1%-Silicon Wire for Semiconductor Lead Bonding

**ASTM-F-584** Practice for Visual Inspection of Semiconductor Lead Bonding

**ASTM-F-638** Specification for Aluminum 1%-Magnesium Wire for Semiconductor Lead Bonding

## 2.7 International Society for Hybrid Microelectronics (ISHM)

### GLOSSARY OF HYBRID CIRCUIT TERMS

**2.8 Terms and Definitions** The definitions of terms shall be in accordance with IPC-T-50 and the following:

**Angled Bond** Bond impression of first and second bond are not in a straight line.

**Back Bonding** Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry face up. The opposite of back bonding is face down bonding.

**Ball Bond** A bond formed when a ball shaped end of an interconnecting wire is deformed by thermocompression against a metallized pad. The bond may also be designated a nail head bond from the appearance of the flattened ball.

**Beam Lead** A long structural member not supported everywhere along its length and subject to the forces of flexure, one end of which is permanently attached to a chip device and the other end intended to be bonded to another material, providing an electrical interconnection or mechanical support or both.

**Beam Lead Device** An active or passive chip component possessing beam leads as its primary interconnection and mechanical attachment means to a substrate.

**Bond** An interconnection which performs a permanent electrical and/or mechanical function.

**Bond Deformation** The change in the form of the lead produced by the bonding tool, causing plastic flow, in making the bond.

**Bond Envelope** The range of bonding parameters over which acceptable bonds may be formed.

**Bond Interface** The interface between the lead and the material to which it was bonded on the substrate.

**Bond Lift-Off** The failure mode whereby the bonded lead separates from the surface to which it was bonded.

**Bond Off** See Bond lift off.

**Bond Pad** See Bonding area.

**Bond Schedule** The values of the bonding machine parameters used when adjusting for bonding. For example, in ultrasonic bonding, the values of the bonding force, time, and ultrasonic power.

**Bond Site** The portion of the bonding areas where the actual bonding took place (see Bonding area).

**Bond Strength** A measure of force or pressure required to separate a layer of material from its base. This may be

measured as peel strength, in pounds per inch of width, or as pull strength, in pounds per square inch, when a perpendicular pull is applied to the surface of the material. In wire bonding, it is the pull force required to rupture the bond interface or wire. Typically measured in gram-force.

**Bond-to-Bond Distance** The distance between successive bonds of a given interconnect wire or lead.

**Bond Tool** The instrument used to position the lead(s) over the desired bonding area and impart sufficient energy to the lead(s) to form a bond.

**Bondability** Those surface characteristics and conditions of cleanliness of a bonding area which must exist in order to provide a capability for successfully bonding an interconnection material by one of several methods, such as ultrasonic, thermosonic, or thermocompression wire bonding.

**Bonding, Die** Attaching the semiconductor chip to the substrate, either with an epoxy, eutectic or solder alloy.

**Bonding Area** The area, defined by the extent of a metallization land or the top surface of the terminal, to which a lead is or is to be bonded.

**Bonding Pad** A metallized area to which a connection is to be made.

**Bonding Wire** Fine gold or aluminum wire for making electrical connections in hybrid circuits between various bonding pads on the semiconductor device, substrate, or package terminals.

**Bulk Conductance** Conductance between two points of a homogeneous material.

**Burn-In** The process of electrically stressing a device (usually at an elevated temperature environment) for an adequate period of time to cause failure of marginal devices.

**Camber** A term that describes the amount of overall warpage present in a substrate.

**Capillary** A hollow bonding tool used to guide the bonding wire during the bonding cycle. Also applies a combination of heat, pressure, mechanical energy, or ultrasonic energy during the bonding cycle (depending upon the bonding process chosen).

**Capillary Tool** A tool used in bonding where the wire is fed to the bonding surface of the tool through a bore located along the long axis of the tool.

**Ceramic Package** (Sometimes referred to as a “cofired ceramic package”)—a package body made up of tape-cast or pressed aluminum, beryllia, or aluminum nitride “pre-forms.” Conductive patterns are defined on multiple layers in the “green” state. Then layers are stacked and laminated and fired at high temperature to yield a monolithic multi-layered structure.



**Centerwire Break** The failure mode in a wire pull test where the wire fractures at approximately midspan.

**Chip** The uncased and normally leadless form of an electronic component part, either passive or active, discrete or integrated.

**Chip-and-Wire** A technology employing face-up-bonded chip devices exclusively, interconnected to the substrate conventionally (i.e., by flying wires). More properly designated as “die and wire.”

**Chisel** A specially shaped bonding tool in the shape of a chisel used for wedge bonding and ultrasonic bonding of aluminum or gold wires to elements or package leads.

**Chopped Bond** Those bonds with excessive deformation such that the strength of the bond is greatly reduced.

**Circuit** The interconnection of a number of electrical elements and/or devices, performing a desired electrical function.

**Coefficient of Thermal Expansion** The ratio of the change in length per unit length to the change in temperature.

**Compliant Bond** A bond which uses an elastically and/or plastically deformable member to impart the required energy to the lead. This member is usually a thin metal foil that is expendable in the process.

**Compliant Member** The elastically and/or plastically deformable medium which is used to impart the required energy to the lead(s) when forming a compliant bond.

**Conductive Adhesive** An adhesive material that has metal power added to increase electrical conductivity.

**Conductive Epoxy** An epoxy material (polymer resin) that has been made conductive by the addition of a metal powder, usually gold or silver.

**Conductivity** The ability of a material to conduct electricity; the reciprocal of resistivity.

**Controlled Collapse** Controlling the reduction in height of the solder balls in a flip-chip processing operation.

**Cratering** Defect in which a portion of an IC chip pad, under a bond, is torn loose by excessive ultrasonic energy or insufficient force.

**Creep** The dimensional change with time of a material under load.

**Cure Time** The total elapsed time between the addition of a catalyst and the complete hardening of a material; also the time for hardening of premixed, frozen, or refrigerated epoxy adhesives.

**Current Carrying Capacity** The maximum current which can be continuously carried by a circuit without causing objectionable degradation of the electrical or mechanical properties.

**Cutoff** The operation following the final bonding step that separates the bond from the wire magazine.

**Die (Plural Dice)** Bare, unprotected Integrated Circuit (IC) chip(s).

**Die Bond** Attachment of a die or chip to the substrate.

**Dielectric Constant** The term used to describe a material's ability to store charge when used as a capacitor dielectric. It is the ratio for the charge that would be stored with free space as the dielectric to that stored with the material in question as the dielectric.

**Dielectric Loss** The power dissipated by a dielectric as the friction of its molecules opposes the molecular motion produced by an alternating electric field.

**Direct Contact** A contact made to the semiconductor die when the wire is bonded directly over the part to be electrically connected, as opposed to the expanded contact.

**Electroless Plating** Deposit of a metallic material on a surface by chemical deposition as opposed to the use of an electric current.

**Electron Beam Bonding** Bonding two conductors by means of heating with a stream of electrons in a vacuum.

**Encapsulate** Sealing up or covering an element or circuit for mechanical and environmental protection.

**Eutectic** The specific proportions of the constituents of an alloy having the lowest melting point. The system from totally molten to totally solid without going through a slushy range at the eutectic composition.

**Eutectic Alloy** An alloy having the same liquidous (melting temperature) as solidus (solidification temperature).

**Hermetic Seal** A seal that is gas tight—there is no exchange of internal gasses with those outside of the package. By definition, a plastic encapsulated package is not hermetic (measured in atm-cm<sup>3</sup>/sec.)

**Intermetallic Bond** The ohmic contact made when two metal conductors are welded or fused together.

**Intermetallic Compound** A compound of two or more metals that has a characteristic crystal structure that may have a definite composition corresponding to a solid solution, often refractory.

**Lid** Abbreviation for “leadless inverted device.” A shaped, metallized ceramic form used as an intermediate carrier for semiconductor chip devices, especially adapted for attachment to conductor lands of a thick-or-thin film network by reflow solder bonding.

**Metallization** A film pattern (single or multilayer) of conductive material deposited on a substrate to interconnect electronic components, or the metal film on the bonding area of a substrate which becomes a part of the bond and performs both an electrical and a mechanical function.

**Microbond** A bond of a small wire, such as 0.025 mm [0.001 inch] diameter gold wire, to a conductor or to a chip device.

**MOS Device** Abbreviation for a metal oxide semiconductor device.

**MTBF** Abbreviation for mean time between failures. A term used to express the reliability level. The reciprocal of the failure rate.

**Nonconductive Epoxy** An epoxy material (polymer resin) either without a filler or with a ceramic or mineral powder filler added for increasing thermal conductivity and improving thixotropic properties. Nonconductive epoxy adhesives are used in chip to substrate bonds where electrical conductivity to the bottom of the chip is unnecessary or in substrate-to-package bonding.

**Nugget** The region of recrystallized material at a bond interface which usually accompanies the melting of the materials at the interface.

**Off Bond** Bond that has some portion of the bond area extending off the bonding pad.

**Parallel Gap Soldering** Passing a high current through a high-resistance gap between two electrodes to remelt solder thereby forming an electrical connection.

**Parallel Gap Welding** Passing a high current through a high-resistance gap between two electrodes that are applying force to two conductors, thereby heating the two workpieces to the welding temperature and effecting a welded connection.

**Passivation** The formation of an insulating layer directly over a circuit or circuit element to protect the surface from contaminants, moisture, or particles.

**Peel Strength (Peel Test)** A measure of adhesion between a conductor and the substrate. The test is performed by pulling or peeling the conductor off the substrate and observing the force required. Units are oz/mil or lb/in. of conductor width.

**Pull Strength** The values of the pressure achieved in a test where a pulling stress is applied to determine breaking strength of a lead or bond.

**Pulse Soldering** Soldering a connection by melting the solder in the joint area by pulsing current through a high-resistance point applied to the joint area and the solder.

**Purple Plague** One of several gold-aluminum compounds formed when bonding gold to aluminum and activated by re-exposure to moisture and high temperature (340°C). Purple plague is purplish in color and is very brittle, potentially leading to time-based failure of the bonds. Its growth is highly enhanced by the presence of silicon to form ternary compounds.

**Push-Off Strength** The amount of force required to dislodge a chip device from its mounting pad by application of force to one side of the device, parallel to the mounting surface.

**Reducing Atmosphere** An atmosphere containing a gas such as hydrogen that will reduce the oxidation state of the subject compound.

**Reflow Soldering** A method of soldering involving application of solder prior to the actual joining. To solder, the parts are joined and heated, causing the solder to remelt, or reflow.

**Resistance Welding** The joining of two conductors by heat and pressure with the heat generated by passing a high current through the two mechanically joined materials.

**Sagging or Wire Sag** The failure of bonding wire to form the loop defined by the path of the bonding tool (droop) between bonds.

**Scrubbing Action** Rubbing a chip device around on a bonding pad during the device attachment operation to break up any oxide layers and improve wetability. Typically part of the solder or eutectic attachment operation.

**Search Height** The height of the bonding tool above the bonding area at which final targeting adjustments are made (prior to lowering the tool for bonding).

**Second Bond** The second bond of a bond pair made to form a conductive connection.

**Second Search** That portion of machine cycle at which final targeting adjustments in the location of the second bond under the tool are made prior to lowering the tool for making the second wire bond. This is analogous to “first search” during the first bond.

**Shear Rate** The relative rate of flow or movement (of viscous fluids).

**Sputtering** The removal of atoms from a source by energetic ion bombardment, the ions supplied by plasma. Process is used to deposit films for various thin-film applications.

**Squashout** The deformed area of a lead which extends beyond the dimensions of the lead prior to bonding.

**Stitch Bond** A bond made with a capillary-type bonding tool when the wire is not formed into a ball prior to bonding.

**Tail (of the Bond)** The free end of wire extending beyond the bond impression.

**Thermal Mismatch** Differences of thermal coefficients of expansion of materials which are bonded together.

**Thermocompression Bonding** A process involving the use of pressure and temperature (substrate temperature)

approximately +300°C.) to join two materials by interdiffusion across the boundary.

**Thermosonic Bonding (TS Bonding)** A wire bonding process using both thermocompression and ultrasonic energy to join two materials by interdiffusion across the interface boundary (substrate temperature 150°C).

**Ultrasonic Bonding** A process involving the use of ultrasonic energy and pressure to join two materials.

**Ultrasonic Cleaning** A method of cleaning that uses cavitation in fluids caused by applying ultrasonic vibrations to the fluid.

**Vacuum Deposition** Deposition of a metal film onto a substrate in a vacuum by metal evaporation techniques.

**Vacuum Pickup** A handling instrument with a small vacuum cup on one end used to pick up chip devices.

**Viscosity** A term used to describe the fluidity of material, or the rate of flow versus pressure. A unit of viscosity is Poise (P) (centipoise (cps) = 1/100 poise, kcps = 1000 centipoise.) Other units of viscosity are Pascal•sec (P•S) and Stokes (st).

**Wafer** A slice of semiconductor crystal ingot used as a substrate for transistors, diodes, and monolithic integrated circuits.

**Warpage** The distortion of a substrate from a flat plane.

**Wedge Bond** The second bond of a thermocompression or thermosonic bonding process. This can also be either the first or second bond of the ultrasonic bonding process.

**Wire Bonding** The method used to attach very fine wire to semiconductor components to interconnect these components with each other or with package leads.

### 3.0 DESIGN OF COB STRUCTURES

The design of COB structures starts with the decision to use direct chip attachment and interconnection to the packaging and interconnecting (P&I) structure. That decision is based on the advantages and disadvantages of the COB assembly technique as outlined in section 1.2 of this document.

The advantages include:

- Lower cost (in high volume),
- Lighter weight,
- Smaller packages,
- Lower “Z” dimension profile (thinner packages),
- Shorter circuit paths (faster switching speed),
- Improved impedance control,
- Reduced number of interconnection levels in the overall system (fewer solder joints), and
- Shorter turn-around time for prototypes and production.

The disadvantages include:

- Specialized capital equipment required,
- Unprotected integrated circuit chip handling techniques required,
- Chip encapsulation and metallurgy must be carefully selected to meet environmental and mechanical requirements,
- User/vendor relationship required for acquisition of fully tested, uncased integrated circuit chips
- For chip and wire, the total number of chips per assembly might be limited by the expected burn-in yield per chip, and
- CAD tools may need to be modified to accommodate chip-on-board

All of these potential advantages and disadvantages will be discussed later in this document.

It is hoped that this document will provide enough direction and background for the careful and informed consideration of these criteria. Whatever the impetus for the choice of COB, a design procedure that can help insure a manufacturable design is as follows in sections 3.1 to 3.1.10.

**3.1 System Requirements** The system specification will identify several factors influencing the selection or determination of design criteria. The environment in which the system must operate, system size, weight, reliability, power, and signal sources and levels should be specified by the system specification. In addition, manufactured-item cost, life-cycle cost, and cost-versus-performance criteria should be available from the systems design activity. System definition may include a schematic diagram or may be limited to block diagrams indicating simple functions and signal flow information. In either case, the system must be partitioned into realizable circuit functions. For some types of COB, the maximum number of chips per board could be a consideration here.

The environmental requirements during storage, shipment and use of the COB assembly could easily indicate the substrate, joining method and/or type of encapsulant used.

The power handling capabilities of COB structures often require the consideration of thermal enhancements (thermal vias, etc., if the power to be dissipated is more than 1/2 to 1 watt per chip, depending on the density of chips on a substrate and the type of substrate material employed.

**3.1.1 Circuit Requirements** Form, fit and function are primary considerations at this stage of design. Partitioning into repetitive functions that can be configured in multiples represents an opportunity for cost reduction, while conversely, increasing complexity within a packaged function may adversely affect producibility. Also, other factors

pinout requirements should be considered in the partitioning step in the interest of final package commonality. The form function, if lowest profile is the prime consideration, could dictate COB.

**3.1.2 Breadboard** Demonstration of the circuit function in breadboard form serves to identify performance restrictions that affect eventual substrate layout. Testability and verification of functional performance are determined at this stage. At this stage, COB could also help lessen turn around time for breadboarding, reducing design interval significantly.

**3.1.3 Final Circuit Schematic** Final definition of the circuit schematic diagram will develop from a successful bread board evaluation. At this stage of development, component definition must be considered that includes performance specification and package or COB compatibility with respect to alternate assembly processes. The availability of unpackaged semiconductor devices may well be the determining factor in the selection of process methods and/or the assembly sequence to be used.

**3.1.4 Component Count and Availability** Component definition and count will affect board size because of topological considerations. Layout restriction associated with alternate process design rule and performance-related criteria developed in the breadboard stage must also be considered. If required, the custom development of a semiconductor function or package may affect the project schedule.

**3.1.5 Process Definition** The completion of final component selection will permit process definition. The assembly techniques to be used (e.g. COB, surface mount, through hole, mounting, mixed technologies), the reflowed solder assembly temperature hierarchy (for solder reflow, epoxy cure) and the system interconnect are influenced by component selection, packaging selection and system requirements.

**3.1.6 Design Review** Evaluation of producibility of the selected process should be conducted at this stage. Compromises made at previous stages should be reconsidered if they affect the manufacturability of the product.

**3.1.7 Substrate Layout** When component process and producibility issues have been resolved, circuit layout can commence. This involves coupling module size, pinout, performance, and testability requirements with established design rules.

**3.1.8 Prototype Fabrication** The inherent electronic performance improvement resulting from reducing the magnitude and complexity of interconnections must be balanced against possible interference due to this increased packag-

ing density. Design verification is best accomplished by prototype evaluation. For any addition to performance criteria, cost projections, producibility and the status of manufacturing resources should be evaluated.

**3.1.9 Critical Design Review** System design, Quality Control and Assurance, Manufacturing, Cost Accounting, and Management functions should participate in a final Critical Design Review Agreement on the design, or at least an awareness of design parameters is desirable if related activities are to perform effectively as a team to meet project objectives.

**3.1.10 Manufacture** Experience accumulated in manufacturing should be communicated to the various activities to ensure that design rules and process capability updates are reflected in product designs.

## 3.2 Components

**3.2.1 Integrated Circuit Dice (Chips)** The integrated circuit chips used to build COB structures are usually in the same form as those used to build hybrid circuits on ceramic substrates, or to fabricate dual-inline packages (DIPs). Bipolar, NMOS, CMOS, HCMOS, or any chip technology used in hybrid packages may be used to fabricate COB structures. Either gold or aluminum chip metallization may be used, with gold or nickel or, in the case of TAB, even solder or conductive polymer on the board. The only requirement is that the metallization on the chip be compatible with that on the board for the type of chip bonding to be used. Chip size and layout from different vendors but for the same application may be different. **Caution:** Be sure process parameters (time, temperature, etc.) are compatible with die suppliers requirements.

**3.2.1.1 Chips for Wire Bonding** The limited availability of bare integrated circuit (IC) chips has impeded the use of COB technology. Many potential COB designs have been done using the more expensive packaged device approach because only packaged devices were available. However, as COB technology gains acceptance as the cheapest and perhaps only technology which will meet physical design requirements, chip manufacturers and equipment assemblers will strike practical agreements.

When shipping bare, unprotected IC chips, usually termed “die” (singular) or “dice” (plural), one must choose the form in which the dice are transported from manufacturer to assembler. With TAB, this form is tape, but with the chip and wire technique, there is a choice of methods:

**A. Waffle Packs**—These are square plastic trays segregated into multiple smaller squares or rectangular cavities (hence the term “waffle”). Each cavity is made to the proper size to house one die. A plastic lid is placed over the

it's respective cavity during shipment. The advantage of waffle packs is that the chip manufacturer can ship electrically "good" dice only, without divulging his wafer yield to his customer. The potential disadvantage of shipping in waffle packs is that the dice are left free to slide and bounce around in their "waffle" cavities, and can be scratched during shipment, rendering them electrically defective in some cases. This can be avoided if the size of the waffle "cell" is properly designed, or the cell is filled with a "gel" material that holds each die in place until use.

**B. Wafer Form**—In this method, the entire silicon wafer, which has not yet been "diced" or sawed into individual chips, is shipped from the supplier to the assembler. The advantage of this method is that the wafers can be shipped easily with minimal scratches. The disadvantage is that the assembler must have a wafer saw to dice the wafer, and must visually or electrically inspect each chip that he saws before assembling it into COB structures. The potential disadvantage to the chip manufacturer is that he reveals his wafer yield to the customer, and some manufacturers are reluctant to do that.

Another manifestation of this shipment method is called "stretch membrane." In this method, the wafer is mounted on an adhesive coated "stretch" film material supported at its edges by a metal frame. A wafer mounted on such a "film frame" can then be sawn at the manufacturer and shipped to the assembler with the sawing already accomplished. The frame is then returned after all the dice are used.

**C. Die-in-Tape**—A proposal for a packaging alternative to the waffle packs and wafers on sticky tape is packaging dice in a carrier tape similar to surface mount technology (SMT) resistors and capacitors. Such a package scheme would offer the promise of adapting standard surface mount equipment for COB placement. This tape would meet the requirements of EIA-481-A (Taping of Surface Mount Components for Automatic Placement), but have more stringent cleanliness requirements. Electrostatic Discharge (ESD) precautions would also need to be more stringent. The reel for die components would be smaller than for SMT since most of the die bonding equipment available is smaller than SMT placement equipment and could not handle the 330 mm size reel that is the smallest called out in the EIA-481-A Standard.

The advantage of tape and reel over waffle pack is that more dice can be placed without having to go to another pack since waffle packs only hold 12 to 100 or so die. A reel of die could hold up to 300 or more parts. With wafers on sticky tape, there can be hundreds of die per wafer, but with die bonder size restrictions, only one or two wafers can be put on the input stage. This requires multiple passes through a die bonder if there are more unique dice to be placed. The tape and reel packaging will be dense enough to allow 5 or 10 different dice to be placed with the die

bonder in one pass. In summary, the tape and reel packaging would represent the best of both worlds, waffle packs and wafers on sticky tape.

**D. Glass Vials**—Some devices having relatively simple geometries may be shipped in bulk. Diodes, for example, are frequently shipped in glass vials of 10,000 to 30,000 dice each. The propensity for scratching is great for dice shipped in this "loose" form, so that this method is often frowned upon. Also, the die attach machine will have to reorient the position of each die before placement. Waffle packs (of proper design), Gel Paks<sup>TM</sup> and stretch membranes all maintain the devices top side up and in neat arrays.

Automatic pick-and-place systems for die placement can usually accept dice either in waffle packs or in diced wafer form. In the case of the diced wafer, defective chips are indicated by the presence of an ink dot placed on each bad chip when tested at the manufacturer in wafer form, or they can have a "wafer map," a paper or software record of defective chip locations on the wafer.

Thus, the technology used to make the IC chips for COB is less of a concern than the method of shipment. When the chip manufacturer and the COB assembler are the same, there is no problem. If they are different organizations, a close user-vendor relationship must exist.

**3.2.1.2 Chips for TAB-Type Lead Bonding** There are basically two types of chips used for Tape Automated Bonding (TAB) or other TAB-type lead bonding. "Bumped chip" lead bonding requires input/output (I/O) pads plated with gold bumps that will allow the inner lead bonding of TAB tape, or circuitized TAB to the chip. Alternatively, bumped leads may be used, and the chip can then be identical to those used for chip and wire COB.

In the bumped chip method, bumps must be applied to the chip by electroplating or by applying some other thick (approximately 0.025 mm [0.001 inch]) metallization (typically pure gold) onto the I/O pads of the chip. This must be accomplished prior to the dicing (or sawing) of the wafer, so that accurate placement of the bumps (typically pure gold) onto the pads is possible. Bump application, therefore, is often done at the chip manufacturers location, although some vendors offer chip bumping service along with inner lead bonding. The structure of a typical chip bump is shown in Figure 3-1. Fabrication of these structures, and use of these processes are discussed in section 4.2.1.

**3.2.1.3 Chips for Flip Chip Bonding** Flip chip interconnection usually requires solder to form the bond between the chip pads and the pads of the printed board or other P&I structure. Flip chip is usually used on a ceramic substrate instead of a printed board substrate because of the

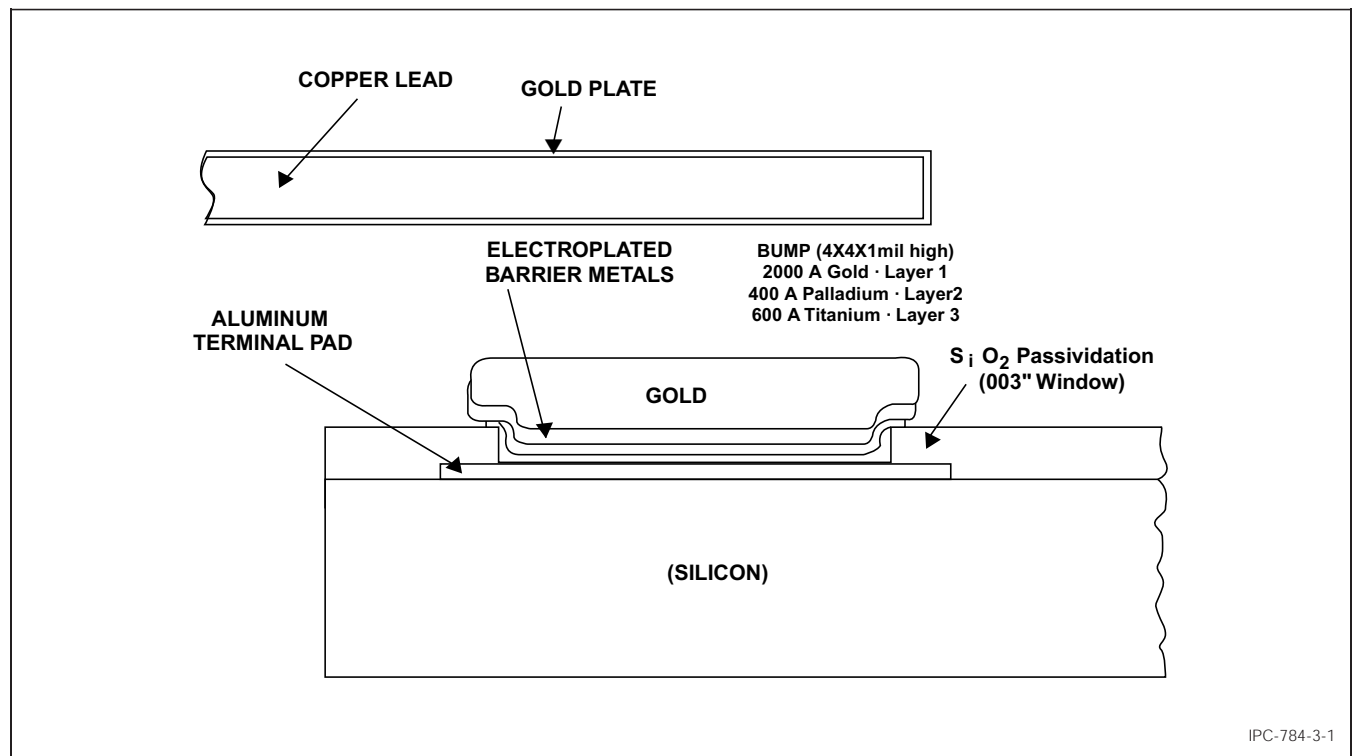


**Figure 3-1 Interconnection geometry of bumped-chip TAB**

difference in coefficient of thermal expansion (CTE) between a silicon chip and an organic-based board is too great for flip chip solder joints. Developments in aramid and graphite reinforced organic materials now make this possible. In addition, the fine pitch of the I/O pads of an IC chip is very difficult to fabricate onto a printed board substrate.

However, some methods of flip chip attachment which use conductive polymer attachment instead of solder require only that the I/O pads of the chip allow good adhesion and electrical connection to the conductive polymer used. For instance, aluminum pads on a CMOS chip may require gold metallization. No further restrictions on size or technology of the die apply. However, like most COB applications, heat transfer could limit the types of chips that could be attached this way.

**3.2.1.4 Other Components** The remaining components that support the COB circuitry will determine whether to complete the circuit with surface mount or through hole components. Avoid mixing surface mount and through hole components. This adds process steps, reduces yield and increases cost. This section deals mostly with surface mount components.

Power resistors, voltage regulators, power transistors, surge suppressors, transformers, fuses, large value/ high voltage capacitors and connectors usually require through hole mounting. Digital or low power analog circuits may be better suited to complete surface mount.

The price and availability of surface mount components have improved dramatically. Most designers are familiar with resistors, capacitors and semiconductors in surface mount form. Less familiar components that have been converted to surface mount recently include fast recovery diodes, ceramic resonators, crystal oscillators, pin and box connectors, relays, transient suppressors and switches.

If bare dice are not available for integrated circuits, SOIC or PLCC packages can be used. Thermal mismatch problems preclude the use of leadless ceramic carriers on most organic materials. Low power two and three terminal devices should be obtained in the SOT23 package. The SOT89 package is presently the most popular surface mount package for higher powers, but the DPAK may reduce its popularity. High power two terminal devices are also available in the MELF (tubular) format. Not all pick and place machines can work with this style of component. Its roundness may make it more likely to roll off the board after placement.

Use rectangular thick film chip resistors. As with chip capacitors, make sure the terminations have a nickel barrier. Standard tolerances are 1% and 5%. Try to use standard values, listed in manufacturer's catalogs. High power resistors may be available in the tubular format.

Use ceramic chip capacitors for the low capacitance values. Tantalum chip capacitors in rectangular molded plastic packages are available for higher capacitance applications.

For applications that are not suitable for tantalum capacitors, surface mount electrolytics will soon become available.

Signals on the COB circuit must ultimately be routed to the outside world, and the connectors used are components also. The type and implementation of the circuit determine the connector system to use. For “modular” circuits that plug into larger circuit boards, consider edge-clip leads. These are attached by solder dipping. Low in price, edge clips have been used to make ceramic DIP and SIP modules for years. The module can, then, be treated as a through hole component and soldered into the main board. A connector on the main board can be used if numerous insertion/removal cycles will be required.

For large pin counts, a surface mount pin and box connector system may be best, provided the connector is not physically stressed.

**3.3 Printed Boards as P&I Structures** Today’s semiconductor technology requires high device speeds and high interconnection density at low cost. Semiconductor packages were originally developed using multilayer ceramic (inorganic based) technology. The relatively high dielectric constant of the ceramic coupled with the low electrical conductivity of the metallization (tungsten or molybdenum) limits the use of ceramic packages for some applications. Therefore, printed wiring board (organic) based technology is replacing some ceramic packages. Printed wiring board packages offer improved electrical and comparable thermal performance, lower cost and reduced lead time from design to production. Another advantage of the printed wiring board package is natural match of the coefficient of thermal expansion to the circuit pack printed wiring board. This makes the printed wiring board based package a perfect choice for surface mount applications on standard printed wiring boards, particularly in low cost applications where hermeticity is not an absolute requirement.

Printed wiring boards for COB applications will require finer line and spacing geometries than applications for mounting packaged components.

**3.3.1 Board Design** Most COB applications are custom designed. This means that pin array patterns, pin input/output functions, package dimensions, wire bond pad location and size, circuit details, and many other features are determined by the requirements of the chip. In a custom package it is possible to control such details as thermal dissipation, critical lead lengths, and circuit impedance. The only disadvantage of custom design is the loss of standardization and the proliferation of designs.

**3.3.1.1 Thermal Vias** Plated-through holes used as thermal vias dissipate heat well. By placing plated-through

holes under the chip, thermal resistance through the COB structure can be reduced. This allows heat sinks to be used effectively on the backside of the COB module. (Section 3.4 discusses this in more detail.) In many cases, such a printed wiring board design gives heat dissipation characteristics superior to ceramic. However, this design technique reduces routing space under the chip. **Caution:** The use of thermal vias, if improperly designed, may cause cleaning or thermal shock concerns.

**3.3.1.2 Electrical Design Issues** The flexibility of the printed wiring board design permits easily controlled lead lengths in critical paths in order to minimize delays and inductance to ground. The lower dielectric constant of epoxy compared to ceramic reduces delay times for the same circuit lengths, although the epoxy will exhibit a higher dissipation factor. In addition, ground planes allow tight control of circuit impedance for designs using emitter coupled logic (ECL). In this case, very tight tolerances (often one mil or less) must be maintained on both line widths and dielectric thickness in order to obtain the required impedance.

**3.3.1.3 Computer-Aided Design (CAD) Issues** Traditionally, a CAD system has been used to design printed wiring boards based on chip and package requirements. The CAD data is then used to make the tools for the printed wiring board manufacturer. A CAD system allows rapid design changes which can then be put into manufacture quickly.

COB circuits can have several characteristics which set them apart from other assembly approaches, i.e.:

- Small size,
- Wire bonds that can cross etched conductors,
- Small number of IC’s (1-5), and
- Fine dimensional features

Hand generated artwork may not satisfy the fine feature requirements, in which case a CAD system with photo-plotted or pattern generated artwork will be required.

A system with autorouting capability may not deal with wire bonds properly; however the system can be fooled into thinking that wire bonded chips are surface mount components, although some density and flexibility may be lost.

Personal computers (PCs) are outstanding design tools. They can be used for circuit design, as well as for tasks that dedicated layout systems cannot handle—word processing, spread sheets etc. A PC based system will quickly pay for itself while a larger system may become obsolete before its pay-back period.

Software for PC’s falls into two classes: dedicated layout and documentation packages and general purpose drawing