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SURFACE MOUNT COUNCIL

An Introduction to
Tape Automated
Bonding & Fine
Pitch Technology



Material in this guideline was voluntarily coordinated by the Surface Mount Council (SMC), and established by Technical Committees of IPC, ASTM, EIA and JEDEC. Members of committees on the four organizations contributed their time, knowledge and expertise to blend a cohesive report on the topic covered by this document. Proposals were sent to key individuals in each of the individual organizations for consensus. Meetings were held to resolve differences or conflicts prior to documenting the information in the final released version.

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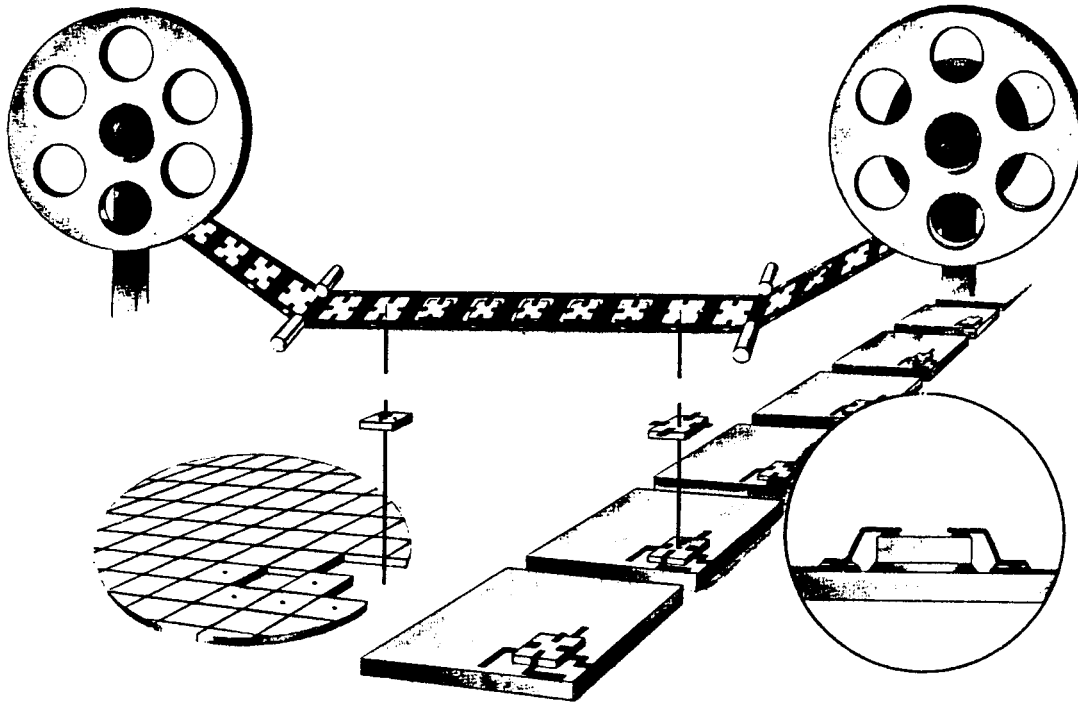
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SMC-TR-001

AN INTRODUCTION TO TAPE AUTOMATED BONDING FINE PITCH TECHNOLOGY



About this Technical Report

This document published by the Surface Mount Council is for **informational purposes only**.

It is not a standard, and in fact, is not a final document.

This document is intended to report to you on the work being done by a variety of organizations concerned with surface mounting. We invite you to review the details in this document. We then encourage you to communicate to the appropriate trade associations or societies any comments or observations you have regarding details published in this report, or ideas for additional details that would serve the industry.

This document contains examples of work being done by the trade associations and societies shown below. For example, only a small sample of Joint Electron Device Engineering Council (JEDEC) outlines are included as a part of this Technical Report. Additional outlines will be in the comprehensive standards to be published later by JEDEC and EIA.

For additional information regarding material published in this Technical Report, we urge you to contact the organizations listed below.

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Acknowledgement

In response to the need for a document covering Fine Pitch Technology and Land Patterns, SMC-TR-001 was developed. Because ASTM, JEDEC, EIA, and IPC have members worldwide who participated in this effort, SMC-TR-001 represents a comprehensive report on the subject of Fine Pitch Technology, with an emphasis on Tape Automated Bonding (TAB) and Design Rules. While the principle members of the Task Group are listed below, a special note of thanks goes to everyone who assisted in the development of this document.

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Foreword

Background

Tape Automated Bonding is a semiconductor assembly and packaging technology originally developed by General Electric in 1968 as a possible replacement for wire bonding. Tape Automated Bonding (TAB) literally involves the automated bonding of a semiconductor device (die) to a flexible lead frame (tape); the tape (also known as carrier tape and beam tape) is the primary characteristic of TAB assembly. After bonding the die to the tape, the die functions can be tested by contacting the tape's test pads prior to committing the TAB unit to further processing.

TAB circuits are produced in many tape widths. The three primary widths are 35 millimeter (mm), 48 mm, and 70 mm. The 35 and 48 mm tapes are primarily for small chip sizes and low lead count. 70 mm tape is primarily used for VLSI and ASIC devices to accommodate the larger chip size as well as allow fan-out of the test pads to a usable layout.

Since 1987, the electronics industry has done considerable work to establish standards for Fine Pitch Technology (FPT) and Tape Automated Bonding (TAB). FPT is emerging as the descriptive term for the interconnection technology for fabricating and assembling integrated circuit (IC) packages with finely pitched leads, ranging from 0.1 to 0.5 mm (0.004" to 0.020").

Fine Pitch Technology offers many advantages over Through Hole Technology and conventional Surface Mount Technology (SMT), including the following:

- Lower Component Package Cost
- Lower Profile
- Greater Density
- Improved Reliability
- Improved Electrical Performance
- Greater Flexibility

Many standards exist to support this technology and the missing pieces are rapidly falling into place. Some suppliers are accepting these standards even before they are finalized. It is also possible to buy compatible TAB tape carriers and sockets. Equipment vendors are moving rapidly to build off-the-shelf handling systems now that some standards have been adopted by the industry.

In March of 1988, the Electronic Industries Association's JC-11 Committee approved registration for TAB tape carriers compatible with outer lead bonding pitches of 0.5 mm (0.020") and 0.25 mm (0.010"). In addition, three tape outlines were registered for "Super" widths.

Presentations were made to members of the Surface Mount Council on all the work done during 1987 regarding standardization for TAB devices and techniques.

The initial work was done by representatives of a "TAB Forum" under the auspices of the American Society for Testing and Materials (ASTM), and then sent to the Electronic Industries Association (EIA) and the Joint Electron Device Engineering Council (JEDEC) Committee. The council recommended that the Institute For Interconnecting and Packaging Electronic Circuits (IPC) form a liaison with the other two groups in order to determine the entire spectrum of standardization for TAB.

The Surface Mount Council recommended that representatives of the three organizations meet to discuss developing a unified orderly definition of standards for Tape Automated Bonding, and techniques for implementing this technology into electronic hardware. At a special two-day meeting, an AD HOC Committee was formed. This Committee recommended the development of this document which provides information on standardization to the electronics community.

During special review meetings the user community reviewed the material contained in this report. All comments received from a world-wide industry circulation were discussed and merged into the present document.

After the appropriate review and comment period, this document was published by the Surface Mount Council so that members of the electronics industry could obtain this important information on standardization and implementation of Fine Pitch Technology.

The SMC-TR-001 document will continue to evolve. As the technology matures, updates will be provided so that the user community is continually apprised of new techniques and progress.

The groups involved in writing of this document are now writing and issuing standards documents for the fine pitch packages, board design and board assembly requirements.

Classifications

Design and performance requirements for Fine Pitch Technology and Tape Automated Bonding vary for different end-product applications.

Three general classes for different end product applications have been established to reflect progressive increases in sophistication, functional performance requirements and testing inspection frequency. These three classes are as follows:

• **Class 1** — Consumer Products

This class includes television, toys, home entertainment, electronics and noncritical consumer and industry control devices. Products in this class are suitable for applications where cosmetic imperfections are not of importance and the major requirement is functionality of the completed product.



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- **Class 2** — General/Industrial

This class includes computers, communication equipment, sophisticated business machines, instruments in certain non-critical military applications. This class of product is suitable for high performance commercial and industrial products in which extended life is required, but for which uninterrupted service is not critical. Certain cosmetic imperfections are allowed.

- **Class 3** — High Reliability

This class includes those equipments where continued performance is critical, equipment down-time cannot be

tolerated, or the equipment is a life-support item. Products in this class are suitable for applications where high levels of assurance are required and uninterrupted service is essential.

Unless otherwise noted, dimensions and tolerances are expressed in metric with inches shown in brackets [], and are not necessarily direct conversions in order to provide usable numbers. Users are cautioned to employ a single system and to not intermix millimeters and inches. Reference information is shown in parentheses ().



An Introduction to Tape Automated Bonding Fine Pitch Technology

1.0 INTRODUCTION

The use of fine pitch technology will increase with the increasing use of higher pin count devices such as Application-Specific Integrated Circuits (ASICs) and microprocessors. A fine pitch package is any package with lead pitches 0.625 mm [0.025"] or less as long as the package is molded or encapsulated to allow pretesting before placement on the substrate. The maximum size of the package is controlled by, among other things, the ability of the pick-and-place machine to accurately place the device on the substrate. This size is generally around 37.5 mm [1.5"] maximum on each side. If the pin counts increase such that the package size must exceed this limit, the lead pitch must drop below 0.625 mm [0.025"] to maintain the size around 37.5 mm [1.5"], depending on the type of pick-and-place machine.

The effect of the fine pitch on the existing Surface Mount Technology (SMT) infrastructure depends on the lead pitch. For example, for lead pitches of 0.625 mm [0.025"] and above the existing SMT processes of screen printing, placement, reflow and rework can be used with some modification. However, FPT requires thinner printing paste. One solution is dual thickness printing, which can deposit 0.2 mm [0.008"] of paste for 1.25 mm [0.050"] packages and 0.15 mm [0.006"] of paste for fine pitch packages. Another solution is geometric reduction in screens/stencils. For accurate placement, the need for vision becomes almost mandatory. Also, the rework process becomes somewhat more difficult, though the hot air systems can still be used effectively.

Some packages with 0.625 mm [0.025"] lead pitch are available with and without corner bumpers. The bumpers protect the fragile leads from damage. The Japanese packages generally do not have corner bumpers and require waffle packs for component handling. This then complicates problems in component placement because a waffle pack handler is generally needed to pick-up parts from the waffle pack to a fixed pick position.

The effect on the SMT infrastructure is even more significant when the lead pitch drops to 0.5 mm [0.020"] or below. The package design itself may have to change so that the package can be held in a carrier. The carrier protects the leads during testing, shipping and handling but it must be excised and bent before placement. This requires either a different pick-and-place system or an attachment for excising the carrier and bending the leads. Also, proper screen or stencil printing of solder paste becomes difficult. Hence, solder is applied by other means such as plating or

solder "bumping" (printing and reflow of paste before component placement).

The reflow process may also have to change. For example, a hot bar process may be easier than infrared or vapor phase. Such a system combines placement, soldering and rework in one machine.

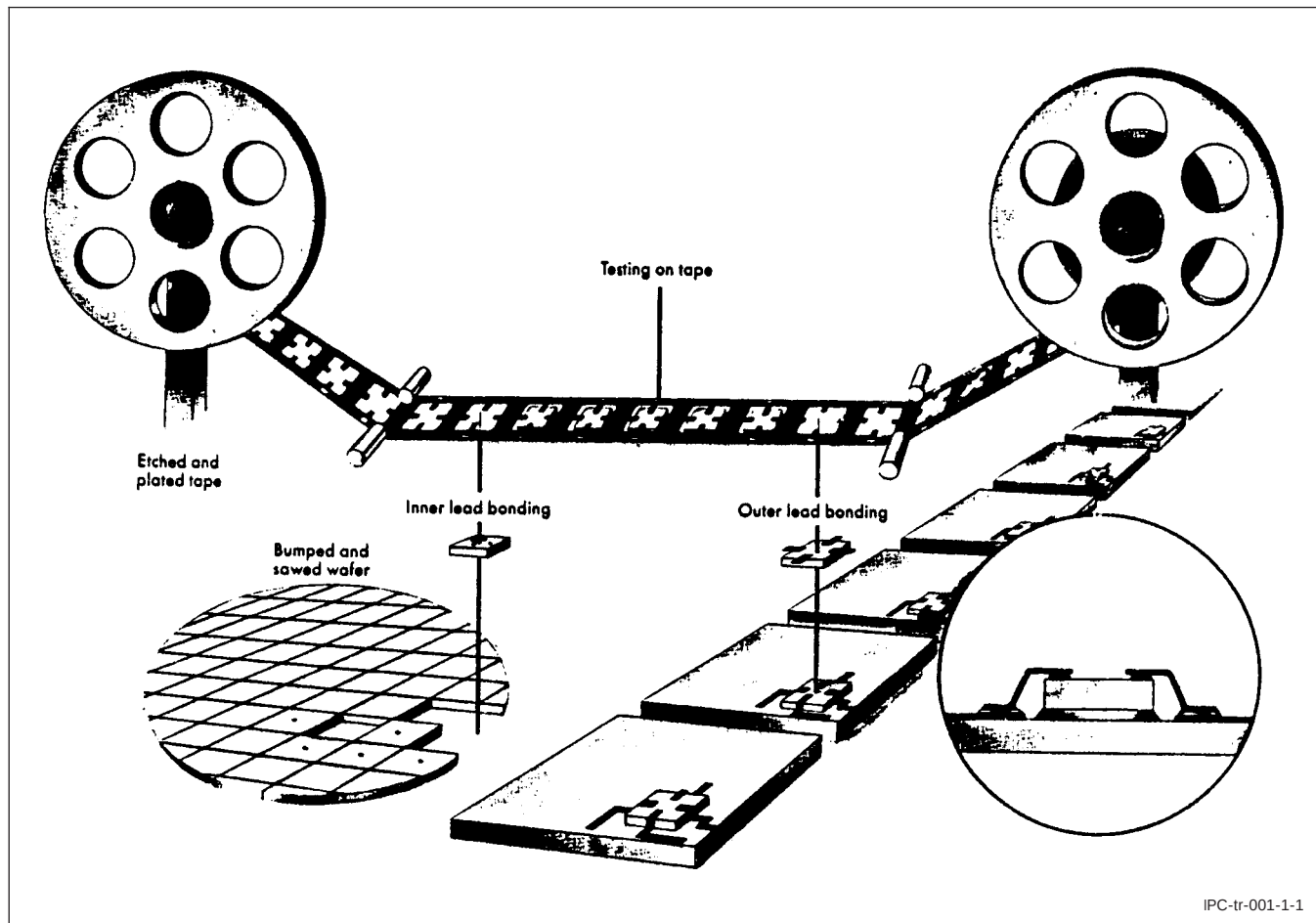
Since the die in the fine pitch packages are usually large, they are also usually susceptible to moisture induced package cracking and hence require baking before reflow. Also, such packages may require heat sinks to provide effective package cooling. However, attaching heat sinks before reflow often interferes with accurate placement.

So, fine pitch may significantly affect the existing SMT processes. Nonetheless, high pin count devices require Fine Pitch Technology. One promising type of Fine Pitch Technology is Tape Automated Bonding (TAB). TAB uses photo-imaging/ etching processes to produce conductors on a dielectric/conductor tape "movie-film" format. (See Figure 1-1).

The most visible aspect of a TAB system is the carrier tape, which is 8 to 70 mm [0.32 to 2.8"] wide and stored on reels. Windows are formed at specific locations in the tape and a thin conductive layer is applied to the tape, usually 0.035 mm (0.0014") thick copper. A conductive pattern is then created in the conductive layer to give the desired interconnection circuitry with "beam-type" leads that extend over the windows in the tape. In subsequent processing, the beams are bonded to an integrated circuit die that is precisely located under the windows. Sprocket holes or features on the tape carrier permits automated tape-handling equipment to accurately position the individual dice for the subsequent processing operations, such as testing, burn-in, and board mounting. Fiducials/registration marks on the tape may be used for alignment with vision systems during bonding/handling.

1.1 Advantages For mounting semi-protected integrated circuit (IC) dice to printed boards, TAB has the following advantages:

- The bonding areas on the die can be hermetically sealed by a bump or cap on the bonding land.
- TAB requires less gold than gold wire bonding.
- TAB test leads provide a means for pretesting and "burn-in" of the dice prior to their final mounting.
- Innerlead Bonding pads can be 0.05 mm [0.002"] square on 0.1 mm [0.004"] spacing, or even smaller.
- High input/output counts (300 or more leads).



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Figure 1-1 Typical TAB process flow (bumped wafer)

- Low (0.75 mm [0.030"]) profile chip-on-board (COB) assemblies.
- Weight reduction.
- Automated mass bonding of the leads is possible.
- TAB chips require only a fraction of the surface area required for packaged IC dice (see Figure 1-2).
- The rectangular TAB lead has a lower lead impedance and inductance than a round wire, thus enhancing high-speed applications.
- Since leads are excised during the placement operations, lead damage due to shipping and handling is minimized.
- Improved heat transfer relative to wire-bonded attach due to copper beam leaded technique.

1.2 Disadvantages Disadvantages of the TAB process are as follows:

- It may require specially designed equipment to match each application, at both the chip and board interfaces.
- Wafers are presently expensive in small quantities.
- There is presently a lack of commercially available "bumped" tape, wafers, or dice.

- TAB bonding and bumping equipment is more sophisticated than printed board assembly equipment.
- Chip-on-tape components (TAB carriers) are presently expensive in small quantities.
- TAB inner- and outer-lead bonding locations have not yet been fully standardized.
- Dynamic burn-in of TAB packages is more costly in both hardware tooling and burn-in.

1.3 Comparison of Interconnect Technologies Fine Pitch Technology (FPT) differs in several respects from both Through-Hole Technology and TAB board assembly Surface Mount Technology (SMT). Table 1-1 lists the main aspects of package interconnecting and rates the applicability of three different technologies for each aspect.

Through-Hole Technology requires component lead mounting holes in printed wiring board lands; they are not required for SMT or FPT. In most SMT design technologies, vias are located away from the land pattern in order to minimize solder flow down the hole and away from the land. This approach wastes real estate. A better alternative is FPT which uses lands with solder-filled vias.

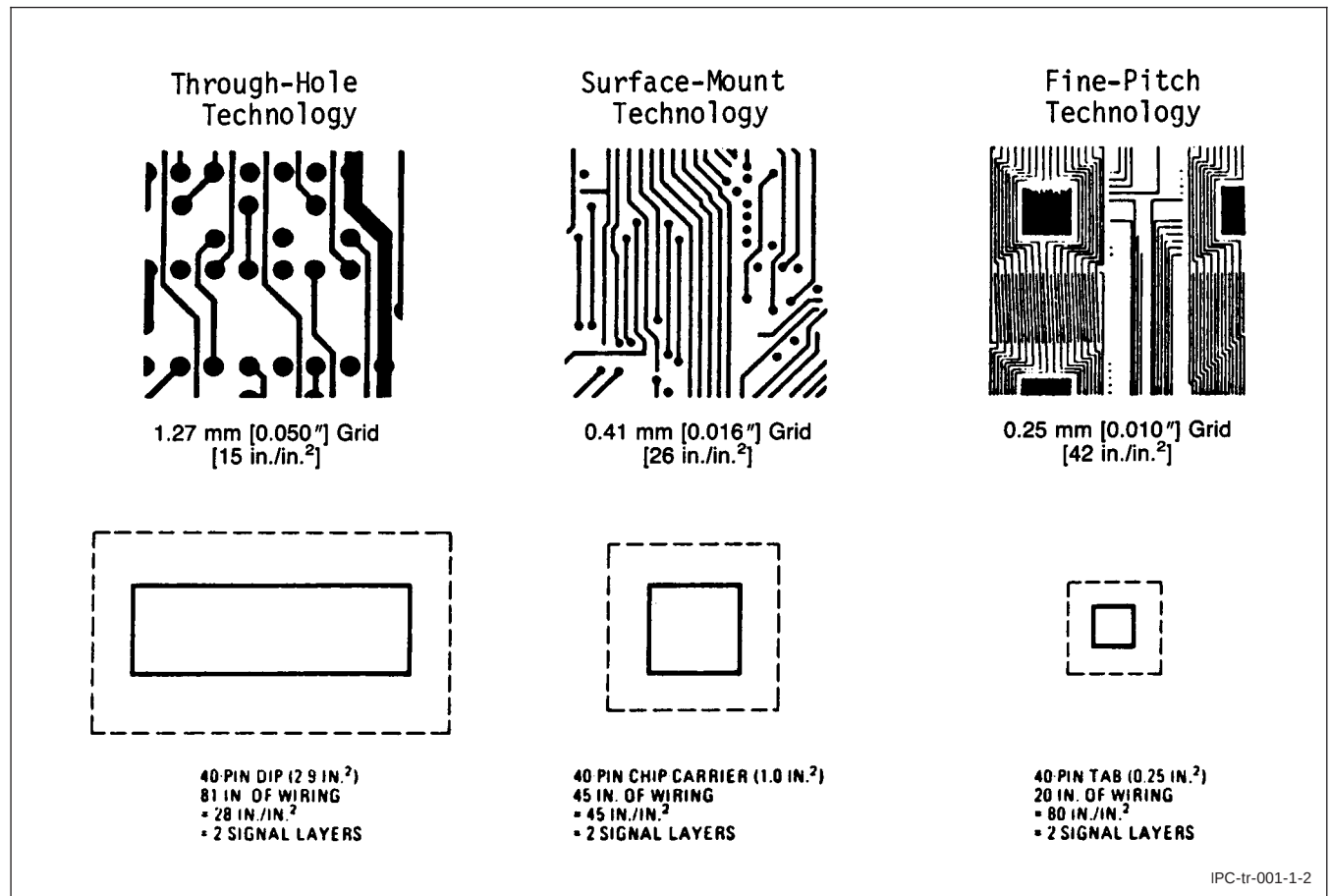


Figure 1-2 Printed board-level density comparisons of component interconnecting techniques

Table 1-1 Process Comparison

	Through-Hole Technology	Surface-Mount Technology	Fine-Pitch Technology
Lands with Lead Mounting Holes	5	—	—
Lands with External Vias	—	5	3
Lands with Internal Vias	—	2	4
Component Insertion	5	—	—
Component Placement	—	5	3
Component Lead Excise, Form & Placement	—	—	3
Use of Solder Paste	—	5	3
Use of Solder Mask	3	4	4
Land Solder Bumping	0	3	4
Use of Conductive Adhesive	0	1	2
Wave Soldering	5	2	0
Mass Reflow soldering	—	5	4
Localized Reflow Soldering	1	3	4
Manual Assembly (in volume)	2	1	1
Automated Assembly (in volume)	5	5	5
Rework and Repair	5	4	4
Process Control	3	4	5

5 = Essential or Common Usage
 4 = Possible and Recommended
 3 = Desirable (but not mandatory)

2 = Not Recommended or Stretching the Technology
 1 = Possible (but impractical)
 0 = Avoid at All Costs

Through-Hole technology commonly uses automated component insertion while FPT and SMT use automated component placement. Manual assembly is possible for each of these approaches but not practical for volume assembly.

SMT assemblies commonly use solder paste to add enough solder to assure a quality solder joint. Unfortunately, solder paste complicates the interconnection process and hides yield problems caused by board solderability. Solder bumped lands avoid some of these problems. Solder bumped lands are made by adding fused solder to each land area prior to assembly. Flux holds the component and cleans the metal oxides during reflow.

Conductive adhesives can replace the solder joint; however, this approach is not recommended in volume production because of high costs and process difficulties. Wave soldering is commonly used for through-hole technology but is not always suitable for SMT components and should not be used for FPT packages. SMT and FPT packages are best reflow soldered either in mass or individually (localized reflow).

Since no process is perfect, rework and repair techniques are always necessary, but you should avoid them because rework and repair costs money and reduces quality. In particular, the cost of rework and repair increases significantly as the lead pitch and lead size decrease.

The best method to reduce the amount of rework and repair and its attendant cost is effective process controls. The complexity of the FPT packages, especially when mixed on boards with through hole and surface mount packages, makes good process control for this technology essential.

1.4 Types of TAB The initial stage of TAB wafer preparation is much the same as that for wire-bonded wafers. A pinhole-free silicon nitride passivation layer, or in some cases silicon dioxide or polyimide, is deposited at low temperatures. The passivation is selectively removed leaving a good portion of the aluminum landed exposed. The die can now be either wire bonded or undergo additional TAB fabrication.

There are basically two methods for fabricating TAB Chip-On-Tape Components: Bumped Die (Basic) TAB and Bumped Tape TAB (BTAB).

1.4.1 Bumped Die (Basic) TAB In the “basic” bumped-chip TAB approach, (Figure 1-3), a barrier metal, such as titanium-tungsten, is deposited over both the exposed aluminum and over the passivation on the periphery of the land. This, plus the addition of 0.025 mm (0.001”) high gold bumps, helps ensure the reliability of the TAB connections to the tape during the innerlead bonding (ILB) process.

The bumping process is typically performed at the wafer level. Wafer bumping may be performed by the semi-

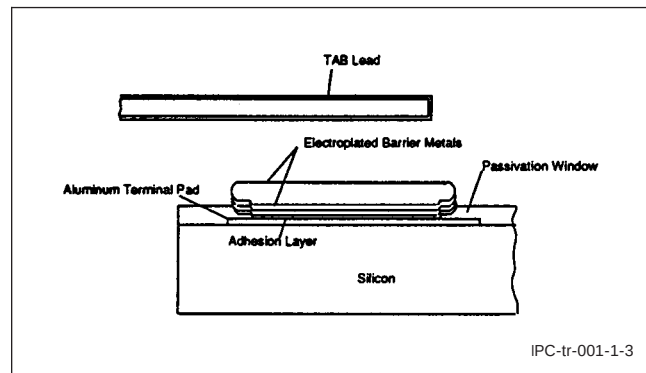


Figure 1-3 Interconnection geometry of bumped-die TAB

conductor manufacturer, independent bumping facilities, or by electronic companies producing “in-house” TAB Chip-On-Tape components.

Since TAB technology is relatively new, bumped wafers from semi-conductor manufacturers are not readily available. In addition, bare wafers may be difficult to obtain (for bumping) because of the manufacturer’s concerns over process propriety and subsequent bumping technology. As TAB technology matures, these problems will probably be resolved (see Section 4.0 for further details of TAB wafer bumping).

Bumps on the die are electroplated onto the barrier metal at each land position. When the bump barrier metal passivation overlaps the passivation, this completely seals the die and further enhances TAB’s reliability as an assembly process. Solder bumps, copper bumps and other metals can also be used, and both copper and gold can be tin plated.

1.4.2 Bumped Tape TAB (BTAB) The other TAB processing approach (Figure 1-4) puts the bump on the tape rather than on the die. This approach is known as BTAB. In either case, the bumps are necessary to elevate the etched tape conductors above the die to prevent shorting of the leads.

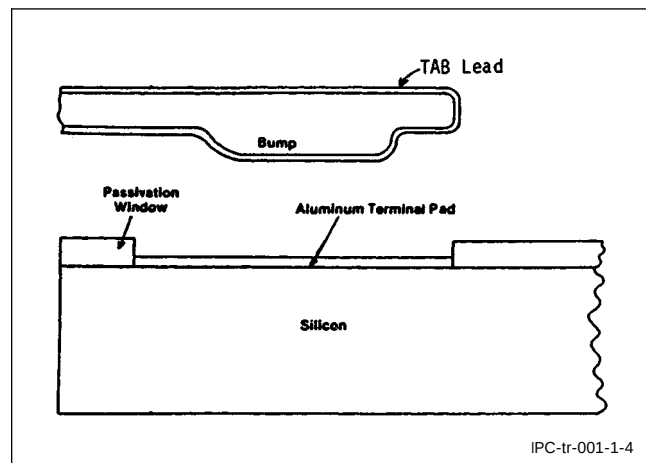


Figure 1-4 Interconnection geometry of bumped-tape TAB (BTAB)

1.4.3 Area TAB One of the most recent interconnection technologies is known as “Area TAB.” In this approach, circuit patterns are fabricated on the tape. This allows the die designer to put the I/O lands at any position on the die, as opposed to being on the periphery of the die.

1.5 Types of Tape In general, there are three types of TAB construction: Single-Layer, Two-Layer, and Three-Layer (Figure 1–5).

1.5.1 Single-Layer Tape Single-layer TAB tape has a conductive foil without any insulating layer. The foil most used for single-layer material is 2 ounce, 0.07 mm (0.0028”), rolled copper. The lead pattern is formed by a photoresist-etch operation. Single-layer TAB is the lowest cost TAB construction, but is not electrically testable because the conductive foil ties all leads together.

1.5.2 Two-Layer Tape Two-layer TAB tape is composed of a conductive layer and an insulating layer. It is made either by depositing copper directly onto a base insulating film, or by casting a film directly onto copper foil. The insulator is usually polyimide.

Sprocket and window patterns in the insulation are formed by chemical etching; lead and sprocket patterns are formed in the copper using normal print-and-etch methods. The insulating film is a carrier, so that copper leads can be electrically isolated from each other in order to allow functional electrical testing of tape-mounted IC dice.

1.5.3 Three-Layer Tape Three-layer TAB tape uses adhesives to hold conductive and insulating layers together. To form sprockets and windows, adhesive-coated insulating film is precisely punched, then conductive foil is laminated to the film. Print-and-etch of the copper side yields the desired lead configurations and test lands. As with two-layer material, the insulator acts as a carrier and electrically isolates the leads to allow functional testing.

1.5.4 Special Configurations Multimetal TAB tapes can be formed in a similar manner. Also, special configurations can be achieved by combining portions of the processes used to make the three basic types of TAB. Multimetal TAB enhances performance and contributes to the feasibility of area TAB.

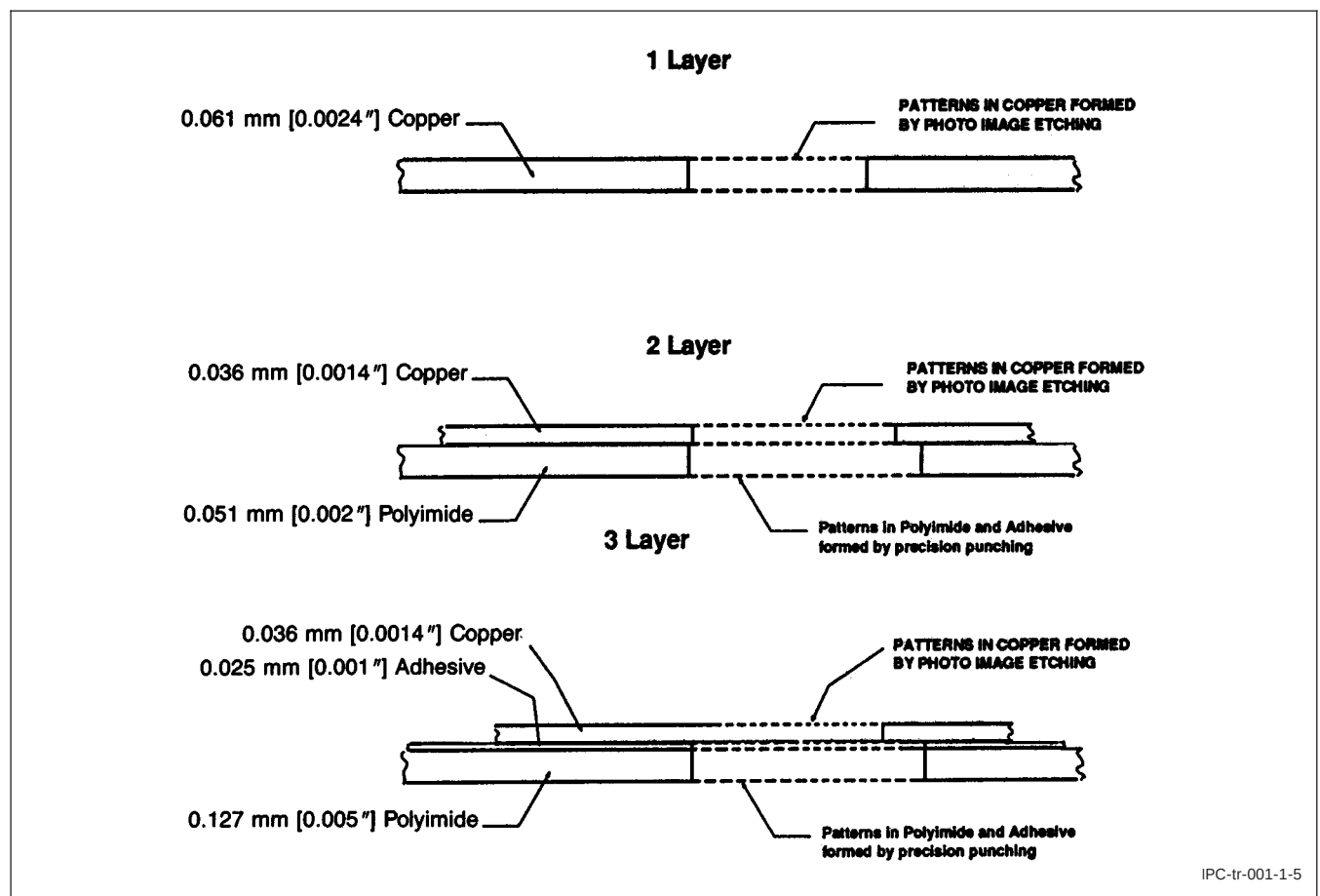


Figure 1–5 1-, 2- and 3-layer TAB constructions

1.6 Lead Bonding

1.6.1 Inner-Lead Bonding (ILB) After the tape is fully fabricated, the next operation is to make the inner-lead bonds between the die and the etched cantilevered conductors on the tape. The positioning for this operation is controlled by the sprocket holes on the tape or by vision systems that directly view the leads and bond pads. Monitoring the die position is done using a television monitor or a microscope.

Simultaneous or sequential bonding of all internal interconnections is then performed by either thermocompression, thermosonic, ultrasonic, laser or reflow bonding. Leads may be bonded one at a time using a single-point bonder with any of these techniques. Mass bonding is also possible using thermocompression and reflow techniques.

Once the die are bonded to the tape, the plating bus points are punched out or otherwise electrically isolated (Figure 1-6) in order to allow the individual dice to be electrically tested and, if required, burned-in. This step is not needed with tin-coated tape because it has no plating bus bar, and thus its leads are already isolated.

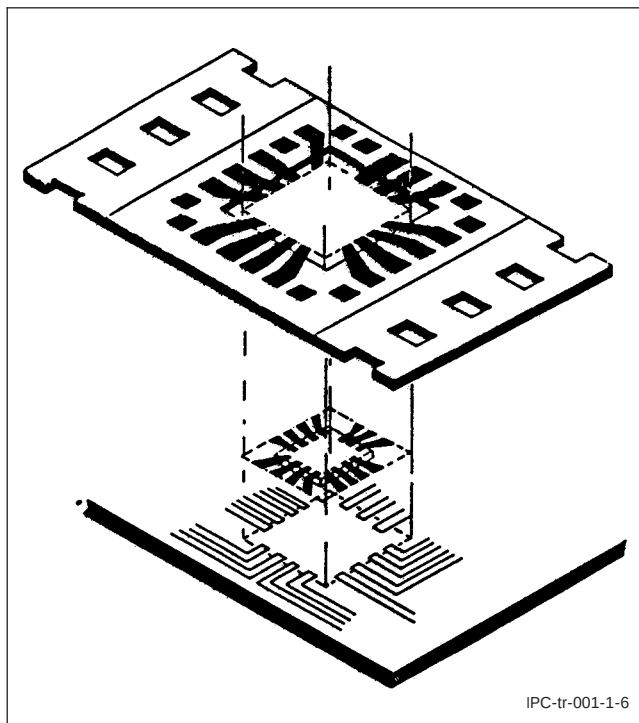


Figure 1-6 Excising of the leaded die from the tape carrier

1.6.2 Outer-Lead Bonding (OLB) After the die has been tested and burned-in, if applicable, the outer-lead bonding operation (OLB) transfers the die, with its leads, to the next-level package or printed wiring board. It is a multiple-step process that is usually done sequentially on a single piece of equipment.

Initially OLB equipment was predominately custom made because of the wide variety of dice, tape and package/board types involved. Standardization efforts by the JC-11 Committee have improved this situation by defining a set number of tape configurations. This tape standardization, especially the window details, helps in dice, package, board and equipment design. However, for nonstandard tapes with a given combination of chip and package/board types, only the excising tool, thermode lead-forming tool (if required) and work fixtures need to be customized.

The first step in the OLB process is to excise the leaded die from the carrier tape (Figure 1-6). The leaded die is then transferred to the board in a way that precisely maintains the original relationship of the die with respect to its tape sprocket holes or to a vision system that positions leads to lands. Thus, the die will be accurately placed on the board.

Depending on the TAB mounting configuration (see Figure 1-7) a secondary lead-forming operation may be included. When required, care must be taken to assure that the leads are shaped down to the board level without shorting them against the electrically-active edge of the die (see also paragraph 6.1.2.)

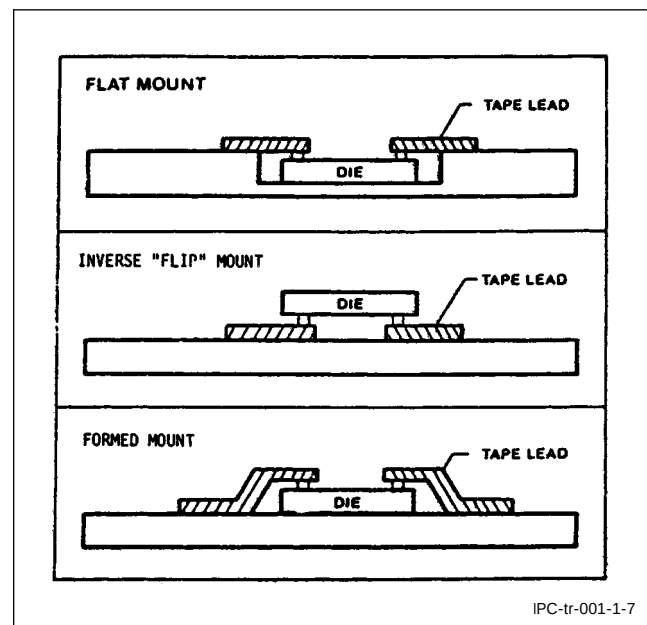


Figure 1-7 TAB mounting options

A bonding operation is then performed on all interconnections by either thermocompression bonding, thermosonic bonding, ultrasonic bonding, reflow, or the use of conductive adhesives. Leads may be bonded one-at-a-time using a single-point bonder, or mass bonded using thermocompression, reflow and conductive adhesive techniques.

1.7 TAB Applications Applications for TAB vary widely depending on overall end-product packaging requirements. TAB is commonly used to attach chips to both organic (printed wiring board) and inorganic (ceramic substrates) substrates.

It has also been used in large assemblies, as well as in single-chip and multi-die packages.

When cost-performance trade-offs are the driving force for the application, assemblies such as the consumer product shown in Figure 1-8 can be made in large quantities. Also, where extremely low assembly profile is important, TAB has been used to assemble “smart” credit cards that are only 0.75 mm (0.030”) thick. Such cards are expected to find a wide usage in banking, telephone, retail and consumer applications.

TAB is also used for small-size and relatively-low cost military personnel “dogtags.” In addition, TAB dice are replacing conventional through-hole and surface mount printed wiring board assemblies in several applications. TAB is also being used to package gate array dice for mid-range and high-end computers, because of its ability to support high lead counts (300+) with good electrical performance.

1.8 Terms and Definitions The following is a list of the terms typically used in the Tape Automated Bonding Industry:

Adhesion Layer The metal layer that adheres the barrier metal to the aluminum bond pad on the surface of the integrated circuit.

Barrier Metal A metal layer used to seal the bond pad on the surface of an integrated circuit die.

Bump A raised metal feature found on either an integrated circuit bond pad or at the end of the inner lead on TAB tape. It is used as part of the interconnect mechanics and metallurgy between the lead and the integrated circuit.

Die Cratering An inner lead bond defect, caused by silicon that has broken away from the integrated circuit die. It is usually under the bump on the bond pad and usually caused by improper bonding conditions.

Die Theta The angle that the edge of the die makes with the tape side.

Edge Shorts Electrical shorts caused by the TAB leads making contact with the edge of the integrated circuit die.

Encapsulation A coating on the surface of an integrated circuit die to provide mechanical and environmental protection.

Excise The severing of the outer leads of a TAB bonded integrated circuit from the excess carrier material in order to isolate the die and leads prior to placement onto a substrate.

Fine Pitch Technology (FPT) A packaging and interconnecting technology for integrated circuits packages with leads on less than 0.6 mm (0.025”) centers.

Gang (Mass) Bonding The bonding of two or more TAB leads at the same time.

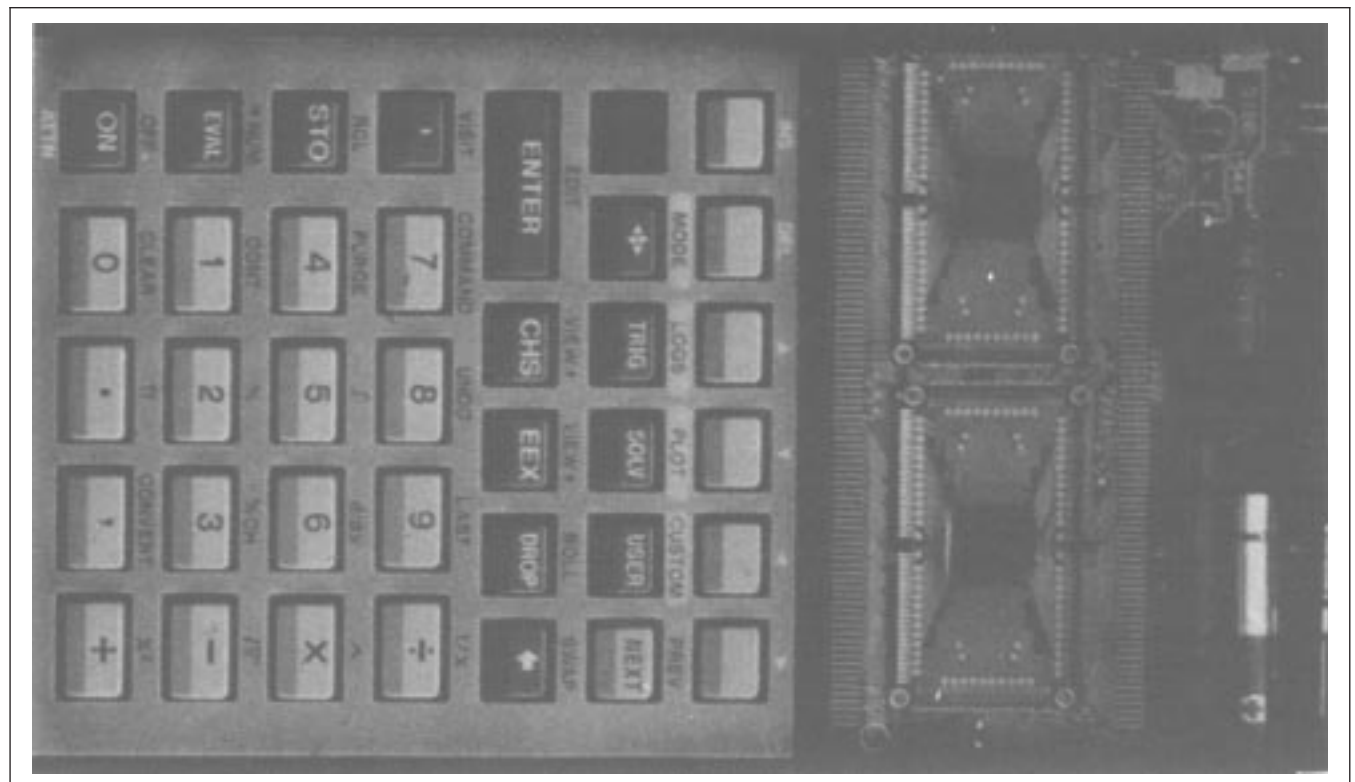


Figure 1-8 Pocket calculator with TAB device

Inner Lead Bonding (ILB) The bonding of the leads on a TAB tape to an integrated circuit die.

Land A portion of a conductive pattern usually used for electrical connection, component attachment, or both.

Lead The conductor formed on the TAB tape that is used to electrically connect an integrated circuit to a substrate.

Lead Forming Bending of the TAB lead so that it will contact a substrate for outer lead bonding.

Negative Lead Egress (NLE) Bending of the lead from the inner-lead bond towards the edge of the die, increasing the likelihood of edge shorts.

Outer Lead Bonding (OLB) The bonding of the excised end of TAB leads to a substrate. It may be either reflow, thermocompression or thermosonic bonding.

Passivation An insulating layer that is directly over an integrated circuit die to protect die surfaces from contamination, moisture and foreign particles.

Single Point Bonding The bonding of only one inner or outer TAB lead at a time.

Slide Carrier A mechanical holder that precisely locates singulated tape to facilitate handling for assembly operations.

Support (Omnibus) Ring A ring of dielectric material that is used to support and hold the TAB leads in place relative to each other.

Tape The carrier for the TAB conductors that interconnect the die to the substrate. It may be a single layer-metal foil; two layer-dielectric with plated conductors; or three layers, i.e., dielectric, adhesive, and metal-foil layers.

Tape Automated Bonding (TAB) A fine pitch technology for providing the interconnections between integrated circuit die and substrates with conductors that are on a carrier tape.

Thermode A contact tool used for inner (ILB) or outer lead (OLB) gang bonding.

Window An opening in a dielectric layer through which the TAB conductor leads are exposed for bonding purposes.

2.0 PATTERN STANDARDIZATION (TAB Tape)

This section describes the preliminary outlines and features for JEDEC registered TAB tape (Figure 2-1). Unlike other surface-mount components, TAB tape is delivered to the user in a format that is different from the package format

after bonding to the substrate. Test lands and supporting areas are cut away or excised prior to packaging or board mounting.

Because each IC die may have different pad pitches, pad dimensions, and pad X and Y locations, only those features outside the die area can be standardized. Features that can be registered are:

- Package size prior to the leads being formed, in an “as-shipped” condition
- Package body size after lead forming and excising
- The outer lead window inside dimension
- Test pad size and location
- Outer lead dimension and pitch
- Registration features

2.1 TAB Tape Formats The interior inner-lead bond pattern of these TAB tapes is user-definable. These patterns allow the development of component carriers (Section 3.0), test and burn-in sockets (Section 9.0), and land patterns on printed wiring boards and hybrids (Section 6.0).

The number of leads required for a particular application may not be the same as the maximum number allowed on a given standard pattern. In this case two options are available, either retain the maximum number of leads the pattern allows with some nonfunctional outer leads or remove the unneeded leads. The convention for removal of leads from the pattern is to remove from the outside ends of all rows of leads symmetrically (if possible).

As an example, a particular user may require a package with 124 lands on a 0.5 mm (0.020) pitch. The user chooses the 20.57 x 20.57 mm (0.810 x 0.810”) window on a 35 mm (1.378”) wide tape. The registered tape pattern allows 132 leads maximum, so the user removes one lead from each outer end of each row (2 leads per row) on all four sides of the tape to satisfy his requirements for 124 leads.

Figure 2-2 shows the preliminary format for “super” format TAB tape. Super format tape has smaller sprocket holes spaced more closely to the tape edge than “standard” format TAB tape. The registration covers only super format tapes. The obvious advantage of the super format is the greater amount of patternable copper area between sprocket holes as compared to a standard format.

Table 2-1 gives the registered (JEDEC UO-017) package body sizes (window sizes) for the S35, S48, and S70 mm tapes as well as the locations of the registration holes used for slide carrier mounting or other physical location schemes. All of the windows are square except for one rectangular window on S35 mm. In every case the OLB window is 2.375 mm (0.095”) wide.

Figure 2-3 shows the three preliminary outer lead pitches — 0.5 mm (0.020”), 0.375 mm (0.015”), and 0.25 mm (0.010”).

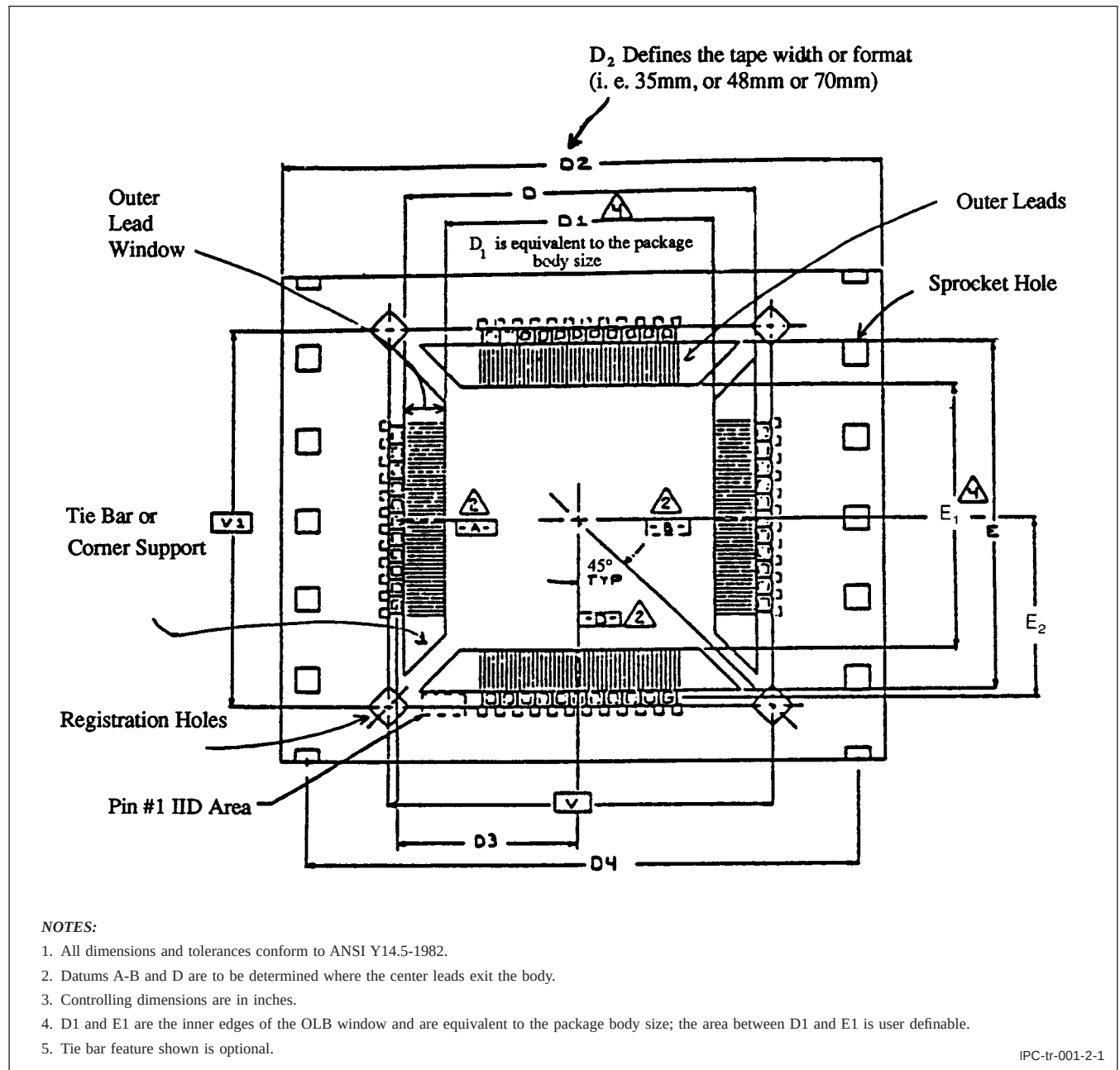


Figure 2-1 Registered features for TAB tape outer-lead bonding (see Table 2-1)—from JEDEC outline UO-017

(0.010") — and their respective lead widths from JEDEC UO-017. Lead width tolerance depends on a given tape manufacturer, but is generally ± 0.0125 mm (0.0005"). Figure 2-4 shows preliminary details for test pads and registration holes.

2.2 Leadforming Section 6 describes OLB land patterns that can be used with a variety of TAB package configuration formats. This section recommends details of the lead forming that can be used as general guidelines (see Figure 2-5).

The following are suggested guidelines for good lead forming:

- Bend radii of 0.125 mm (0.005")
- Lead forming angle of 10 degrees
- Polyimide-up configuration
- Foot length of 0.75 mm (0.030")
- Inner clamping distance, S1 of 0.375 mm (0.015")
- Height above board or substrate to be determined by user (depending on die thickness, board clearance desired, etc.).

This height determines the leg length. Heights less than 0.9 mm (0.036") are consistent with other dimensions in Table 2-1, the JEDEC registered TAB tape, and the footprints and guidelines of Section 6.



Documents

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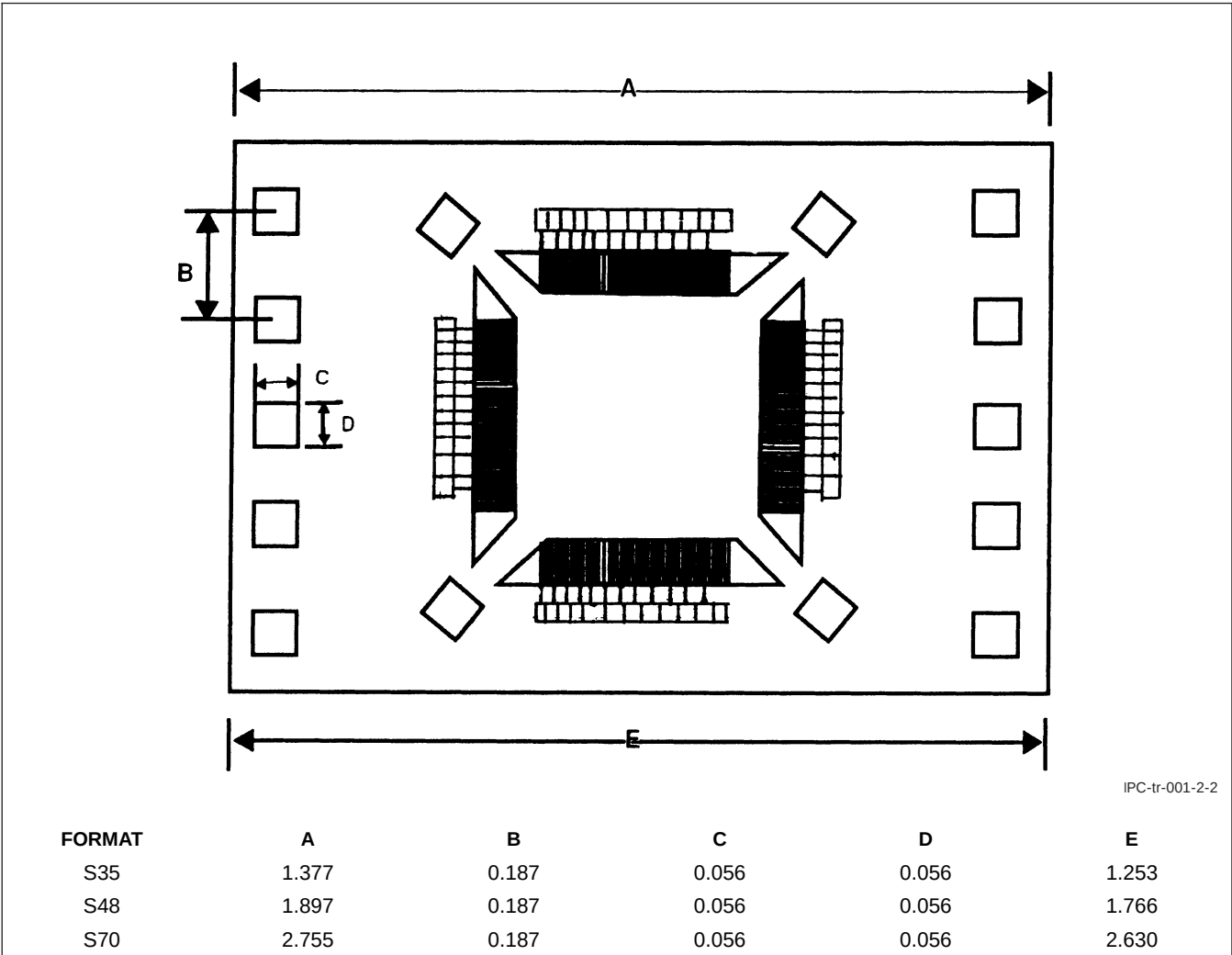


Figure 2-2 Super format TAB tape dimensions (inches)—preliminary dimensions for reference only

Table 2-1 Registered Package Body Sizes, Hole Locations and Maximum Number of Leads (Inches) (See Figure 2-1)					
Tape Format	Package Body Size (D1/E1)	Registration Hole Locations (V/V1)	Maximum Number of Leads		
			0.020 OLB Pitch	0.015 OLB Pitch	0.010 OLB Pitch
S35	0.410	0.670	60	84	124
S35	0.610	0.870	100	132	204
S35	0.810	1.070	140	188	284
S35	0.810/1.620	1.070/1.880	220	296	444
S48	1.010	1.270	180	244	364
S48	1.310	1.570	244	324	484
S70	1.510	1.770	284	372	564
S70	1.710	1.970	324	428	644
S70	1.910	2.170	364	484	724
S70	2.110	2.370	404	532	804

From JEDEC registered outline UO-017

Table 2-2 Lead Pitch versus Maximum Number of Leads

Lead Count	JEDEC TAB Tape Outlines						ASTM TAB Standard Chip Bond Pad Pitch Progression			
	Tape Width			Lead Pitch			0.220 mm [0.0067]	0.185 mm [0.0073]	0.150 mm [0.0059]	0.100 mm [0.0039]
	35 mm	48 mm	70 mm	0.51 mm [0.020]	0.38 mm [0.015]	0.25 mm [0.010]				
38							X	X	X	
32							X	X	X	
40							X	X	X	
44							X	X	X	
60	X			X						
68							X	X	X	X
84	X				X		X	X	X	X
100	X			X			X	X	X	X
124	X					X				
132	X				X		X	X	X	X
140	X			X						
144							X	X	X	X
168							X	X	X	X
180		X		X			X	X	X	X
188	X					X				
196							X	X	X	X
204	X					X				
220	X			X						
244		X		X	X					
256					X			X	X	X
284	X		X	X		X				
296	X				X					
300									X	X
324		X	X	X	X					
360										X
364		X	X	X		X				
372			X		X					
384										X
400										X
404			X	X						
420										X
428			X		X					
444	X					X				
484		X	X		X	X				
532			X		X					
564			X			X				
644			X			X				
724			X			X				
804			X			X				

Table 2-3 Preliminary European TAB Dimensions (See Figure 2-11)

Window Geometries								
Std. TAB	A	B	C	D max.	E max.	F min.	G exc.	H
A & A-A	7.0 [0.275]	6.20 [0.244]	2.0 [0.070]	5.0 [0.197]	4.20 [0.165]	1.00 [0.039]	10.60 [0.417]	10.25 [0.4035]
B	9.60 [0.378]	8.70 [0.3425]	2.0 [0.070]	7.60 [0.300]	6.80 [0.268]	1.00 [0.039]	13.20 [0.520]	12.70 [0.500]

Suggested OLB Leads				
P Pitch	W Width	S Space	I/O's A&A-A	I/O's B
0.580 [0.020]	0.229 [0.009]	0.280 [0.011]	48	64
0.381 [0.015]	0.178 [0.007]	0.203 [0.008]	60	84
0.304 [0.012]	0.152 [0.006]	0.152 [0.006]	84	108

Tolerances	Contour	Position
Specific Forms to Sprocket Holes	$\pm 50 \mu\text{m} / 0.002''$	$\pm 50 \mu\text{m} / 0.002''$
Metal Layer to Sprocket Holes	$\pm 10 \mu\text{m} / 0.0004''$	$\pm 50 \mu\text{m} / 0.002''$

Note: mm [inches]

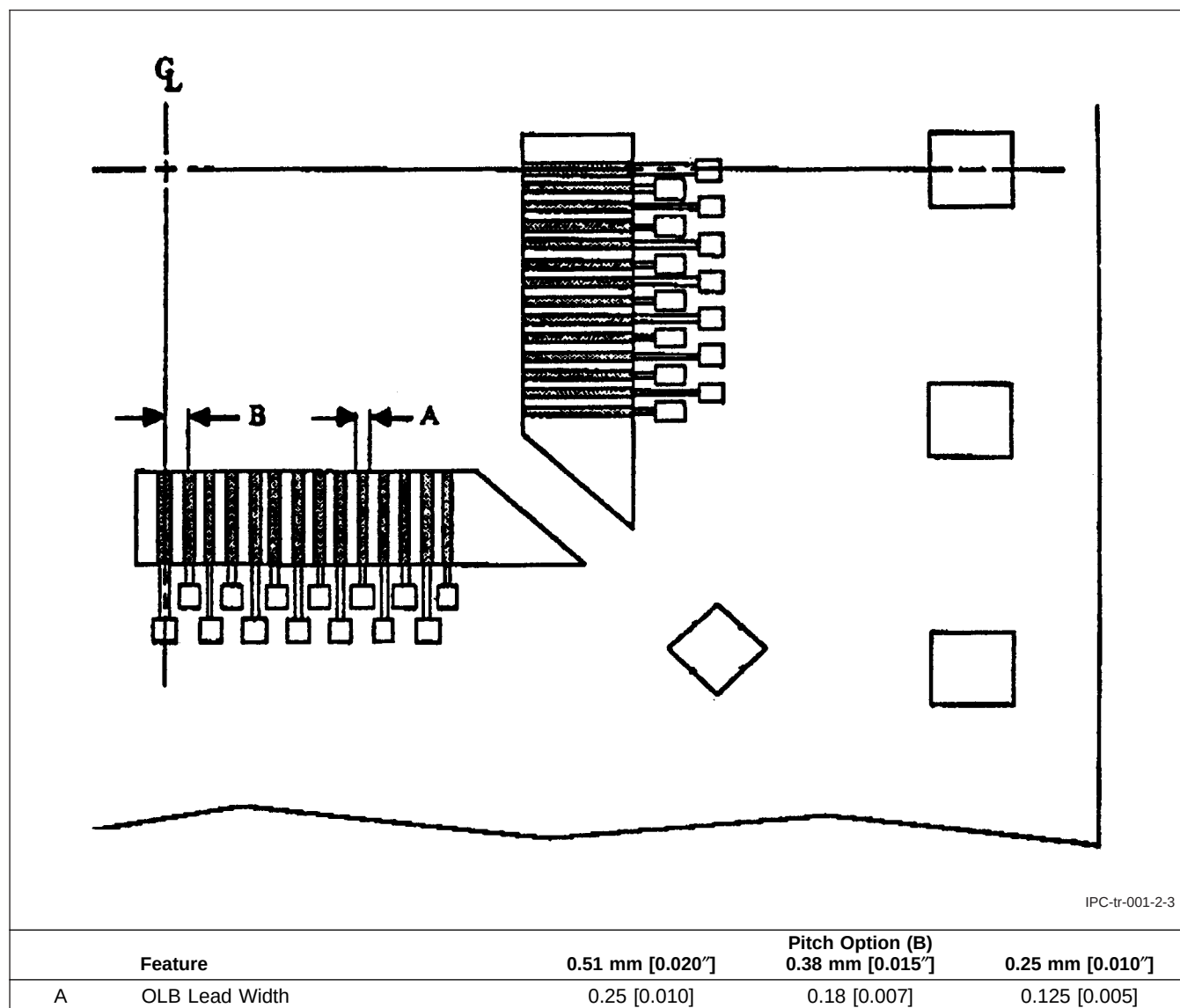


Figure 2-3 Outer lead pitch versus lead width—preliminary dimensions for reference only (mm [inches])—from JEDEC registered outline UO-017